TLC6C598 8 位移位寄存器 LED 驱动器

1 特性

- 3V 至 5.5V 的宽 V_{CC}范围
- 40V 的最大输出额定值
- 8 路功率双扩散金属氧化物半导体 (DMOS) 晶体管输出：50mA 持续电流 (V_{CC} = 5V) 或者 200mA 脉宽调制 (PWM) 电流（单脉冲持续时间短于 1ms 且平均电流低于 50mA）
- 热关断保护
- 针对多级的增强型级联
- 所有寄存器由单一输入清零
- 低功耗
- 缓开关时间（t_r和 t_f），这十分有助于减少电磁干扰 (EMI)
- 16 引脚薄型小外形尺寸 (TSSOP)-PW 封装

2 应用

- 电器显示面板
- 电梯显示面板
- PLC 功能指示器
- 七段显示器

3 说明

TLC6C598 器件是一款单片、中等电压、低电流功率 8 位移位寄存器，专为负载功率要求相对适中的系统（例如，LED）而设计。

此器件包含一个 8 位串入、并出移位寄存器，此寄存器为一个 8 位 D 类存储寄存器提供数据。移位寄存器和存储寄存器分别有单独的时钟。输出为低侧、漏极开路 DMOS 晶体管输出：输出额定值为 40V 及 50mA 持续灌电流或者 200mA PWM 电流（V_{CC} = 5V 时，单脉冲持续时间短于 1ms 且平均电流低于 50mA）。该器件内置热关断保护，在人体模型和 200V 机器模型测试下可提供高达 2000V 的静电放电 (ESD) 保护。

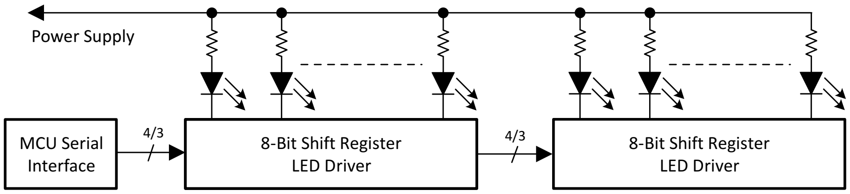
TLC6C598 的额定工作环境温度范围为 -40°C 至 105°C。

器件信息[1]

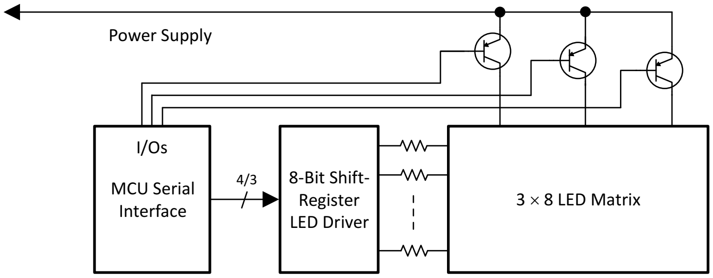
器件型号	封装	封装尺寸（标称值）
TLC6C598	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



Typical Cascade Topology



Typical Scan Topology

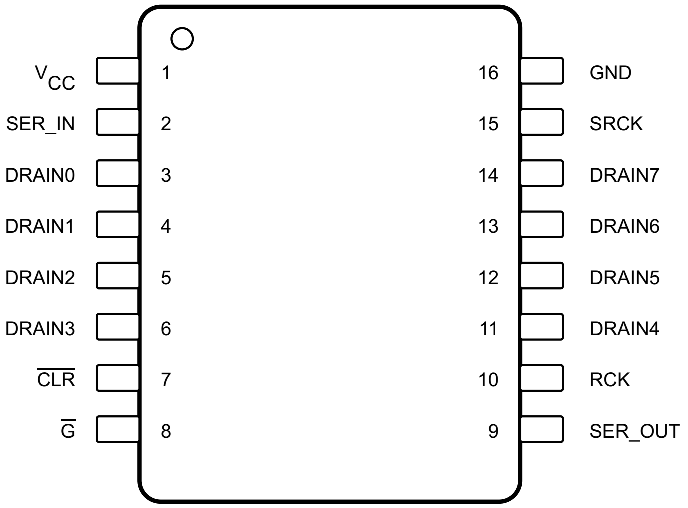
目录

4 修订历史记录

日期	修订版本	注
2016 年 5 月	*	最初发布版本

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CLR}}$	7	I	Shift register clear, active-low. The storage register transfers data to the output buffer when $\overline{\text{CLR}}$ is high. Driving $\overline{\text{CLR}}$ low clears all the registers in the device.
DRAIN0	3	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN1	4	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN2	5	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN3	6	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN4	11	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN5	12	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN6	13	O	Open-drain output, LED current-sink channel, connect to LED cathode
DRAIN7	14	O	Open-drain output, LED current-sink channel, connect to LED cathode
$\overline{\text{G}}$	8	I	Output enable, active-low. LED-channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
GND	16	—	Power ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	10	I	Register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK.
SER IN	2	I	Serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.
SER OUT	9	O	Serial data output of the 8-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus.
SRCK	15	I	Serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	1	I	Power supply pin for the device. TI recommends adding a 0.1-μF ceramic capacitor close to the pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	–0.3	8	V
V_I	Logic input-voltage range	–0.3	8	V
V_{DS}	Power DMOS drain-to-source voltage	–0.3	42	V
	Continuous total dissipation	See *Thermal Information*		
T_J	Operating junction temperature range	–40	125	°C
T_{stg}	Storage temperature range	–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±750	
			Corner pins (1, 8, 9, and 16)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
T_A	Operating ambient temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC6C598 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DRAIN0 to DRAIN7. Drain-to-source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = −4 mA		4.5	4.69		V
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 µA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	V
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		µA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		µA
I_{CC}	Logic supply current	V_{CC} = 5 V, no clock signal	All outputs off		0.1	1	µA
			All outputs on		88	160	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF	All outputs on		200		µA
I_{DSx}	Off-state drain current	V_{DS} = 30 V	V_{CC} = 5 V			0.1	µA
		V_{DS} = 30 V, T_C = 105°C	V_{CC} = 5 V		0.15	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, Single channel ON		6	7.41	8.6	Ω
		I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, All channels ON		6.7	8.3	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, Single channel ON		7.9	9.34	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, All channels ON		8.7	10.25	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, Single channel ON		9.1	11.13	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, All channels ON		10.3	12.28	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, Single channel ON		11.6	13.69	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, All channels ON		12.8	14.89	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	ºC
T_{hys}	Hysteresis				15		ºC

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{su}	Setup time, SER IN high before SRCK↑	15			ns
t_h	Hold time, SER IN high after SRCK↑	15			ns
t_w	SER IN pulse duration	40			ns

6.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from $\overline{G}$ to output, low-to-high level	C_L = 30 pF, I_D = 48 mA		220		ns
t_{PHL}	Propagation delay time from $\overline{G}$ to output, high-to-low level			75		ns
t_r	Rise time, drain output			210		ns
t_f	Fall time, drain output			128		ns
t_{pd}	Propagation delay time, SRCK↓ to SER OUT	C_L = 30 pF, I_D = 48 mA		49.4		ns
t_{or}	SER OUT rise time (10% to 90%)	C_L = 30 pF		20		ns
t_{of}	SER OUT fall time (90% to 10%)	C_L = 30 pF		20		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
t_{SRCK_WH}	SRCK pulse duration, high		30			ns
t_{SRCK_WL}	SRCK pulse duration, low		30			ns

6.8 Timing Waveforms

图 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see 图 13). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

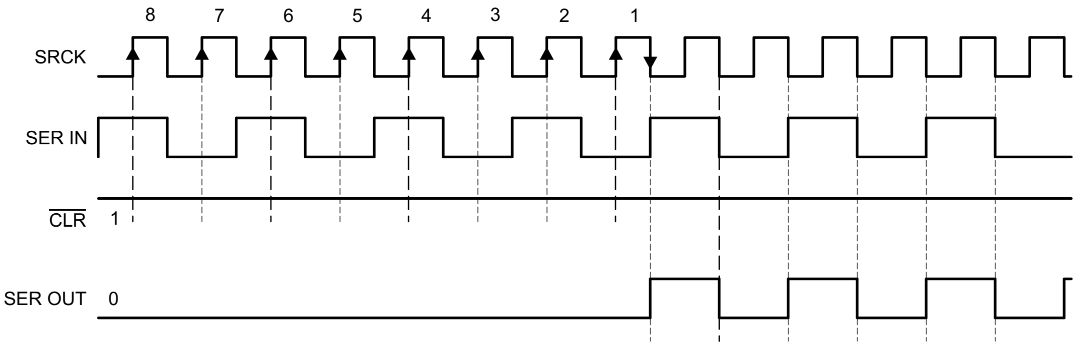
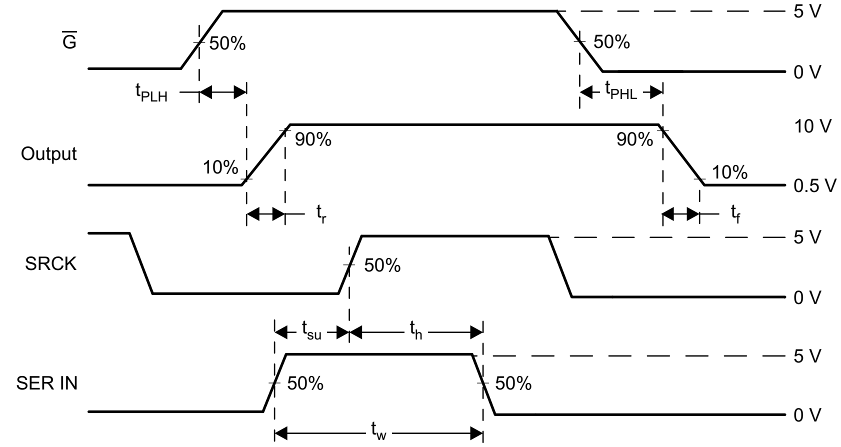
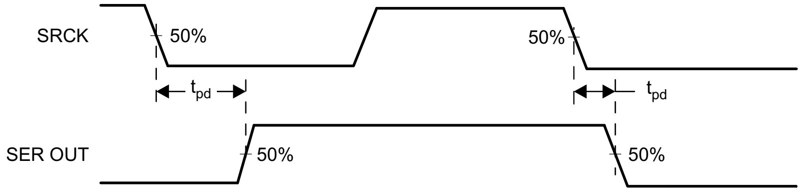


图 1. SER IN to SER OUT Waveform

图 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in 图 11.



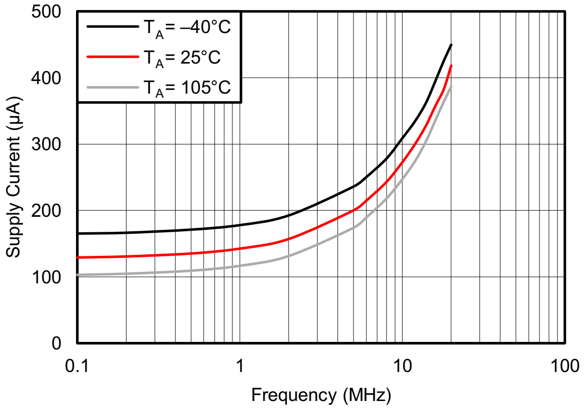
Switching Times, Input Setup and Hold Waveforms



SER OUT Propagation Delay Waveform

图 2. Switching Times and Voltage Waveforms

6.9 Typical Characteristics



V_{CC} = 5 V

图 3. Supply Current vs Frequency

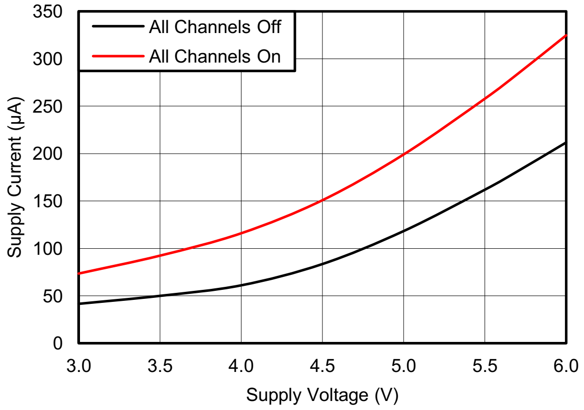
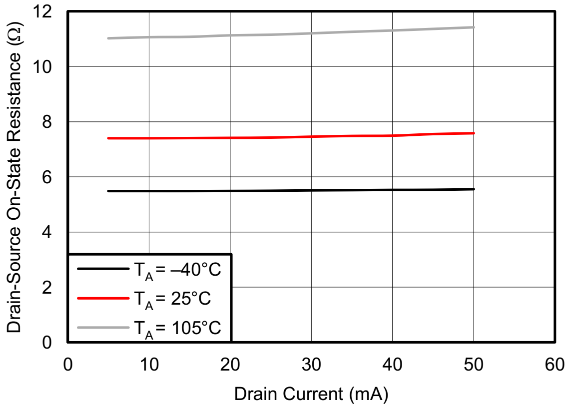
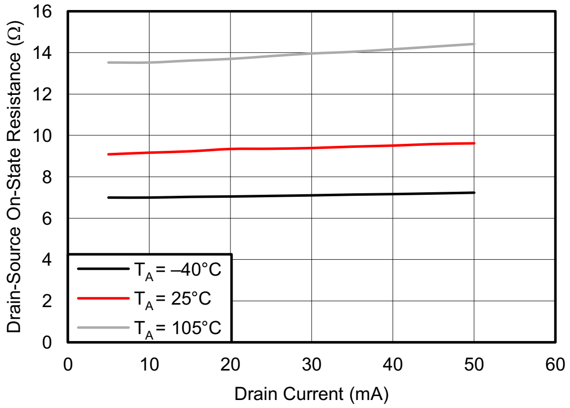


图 4. Supply Current vs Supply Voltage



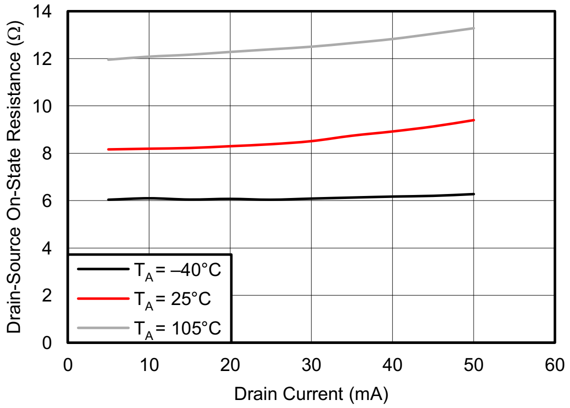
Single channel on V_{CC} = 5 V

图 5. Drain-to-Source On-State Resistance vs Drain Current



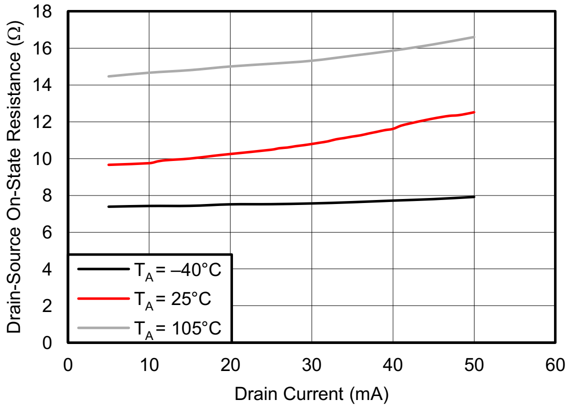
Single channel on V_{CC} = 3.3 V

图 6. Drain-to-Source On-State Resistance vs Drain Current



All channels on V_{CC} = 5 V

图 7. Drain-to-Source On-State Resistance vs Drain Current



All channels on V_{CC} = 3.3 V

图 8. Drain-to-Source On-State Resistance vs Drain Current

Typical Characteristics (接下页)

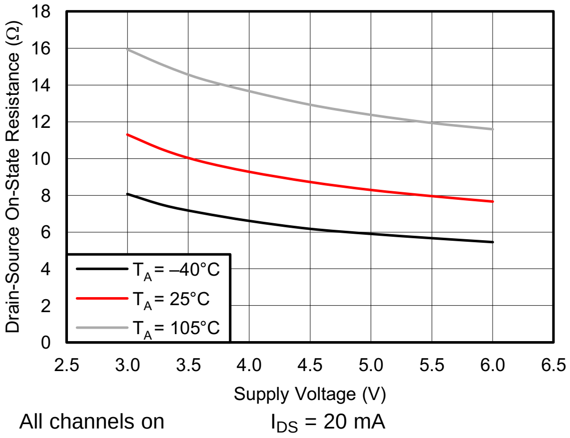


图 9. Drain-to-Source On-State Resistance vs Supply Voltage

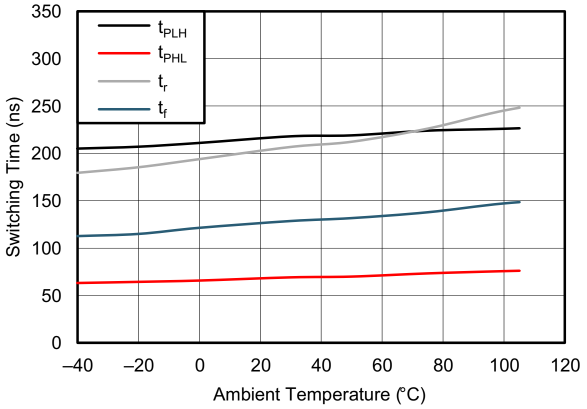
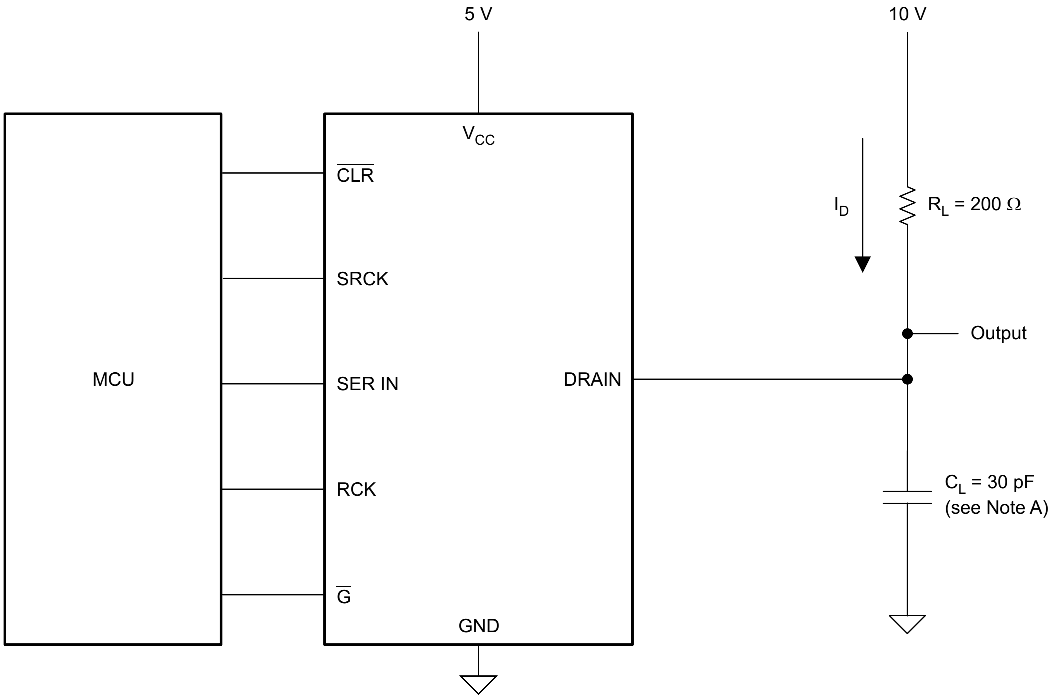


图 10. Switching Time vs Ambient Temperature

7 Parameter Measurement Information

图 11 and 图 12 show the resistive-load test circuit and voltage waveforms. One can see from 图 12 that with $\overline{G}$ held low and $\overline{CLR}$ held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.



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A. C_L includes probe and jig capacitance.

图 11. Resistive-Load Test Circuit

Parameter Measurement Information (接下页)

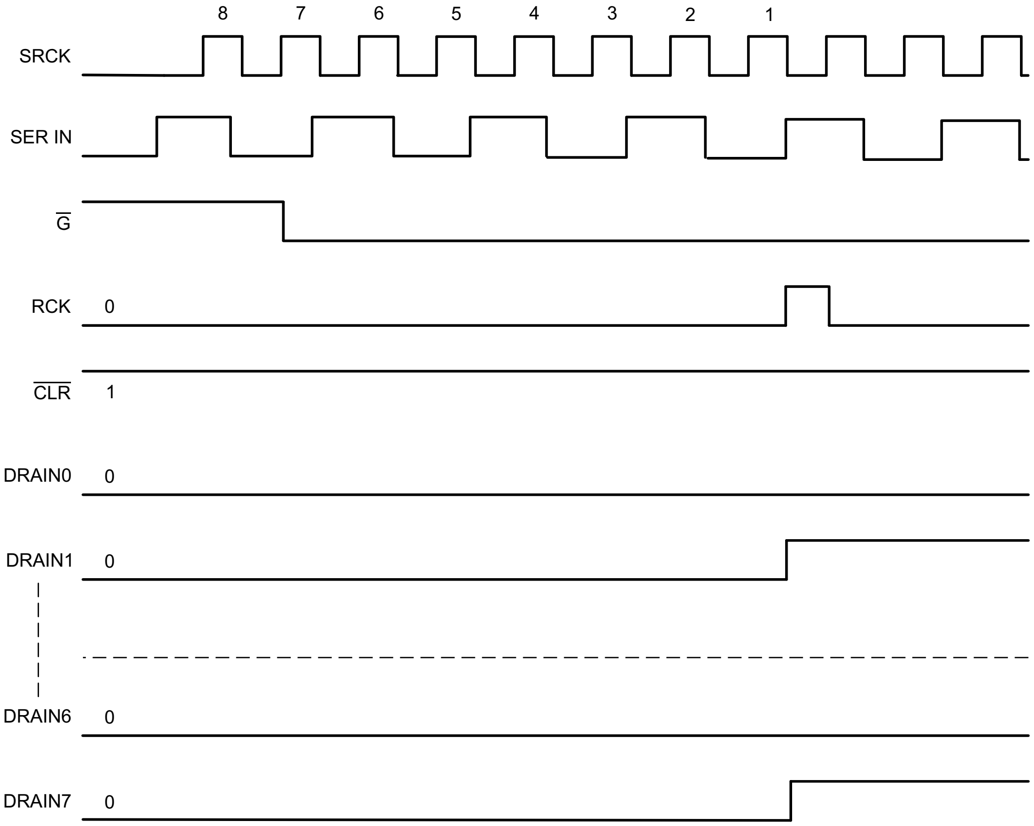

图 12. Voltage Waveforms

8 Detailed Description

8.1 Overview

The TLC6C598 device is a monolithic, medium-voltage, low-current 8-bit shift register designed to drive relatively moderate load power such LEDs. The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Thermal shutdown protection is also built-into the device.

8.2 Functional Block Diagram

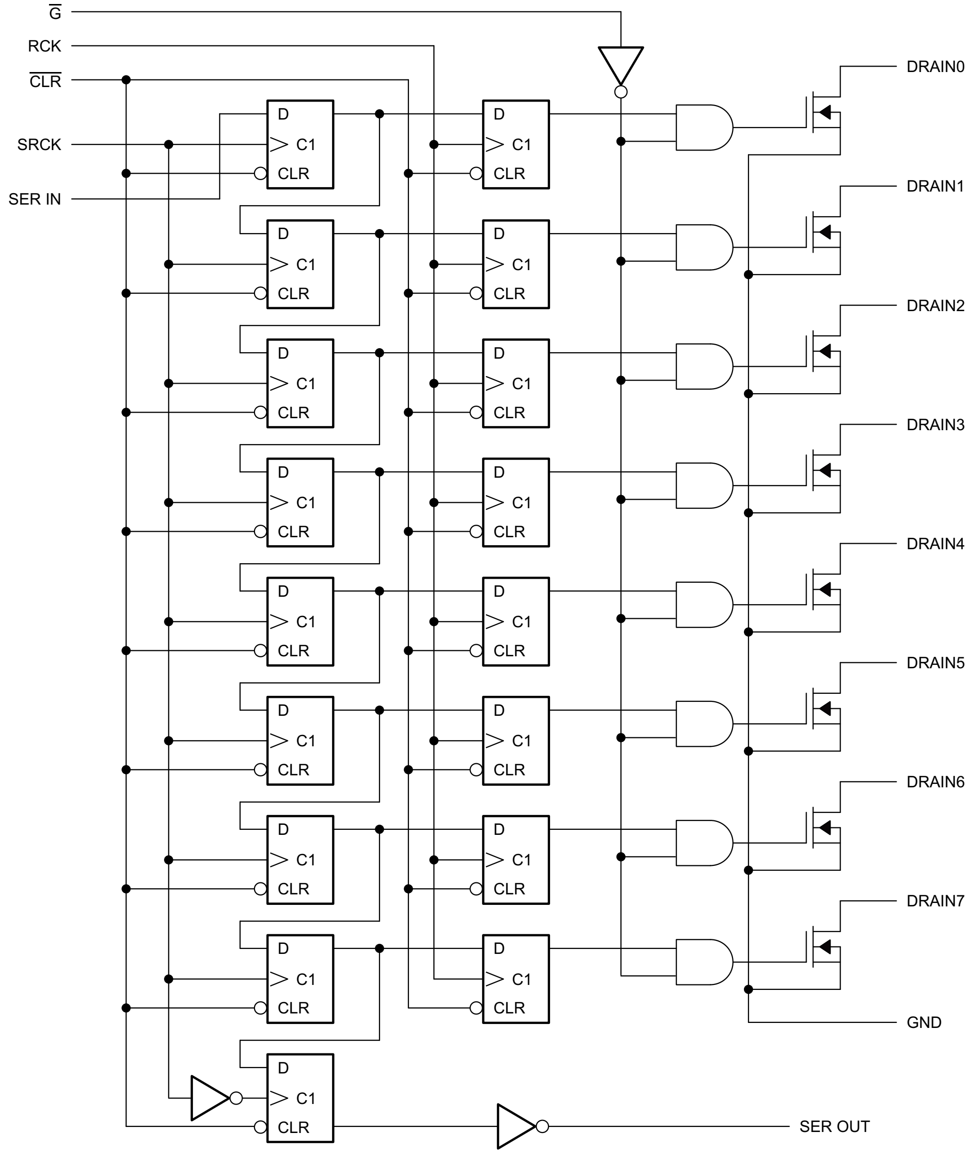

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图 13. Logic Diagram (Positive) of TLC6C598

8.3 Feature Description

8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfer through the shift and storage registers is on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{CLR}}$) is high.

8.3.3 Clear Registers

A logic low on the $\overline{\text{CLR}}$ pin clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.4 Output Channels

DRAIN0–DRAIN7. These pins can survive up to 40-V LED supply voltage.

8.3.5 Register Clock

RCK is the storage-register clock. Data in the storage register appears at the output whenever the output enable ($\overline{\text{G}}$) input signal is high.

8.3.6 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus in cascade, the data transfers to the next device on the falling edge of SRCK. This connection can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input on the same rising edge of SRCK.

8.3.7 Output Control

Holding the output enable (pin $\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{\text{G}}$ low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sinking current. This pin also can be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With V_{CC} < 3 V

This device works normally within the range 3 V ≤ V_{CC} ≤ 5.5 V. When the operating voltage is lower than 3 V, correct behavior of the device, including communication interface and current capability, is not assured.

8.4.2 Operation With 5.5 V ≤ V_{CC} ≤ 8 V

The device works normally in this voltage range, but reliability issues may occur if the device works for a long time in this voltage range.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC6C598 device is a serial-in, parallel-out, power and logic, 8-bit shift register with low-side open-drain DMOS output ratings of 40-V and 50-mA continuous sink-current capabilities when V_{CC} = 5 V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

9.2 Typical Application

图 14 shows a typical cascade application circuit with two TLC6C598 chips configured in cascade topology. The MCU generates all the input signals.

Typical Application (接下页)

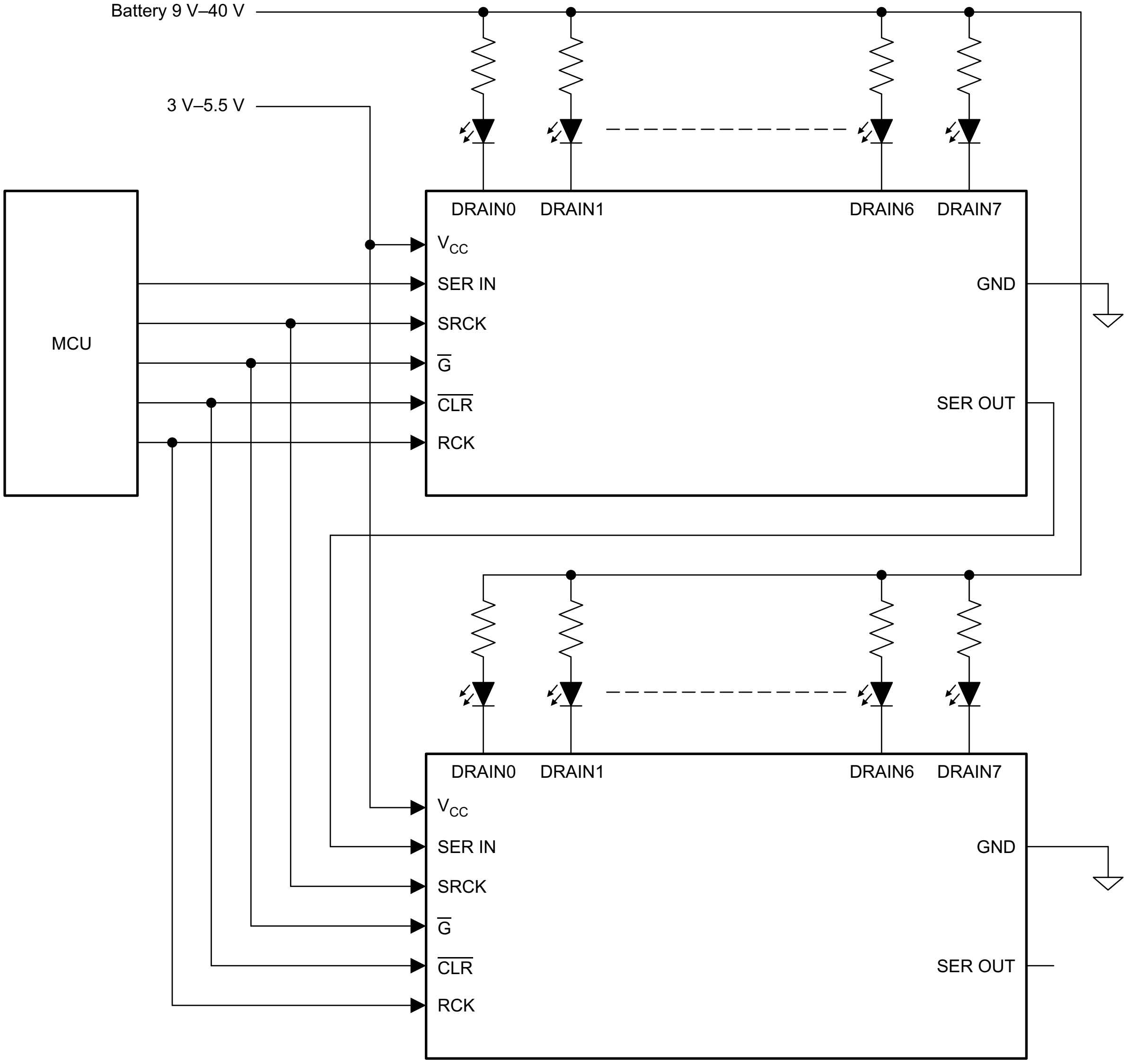

图 14. Typical Application Circuit

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
$V_{Battery}$	9 V to 40 V
V_{CC_1}	3.3 V
I(D0), I(D1), I(D2), I(D3) , I(D4), I(D5), I(D6), I(D7)	30 mA
V_{CC_2}	5 V
I(D8), I(D9), I(D10), I(D11) , I(D12), I(D13), I(D14), I(D15)	50 mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- V_{supply}: LED supply voltage
- V_{Dx}: LED forward voltage
- I: LED current

With these parameters determined, the resistor in series with the LED can be calculated by using the following equation:

$$R_X = (V_{Supply} - V_{Dx}) / I \tag{1}$$

9.2.3 Application Curve

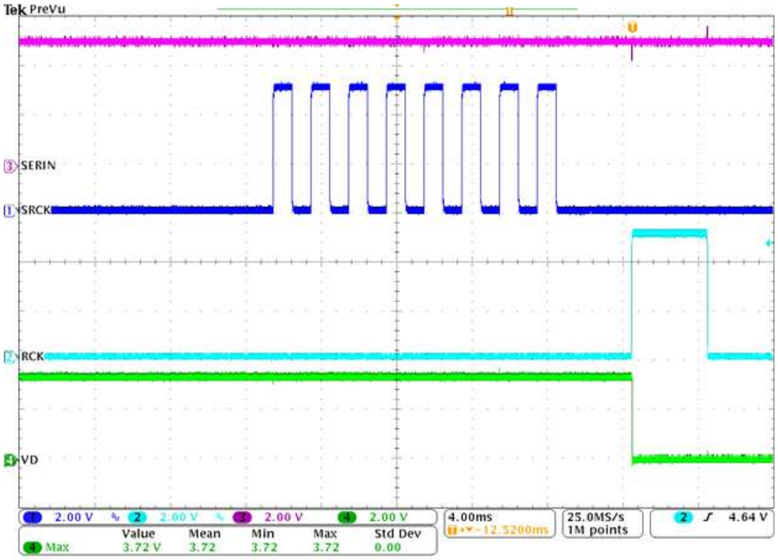

图 15. TLC6C598 Application Waveform

10 Power Supply Recommendations

The TLC6C598 device is designed to operate with an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirements for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pins.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.

All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

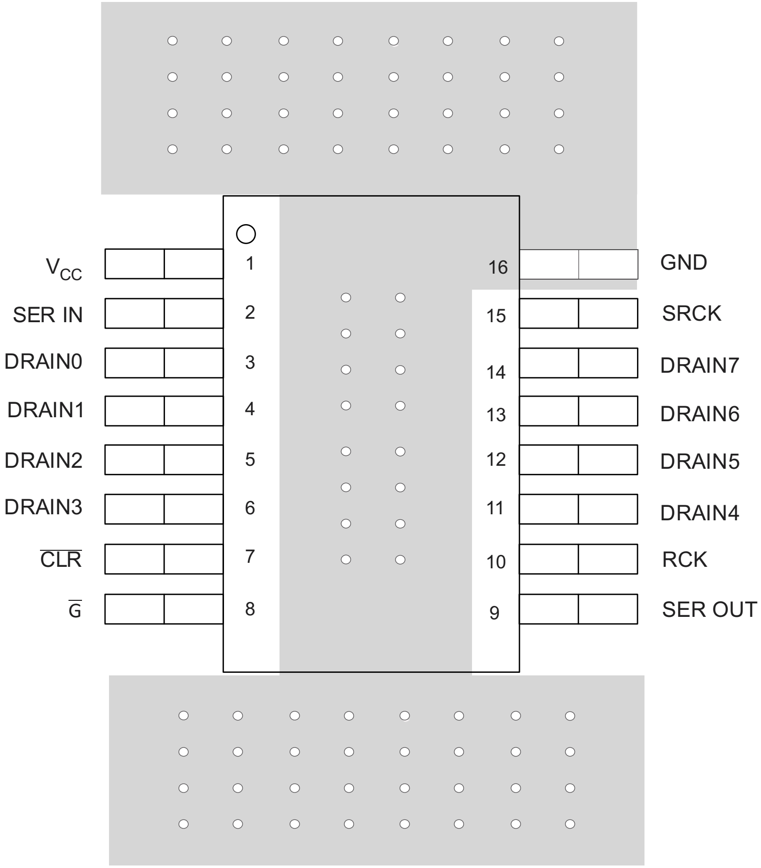

图 16. TLC6C598 Example Layout

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

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All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧的导航窗格。

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C598PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	6C598I	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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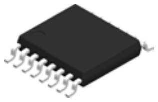
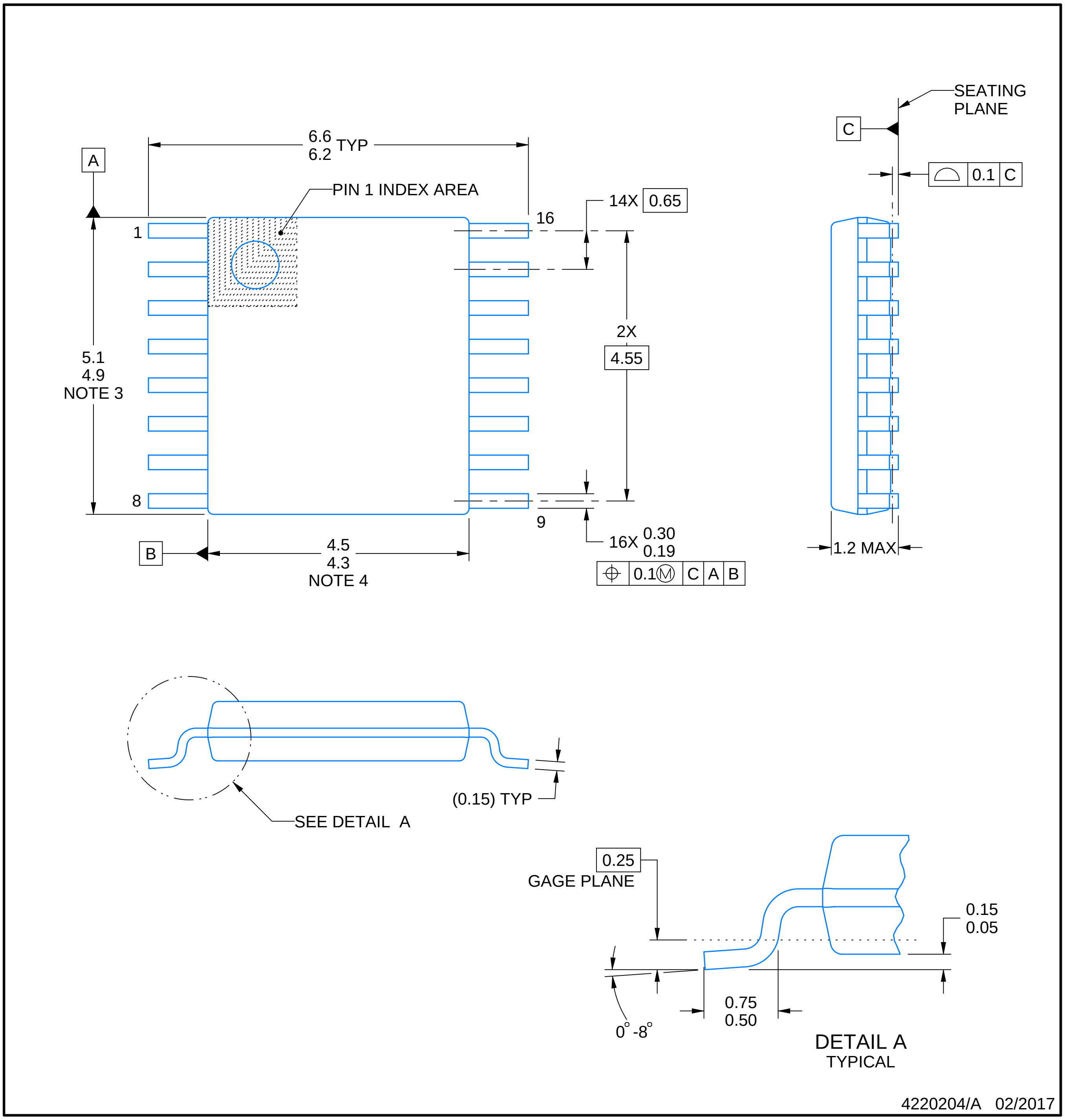


PACKAGE OUTLINE

PW0016A

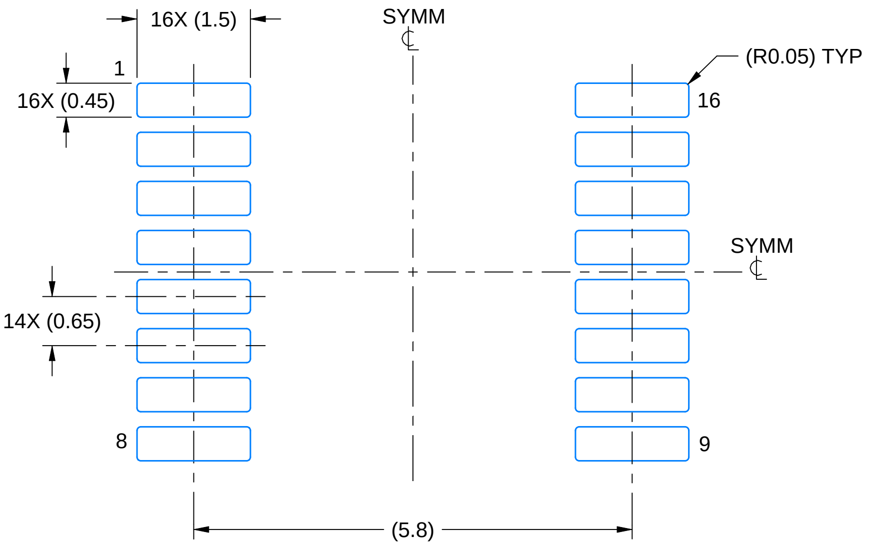
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

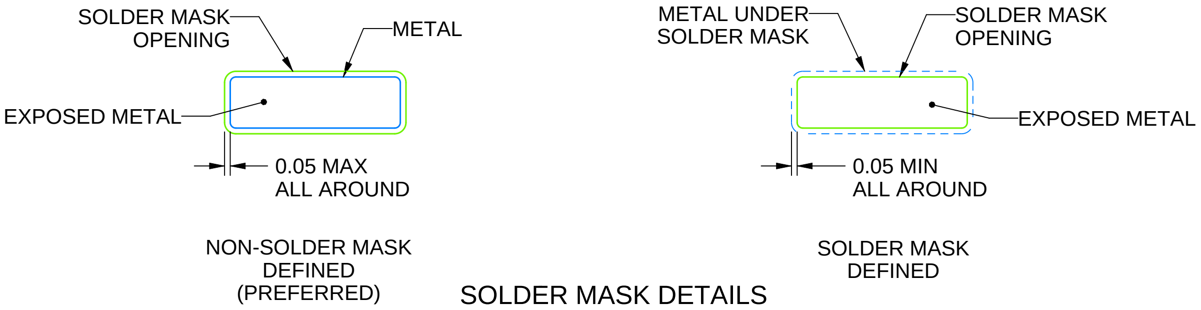


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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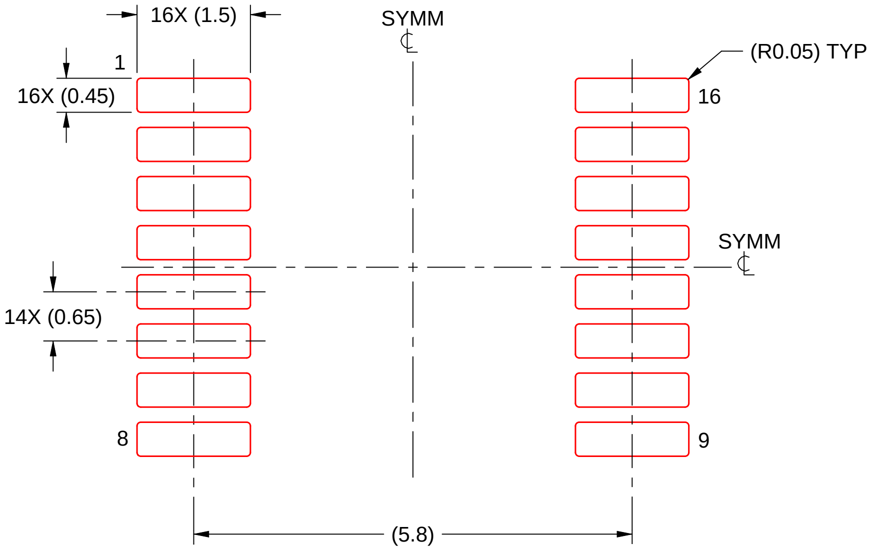
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.