TLC6C5748-Q1 具有内部电流设置的 48 通道、16 位 PWM LED 驱动器

1 特性

- 适用于汽车电子应用
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的工作环境温度范围
- 48 个恒定灌电流输出通道
- 在最大 MC、DC 和 BC 下的灌电流能力：
  - 23.9mA (V_{CC} ≤ 3.6V，MC = 5)
  - 31.9mA (V_{CC} > 3.6V, MC = 7)
- 灰度 (GS) 控制：
  - 16 位（65、536 步长），具有增强型频谱或传统 PWM
- 最大电流 (MC) 控制：
  - 3 位（8 步长），电流范围为 3mA 至 30mA
  - 每个色彩组有 3 个 MC 设置
- 点校正 (DC) 控制：
  - 26.2% 至 100% 范围内的 7 位（128 步长）
- 全局亮度控制 (BC)：
  - 10% 至 100% 范围内的 7 位（128 步长）
  - 每个色彩组有 3 个 BC 设置
- LED 电源电压：高达 10V
- VCC：3.0V 至 5.5V
- 恒定电流精度：
  - 通道间：±2%（典型值），±5%（最大值）
  - 器件间：±2%（典型值），±4%（最大值）
- 数据传输速率：25MHz
- 灰度控制时钟：33MHz
- 自动重复显示
- 显示时序复位
- 自动数据刷新（仅 GS 和 DC）
- LED 开路检测 (LOD)
- LED 短路检测 (LSD)
- UVLO 设置默认数据
- 延迟开关可防止浪涌电流
- 工作温度：–40°C 至 +125°C

2 应用

- 汽车中心信息显示屏
- 汽车仪表组显示屏
- 抬头显示
- 汽车照明

3 说明

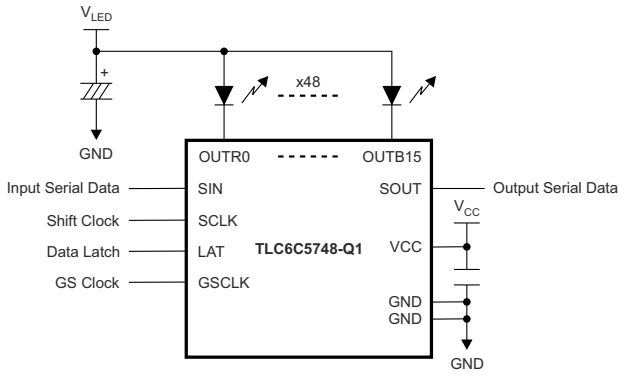
TLC6C5748-Q1 是一款 48 通道、恒定灌电流驱动器。每个通道具有一个独立可调节，脉宽调制 (PWM)，灰度 (GS) 亮度控制，此控制有 65,536 步长和 128 步长的恒定电流点校正 (DC)。DC 可调节通道间的亮度偏差。所有通道具有一个 128 步长的全局亮度控制 (BC)。BC 调节 R，G，B 色彩组之间的亮度偏差。8 步长最大电流控制 (MC) 为每个色彩组的所有通道选择最大输出电流范围。可通过一个串行接口端口来访问 GS，DC，BC 和 MC 数据。

TLC6C5748-Q1 有三个错误标签：LED 开路检测 (LOD)、LED 短路检测 (LSD) 和热关断 (TSD)。可使用一个串行接口端口来读取错误检测结果。

器件信息

器件型号	封装(1)	封装尺寸
TLC6C5748-Q1	HTSSOP (56)	14.0mm x 6.1mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用电路

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4 Revision History

Changes from Revision * (October 2020) to Revision A (December 2020)	Page
• 将状态从“预告信息”更改为“量产数据”	1

5 Terminal Configurations and Functions

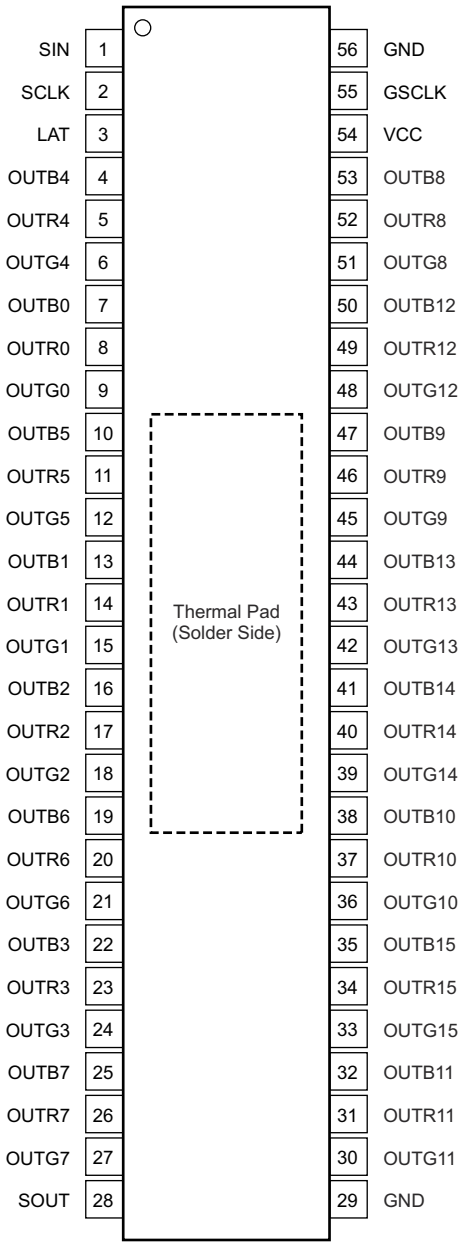


图 5-1. DCA Package HTSSOP-56 (Top View)

表 5-1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	PIN NUMBER		
GND	29, 56	—	Power ground.
GSCLK	55	I	Reference clock for the grayscale (GS) pulse width modulation (PWM) control for all outputs. Each GSCLK rising edge increments the grayscale counter for PWM control. When the LAT signal is input for a GS data write with the timing reset mode enabled, all constant-current outputs (OUTX0-OUTX15, where X = R, G, or B) are forced off, the grayscale counter is reset to 0, and the grayscale PWM timing controller is initialized.
LAT	3	I	The LAT rising edge either latches the data from the common shift register into the GS data latch when the MSB of the common shift register is 0 or latches the data into the control data latch when the MSB of the common shift register is 1. When the display timing reset bit (TMGRST) in the control data latch is 1, the grayscale counter initialized at the LAT signal is input for a grayscale data write. Dot correction (DC) data in the control data latch are copied to DC data latch at the same time.

表 5-1. Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	PIN NUMBER		
OUTB0 to OUTB15	4, 7, 10, 13, 16, 19, 22, 25, 32, 35, 38, 41, 44, 47, 50, 53	O	Constant-current outputs for the blue color group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUTG0 to OUTG15	6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51	O	Constant-current outputs for the green color group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUTR0 to OUTR15	5, 8, 11, 14, 17, 20, 23, 26, 31, 34, 37, 40, 43, 46, 49, 52	O	Constant-current outputs for the red color group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
SCLK	2	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the common shift register with the SCLK rising edge. Data in the shift register are shifted toward the MSB at each SCLK rising edge. The MSB data of the common shift register appears on SOUT.
SIN	1	I	Serial data input for the 769-bit common shift register.
SOUT	28	O	This bit is the serial data output of the 769-bit common shift register. LED open detection (LOD) and LED short detection (LSD) can be read out with SOUT in the form of status information data (SID) after the LAT falling edge is input for a GS data write. SOUT is connected to the MSB of the 769-bit common shift register. Data are clocked out at the SCLK rising edge.
VCC	54	—	Power-supply voltage.
Thermal pad		—	The thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VCC	–0.3	6	V
	SIN, SCLK, LAT, SOUT, GSCLK	–0.3	V_{CC} + 0.3	V
	OUTX0 to OUTX15	–0.3	11	V
Junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (SIN, SOUT, GND)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage on pins	VCC	3		5.5	V
	OUTX0 to OUTX15	0		10	V
	SIN, SCLK, LAT, SOUT, GSCLK	0		V_{CC}	V
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLC6C5748-Q1 HTTSOP 56-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics

Limits apply over the full operation temperature range -40°C≤T_A≤105°C, unless otherwise specified, V_{CC} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Electrical Characteristics						
I_Q	Supply Current (V_{CC})	SIN, SCLK, and LAT = GND, all OUTXn = off, GSCLK = GND, GSXn = 0000h, DCXn and BCX = 7Fh, VOUTXn = 0.8 V, MCX = 0 (3.2-mA target)		15	20	mA
		SIN, SCLK, and LAT = GND, all OUTXn = off, GSCLK = GND, GSXn = 0000h, DCXn and BCX = 7Fh, VOUTXn = 0.8 V, MCX = 4 (19.1-mA target)		16	22	mA
		SIN, SCLK, and LAT = GND, auto display repeat enabled, GSCLK = 33MHz, GSXn = FFFFh, DCXn and BCX = 7Fh, VOUTXn = 0.8 V, MCX = 4 (19.1-mA target)		18	26	mA
		V_{CC} = 5.0 V, SIN, SCLK, and LAT = GND, auto display repeat enabled, GSCLK = 33MHz, GSXn = FFFFh, DCXn and BCX = 7Fh, VOUTXn = 0.8 V, MCX = 7 (31.9-mA target)		20	29	mA
LED Current Sink Electrical Characteristics						
I_{OLC}	Constant output sink current (OUTXn)	All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 4	17.4	19.1	20.8	mA
		All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 5		23.9		mA
		V_{CC} = 5.0V, All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 7	29.1	31.9	34.7	mA
I_{OLKG}	Output leakage current (OUTXn)	All OUTXn = off, V_{OUTXn} = V_{OUTfix} = 10V, MCX = 7, TJ = +25°C			0.1	µA
		All OUTXn = off, V_{OUTXn} = V_{OUTfix} = 10V, MCX = 7, TJ = +125°C		0.3	0.8	µA
V_{SAT}	Saturation Voltage (OUTXn)	All OUTXn = on, DCXn and BCX = 7Fh, I_{OLC} = 90% normal current, MCX = 4		0.22	0.28	V
		All OUTXn = on, DCXn and BCX = 7Fh, I_{OLC} = 90% normal current, MCX = 7		0.28	0.38	V
ΔI_{OLC}	Constant-current error (channel-to-channel, OUTXn)(1)	All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 4		±2	±5	%
	Constant-current error (device-to-device, OUTXn)(2)	All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 4		±2	±4	%
	Line regulation (OUTXn)	V_{CC} = 3.0 V to 5.5 V, All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 0.8V, MCX = 4		±0.1	±1	%/V
	Load regulation (OUTXn)	V_{CC} = 3.0 V to 5.5 V, All OUTXn = on, DCXn and BCX = 7Fh, V_{OUTXn} = 0.8V to 3.0V, V_{OUTfix} = 0.8V, MCX = 4		±0.1	±1	%/V
t_{R1}	Rise time	OUTXn, VCC = 3.6 V, DCXn and BCX = 7Fh, TA = +25°C		30		ns
t_{F1}	Fall time	OUTXn, VCC = 3.6 V, DCXn and BCX = 7Fh, TA = +25°C		40		ns
Fault Detection Electrical Characteristics						
V_{LOD}	LED open-detection threshold	All OUTXn = on	0.28	0.31	0.35	V

6.5 Electrical Characteristics (continued)

Limits apply over the full operation temperature range -40°C≤T_A≤105°C, unless otherwise specified, V_{CC} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LSD}	LED short-detection threshold	All OUTXn = on, LSDVLT = 0	0.65 × V_{CC}	0.70 × V_{CC}	0.75 × V_{CC}	V
		All OUTXn = on, LSDVLT = 1	0.85 × V_{CC}	0.9 × V_{CC}	0.95 × V_{CC}	V
T_{SD_R}	Thermal shutdown threshold(3)	Temperature rising	155	172		℃
T_{SD_HYS}	Thermal shutdown hysteresis(3)	TSD rising threshold - TSD falling threshold		20		℃

(1) The deviation of each output from the 48 OUTXn channels' average current
(2) The deviation of devices' 48 OUTXn channels' average current from the ideal current output
(3) Guaranteed only by design

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	SIN, SCLK, LAT, GSCLK	0.70 × V_{CC}			V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, GSCLK			0.30 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–2	mA
I_{OL}	Low-level output current	SOUT			2	mA
f_{SCLK}	Data shift clock frequency	SCLK			25	MHz
f_{GSCLK}	Grayscale control clock frequency	GSCLK			33	MHz
t_{WH0}	High Pulse duration	SCLK	10			ns
t_{WL0}	Low Pulse duration	SCLK	10			ns
t_{WH1}	High Pulse duration	GSCLK	10			ns
t_{WL1}	Low Pulse duration	GSCLK	10			ns
t_{SU0}	Setup time	SIN to SCLK posedge	5			ns
t_{SU1}		LAT negedge to SCLK posedge (REFRESH = 0)	30			ns
t_{SU2}		LAT posedge for GS data written to GSCLK posedge when TMGRST = 0	50			ns
t_{SU3}		LAT posedge for GS data written to GSCLK posedge when TMGRST = 1	70			ns
t_{H0}	Hold time	SCLK posedge to SIN	2			ns
t_{H1}		SCLK posedge to LAT posedge	5			ns
t_{R0}	Rise time	SOUT		3	5	ns
t_{R0}	Fall time	SOUT		3	5	ns

6.6 Switching Characteristics (continued)

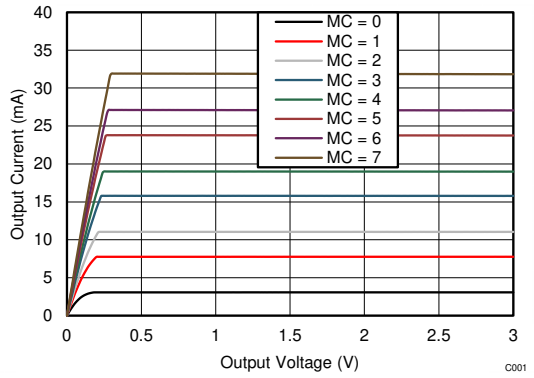
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D0}	Propogation delay	SCLK posedge to SOUT		20	30	ns
t_{D1}		VCC = 3.6 V, GSCLK posedge to OUTX4 and OUTX11 on or off		40		ns
t_{D2}		VCC = 3.6 V, GSCLK posedge to OUTX0 and OUTX15 on or off		43		ns
t_{D3}		VCC = 3.6 V, GSCLK posedge to OUTX5 and OUTX10 on or off		46		ns
t_{D4}		VCC = 3.6 V, GSCLK posedge to OUTX1 and OUTX14 on or off		49		ns
t_{D5}		VCC = 3.6 V, GSCLK posedge to OUTX2 and OUTX13 on or off		52		ns
t_{D6}		VCC = 3.6 V, GSCLK posedge to OUTX6 and OUTX9 on or off		55		ns
t_{D7}		VCC = 3.6 V, GSCLK posedge to OUTX3 and OUTX12 on or off		58		ns
t_{D8}		VCC = 3.6 V, GSCLK posedge to OUTX7 and OUTX8 on or off		61		ns
t_{ON_ERR}	Output on-time error(1)	tOUTON-tGSCLK, VCC = 3.6 V to 5.5 V, GSXn = 0001h, GSCLK = 33MHz, DCXn and BCXn = 7Fh	–20		20	ns

(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: $t_{ON\_ERR} = t_{OUT\_ON} - t_{GSCLK}$. t_{OUTON} is the actual on-time of the constant current driver. t_{GSCLK} is the GSCLK period.

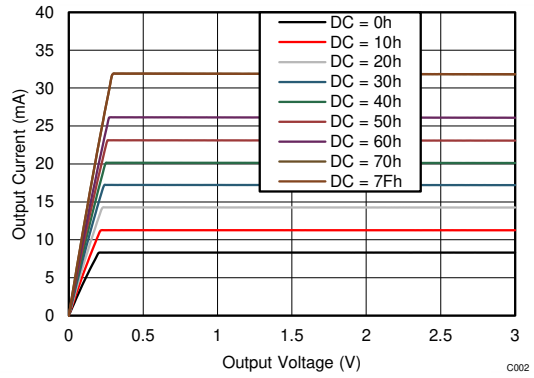
6.7 Typical Characteristics

At T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.



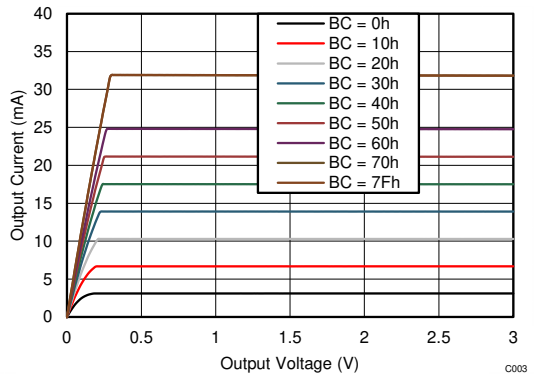
BCX = DCX*n* = 7Fh

图 6-1. Output Current vs Output Voltage (MCX Changing)



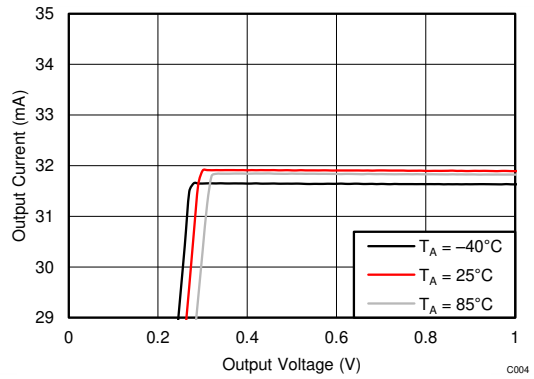
BCX = DCX*n* = 7Fh

图 6-2. Output Current vs Output Voltage (DCX*n* Changing)



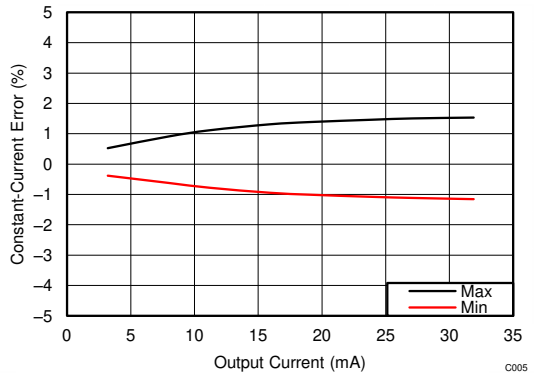
BCX = DCX*n* = 7Fh

图 6-3. Output Current vs Output Voltage (BCX Changing)



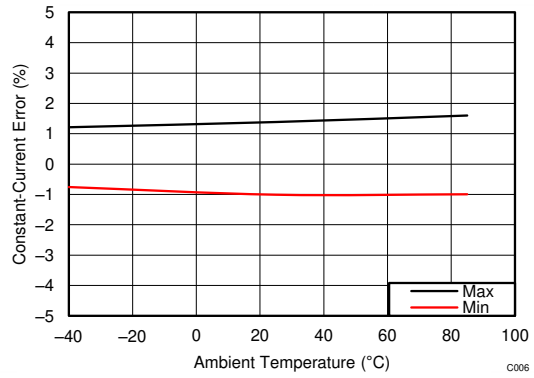
BCX = DCX*n* = 7Fh

图 6-4. Output Current vs Output Voltage (Temperature Changing)



BCX = DCX*n* = 7Fh V_{OUTXn} = 0.8 V

图 6-5. Constant-Current Error vs Output Current (Channel-to-Channel in Each Color Group)

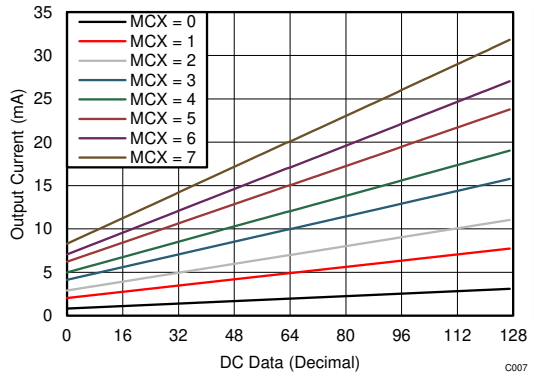


MCX = 4 BCX = DCX*n* = 7Fh V_{OUTXn} = 0.8 V

图 6-6. Constant-Current Error vs Ambient Temperature (Channel-to-Channel in Each Color Group)

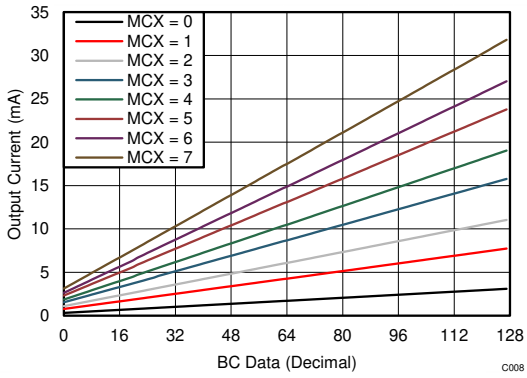
6.7 Typical Characteristics (continued)

At T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.



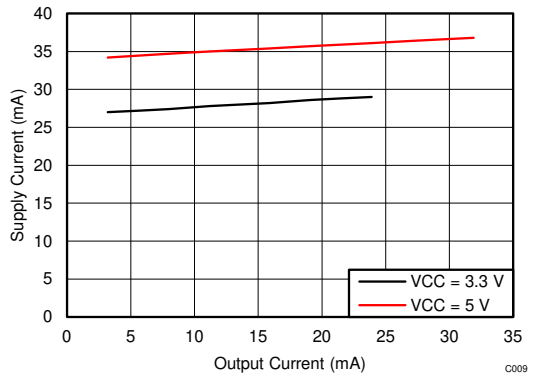
BCX = 7Fh V_{OUTXn} = 0.8 V

图 6-7. Dot Correction (DC) Linearity



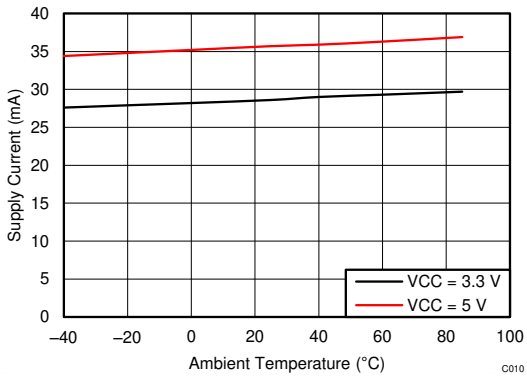
DCX*n* = 7Fh V_{OUTXn} = 0.8 V

图 6-8. Global Brightness Control (BC) Linearity



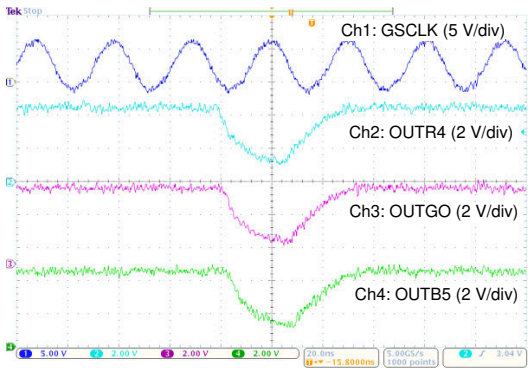
BCX = DCX*n* = 7Fh SIN = 12.5 MHz SCLK = 25 MHz
GSCLK = 33 MHz V_{OUT} = 0.8 V GSX*n* = FFFFh

图 6-9. Supply Current vs Output Current



MCX = 4 BCX = DCX*n* = 7Fh SIN = 12.5 MHz
SCLK = 25 MHz GSCLK = 33 MHz V_{OUT} = 0.8 V
GSX*n* = FFFFh

图 6-10. Supply Current vs Ambient Temperature



MCX = 7 BCX = DCX*n* = 7Fh GSCLK = 33 MHz
V_{LED} = 4.5 V R_L = 120 Ω GSX*n* = 0001h

图 6-11. Constant-Current Output Voltage Waveform

7 Parameter Measurement Information

7.1 Terminal-Equivalent Input and Output Schematic Diagrams

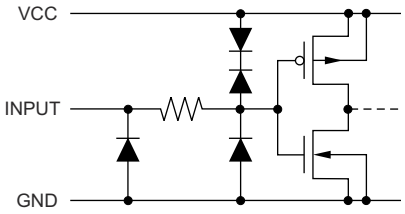


图 7-1. SIN, SCLK, LAT, GSCLK

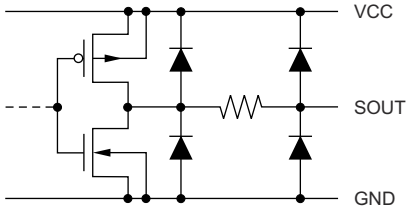
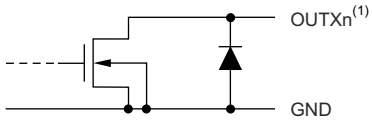


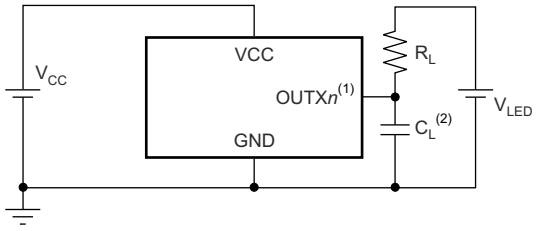
图 7-2. SOUT



A. X = R, G, or B; n = 0 to 15.

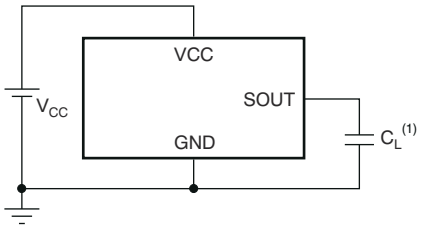
图 7-3. OUTX0 Through OUTX15

7.2 Test Circuits



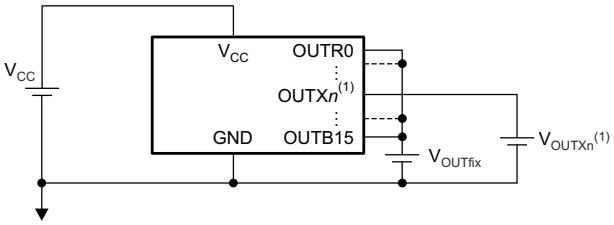
A. X = R, G, or B; n = 0 to 15.
B. C_L includes measurement probe and jig capacitance.

图 7-4. Rise Time and Fall Time Test Circuit for OUTX*n*



A. C_L includes measurement probe and jig capacitance.

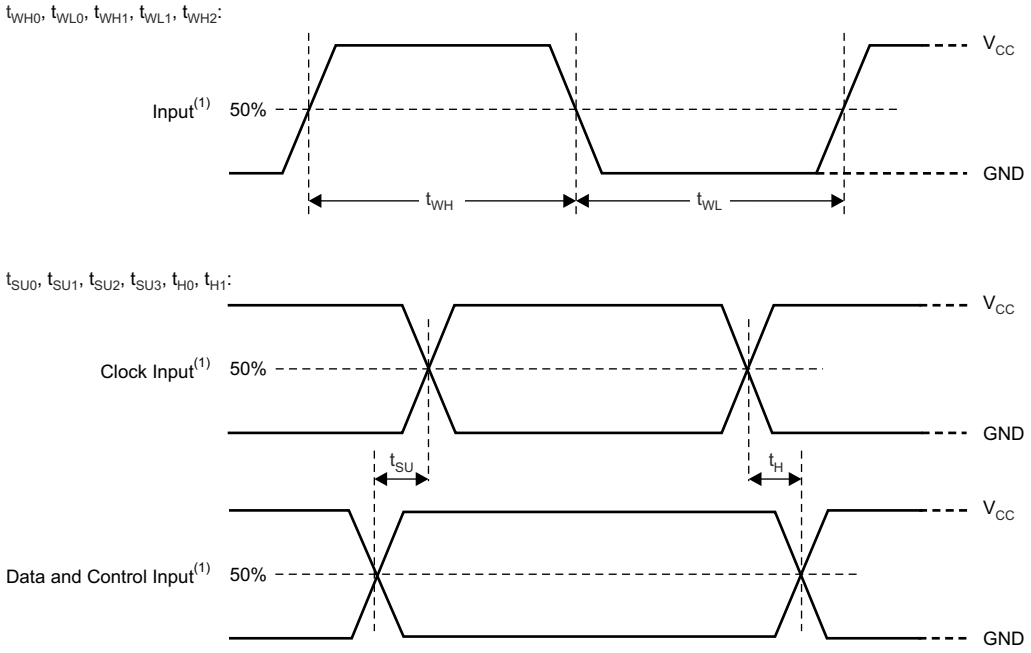
图 7-5. Rise Time and Fall Time Test Circuit for SOUT



A. X = R, G, or B; n = 0 to 15.

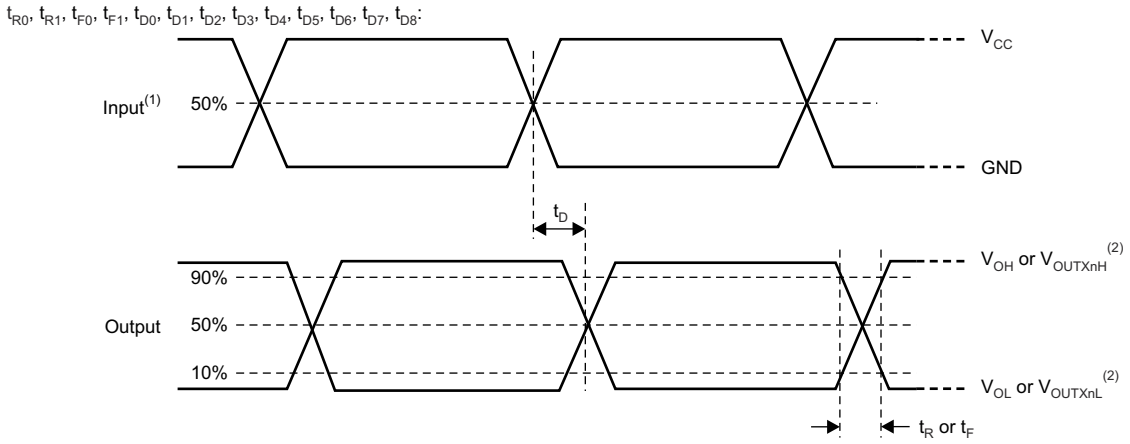
图 7-6. Constant-Current Test Circuit for OUTX*n*

7.3 Timing Diagrams



A. Input pulse rise and fall time is 1 ns to 3 ns.

图 7-7. Input Timing



A. Input pulse rise and fall time is 1 ns to 3 ns.
B. X = R, G, or B; n = 0 to 15.

图 7-8. Output Timing

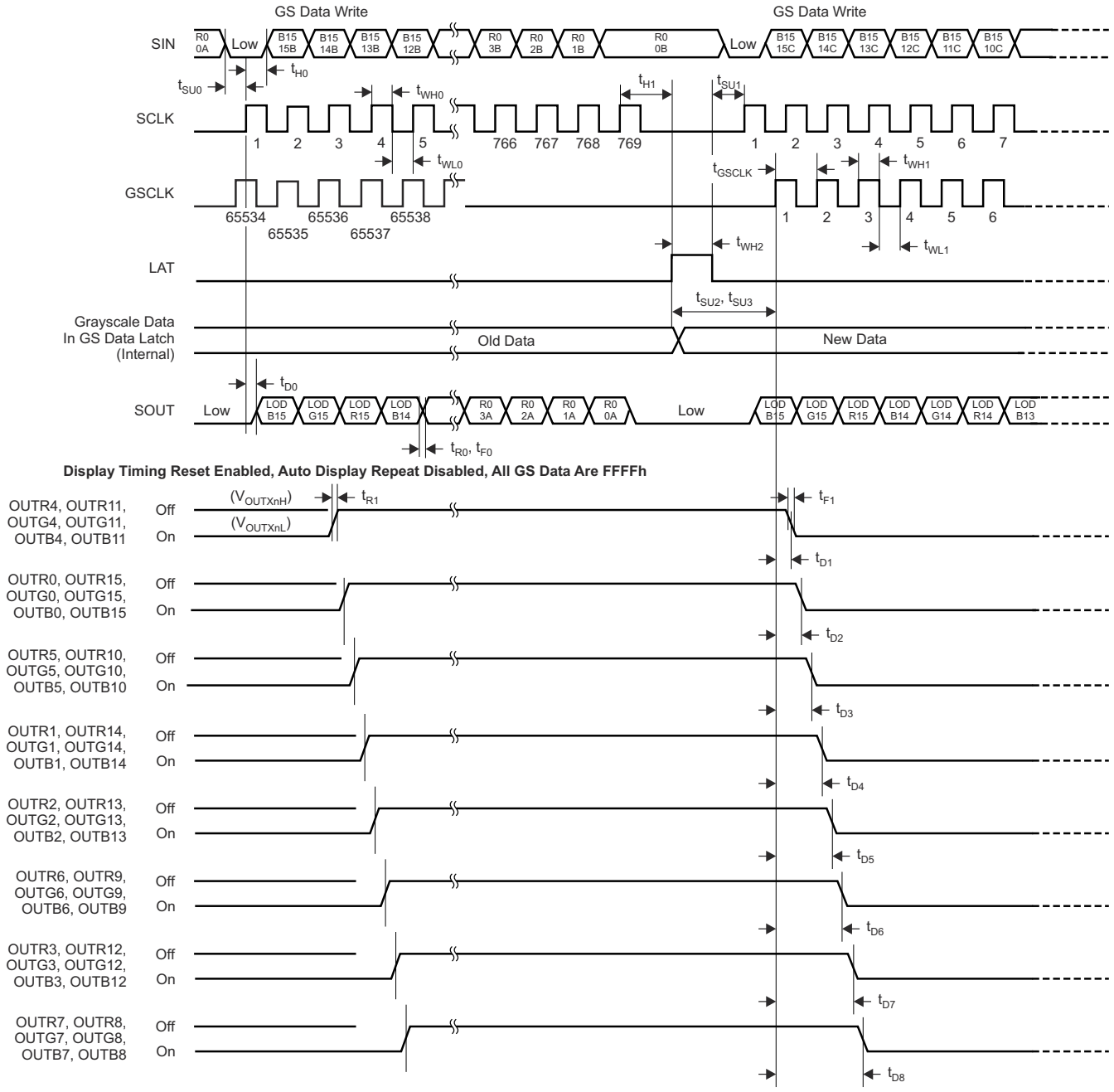


图 7-9. Data Input, Output, and Constant Output Timing

8 Detailed Description

8.1 Overview

The TLC6C5748-Q1 is 48-channel, 30-mA, constant-current LED driver that can control LED on-time with pulse width modulation (PWM) in 65,536 steps for grayscale (GS) control. A maximum of 281 trillion colors can be generated with red, green, and blue LEDs connected to the constant-current outputs.

The device has a 128-step, 7-bit, output current control function called *dot correction* (DC) that can control each constant-current output. Inherently, LED lamps have different intensities resulting from manufacturing differences. The DC function can reduce the inherent differences in intensity and improve LED lamp brightness uniformity.

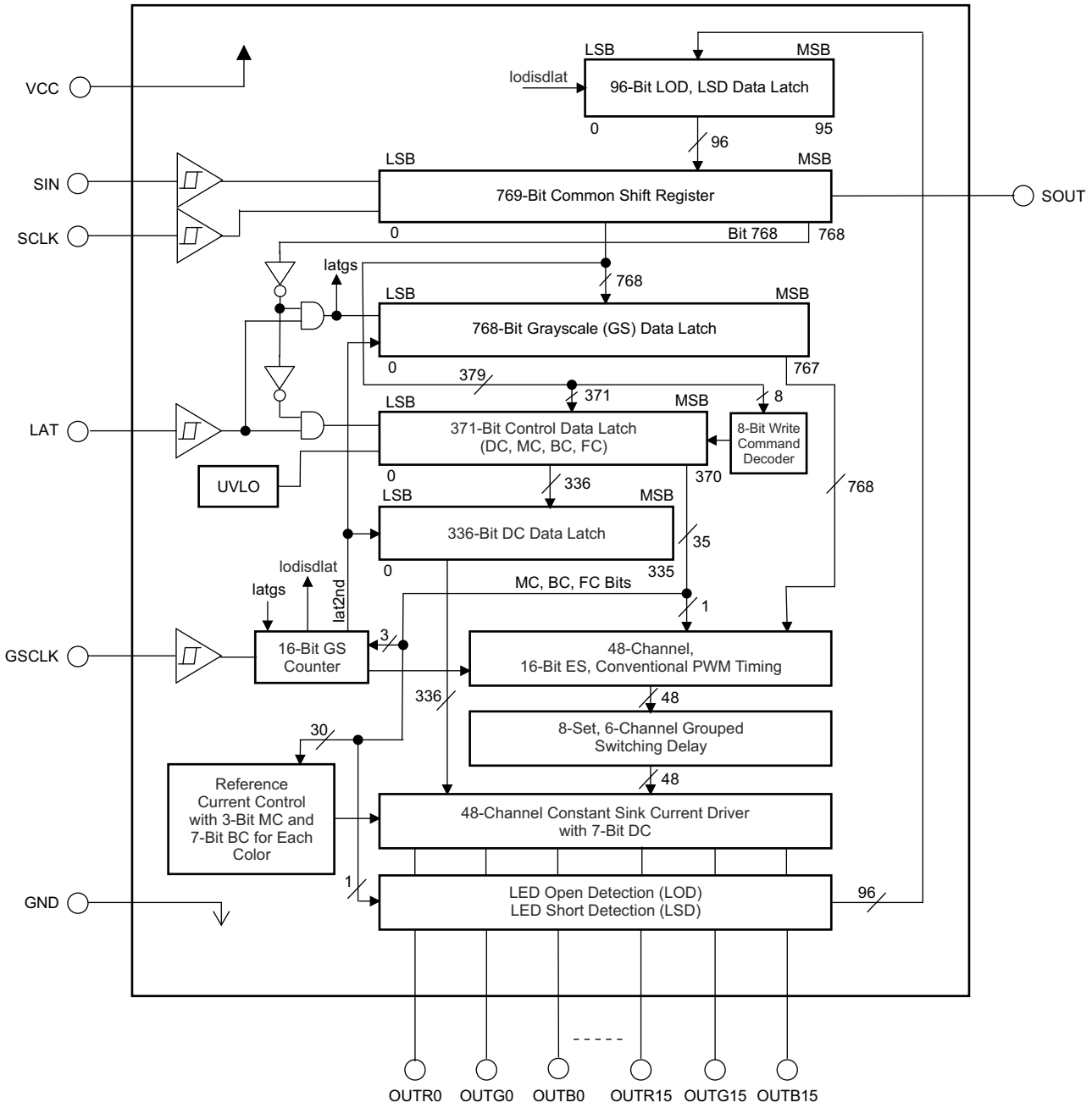
The device also has a 128-step, 7-bit, output current control function called *global brightness control* (BC) that can control each color group output. The BC function can adjust the red, green, and blue LED intensity for true white with constant-current control. The device contributes higher image quality to LED displays with fine white balance tuning by using these GS, DC, and BC functions.

The display controller can locate LED lamp failures via the device because the controller can detect LED lamp failures with the LED open detection (LOD) and LED short detection (LSD) functions and the reliability of the display can be improved by the LOD, LSD function.

The device maximum constant-current output value can be set by internal register data instead of the general method of using an external resistor setting. Thus, any failure modes that occur from the external resistor can be eliminated and one resistor can be eliminated.

The device constant-current output can drive approximately 19 mA at a 0.25-V output voltage and a +25°C ambient temperature. This voltage is called *knee* voltage. This 0.25-V, low-knee voltage can contribute to the design of a lower-power display system. The total number of LED drivers on one display panel can be reduced because 48 LED lamps can be driven by one LED driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Current Calculation

The output current value controlled by MC, DC, and BC can be calculated by 方程式 1.

$$I_{OUTn}\,(mA) = I_{OLCMax}\,(mA) \times \left[0.262 + 0.738 \times \frac{DCXn}{127}\right] \times \left[0.10 + 0.90 \times \frac{BCX}{127}\right] \quad (1)$$

where:

- I_{OLCMax} = the maximum constant-current value for all OUTX*n* for each color group programmed by MC data,
- DCX*n* = the dot correction value for each channel (0h to 7Fh),
- BCX = the global brightness control value (0h to 7Fh),
- X = R, G, or B for the red, green, or blue color group, and
- n = 0 to 15.

Each output sinks the I_{OLCMax} current when they turn on and the dot correction (DC) data and the global brightness control (BC) data are set to the maximum value of 7Fh (127d). Each output sink current can be reduced by lowering the DC and BC values.

When I_{OUT} is set lower than 1 mA by both MC and BC or BC only, the output may be unstable. Output currents lower than 1 mA can be achieved by setting I_{OUT} to 1 mA with MC and BC or BC only and then using DC to lower the output current.

8.3.2 Register and Data Latch Configuration

The TLC6C5748-Q1 has one common shift register and three data latches: the grayscale (GS) data latch, the control data latch, and the dot correction (DC) data latch. The common shift register is 769 bits long, the GS data latch is 768 bits long, the control data latch is 371 bits long, and the DC data latch is 336 bits long.

If the common shift register MSB is 0, the least significant 768 bits from the common shift register are latched into the GS data latch. If the MSB is 1, and bits 767 to 760 are 96h (10010110b), the data are latched into the control data latch. Refer to 图 8-1 for the common shift register, GS data latch, control data latch, and DC data latch configurations.

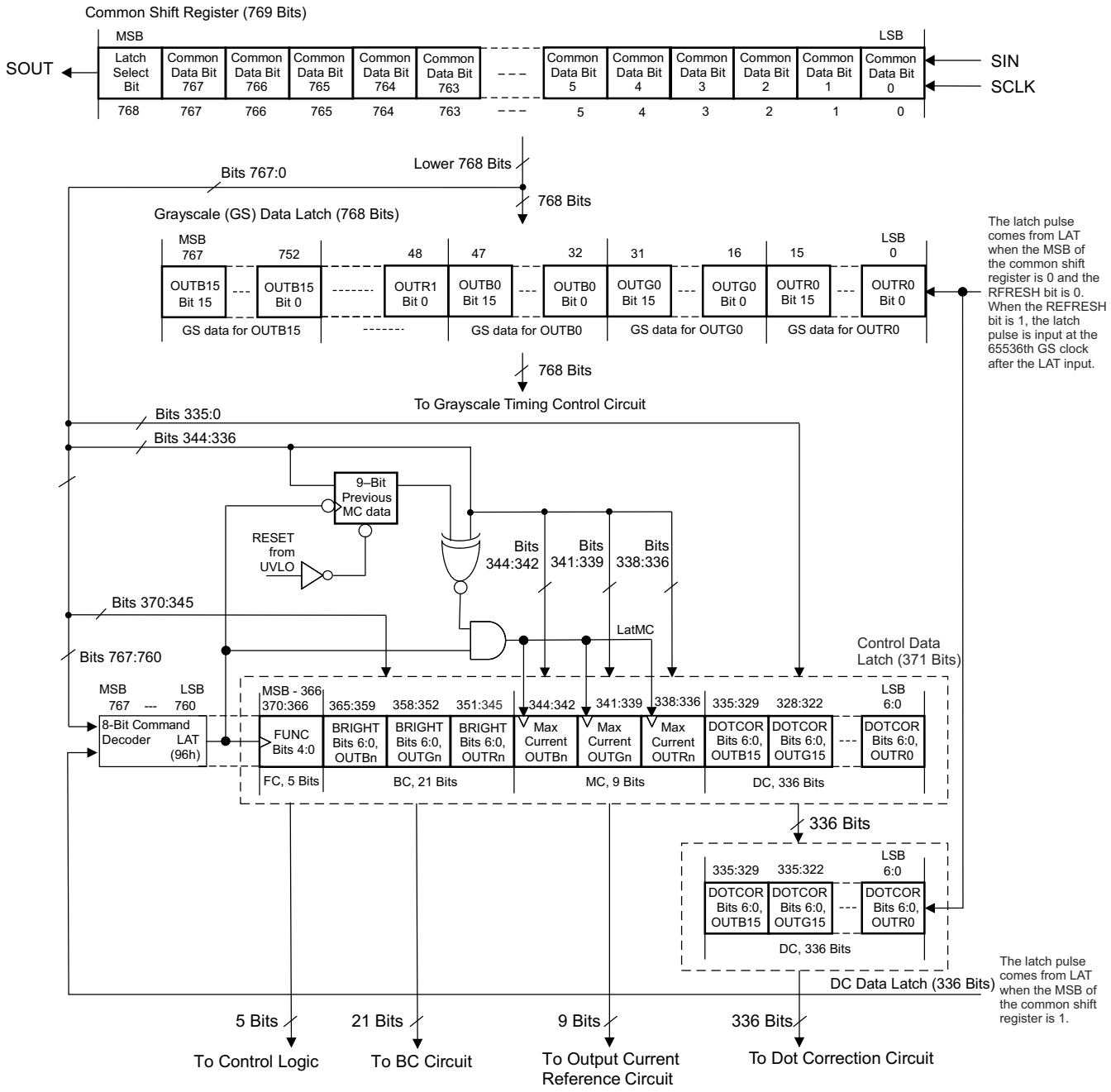


图 8-1. Common Shift Register and Data Latches Configuration

8.3.2.1 769-Bit Common Shift Register

The 769-bit common shift register is used to shift data from the SIN terminal into the TLC6C5748-Q1. The data shifted into the register are used for GS, DC, maximum output current, global BC functions, and function control data write operations. The common shift register LSB is connected to SIN and the MSB is connected to SOUT. On each SCLK rising edge, the data on SIN are shifted into the LSB and all 769 bits are shifted towards the MSB. The register MSB is always connected to SOUT. When the device is powered up, the data in the 769-bit common shift register are random.

8.3.2.2 Grayscale (GS) Data Latch

The GS data latch is 768 bits long, and sets the PWM timing for each constant-current output. The on-time of all constant-current outputs is controlled by the data in this data latch. The 768-bit GS data in the common shift register are copied to the data latch at a LAT rising edge when the common shift resister MSB is 0.

When the device is powered up, the data are random and all constant-current outputs are forced off. However, no outputs turn on until GS data are written to the GS data latch even if a GSCLK is input. The data bit assignment is shown in 表 8-1. Refer to 图 8-2 for a GS data write timing diagram.

表 8-1. Grayscale Data Latch Bit Description

GS DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL	GS DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL
15-0	GSR0[15:0]	N/A (no default value)	Bits[15:0] for OUTR0	399-384	GSR8[15:0]	N/A (no default value)	Bits[15:0] for OUTR8
31-16	GSG0[15:0]		Bits[15:0] for OUTG0	415-400	GSG8[15:0]		Bits[15:0] for OUTG8
47-32	GSB0[15:0]		Bits[15:0] for OUTB0	431-416	GSB8[15:0]		Bits[15:0] for OUTB8
63-48	GSR1[15:0]		Bits[15:0] for OUTR1	447-432	GSR9[15:0]		Bits[15:0] for OUTR9
79-64	GSG1[15:0]		Bits[15:0] for OUTG1	463-448	GSG9[15:0]		Bits[15:0] for OUTG9
95-80	GSB1[15:0]		Bits[15:0] for OUTB1	479-464	GSB9[15:0]		Bits[15:0] for OUTB9
111-96	GSR2[15:0]		Bits[15:0] for OUTR2	495-480	GSR10[15:0]		Bits[15:0] for OUTR10
127-112	GSG2[15:0]		Bits[15:0] for OUTG2	511-496	GSG10[15:0]		Bits[15:0] for OUTG10
143-128	GSB2[15:0]		Bits[15:0] for OUTB2	527-512	GSB10[15:0]		Bits[15:0] for OUTB10
159-144	GSR3[15:0]		Bits[15:0] for OUTR3	543-528	GSR11[15:0]		Bits[15:0] for OUTR11
175-160	GSG3[15:0]		Bits[15:0] for OUTG3	559-544	GSG11[15:0]		Bits[15:0] for OUTG11
191-176	GSB3[15:0]		Bits[15:0] for OUTB3	575-560	GSB11[15:0]		Bits[15:0] for OUTB11
207-192	GSR4[15:0]		Bits[15:0] for OUTR4	591-576	GSR12[15:0]		Bits[15:0] for OUTR12
223-208	GSG4[15:0]		Bits[15:0] for OUTG4	607-592	GSG12[15:0]		Bits[15:0] for OUTG12
239-224	GSB4[15:0]		Bits[15:0] for OUTB4	623-608	GSB12[15:0]		Bits[15:0] for OUTB12
255-240	GSR5[15:0]		Bits[15:0] for OUTR5	639-624	GSR13[15:0]		Bits[15:0] for OUTR13
271-256	GSG5[15:0]		Bits[15:0] for OUTG5	655-640	GSG13[15:0]		Bits[15:0] for OUTG13
287-272	GSB5[15:0]		Bits[15:0] for OUTB5	671-656	GSB13[15:0]		Bits[15:0] for OUTB13
303-288	GSR6[15:0]		Bits[15:0] for OUTR6	687-672	GSR14[15:0]		Bits[15:0] for OUTR14
319-304	GSG6[15:0]		Bits[15:0] for OUTG6	703-688	GSG14[15:0]		Bits[15:0] for OUTG14
335-320	GSB6[15:0]		Bits[15:0] for OUTB6	719-704	GSB14[15:0]		Bits[15:0] for OUTB14
351-336	GSR7[15:0]		Bits[15:0] for OUTR7	735-720	GSR15[15:0]		Bits[15:0] for OUTR15
367-352	GSG7[15:0]		Bits[15:0] for OUTG7	751-736	GSG15[15:0]		Bits[15:0] for OUTG15
383-368	GSB7[15:0]		Bits[15:0] for OUTB7	767-752	GSB15[15:0]		Bits[15:0] for OUTB15

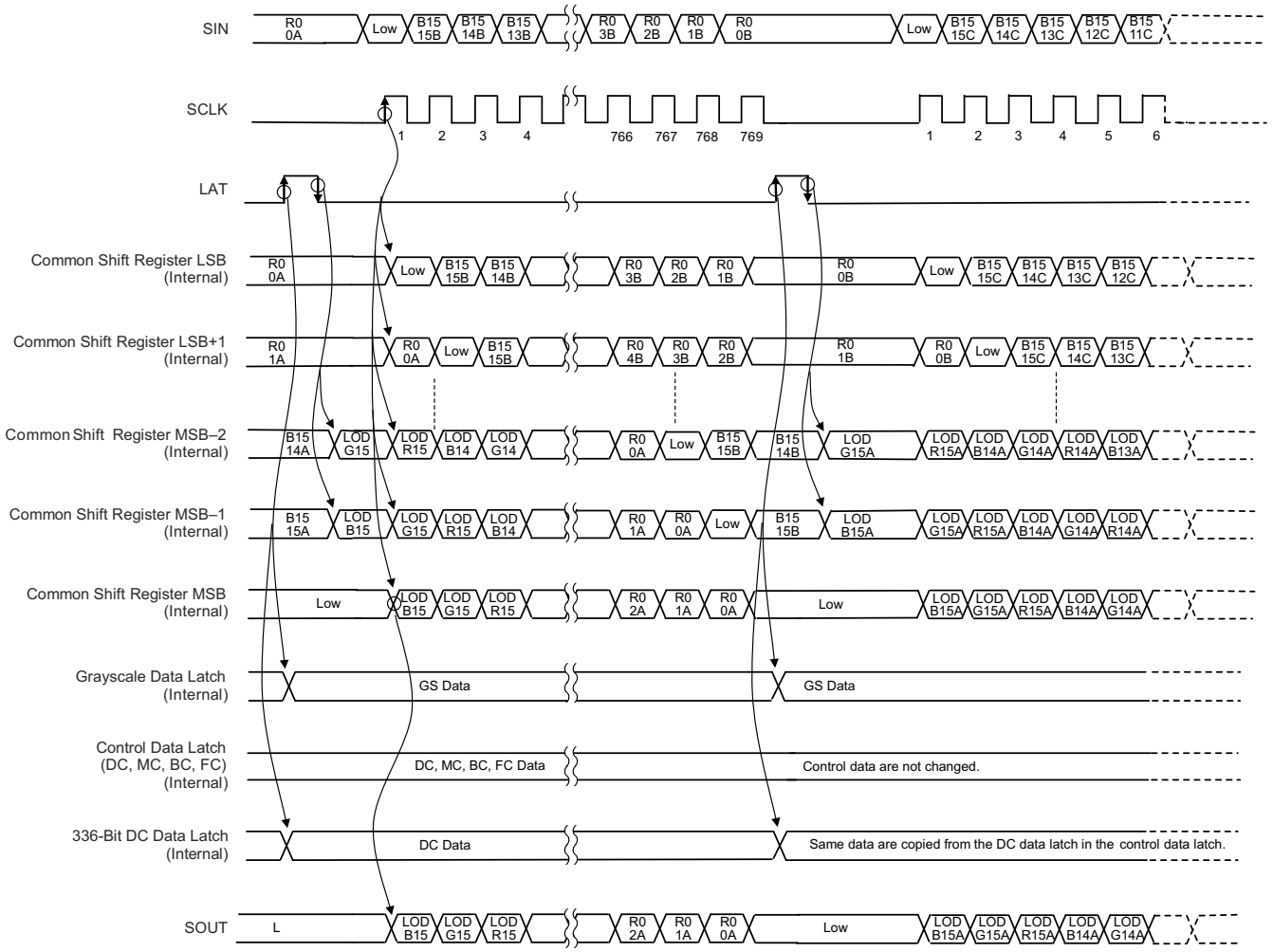


图 8-2. Grayscale Data Write Timing Diagram (RFRESH = 0)

8.3.2.3 Control Data Latch

The control data latch is 371 bits long. The data latch contains dot correction (DC) data, maximum current (MC) data, global brightness control (BC) data, and function control (FC) data. The DC for each constant-current output are controlled by the data in the DC data latch. The control data in the data latch are updated with the lower 371 bits of the common shift register at the LAT rising edge when the common shift register MSB is 1. The 336 bits of DC data are copied from the control data latch when the 65,536th GSCLK is input with RFRESH set to 1 in the control data latch after the GS data are written or the LAT rising edge for GS data writes is input when the RFRESH bit is 0.

When the device is powered up, the data in the control data latch (except the MC bits) are random. Therefore, DC, BC, and FC data must be written to the control data latch before turning on the constant-current outputs. Furthermore, MC data should be set appropriately for the application. Refer to 图 8-3 for a control data write timing diagram.

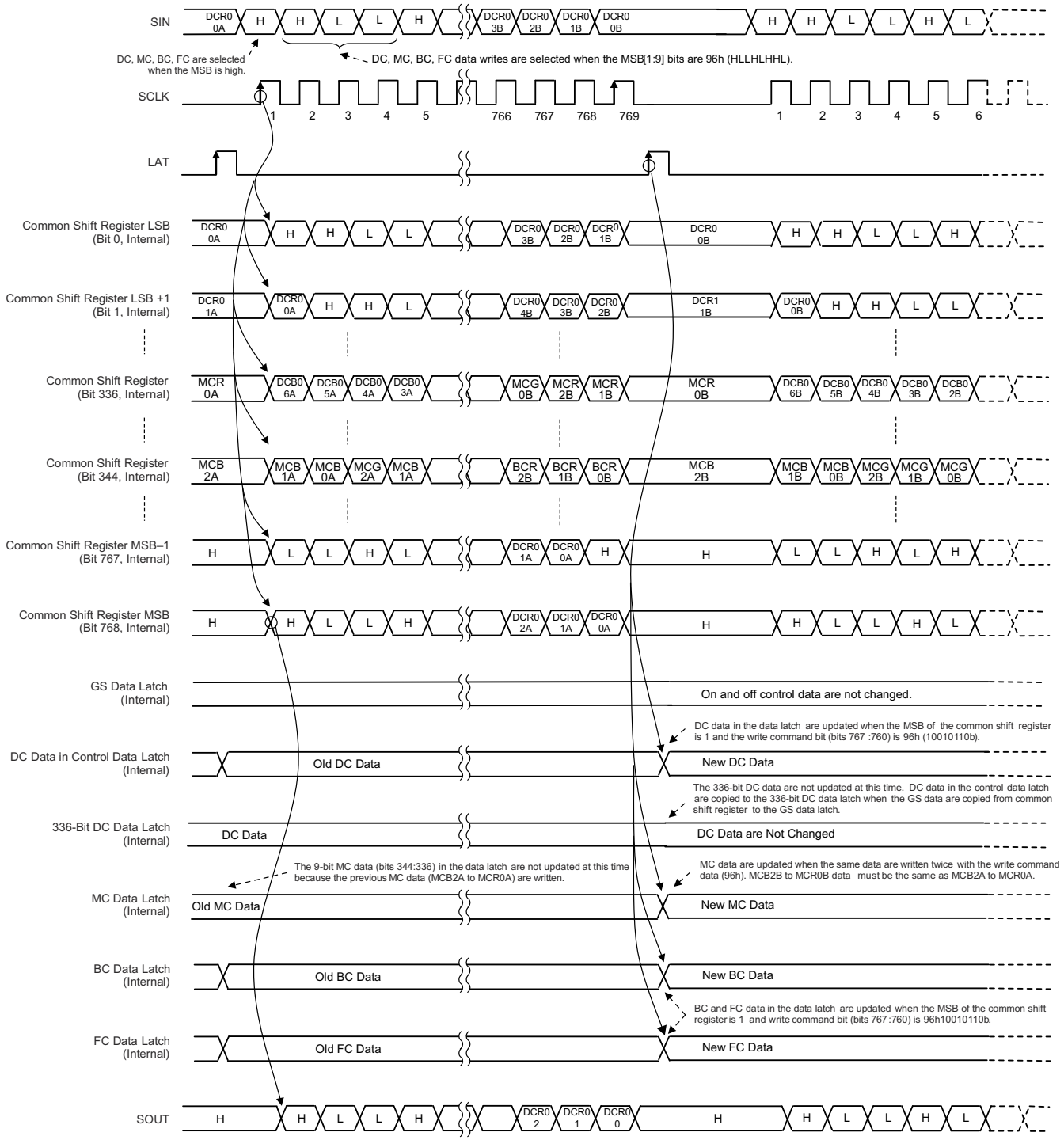


图 8-3. Control Data Write Timing Diagram for DC, MC, BC, and FC

8.3.2.4 Dot Correction (DC) Data Latch

DC data are 336 bits long; the data for each constant-current output are controlled by seven bits. Each constant-current output DC is controlled by the DC data latch. Each DC value individually adjusts the output current for each constant-current output. As explained in the *Dot Correction (DC) Function* section, the DC values are used to adjust the output current from 26.2% to 100% of the current value set by MC and BC data. When the device is powered on, the data in the DC data latch are random.

The DC data bit assignment is shown in 表 8-2. See 表 8-9 for a summary of the DC data value versus set current value.

表 8-2. Dot Correction Data Bit Description

CONTROL DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL	CONTROL DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL
6-0	DCR0[6:0]	N/A (no default value)	DC bits[6:0] for OUTR0	174-168	DCR8[6:0]	N/A (no default value)	DC bits[6:0] for OUTR8
13-7	DCG0[6:0]		DC bits[6:0] for OUTG0	181-175	DCG8[6:0]		DC bits[6:0] for OUTG8
20-14	DCB0[6:0]		DC bits[6:0] for OUTB0	188-182	DCB8[6:0]		DC bits[6:0] for OUTB8
27-21	DCR1[6:0]		DC bits[6:0] for OUTR1	195-189	DCR9[6:0]		DC bits[6:0] for OUTR9
34-28	DCG1[6:0]		DC bits[6:0] for OUTG1	202-196	DCG9[6:0]		DC bits[6:0] for OUTG9
41-35	DCB1[6:0]		DC bits[6:0] for OUTB1	209-203	DCB9[6:0]		DC bits[6:0] for OUTB9
48-42	DCR2[6:0]		DC bits[6:0] for OUTR2	216-210	DCR10[6:0]		DC bits[6:0] for OUTR10
55-49	DCG2[6:0]		DC bits[6:0] for OUTG2	223-217	DCG10[6:0]		DC bits[6:0] for OUTG10
62-56	DCB2[6:0]		DC bits[6:0] for OUTB2	230-224	DCB10[6:0]		DC bits[6:0] for OUTB10
69-63	DCR3[6:0]		DC bits[6:0] for OUTR3	237-231	DCR11[6:0]		DC bits[6:0] for OUTR11
76-70	DCG3[6:0]		DC bits[6:0] for OUTG3	244-238	DCG11[6:0]		DC bits[6:0] for OUTG11
83-77	DCB3[6:0]		DC bits[6:0] for OUTB3	251-245	DCB11[6:0]		DC bits[6:0] for OUTB11
90-84	DCR4[6:0]		DC bits[6:0] for OUTR4	258-252	DCR12[6:0]		DC bits[6:0] for OUTR12
97-91	DCG4[6:0]		DC bits[6:0] for OUTG4	265-259	DCG12[6:0]		DC bits[6:0] for OUTG12
104-98	DCB4[6:0]		DC bits[6:0] for OUTB4	272-266	DCB12[6:0]		DC bits[6:0] for OUTB12
111-105	DCR5[6:0]		DC bits[6:0] for OUTR5	279-273	DCR13[6:0]		DC bits[6:0] for OUTR13
118-112	DCG5[6:0]		DC bits[6:0] for OUTG5	286-280	DCG13[6:0]		DC bits[6:0] for OUTG13
125-119	DCB5[6:0]		DC bits[6:0] for OUTB5	293-287	DCB13[6:0]		DC bits[6:0] for OUTB13
132-126	DCR6[6:0]		DC bits[6:0] for OUTR6	300-294	DCR14[6:0]		DC bits[6:0] for OUTR14
139-133	DCG6[6:0]		DC bits[6:0] for OUTG6	307-301	DCG14[6:0]		DC bits[6:0] for OUTG14
146-140	DCB6[6:0]		DC bits[6:0] for OUTB6	314-308	DCB14[6:0]		DC bits[6:0] for OUTB14
153-147	DCR7[6:0]		DC bits[6:0] for OUTR7	321-315	DCR15[6:0]		DC bits[6:0] for OUTR15
160-154	DCG7[6:0]		DC bits[6:0] for OUTG7	328-322	DCG15[6:0]		DC bits[6:0] for OUTG15
167-161	DCB7[6:0]		DC bits[6:0] for OUTB7	335-329	DCB15[6:0]		DC bits[6:0] for OUTB15

8.3.2.5 Maximum Current (MC) Data Latch

The maximum output current per channel, I_{OLCMax}, is programmed by MC data and can be set with the serial interface. I_{OLCMax} is the largest current for each output. Each output sinks the I_{OLCMax} current when they turn on with DC and BC data set to the maximum value of 7Fh (127d). MC data must have the same data continuously written twice in order to change the data. When the device is powered on, the MC data are set to 0.

The MC data bit assignment is shown in 表 8-3. See 表 8-8 for a summary of the MC data value for each color group versus the set current value.

表 8-3. Maximum Current Data Bit Assignment in the Control Data Latch

CONTROL DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL
338-336	MCR[2:0]	0	MC bits[2:0] for red color group channels (OUTR0 to OUTR15)
341-339	MCG[2:0]	0	MC bits[2:0] for green color group channels (OUTG0 to OUTG15)

表 8-3. Maximum Current Data Bit Assignment in the Control Data Latch (continued)

CONTROL DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL
344-342	MCB[2:0]	0	MC bits[2:0] for blue color group channels (OUTB0 to OUTB15)

8.3.2.6 Global Brightness Control (BC) Data Latch

Global BC data are seven bits long. The global brightness for all outputs is controlled by the data in the control data latch. The data are used to adjust the constant-current values for the 48-channel constant-current outputs. As explained in the *Global Brightness Control (BC) Function* section, the BC values are used to adjust the output current from 10% to 100% of the maximum value. When the device is powered on, the BC data are random.

The global BC data bit assignment in the control data latch is shown in 表 8-4. See 表 8-10 for a summary of the BC data value versus set current value.

表 8-4. Global Brightness Control Data Bit Assignment in the Control Data Latch

CONTROL DATA LATCH BIT NUMBER	BIT NAME	DEFAULT VALUE	CONTROLLED CHANNEL
351-345	BCR[6:0]	N/A (no default value)	BC bits[6:0] for red color group channels (OUTR0 to OUTR15)
358-352	BCG[6:0]		BC bits[6:0] for green color group channels (OUTG0 to OUTG15)
365-359	BCB[6:0]		BC bits[6:0] for blue color group channels (OUTB0 to OUTB15)

8.3.2.7 Function Control (FC) Data Latch

The FC data latch is 5 bits long. This latch enables the auto display repeat and display timing reset functions, and sets the DC data auto refresh, PWM control mode, and the LSD detection voltage. Each function is selected by the data in the control data latch. When the device is powered on, the FC data are random. The FC data bit assignment in the control data latch is shown in 表 8-5.

表 8-5. Function Control Data Latch Bit Description

BIT NUMBER	BIT NAME	DEFAULT VALUE (Binary)	DESCRIPTION
366	DSPRPT	N/A (no default value)	Auto display repeat mode enable bit. 0 = Disabled, 1 = Enabled. When this bit is 0, the auto display repeat function is disabled. Each constant-current output is turned on and off for one display period. When this bit is 1, each output repeats the PWM control every 65,536 GSCLKs.
367	TMGRST		Display timing reset mode enable bit. 0 = Disabled, 1 = Enabled. When this bit is 0, the GS counter is not reset and the outputs are not forced off even when a LAT rising edge is input for a GS data write. When this bit is 1, the GS counter is reset to 0 and all outputs are forced off at the LAT rising edge for a GS data write. Afterwards, PWM control resumes from the next GSCLK rising edge.
368	RFRESH		Auto data refresh mode enable bit. 0 = Disabled, 1 = Enabled. When this bit is 0, the auto data refresh function is disabled. The data in the common shift register are copied to the GS data latch at the next LAT rising edge for a GS data write. DC data in the control data latch are copied to the DC data latch at the same time. When this bit is 1, the auto data refresh function is enabled. The data in the common shift register are copied to the GS data latch at the 65,536th GSCLK after the LAT rising edge for a GS data write. DC data in the control data latch are copied to the DC data latch at the same time.
369	ESPWM		ES-PWM mode enable bit. 0 = Disabled, 1 = Enabled. When this bit is 0, the conventional PWM control mode is selected. If the TLC6C5748-Q1 is used for multiplexing a drive, the conventional PWM mode should be selected to prevent excess on or off switching. When this bit is 1, ES-PWM control mode is selected.
370	LSDVLT		LSD detection voltage selection bit. LED short detection (LSD) detects a fault caused by a shorted LED by comparing the OUTX*n* voltage to the LSD detection threshold voltage. The threshold voltage is selected by this bit. When this bit is 0, the LSD voltage is VCC × 70%. When this bit is 1, the LSD voltage is VCC × 90%.

8.3.3 Status Information Data (SID)

The status information data (SID) contains the status of the LED open detection (LOD), LED short detection (LSD) and thermal shutdown faults(TSD). When the MSB of the common shift register is set to 0 and the RFRESH bit in the control data latch is 0, the SID are loaded to the common shift register at the LAT falling edge after the data in the common shift register are loaded to the grayscale data latch. If the common shift register MSB is 1, the SID are not loaded to the common shift register.

When the MSB of the common shift register is set to 0 and the RFRESH bit in the control data latch is 1, the SID are loaded to the common shift register at the GS counter 0000h just after LAT when the GS data are input. If the common shift register MSB is 1, the SID are not loaded to the common shift register. When the RFRESH bit is 1, the SCLK rising edge must be input with a low-level LAT signal after 65,538 GSCLKs (or more) are input from the LAT rising signal input.

After being loaded into the common shift register, new SID data cannot be loaded until at least one new bit of data is written into the common shift register. To recheck SID without changing the GS data, reprogram the common shift register with the same data currently programmed into the GS latch. When LAT goes high, the GS data do not change, but new SID data are loaded into the common shift register. LOD and LSD are shifted out of SOUT with each SCLK rising edge. The SID load configuration is shown in 图 8-4 and 表 8-6.

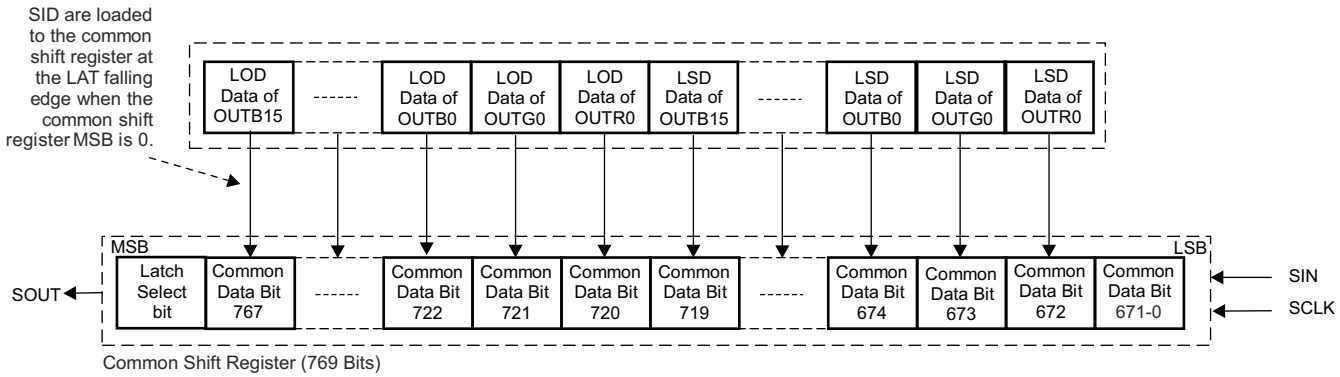


图 8-4. SID Load Configuration

表 8-6. SID Load Description

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID	COMMON SHIFT REGISTER BIT NUMBER	LOADED SID
671-0	No data loaded	720	OUTR0 LOD data
672	OUTR0 LSD data (0 = No error, 1 = Error)	721	OUTG0 LOD data
673	OUTG0 LSD data	722	OUTB0 LOD data
674	OUTB0 LSD data	723	OUTR1 LOD data
675	OUTR1 LSD data	724	OUTG1 LOD data
676	OUTG1 LSD data	725	OUTB1 LOD data
677	OUTB1 LSD data	726	OUTR2 LOD data
678	OUTR2 LSD data	727	OUTG2 LOD data
679	OUTG2 LSD data	728	OUTB2 LOD data
680	OUTB2 LSD data	729	OUTR3 LOD data
681	OUTR3 LSD data	730	OUTG3 LOD data
682	OUTG3 LSD data	731	OUTB3 LOD data
683	OUTB3 LSD data	732	OUTR4 LOD data
684	OUTR4 LSD data	733	OUTG4 LOD data
685	OUTG4 LSD data	734	OUTB4 LOD data
686	OUTB4 LSD data	735	OUTR5 LOD data
687	OUTR5 LSD data	736	OUTG5 LOD data
688	OUTG5 LSD data	737	OUTB5 LOD data
689	OUTB5 LSD data	738	OUTR6 LOD data
690	OUTR6 LSD data	739	OUTG6 LOD data
691	OUTG6 LSD data	740	OUTB6 LOD data
692	OUTB6 LSD data	741	OUTR7 LOD data
693	OUTR7 LSD data	742	OUTG7 LOD data
694	OUTG7 LSD data	743	OUTB7 LOD data
695	OUTB7 LSD data	744	OUTR8 LOD data
696	OUTR8 LSD data	745	OUTG8 LOD data
697	OUTG8 LSD data	746	OUTB8 LOD data
698	OUTB8 LSD data	747	OUTR9 LOD data
699	OUTR9 LSD data	748	OUTG9 LOD data
700	OUTG9 LSD data	749	OUTB9 LOD data
701	OUTB9 LSD data	750	OUTR10 LOD data
702	OUTR10 LSD data	751	OUTG10 LOD data
703	OUTG10 LSD data	752	OUTB10 LOD data
704	OUTB10 LSD data	753	OUTR11 LOD data
705	OUTR11 LSD data	754	OUTG11 LOD data
706	OUTG11 LSD data	755	OUTB11 LOD data
707	OUTB11 LSD data	756	OUTR12 LOD data
708	OUTR12 LSD data	757	OUTG12 LOD data
709	OUTG12 LSD data	758	OUTB12 LOD data
710	OUTB12 LSD data	759	OUTR13 LOD data
711	OUTR13 LSD data	760	OUTG13 LOD data
712	OUTG13 LSD data	761	OUTB13 LOD data
713	OUTB13 LSD data	762	OUTR14 LOD data
714	OUTR14 LSD data	763	OUTG14 LOD data
715	OUTG14 LSD data	764	OUTB14 LOD data
716	OUTB14 LSD data	765	OUTR15 LOD data
717	OUTR15 LSD data	766	OUTG15 LOD data
718	OUTG15 LSD data	767	OUTB15 LOD data

表 8-6. SID Load Description (continued)

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID	COMMON SHIFT REGISTER BIT NUMBER	LOADED SID
719	OUTB15 LSD data	768	No data loaded

8.3.4 LED Open Detection (LOD)

LOD detects a fault caused by an LED open circuit or a short from OUTX*n* to ground with low resistance by comparing the OUTX*n* voltage to the LOD detection threshold voltage (0.3 V, typically). If the OUTX*n* voltage is lower than the threshold voltage when OUTX*n* is on, that output LOD bit is set to 1 to indicate an open LED. Otherwise, the LOD bit is set to 0. LOD data are only valid for outputs that are programmed to be on. LOD data are latched into the LOD, LSD data latch at the 33rd GSCLK. LOD data for outputs programmed to be off at the 33rd GSCLK are always 0. The LED open detection circuit is shown in 图 8-5 and 表 8-7 lists an LOD truth table. Refer to 图 8-6 for an LOD read timing diagram.

8.3.5 LED Short Detection (LSD)

LSD data detect a fault caused by a shorted LED between LED terminals by comparing the OUTX*n* voltage to the LSD detection threshold voltage level set by LSDVLT in the control data latch. If the OUTX*n* voltage is higher than the programmed voltage when OUTX*n* is on, the corresponding output LSD bit is set to 1 to indicate a shorted LED. Otherwise, the LSD bit is set to 0. LSD data are only valid for outputs that are programmed to be on. LSD data are latched into the LOD, LSD data latch at the 33rd GSCLK. LSD data for outputs programmed to be off at the 33rd GSCLK are always 0. The LSD open detection circuit is shown in 图 8-5 and 表 8-7 lists an LSD truth table. Refer to 图 8-6 for an LSD read timing diagram.

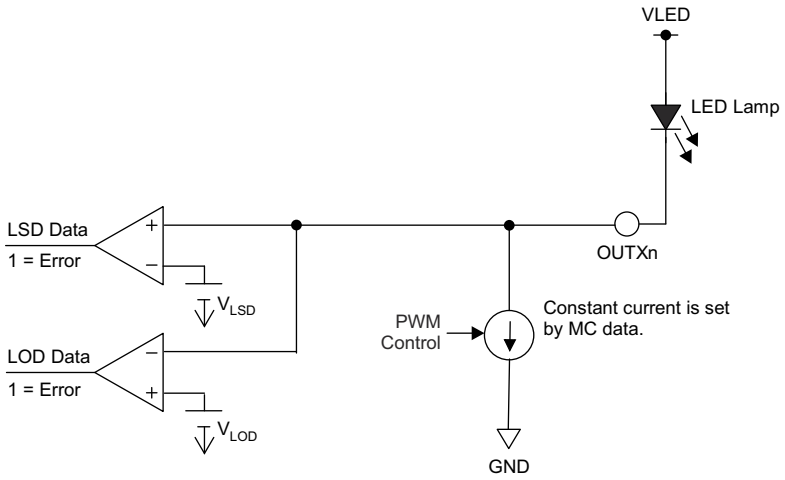


图 8-5. LOD and LSD Circuit

表 8-7. LOD and LSD Truth Table

SID DATA	CONDITION	
	LOD	LSD
0	LED is not opened ($V_{OUTXn} > V_{LOD}$)	LED is not shorted ($V_{OUTXn} \leqslant V_{LSD}$)
1	LED is open or shorted to GND ($V_{OUTXn} \leqslant V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTXn} > V_{LSD}$)

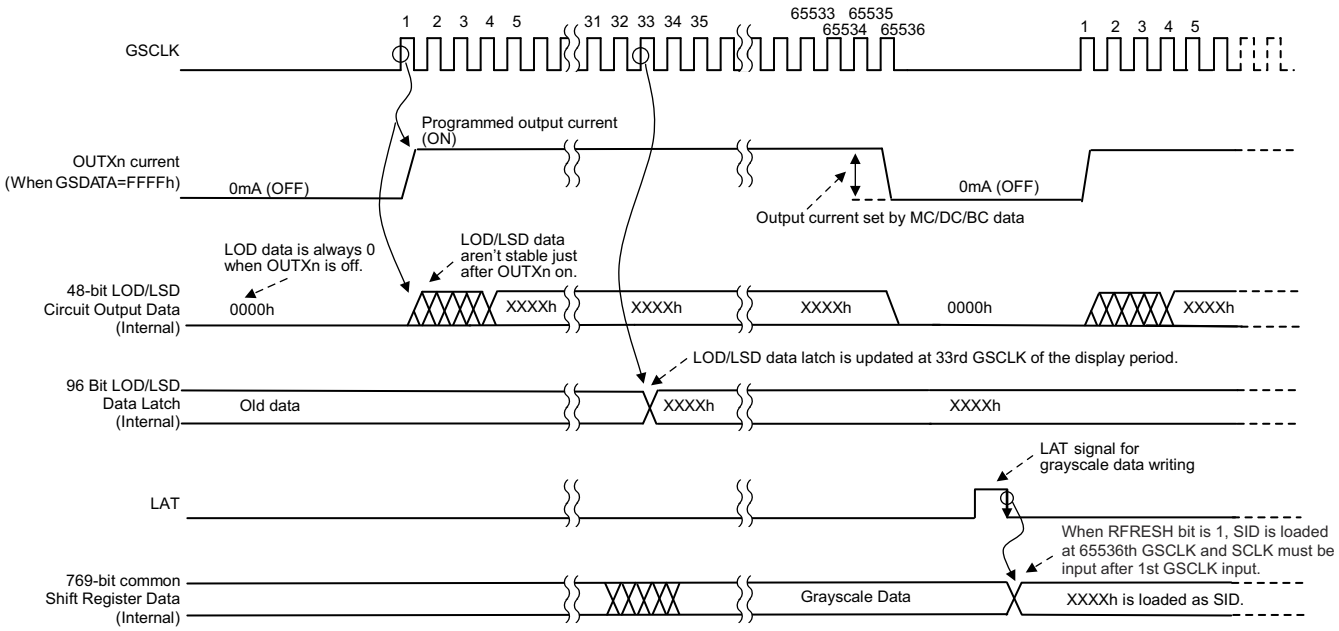


图 8-6. LOD and LSD Read and Load Timing Diagram

8.3.6 Thermal Shutdown Faults (TSD)

If the die temperature of TLC6C5748-Q1 reaches the thermal shutdown threshold T_{SD_R}, the LED outputs of TLC6C5748-Q1 shut down to protect the device from damage. OUTB8's LOD & LSD bit will be set simultaneously to indicate this fault. The device restarts the LED outputs when temperature drops by T_{SD_HYS} amount. OUTB8's LOD & LSD bit will also be reset when TSD fault is recovered.

The internal temperature sensing block is closest to OUTB8 channel. If some channels of TLC6C5748-Q1 need to be left unused, not leaving OUTB8 / OUTG8 / OUTR8 channel unused is recommended. This is to avoid the internal temperature sensing block in the coldest area of the die.

8.3.7 Noise Reduction

Large surge currents may flow through the device and the board on which the device is mounted if all 48 outputs turn on simultaneously at the start of each GS cycle. These large current surges can introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC6C5748-Q1 independently turns the outputs on with a series delay for each group to provide a soft-start feature. The output current sinks are grouped into eight groups. The first output group that is turned on or off are OUTR4, OUTG4, OUTB4, OUTR11, OUTG11, and OUTB11; the second output group is OUTX0 and OUTX15; the third output group is OUTX5 and OUTX10; the fourth output group is OUTX1 and OUTX14; the fifth output group is OUTX2 and OUTX13; the sixth output group is OUTX6 and OUTX9; the seventh output group is OUTX3 and OUTX12; and the eighth output group is OUTX7 and OUTX8. Each output group is turned on and off sequentially with a small delay between groups.

8.4 Device Functional Modes

8.4.1 Maximum Current Control (MC) Function

The maximum output current per channel, I_{OLCMax}, is programmed by the MC data and is set with the serial interface. I_{OLCMax} is the largest current for each output. Each OUTX*n* sinks the I_{OLCMax} current when they turn on and the dot correction and global brightness control data are set to the maximum value of 7Fh (127d).

When the device is powered on, the MC data are set to 0. MC data should be changed when all constant-current outputs (OUTX*n*, where X = R, G, or B; n = 0 to 7) are off. MCX = 6 and MCX = 7 are used when V_{CC} is greater than 3.6 V. The same MC data must be written twice to change the maximum constant-current output. 表 8-8 shows the characteristics of the constant-current sink versus the maximum current (MC) control data.

表 8-8. Maximum Constant-Current Output versus MC Data

MCX(2) DATA			I_{OLCMax} (mA), OUTX*n* (3)
BINARY	DECIMAL	HEX	
000 (default)	0 (default)	0 (default)	3.2
001	1	1	8.0
010	2	2	11.2
011	3	3	15.9
100	4	4	19.1
101	5	5	23.9
110(1)	6	6	27.1
111(1)	7	7	31.9

(1) MCX7 and MCX6 can be used when V_{CC} is greater than 3.6 V.
(2) X = R, G, or B.
(3) X = R, G, or B. n = 0 to 15.

8.4.2 Dot Correction (DC) Function

The TLC6C5748-Q1 can individually adjust the output current of each channel (OUTx0 to OUTx15, where x is R, G, or B) by using DC. The DC function allows the brightness deviations of the LEDs connected to each output to be individually adjusted. Each output DC is programmed with a 7-bit word, so the value is adjusted with 128 steps within the range of 26.2% to 100% of I_{OLCMax}. DC data are programmed into the TLC6C5748-Q1 with the serial interface. When the device is powered on, the DC data in the control latch contains random data. Therefore, DC data must be written to the DC data latch before turning the constant-current outputs on. 表 8-9 summarizes the DC data value versus the set current value.

表 8-9. DC Data versus Current Ratio and Set Current Value

DCX*n* (3) DATA			BC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax} (%)	I_{OUT} (mA) (MC = 7, typical)	I_{OUT} (mA) (MC = 0, typical)
BINARY	DECIMAL	HEX				
000 0000	0	00	7F	26.2	8.36	0.84
000 0001	1	01	7F	26.7	8.54	0.86
000 0010	2	02	7F	27.3	8.73	0.88
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.8	31.5	3.16
111 1110	126	7E	7F	99.4	31.7	3.18
111 1111	127	7F	7F	100.0	31.9	3.20

8.4.3 Global Brightness Control (BC) Function

The TLC6C5748-Q1 has the ability to adjust the output current of all constant-current outputs of each color group (OUTR0 to OUTR15, OUTG0 to OUTG15, and OUTB0 to OUTB15) simultaneously to the same current ratio. This function is called *global brightness control* (BC). The BC function allows the global brightness of LEDs

connected to the output to be adjusted. All outputs of each color group can be adjusted in 128 steps from 10% to 100% of the maximum output current, I_{OLCMax}. BC data are programmed into the TLC6C5748-Q1 with the serial interface. When the BC data change, the output current also changes immediately. When the device is powered on, the BC data contain random data. 表 8-10 summarizes the BC data versus the set current value.

表 8-10. BC Data versus Constant-Current Ratio and Set Current Value

BCX[2] DATA			DCX*n* [3] DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax}(%)	I_{OUT} (mA) (MC = 7, typical)	I_{OUT} (mA) (MC = 0, typical)
BINARY	DECIMAL	HEX				
000 0000	0	00	7F	10.0	3.19	0.32
000 0001	1	01	7F	10.7	3.42	0.34
000 0010	2	02	7F	11.4	3.64	0.37
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.6	31.5	3.15
111 1110	126	7E	7F	99.3	31.7	3.18
111 1111	127	7F	7F	100.0	31.9	3.20

8.4.4 Grayscale (GS) Function (PWM Control)

The TLC6C5748-Q1 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65,536 brightness steps, from 0% up to 100% brightness.

The PWM operation for OUT*n* is controlled by a 16-bit grayscale (GS) counter. The GS counter increments on each GS reference clock (GSCLK) rising edge. The GS counter resets to 0000h when the LAT rising signal for a GS data write is input with the display timing reset mode enabled.

The TLC6C5748-Q1 has two types of PWM control: conventional PWM control and enhanced spectrum (ES) PWM control. The conventional PWM control can be selected when the ESPWM bit in the control data latch is 0. The ES PWM control is selected when the ESPWM bit is 1. The conventional PWM control should be selected for multiplexing a drive. The ES-PWM control should be selected for a static drive.

The on-time (t_{OUT_ON}) of each output (OUT*n*) can be calculated by Equation 2.

$$t_{OUT\_ON}\ (ns) = t_{GSCLK}\ (ns) \times GSXn \quad (2)$$

where:

- t_{GSCLK} = one GS clock period,
- GSX*n* = the programmed GS value for OUTX*n* (GSX*n* = 0d to 65535d),
- X = R, G, or B for the red, green, or blue color group, and
- n = 0 to 15.

表 8-11 summarizes the GS data values versus the output on-time duty cycle. When the device powers up, all OUTX*n* are forced off, the GS counter initializes to 0000h, and the status remains the same until GS data are written. After that, each OUTX*n* on and off status can be controlled by GS data and GSCLK.

表 8-11. Output Duty Cycle and On-Time versus GS Data

GS DATA		ON-TIME DUTY (%)	GS DATA		ON-TIME DUTY (%)
DECIMAL	HEX		DECIMAL	HEX	
0	0	0	32768	8000	50.000
1	1	0.002	32769	8001	50.002
2	2	0.003	32770	8002	50.003
3	3	0.005	32771	8003	50.005
—	—	—	—	—	—
8191	1FFF	12.498	40959	9FFF	62.498
8192	2000	12.500	40960	A000	62.500
8193	2001	12.502	40961	A001	62.502
—	—	—	—	—	—
16381	3FFD	24.996	49149	BFFD	74.995
16382	3FFE	24.997	49150	BFFE	74.997
16383	3FFF	24.998	49151	BFFF	74.998
16384	4000	25.000	49152	C000	75.000
16385	4001	25.002	49153	C001	75.002
16386	4002	25.003	49154	C002	75.003
16387	4003	25.005	49155	C003	75.005
—	—	—	—	—	—
24575	5FFF	37.498	57343	DFFF	87.498
24576	6000	37.500	57344	E000	87.500
24577	6001	37.502	57345	E001	87.502
—	—	—	—	—	—
32765	7FFD	49.995	65533	FFFD	99.995
32766	7FFE	49.997	65534	FFFE	99.997
32767	7FFF	49.998	65535	FFFF	99.998

8.4.4.1 Conventional PWM Control

The first GS clock rising edge increments the GS counter by one and switches on all outputs with a non-zero GS value programmed into the GS data latch. Each additional GS clock rising edge increases the corresponding GS counter by one.

The GS counter keeps track of the number of clock pulses from the respective GS clock inputs. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off at the GS counter value rising edge when the counter becomes greater than the output GS latch value. 图 8-7 illustrates the conventional PWM operation.

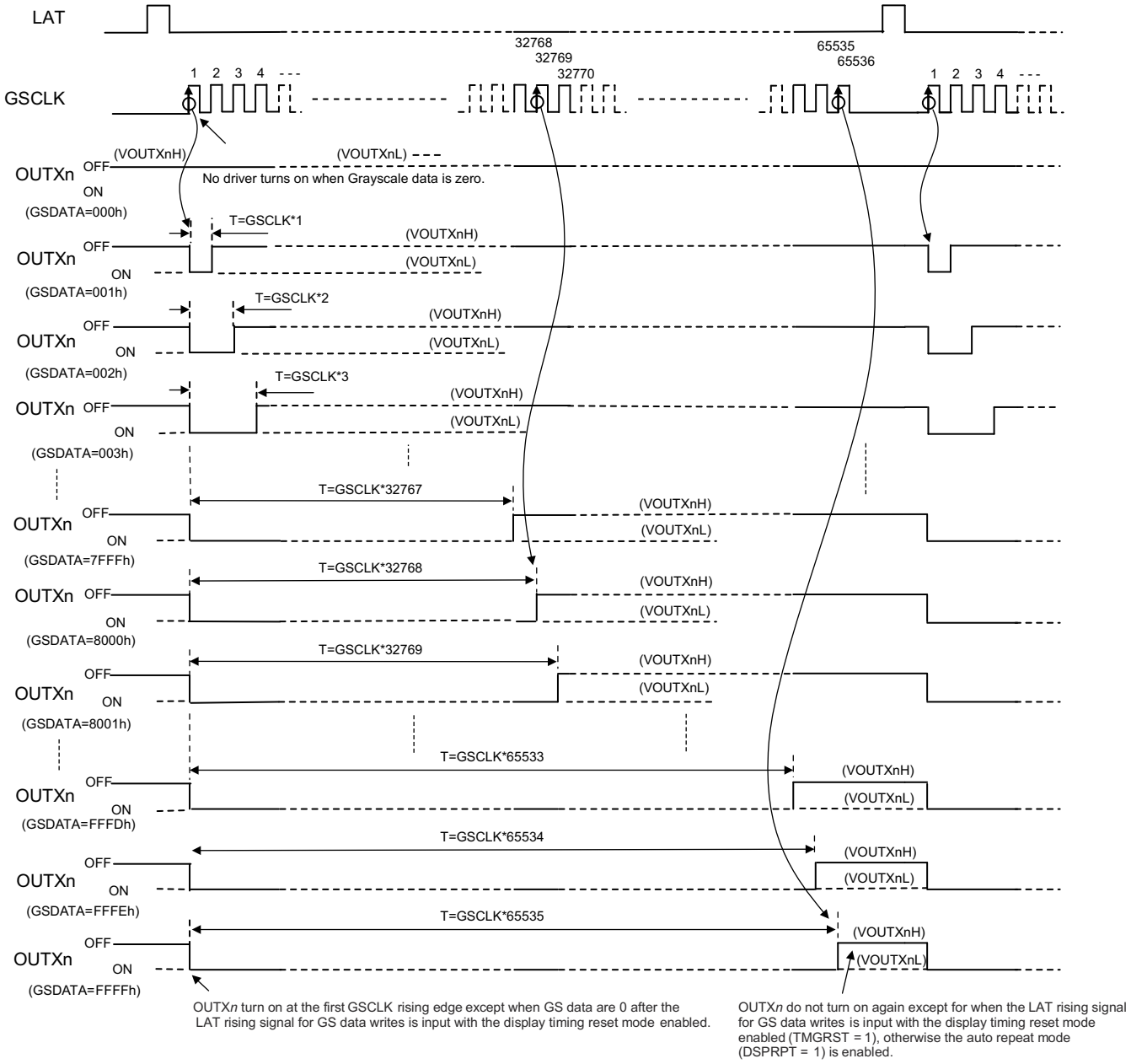


图 8-7. Conventional PWM Operation

8.4.4.2 Enhanced Spectrum (ES) PWM Control

In this PWM control, the total display period is divided into 128 display segments. The total display period is the time from the first GS clock (GSCLK) to the 65,536th GSCLK input. Each display segment has a maximum of

512 GSCLKs. The OUTX*n* on-time changes, depending on the 16-bit GS data. Refer to 表 8-12 for the sequence of information and to 图 8-8 for the timing information.

表 8-12. ES PWM Drive Turn On-Time Length

GS DATA		OUT*n* DRIVER OPERATION
DECIMAL	HEX	
0	0000h	Does not turn on
1	0001h	Turns on for one GSCLK period in the first display segment
2	0002h	Turns on for one GSCLK period in the first and 65th display segments
3	0003h	Turns on for one GSCLK period in the first, 65th, and 33rd display segments
4	0004h	Turns on for one GSCLK period in the first, 65th, 33rd, and 97th display segments
5	0005h	Turns on for one GSCLK period in the first, 65th, 33rd, 97th, and 17th display segments
6	0006h	Turns on for one GSCLK period in the first, 65th, 33rd, 97th, 17th, and 81st display segments
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
127	007Fh	Turns on for one GSCLK period in the first to 127th display segments, but does not turn on in the 128th display segment
128	0080h	Turns on for one GSCLK period in all display segments (first to 128th)
129	0081h	Turns on for two GSCLK periods in the first display period and for one GSCLK period in all other display periods
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
255	00FFh	Turns on for two GSCLK periods in the first to 127th display segments and turns on one GSCLK period in the 128th display segment
256	0100h	Turns on for two GSCLK periods in all display segments (first to 128th)
257	0101h	Turns on for three GSCLK periods in the first display segments and for two GSCLK periods in all other display segments
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
65479	FEFFh	Turns on for 511 GSCLK periods in the first to 127th display segments, but only turns on for 510 GSCLK periods in the 128th display segment
65480	FF00h	Turns on for 511 GSCLK periods in all display segments (first to 128th)
65481	FF01h	Turns on for 512 GSCLK periods in the first display period and for 511 GSCLK periods in the second to 128th display segments
—	—	—
65534	FFFEh	Turns on for 512 GSCLK periods in the first to 63rd and 65th to 127th display segments; also turns on for 511 GSCLK periods in the 64th and 128th display segments
65535	FFFFh	Turns on for 512 GSCLK periods in the first to 127th display segments but only turns on for 511 GSCLK periods in the 128th display segment

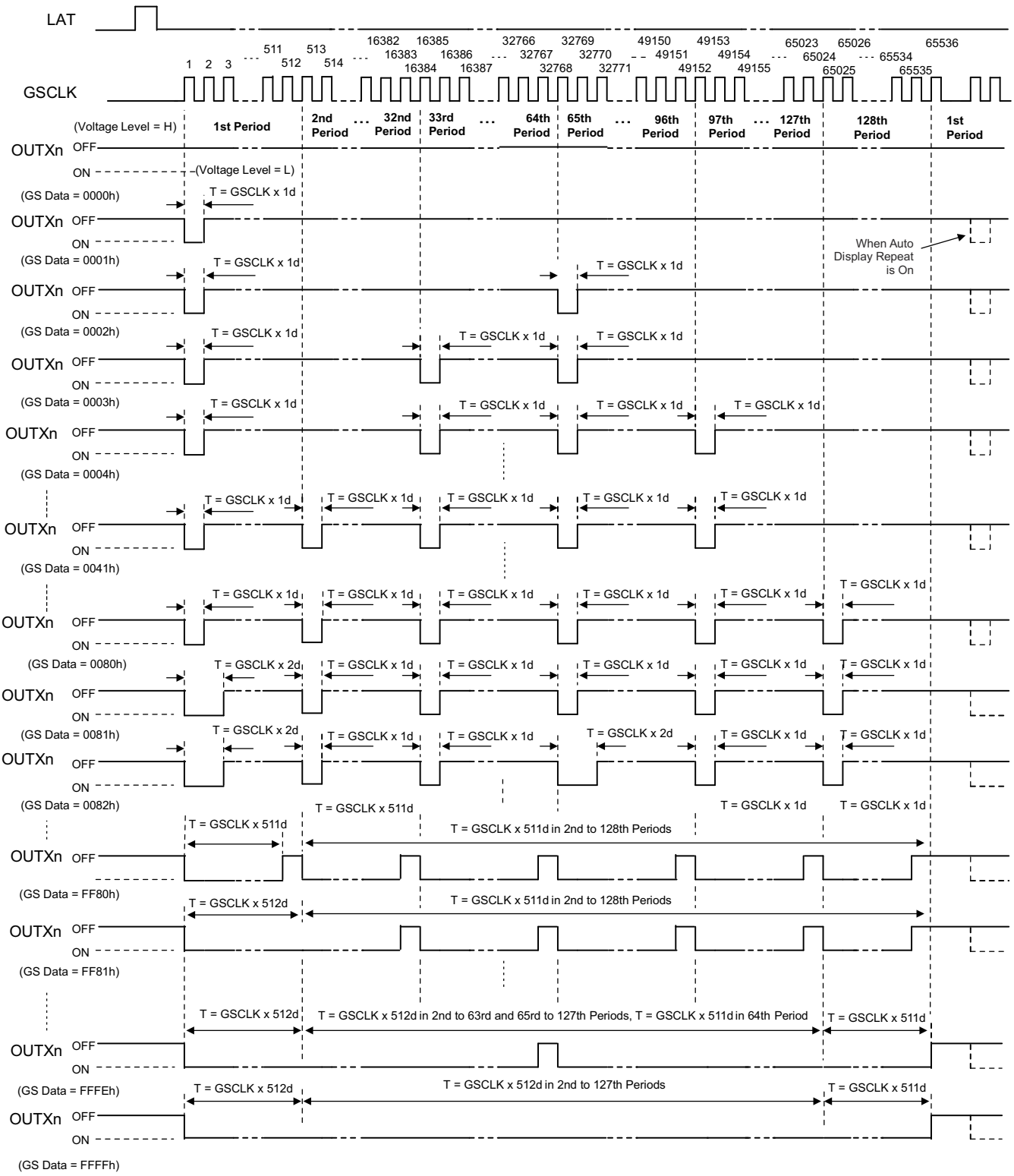


图 8-8. ES PWM Operation

8.4.4.3 Auto Display Repeat Function

This function can repeat the total display period as long as GSCLK is present, as shown in 图 8-9. This function is switched on or off by the content of the DSPRPT bit in the control data latch.

When the DSPRPT bit is 1, auto display repeat is enabled and the entire display period repeats. When the DSPRPT bit is 0, auto display repeat is disabled and the entire display period only executes one time after a LAT signal rising edge is input for GS data writes when the display timing reset is enabled.

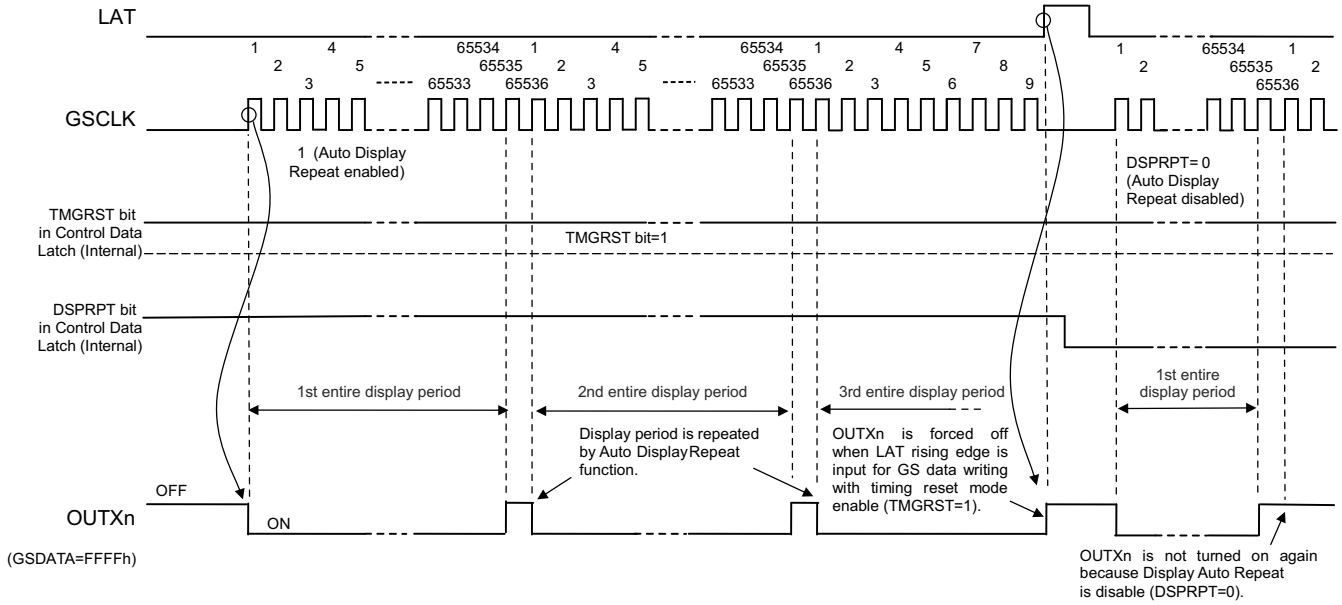


图 8-9. Auto Display Repeat Function

8.4.4.4 Display Timing Reset Function

The display timing reset function allows initializing the display timing with a LAT rising edge. This function can be switched on or off with the TMGRST bit in the control data latch. When the TMGRST bit is 1, the GS counter is reset to 0 and all outputs are forced off at the LAT rising edge for a GS data write. Furthermore, the 768-bit GS data latch is updated with the data from the common shift register and the 336-bit DC data latch is updated with the DC data in the 371-bit control data latch. When the TMGRST bit is 0, the GS counter is not reset and the outputs are not forced off, even if a LAT rising edge is input. A timing diagram for this function is shown in 图 8-10.

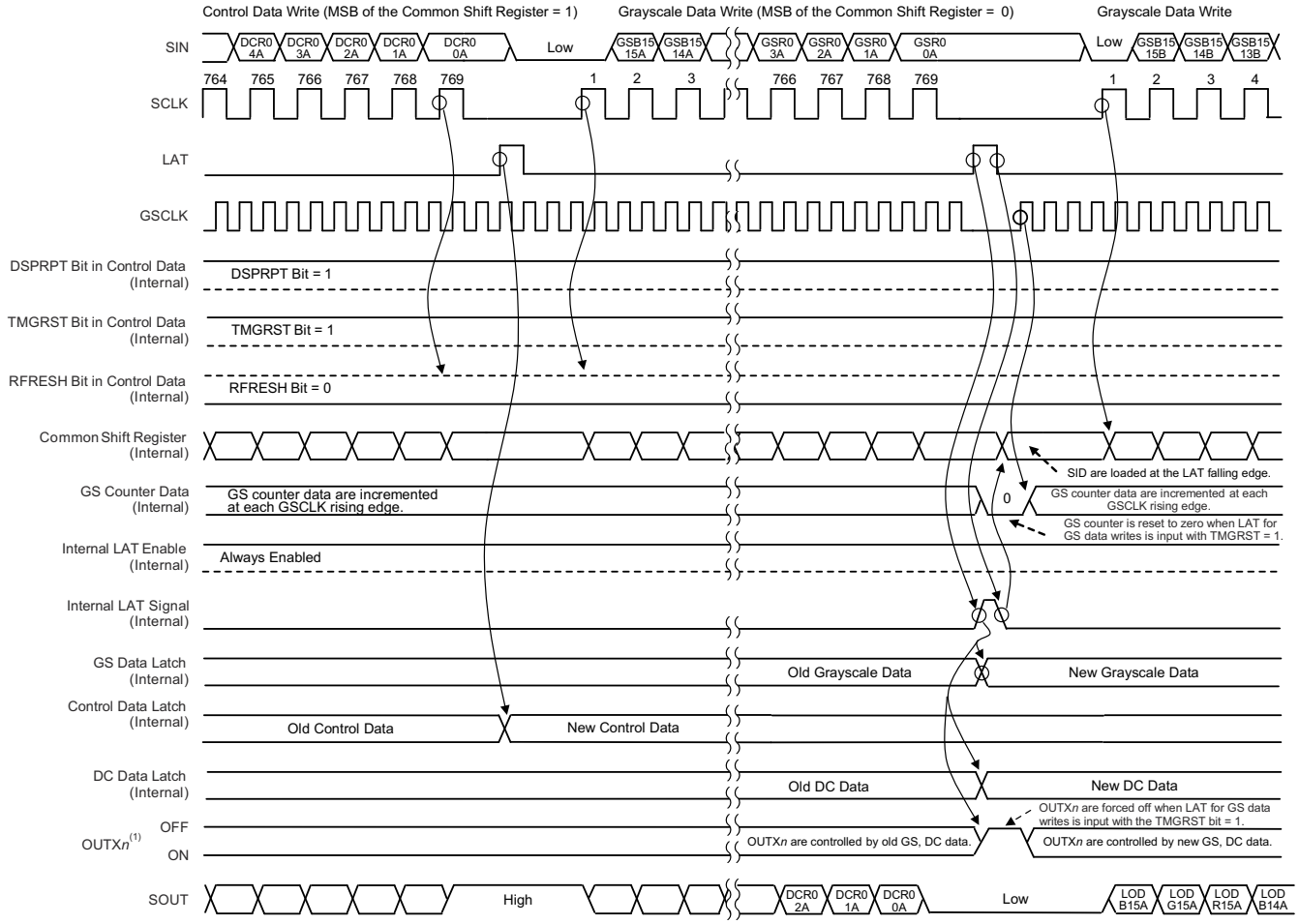


图 8-10. Display Timing Reset Function (DSPRPT = 1, TMGRST = 1, and RFRESH = 0)

8.4.4.5 Auto Data Refresh Function

This function delays updating the grayscale (GS) and dot correction (DC) data until the end of one entire display period. If both DC data and GS data are written by the end of an entire display period, the input DC data are held in the control data latch and the GS data are held in the common shift register. Both DC and GS data are copied to the 336-bit DC data latch and 768-bit GS data latch at the end of an entire display period. The data latches are used for the next display period. GS data are directly copied from the common shift register to the GS data latch. Therefore, GS data must be written after the DC data are written. Furthermore, the GS data in the common shift resistor must not be changed until all data are copied to the GS data latch. 图 8-11 and 图 8-12 show timing diagrams for this function.

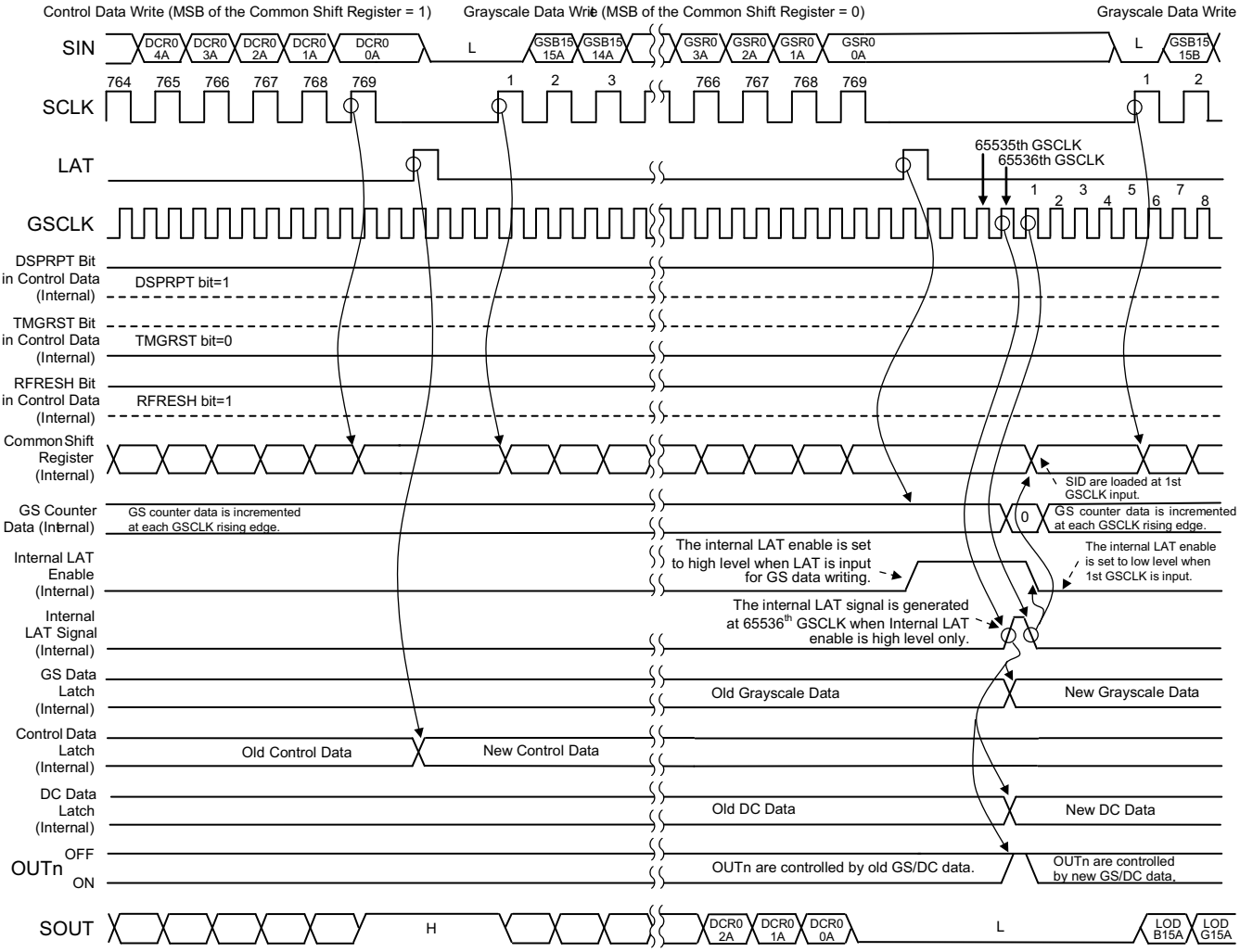


图 8-11. Auto Data Refresh Function 1 (DSPRPT = 1, TMGRST = 0, and RFRESH = 1)

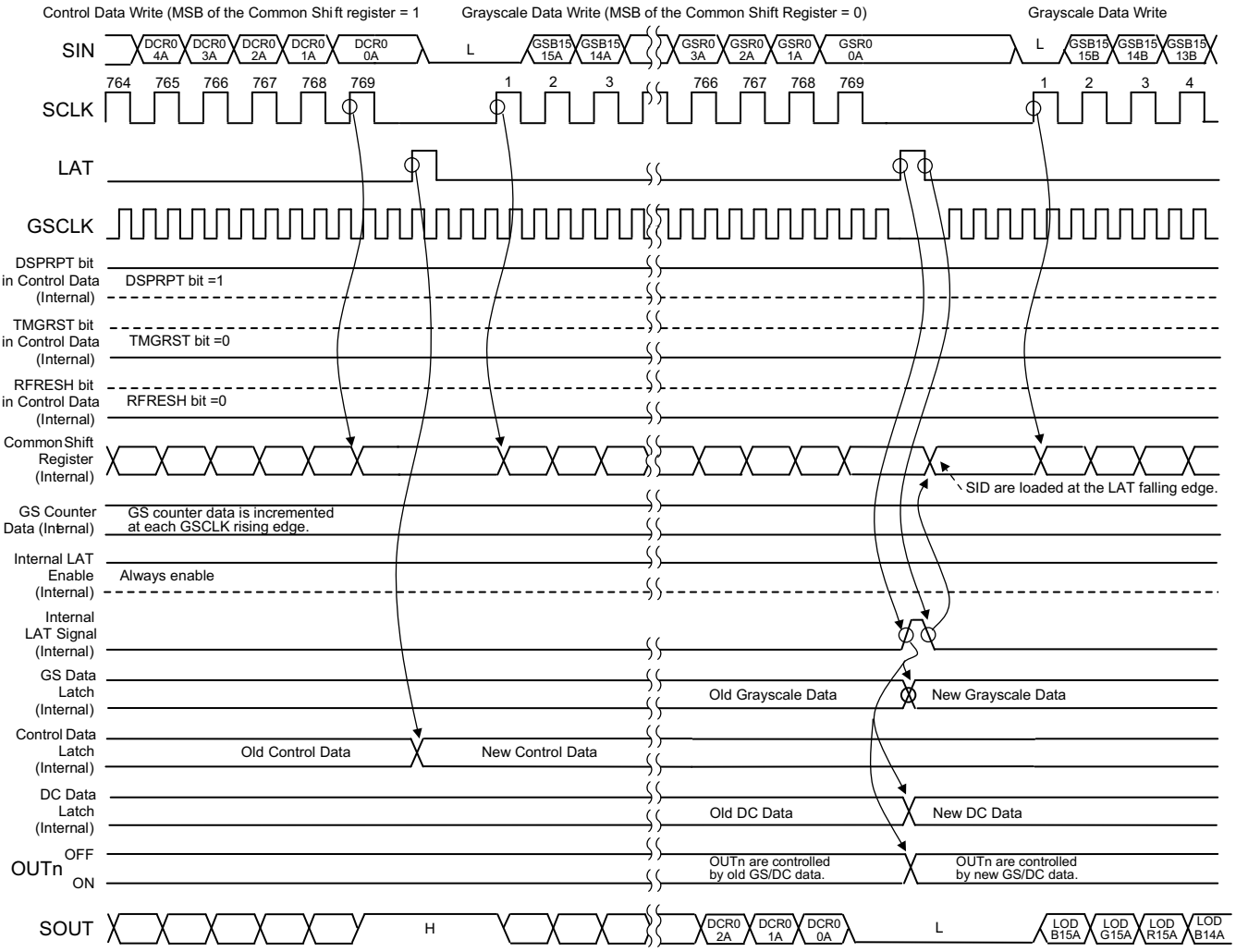


图 8-12. Auto Data Refresh Function 2 (DSPRPT = 1, TMGRST = 0, and RFRESH = 0)

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The device is a 48-channel, constant sink current, LED driver. This device is typically connected in series to drive many LED lamps with only a few controller ports. Output current control data and PWM control data can be written from the SIN input terminal. The PWM timing reference clock can be supplied from the GSCLK input terminal. Also, the LED open and short error flag can be read out from the SOUT output terminal. Furthermore, the device maximum GSCLK clock frequency is 33 MHz and can reduce flickering discernable by the human eye.

9.2 Typical Application

9.2.1 Daisy-Chain Application

In this application, the device VCC and LED lamp anode voltages are supplied from different power supplies.

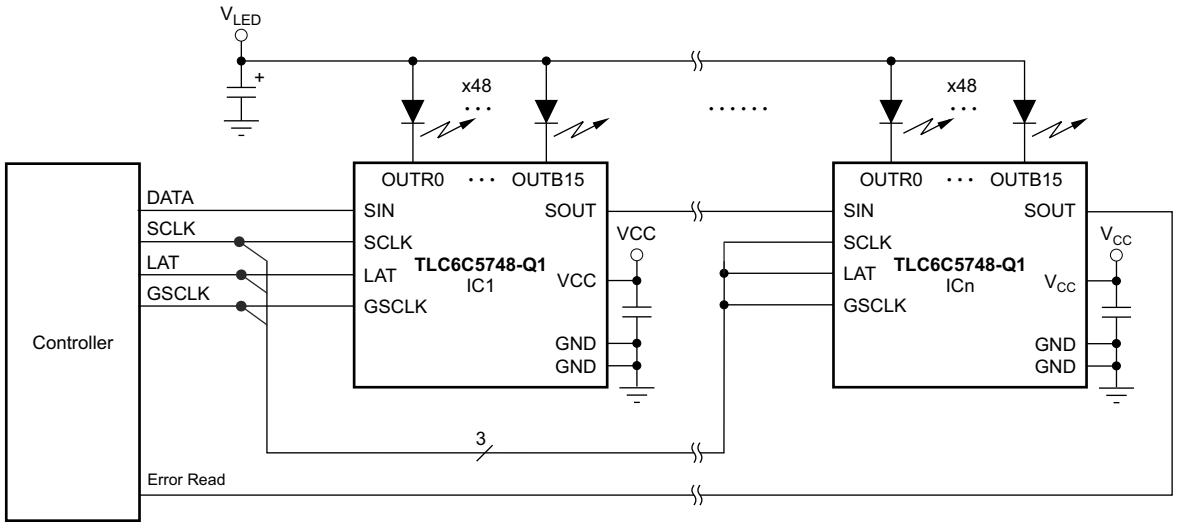


图 9-1. Multiple Daisy-Chained TLC6C5748-Q1 Devices

9.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC input voltage range	3.0 V to 5.5 V
LED lamp (V_{LED}) input voltage range	Maximum LED forward voltage (V_F) + 0.3 V (knee voltage)
SIN, SCLK, LAT, and GSCLK voltage range	Low level = GND, High level = VCC

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Step-by-Step Design Procedure

To begin the design process, a few parameters must be decided upon. The designer needs to know the following:

- Maximum output constant-current value for each color LED ramp.
- Maximum LED forward voltage (V_F).
- Current ratio of red, green, and blue LED lamps for the best white balance.
- Are the auto display repeat function, display timing reset function, or auto data refresh function used?
- Which PWM control method is used: ES-PWM or conventional PWM?
- Is the LED short detect (LSD) function used? If so, which detection level (70% VCC or 90% VCC) is used?

9.2.1.2.2 Maximum Current (MC) Data

There are a total of nine bits of MC data for the red, green, and blue LED ramp. Select the MC data to be greater than each LED ramp current and write the data with other control data.

9.2.1.2.3 Global Brightness Control (BC) Data

There are a total of three sets of 7-bit BC data for the red, green, and blue LED ramp. Select the BC data for the best white balance of the red, green, and blue LED ramp and write the data with other control data.

9.2.1.2.4 Dot Correction (DC) Data

There are a total of 48 sets of 7-bit DC data for each current adjustment. Select the DC data for the best uniformity of each color LED ramp and write the data with other control data.

9.2.1.2.5 Grayscale (GS) Data

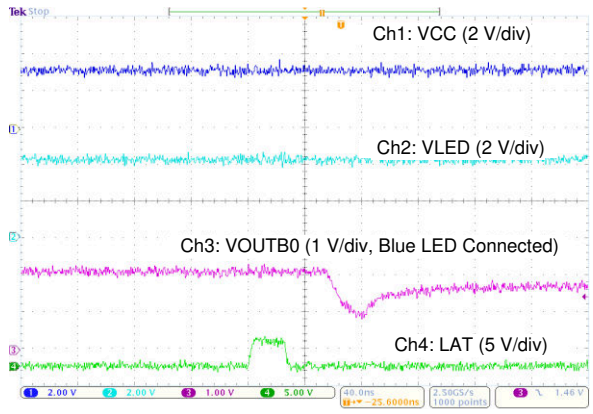
There are a total of 48 sets of 16-bit GS data for the PWM control of each output. Select the GS data of the LED ramp intensity and color control and write the data with other GS data.

9.2.1.2.6 Other Control Data

There are five bits control data to set the function mode for the auto display repeat, display timing reset, auto data refresh, ES-PWM, and LSD functions explained in the *Device Functional Modes* section. Write the 5-bit control data for the appropriate operation of the display system with MC, BC, and DC data as the control data.

9.2.1.3 Application Curves

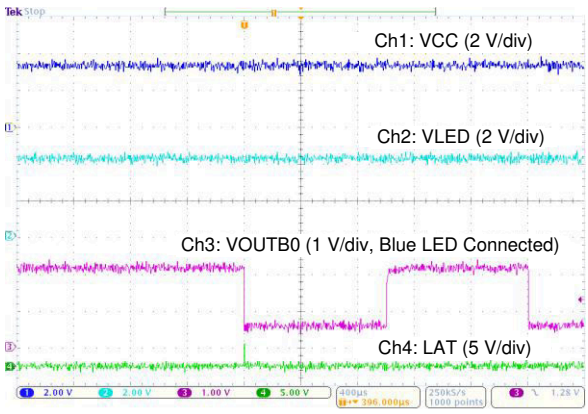
One LED connected to each output.



Time (40 ns/div)

MCX = 4 BCX = DCX*n* = 7Fh GSCLK = 33 MHz
V_{LED} = 4.2 V V_{CC} = 3.3 V DSPRPT = 1
TMGRST, RFRESH, ESPWM, LSDVLT = 0

图 9-2. Output Waveform Immediately After First GS Data Latch Input (GSX*n* = 0001h)



Time (400 µs/div)

MCX = 4 BCX = DCX*n* = 7Fh GSCLK = 33 MHz
V_{LED} = 4.2 V V_{CC} = 3.3 V DSPRPT = 1
TMGRST, RFRESH, ESPWM, LSDVLT = 0

图 9-3. Output Waveform Immediately After First GS Data Latch Input (GSX*n* = 7FFFh)

10 Power Supply Recommendations

The V_{CC} power-supply voltage should be well regulated. A capacitor must be placed closely to IC to reduce the voltage ripple to less than 5% of the input voltage. Furthermore, the V_{LED} voltage should be set to the voltage calculated by Equation 3:

$$V_{LED} \geqslant \text{LED } V_F \times \text{Number of LED Lamps Connected in Series} + 1.1 \times V_{SAT} \quad (3)$$

where:

- V_F = Forward voltage

Because the total current of the constant-current output is large, multiple capacitors must be used to prevent the OUTX*n* terminal voltage from dropping lower than the calculated voltage from Equation 3.

11 Layout

11.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC and GND terminals.
2. Route the GND pattern as widely as possible for large GND currents. Maximum GND current is approximately 1.53 A.
3. Routing between the LED cathode side and the device OUTX*n* should be as short and straight as possible to reduce wire inductance. Route them on LED layer to guarantee the continous GND plane in IC layer.
4. The PowerPAD must be connected to the GND layer because the pad is not internally connected to GND and should be connected to a heat sink layer to reduce device temperature.
5. The GND plane should be as large as possible, especially for the two-layer board. The reason is that the two-layer board normally couldn't provide a continuous GND plane beneath the chip for thermal dissipation. The only area for thermal dissipation is the GND plane around the chip.

11.2 Layout Example

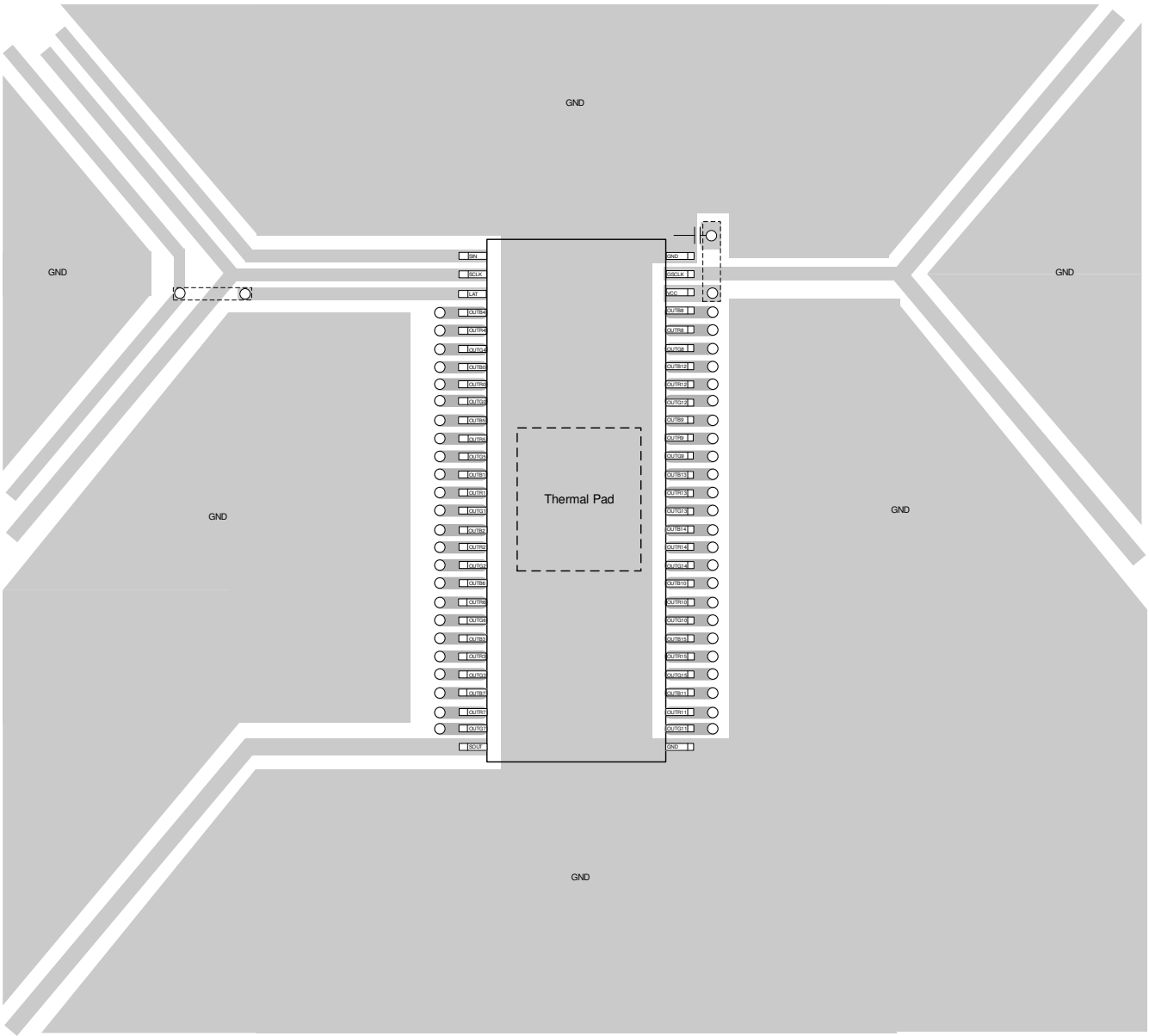


图 11-1. Layout Example

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6C5748QDCARQ1	Active	Production	HTSSOP (DCA) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5748Q1
TLC6C5748QDCARQ1.A	Active	Production	HTSSOP (DCA) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5748Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

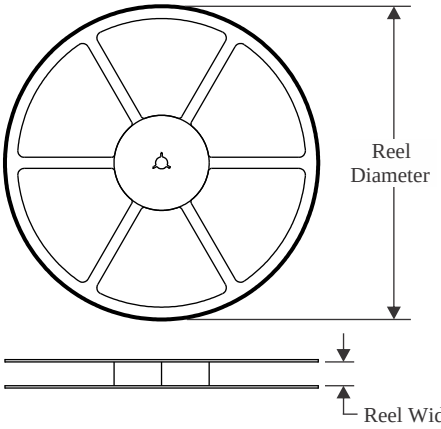
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

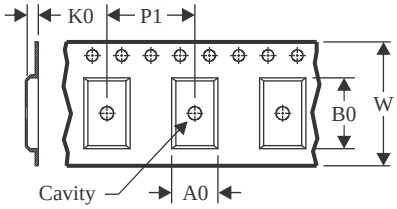
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

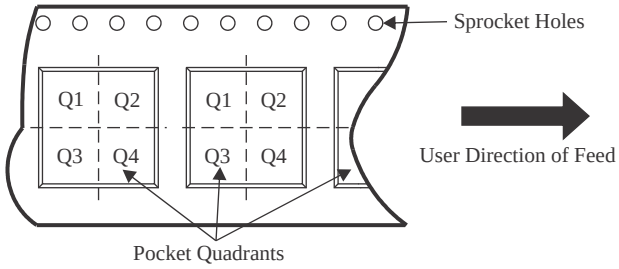


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

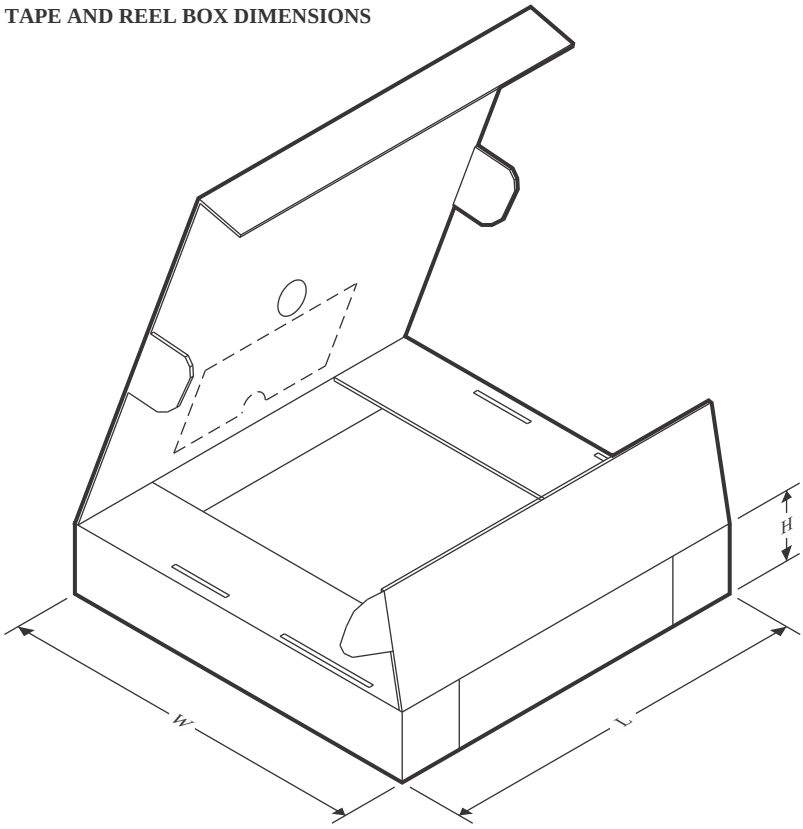
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5748QDCARQ1	HTSSOP	DCA	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
TLC6C5748QDCARQ1	HTSSOP	DCA	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5748QDCARQ1	HTSSOP	DCA	56	2000	350.0	350.0	43.0
TLC6C5748QDCARQ1	HTSSOP	DCA	56	2000	356.0	356.0	45.0

GENERIC PACKAGE VIEW

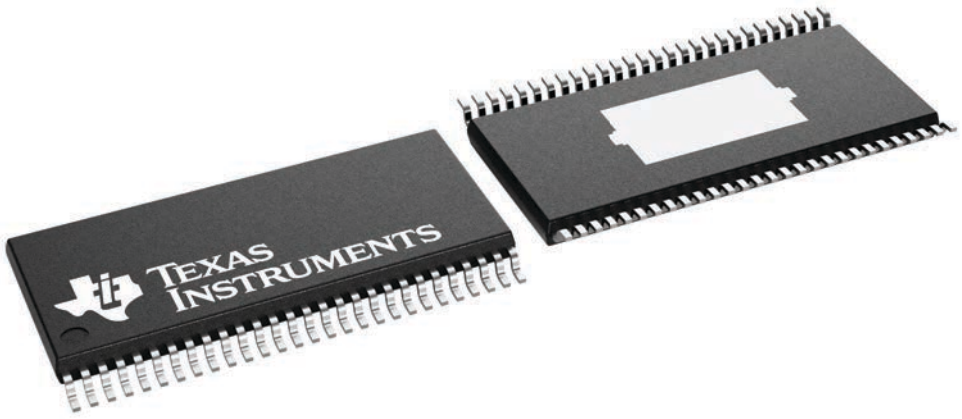
DCA 56

PowerPAD™ TSSOP - 1.2 mm max height

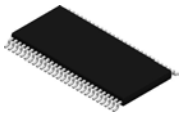
8.1 x 14, 0.5 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231600/A

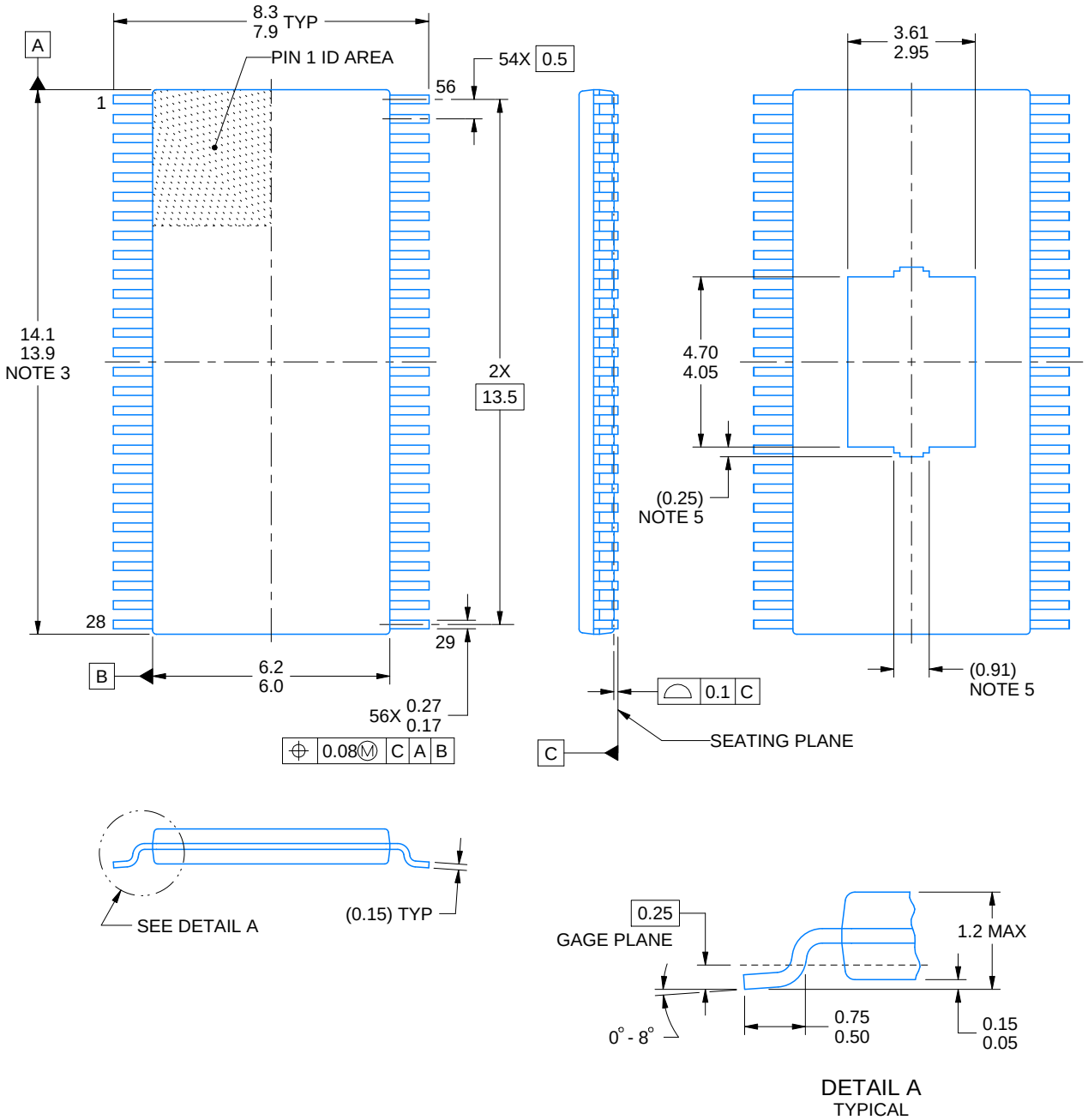


PACKAGE OUTLINE

DCA0056F

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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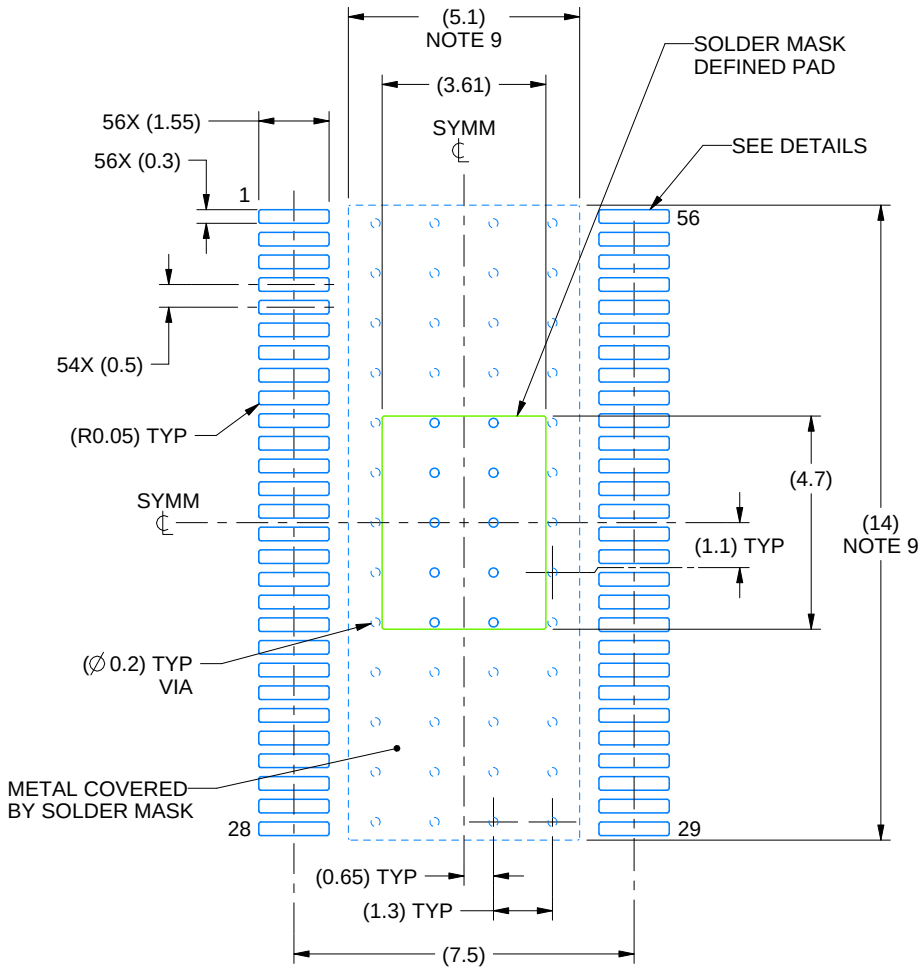
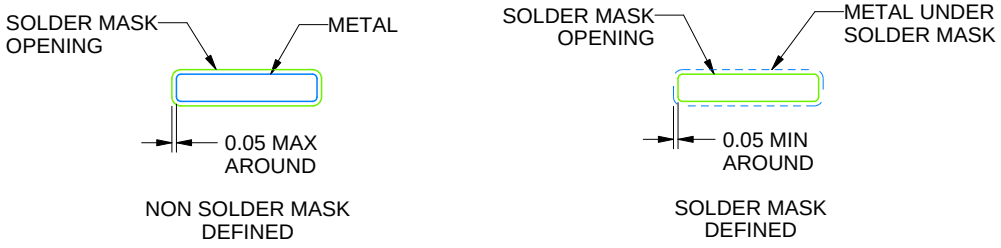
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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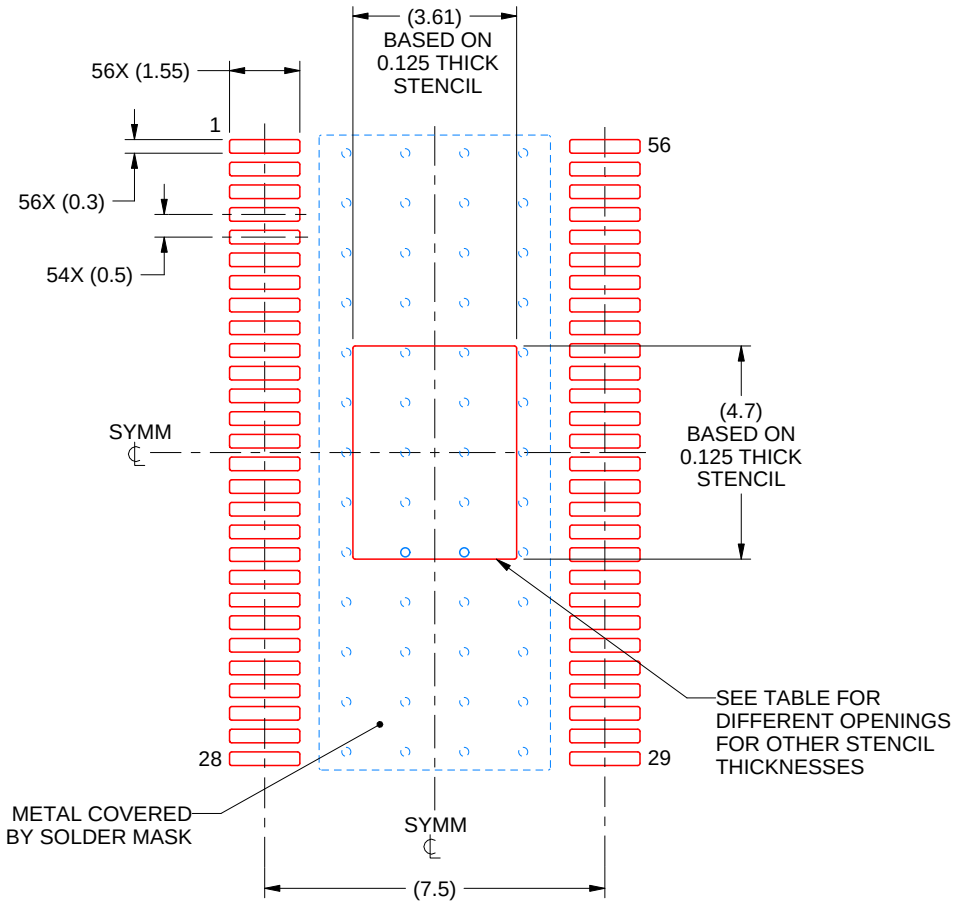
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.04 X 5.25
0.125	3.61 X 4.70 (SHOWN)
0.15	3.30 X 4.29
0.175	3.95 X 3.97

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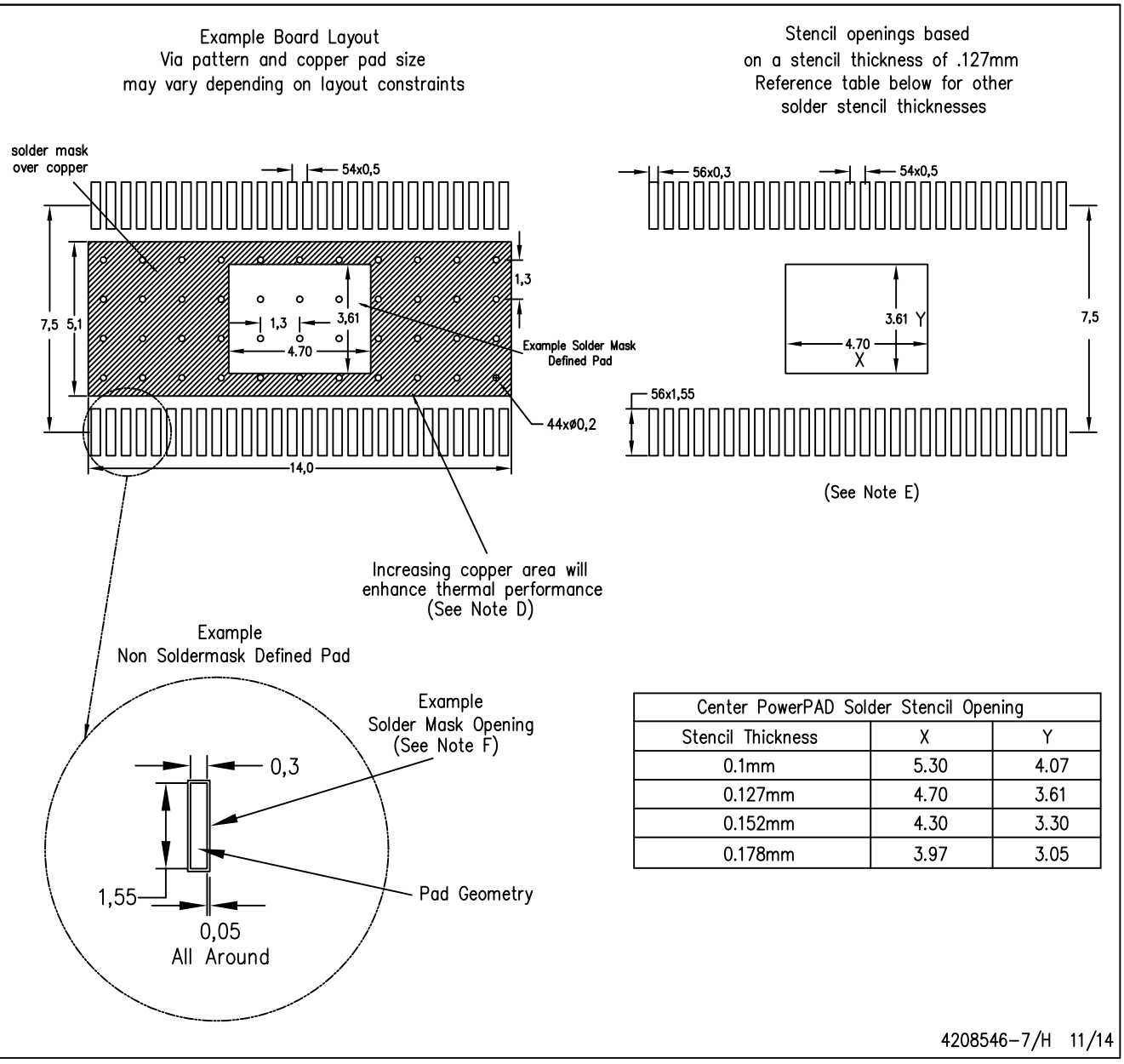
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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最后更新日期：2025 年 10 月