具有全局亮度控制和 LED 开路/短路检测的 24 通道恒定电流 LED 驱动器

1 特性

- 具有开关控制的 24 通道恒定灌电流输出
- 电流能力：
  - 16 个通道为 35mA
  - 8 个通道为 26.2mA
- 每个颜色组的全局亮度控制 (BC)：7 位（128 步长），三组
- LED 电源电压高达 15V
- V_{CC}=3V 至 5.5V
- 恒定电流精度：
  - 通道至通道 = ±1%
  - 器件到器件 = ±3%
- CMOS 逻辑电平 I/O
- 数据传输速率：35MHz
- BLANK 脉冲持续时间：15ns
- 开路负载、短路负载和过热检测
- 带有自动重启的热关断 (TSD)
- 可防止输入浪涌电流的延迟开关
- 工作温度：-40°C 至 85°C
- 封装：HTSSOP-32、QFN-32

2 应用

- 全色 LED 显示
- LED 信号板

3 说明

TLC5952 器件是一款 24 通道恒定灌电流驱动器。每个通道都可以通过内部寄存器数据进行开关。输出通道被分成三组，每组 8 个通道。每个通道组都具有 128 步长全局亮度控制 (BC) 功能。该器件支持通过串行接口写入开关和 BC 数据。它使用单个外部电阻器设置所有 24 个通道的最大电流值。

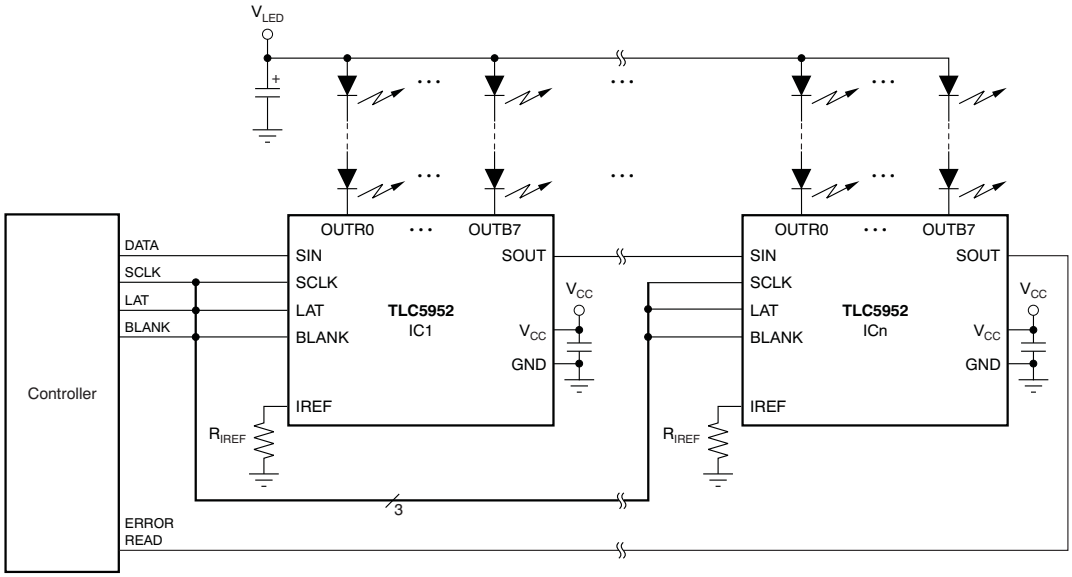
TLC5952 器件具有三个错误检测电路：LED 开路检测 (LOD)、LED 短路检测 (LSD) 和热错误标志 (TEF)。错误检测通过串行接口读取。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLC5952	HTSSOP (32)	11.00mm × 6.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路（多个菊链式 **TLC5952**）



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4 修订历史记录

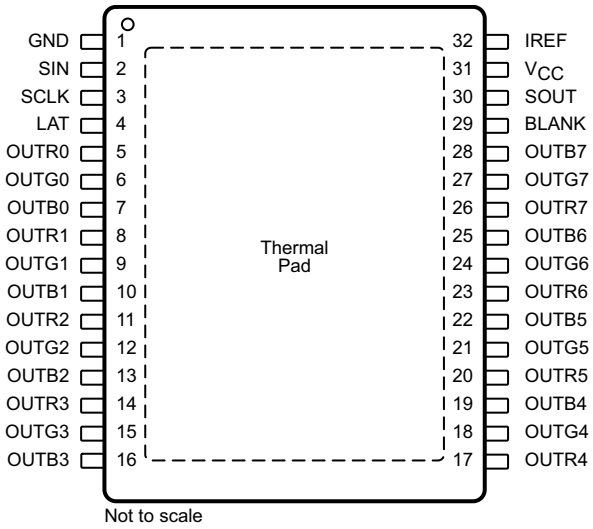
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2009) to Revision A **Page**

- 将“脉宽”更改为“脉冲持续时间” ... 1
- 添加了 *器件信息* 表 ... 1
- Deleted pinout diagram for the RHB package ... 3
- Deleted the RHB column and corresponding table note from the *Pin Functions* table ... 3
- Changed "free-air" in the *Absolute Maximum Ratings* condition statement to "junction" ... 4
- Deleted ESD ratings from the Absolute Maximum Ratings table ... 4
- Deleted the *Dissipation Ratings* section ... 4
- Added the *ESD Ratings* section ... 4
- Changed T_{WH0} to t_{WH0} in the *Recommended Operating Conditions* table ... 5
- Added the *Thermal Information* table to the data sheet ... 5
- Changed Condition statement of Electrical Characteristics table from T_A = –40°C to 85°C to T_J = –40°C to 150°C ... 6
- Changed the *Electrical Characteristics* table to combine multiple symbols for the *Supply current* and *Constant-output current* parameters ... 6
- Changed MAX value of V_{IREEF} in *Electrical Characteristics* from 1.23 V to 1.25 V ... 7
- Changed T_{xx} to t_{xx} at multiple locations in Figure 1 ... 8
- Changed T_{xx} to t_{xx} at multiple locations in Figure 3 ... 10
- Changed Figure 6 ... 11
- Added the *Overview* section ... 16
- Added the *Device Functional Modes* section ... 19
- 添加了 *器件和文档支持* 以及 *机械、封装和可订购信息* 部分 ... 26

5 Pin Configuration and Functions

DAP PowerPAD™ Package
32-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLANK	29	I	All outputs are blank. When BLANK is high, all constant-current outputs (OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7) are forced off. When BLANK is low, all constant current outputs are controlled by the on-off control data in the data latch.
GND	1	—	Power ground
IREF	32	I/O	Reference current terminal. The maximum current for the outputs OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7 is set with a resistor from IREF to GND.
LAT	4	I	Edge-triggered latch. The rising edge of LAT latches the data from the common shift register into the output on-off data latch. See the *Output On-Off Data Latch* section for more details.
OUTB0–OUTB7	7, 10, 13, 16, 19, 22, 25, 28	O	Constant-current outputs for the BLUE LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on-off control data latch.
OUTG0–OUTG7	6, 9, 12, 15, 18, 21, 24, 27	O	Constant-current outputs for the GREEN LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on-off control data latch.
OUTR0–OUTR7	5, 8, 11, 14, 17, 20, 23, 26	O	Constant-current outputs for the RED LED group. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on-off control data latch.
SCLK	3	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the common shift register with the rising edge of SCLK. Data in the shift register are shifted toward the MSB at each rising edge of SCLK. The MSB data of the common shift register appear on SOUT.
SIN	2	I	Serial data input for the 25-bit common shift register
SOUT	30	O	Serial data output. The MSB of the 25-bit common shift register is shifted out at the rising edge of SCLK.
V_{CC}	31	—	Power-supply voltage

6 Specifications

6.1 Absolute Maximum Ratings(1) (2)

Over operating junction temperature range, unless otherwise noted.

PARAMETER			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}	–0.3	6	V
I_{OUT}	Output current (dc)	OUTR0–OUTR7, OUTG0–OUTG7		45	mA
		OUTB0–OUTB7		35	
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK, IREF	–0.3	V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT	–0.3	V_{CC} + 0.3	V
		OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7	–0.3	16	
$T_{J(max)}$	Operation junction temperature			150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

At T_A = –40°C to 85°C, unless otherwise noted.

PARAMETER			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output	OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7			15	V
V_{IH}	High-level input voltage	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, BLANK	GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
I_{OLC}	Constant-output sink current	OUTR0–OUTR7, OUTG0–OUTG7			35	mA
		OUTB0–OUTB7			26.2	
T_A	Operating ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C
AC CHARACTERISTICS, V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			35	MHz
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		LAT	15			ns
t_{WH2}		BLANK	15			ns
t_{WL2}		BLANK	15			ns
t_{SU0}	Setup time	SIN – SCLK↑	4			ns
t_{SU1}		LAT↑ – SCLK↑	150			ns
t_{H0}	Hold time	SIN – SCLK↑	3			ns
t_{H1}		LAT↑ – SCLK↑	10			ns

6.4 Thermal Information

THERMAL METRIC(1)		TLC5952 DAP (TSSOP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

At T_J = –40°C to 150°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = 25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT			0.4	V
I_{IN}	Input current	V_I = V_{CC} or GND at SIN, SCLK, LAT, and BLANK	–1		1	μA
I_{CC}	Supply current	SIN, SCLK, LAT = low, BLANK = high, $V_{OUTRn, -Gn, -Bn}$ = 1 V, BCR, -G, -B = 7Fh, R_{IREF} = 24 kΩ ($I_{OUTRn/Gn}$ = 2 mA target, I_{OUTBn} = 1.5 mA target)		1	3	mA
		SIN, SCLK, LAT = low, BLANK = high, $V_{OUTRn, -Gn, -Bn}$ = 1 V, BCR, -G, -B = 7Fh, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn}$ = 20 mA target, I_{OUTBn} = 15 mA target)		8	14	
		SIN, SCLK, LAT = low, BLANK = low, all OUTRn, -Gn, -Bn = on, $V_{OUTRn, -Gn, -Bn}$ = 1 V, BCR, -G, -B = 7Fh, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn}$ = 20 mA target, I_{OUTBn} = 15 mA target)		12	30	
		SIN, SCLK, LAT = low, BLANK = low, all OUTRn, -Gn, -Bn = on, $V_{OUTRn, -Gn, -Bn}$ = 1 V, BCR, -G, -B = 7Fh, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target)		20	50	
I_{OLC}	Constant-output current	At OUTR0–OUTR7 and OUTG0–OUTG7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target)	29	32	35	mA
		At OUTB0–OUTB7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ (I_{OUTBn} = 24 mA target)	21.8	24	26.2	
I_{OLKG}	Leakage output current	At OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7, BLANK = high, $V_{OUTRn, -Gn, -Bn}$ = V_{OUTfix} = 15 V, R_{IREF} = 1.5 kΩ			0.1	μA
ΔI_{OLC}	Constant-current error(1) (channel-to-channel in same color group)	At OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target), at same color group output		±1%	±3%	
ΔI_{OLC1}	Constant current error(2) (device to device in same color group)	At OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn}$ = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ ($I_{OUTRn/Gn}$ = 32 mA target, I_{OUTBn} = 24 mA target), at same color group output		±3%	±6%	

(1) The deviation of each output in the same color group from the average of the same color group (OUTR0–OUTR7, OUTG0–OUTG7, or OUTB0–OUTB7) constant current. The deviation is calculated by the formula (X = R, G, or B; n = 0–7):

$$\Delta\ (\%) = \left(\frac{I_{OUTXn}}{\frac{(I_{OUTX0} + I_{OUTX1} + ... + I_{OUTX6} + I_{OUTX7})}{8}} - 1 \right) \times 100$$

(2) The deviation of the constant-current average of each color group from the ideal constant-current value. The deviation is calculated by the formula (X = R, G, or B):

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUTX0} + I_{OUTX1} + ... + I_{OUTX7})}{8} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the following equation for OUTR0–OUTR7 and OUTG0–OUTG7 (X = R, G, or B):

$$I_{OUTRn/Gn(IDEAL, mA)} = 40 \times \left(\frac{1.20}{R_{IREF}\ (\Omega)} \right)$$

Ideal current is calculated by the following equation for OUTR0–OUTR7 and OUTG0–OUTG7 (X = R, G, or B):

$$I_{OUTBn(IDEAL, mA)} = 30 \times \left(\frac{1.20}{R_{IREF}\ (\Omega)} \right)$$

Electrical Characteristics (continued)

At T_J = –40°C to 150°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = 25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC2}	Line regulation(3)	At OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn} = V_{OUTfix}$ = 1 V, R_{IREF} = 1.5 kΩ		±0.5%	±1%	
ΔI_{OLC3}	Load regulation(4)	At OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7, All OUTRn, -Gn, -Bn = on, BCR, -G, -B = 7Fh, $V_{OUTRn, -Gn, -Bn}$ = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		±1	±3	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature(5)	150	165	180	°C
T_{HYS}	Thermal error flag hysteresis	Junction temperature(5)	5	10	20	°C
V_{LOD0}	LED open detection threshold	All OUTRn, -Gn, -Bn = on, detection voltage select code = 0h	0.25	0.3	0.35	V
V_{LOD1}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 1h	0.5	0.6	0.7	V
V_{LOD2}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 2h	0.8	0.9	1	V
V_{LOD3}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 3h	1.1	1.2	1.3	V
V_{LSD0}	LED short detection threshold	All OUTRn, -Gn, -Bn = on, detection voltage select code = 4h	0.55 × V_{CC}	0.6 × V_{CC}	0.65 × V_{CC}	V
V_{LSD1}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 5h	0.65 × V_{CC}	0.7 × V_{CC}	0.75 × V_{CC}	V
V_{LSD2}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 6h	0.75 × V_{CC}	0.8 × V_{CC}	0.85 × V_{CC}	V
V_{LSD3}		All OUTRn, -Gn, -Bn = on, detection voltage select code = 7h	0.85 × V_{CC}	0.9 × V_{CC}	0.95 × V_{CC}	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ	1.17	1.2	1.25	V

(3) Line regulation is calculated by the following equation (X = R, G, or B; n = 0–7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)}{(I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(4) Load regulation is calculated by the following equation (X = R, G, or B; n = 0–7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{OUTXn} = 3\ V) - (I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)}{(I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

(5) Not tested; specified by design.

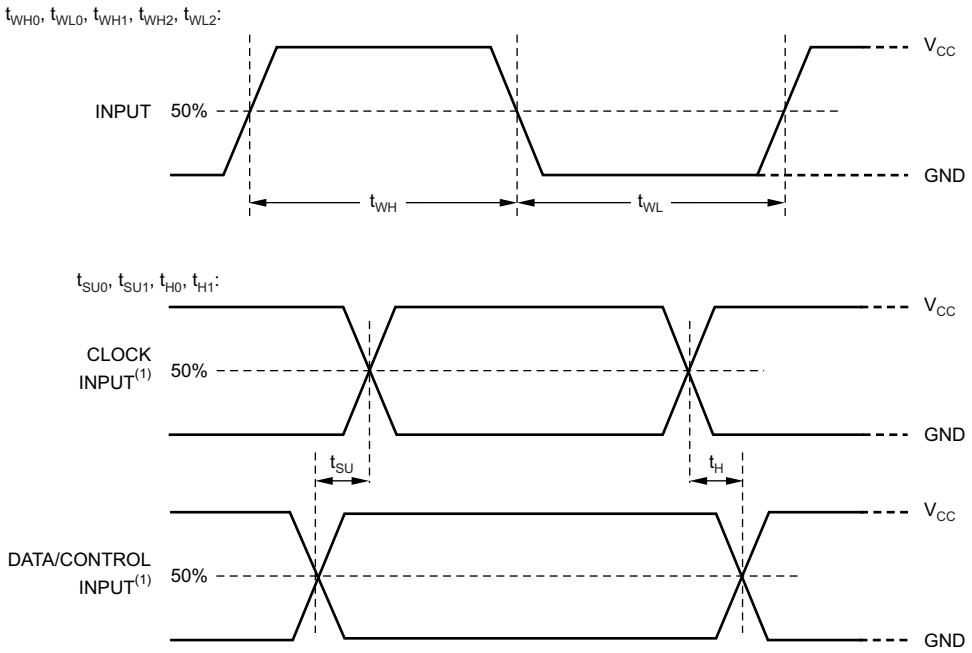
6.6 Switching Characteristics

At T_A = –40°C to 85°C, V_{CC} = 3 V to 5.5 V, C_L = 15 pF, R_L = 120 Ω, R_{IREF} = 1.5 kΩ, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = 25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT		6	15	ns
t_{R1}		OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7, BCR, -G, -B = 7Fh		10	30	ns
t_{F0}	Fall time	SOUT		6	15	ns
t_{F1}		OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7, BCR, -G, -B = 7Fh		10	30	ns
t_{D0}	Propagation delay time(1)	SCLK↑ to SOUT		8	20	ns
t_{D1}		LAT↑ to OUTR0 on-off, BCR, -G, -B = 7Fh		22	45	ns
t_{D2}		BLANK↓↑ to OUTR0 on-off, BCR, -G, -B = 7Fh		15	30	ns
t_{D3}		OUTRn on to OUTGn on, OUTGn on to OUTBn on, OUTBn on to OUTRn + 1 on, BCR, -G, -B = 7Fh		3	6	ns
t_{D4}		OUTRn off to OUTGn off, OUTGn off to OUTBn off, OUTBn off to OUTRn + 1 off, BCR, -G, -B = 7Fh		3	6	ns
t_{D5}		LAT↑ to I_{OUTn} changing by global brightness control (BC data are 0Ch–72h or 72h–0Ch)		20	50	ns
t_{ON_ERR}	Output on-time error(2)	On-off latched data = 1, BCR, -G, -B = 7Fh, 20 ns BLANK low level one-shot pulse input	–11		5	ns

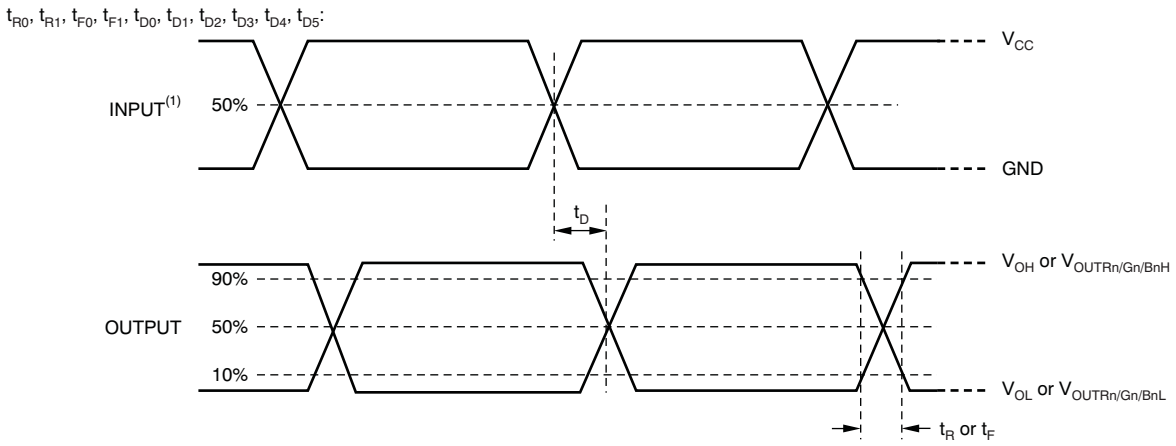
(1) Propagation delay, t_{D3} (OUTRn on to OUTGn on, OUTGn on to OUTBn on, OUTBn on to OUTRn + 1 on) is calculated by the formula:
t_{D3} (ns) = (the propagation delay between OUTR0 to OUTB7 = on) / 23
t_{D4} (OUTRn to OUTGn = off, OUTGn to OUTBn = off, OUTBn to OUTRn + 1 = off) is calculated by the formula:
t_{D4} (ns) = (the propagation delay between OUTR0 to OUTB7 = off) / 23

(2) Output on-time error is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low-level pulse duration. t_{OUT_ON} is the actual on-time of the constant current output.



Input pulse rise and fall time is 1 ns to 3 ns.

Figure 1. Input Timing



Input pulse rise and fall time is 1 ns to 3 ns.

Figure 2. Output Timing

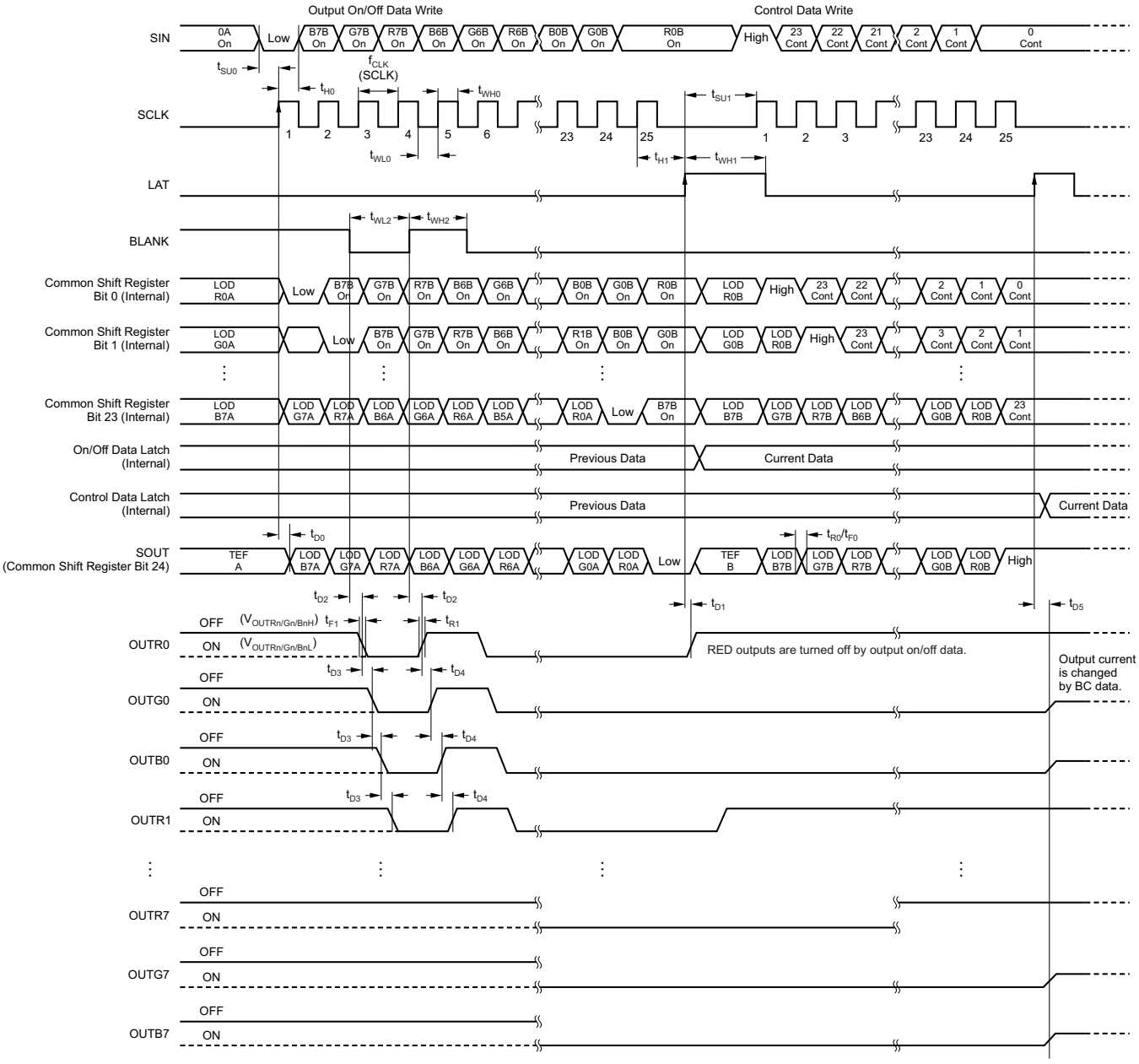


Figure 3. Timing Diagram

6.7 Typical Characteristics

At T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

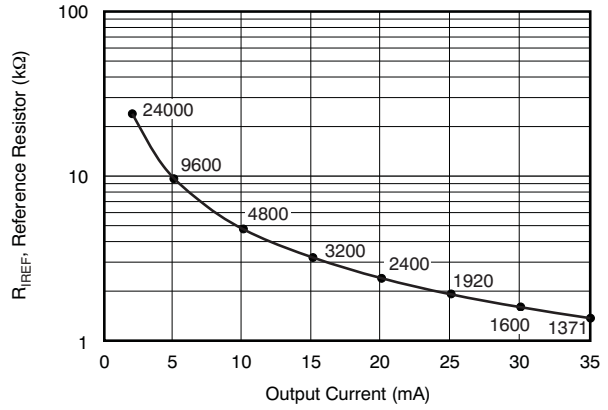


Figure 4. Reference Resistor vs Output Current (Red and Green Color Group)

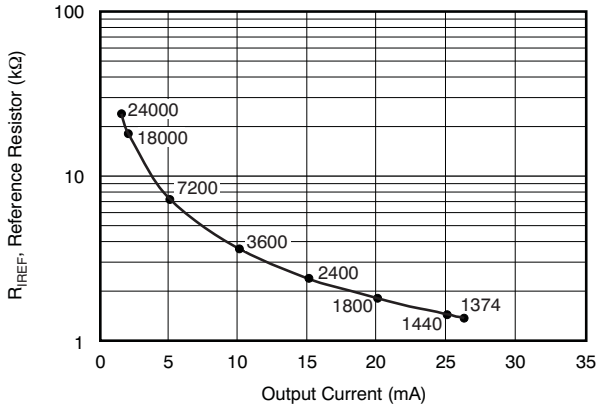


Figure 5. Reference Resistor vs Output Current (Blue Color Group)

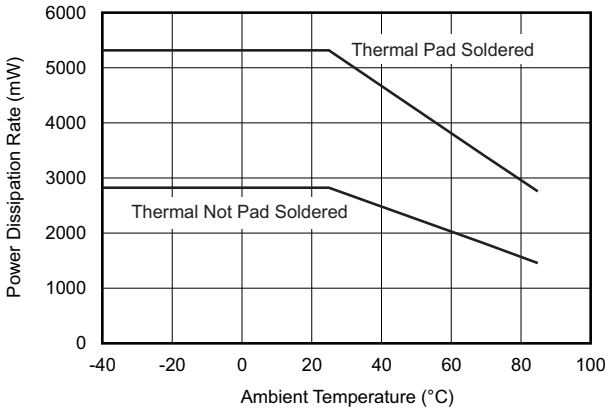


Figure 6. Power Dissipation Rate

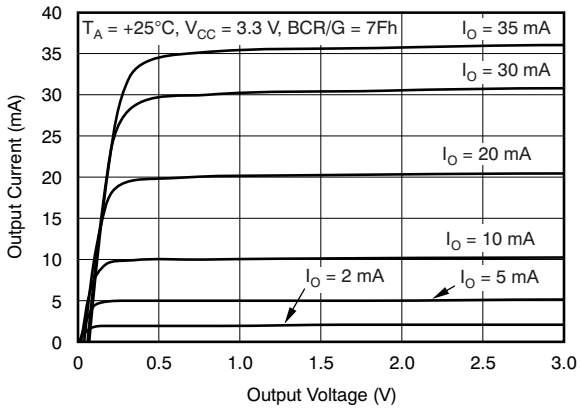


Figure 7. Output Current vs Output Voltage (Red and Green Color Group)

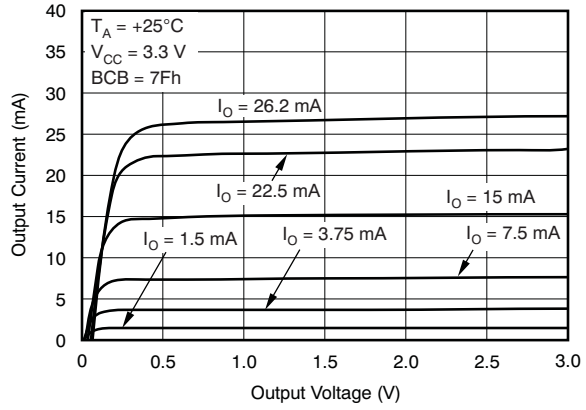


Figure 8. Output Current vs Output Voltage (Blue Color Group)

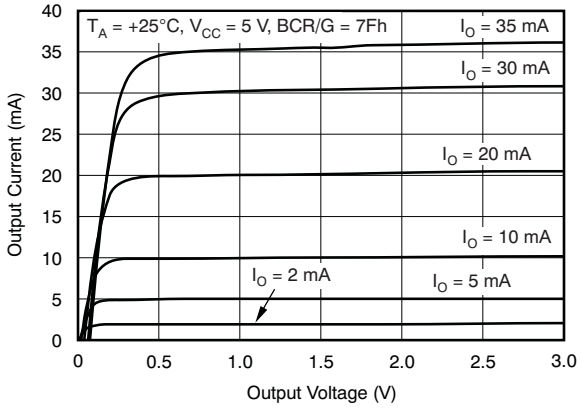


Figure 9. Output Current vs Output Voltage (Red and Green Color Group)

Typical Characteristics (continued)

At T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

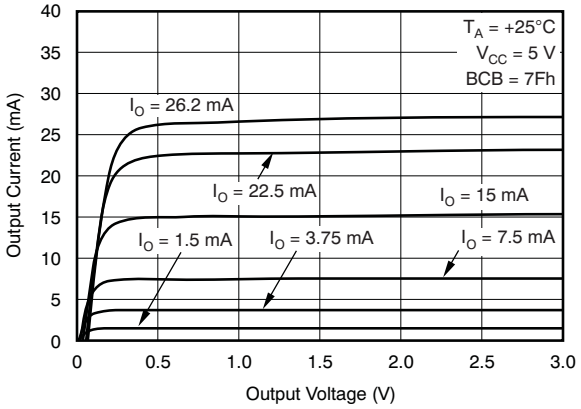


Figure 10. Output Current vs Output Voltage (Blue Color Group)

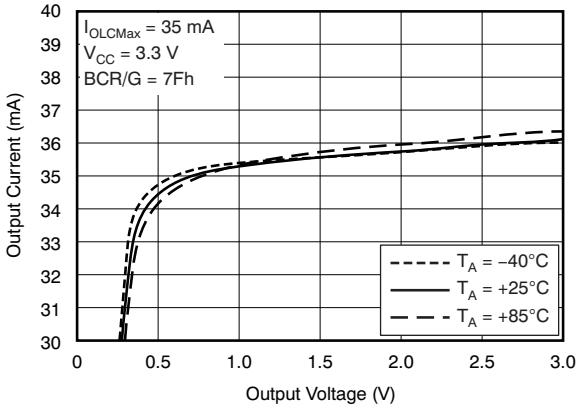


Figure 11. Output Current vs Output Voltage (Red and Green Color Group)

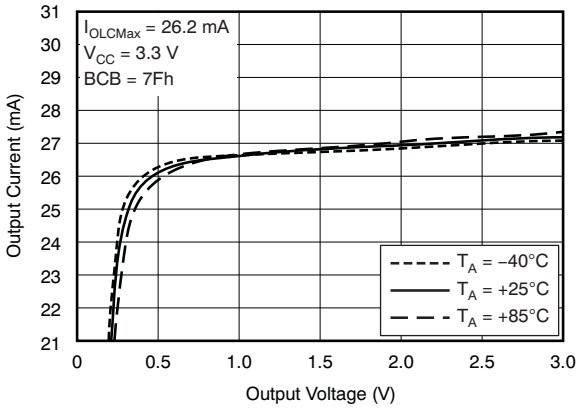


Figure 12. Output Current vs Output Voltage (Blue Color Group)

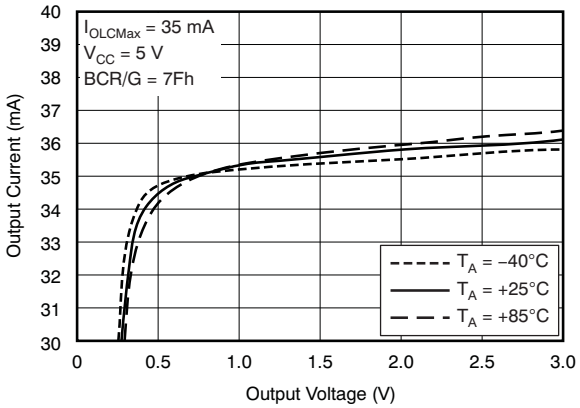


Figure 13. Output Current vs Output Voltage (Red and Green Color Group)

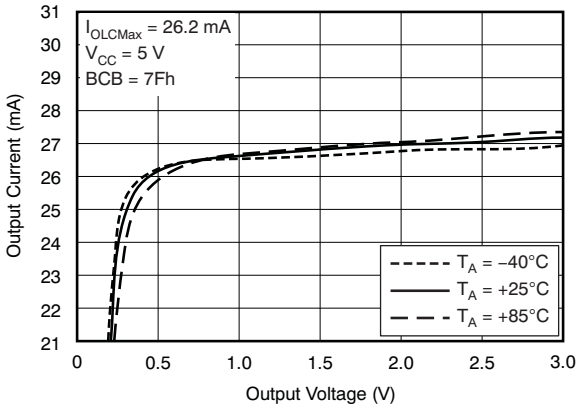


Figure 14. Output Current vs Output Voltage (Blue Color Group)

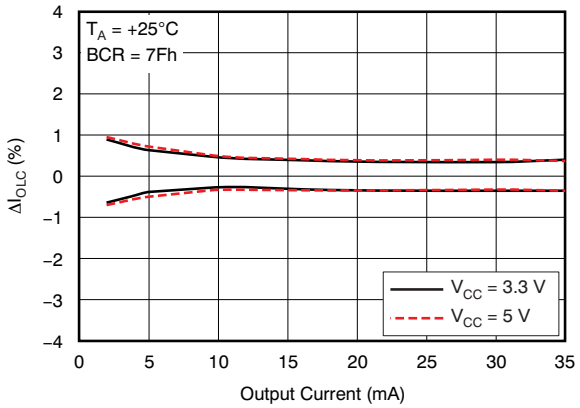


Figure 15. Constant-Current Error vs Output Current (Channel-to-Channel in Red Color Group)

Typical Characteristics (continued)

At T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

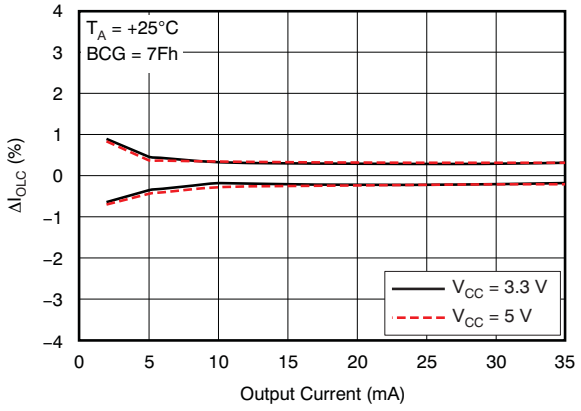


Figure 16. Constant-Current Error vs Output Current (Channel-to-Channel in Green Color Group)

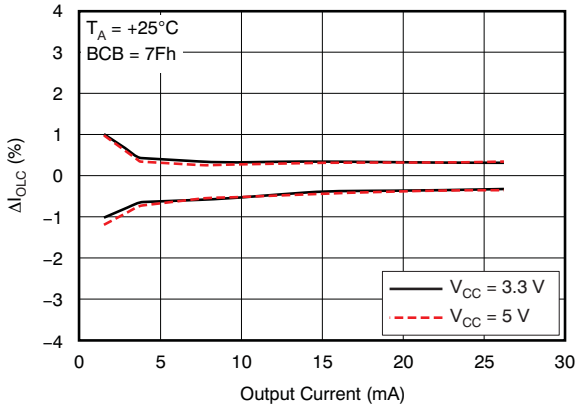


Figure 17. Constant-Current Error vs Output Current (Channel-to-Channel in Blue Color Group)

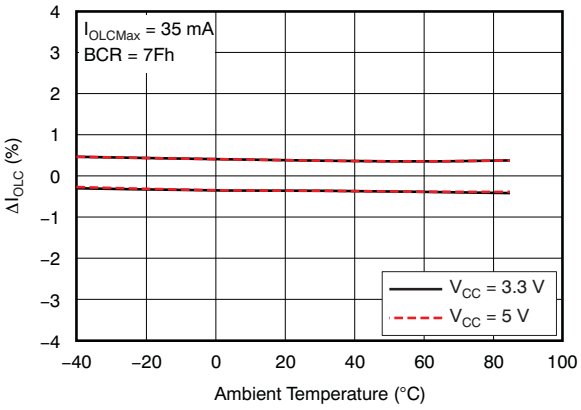


Figure 18. Constant-Current Error vs Ambient Temperature (Channel-to-Channel in Red Color Group)

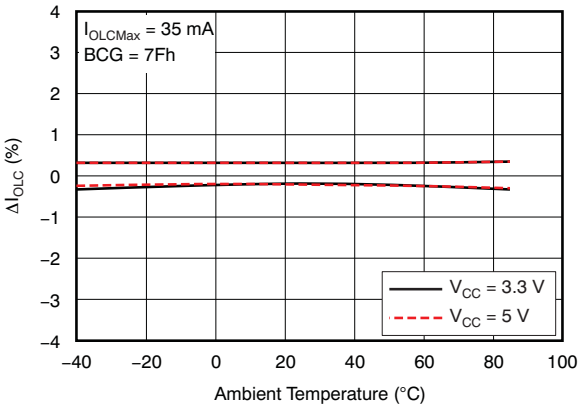


Figure 19. Constant-Current Error vs Ambient Temperature (Channel-to-Channel in Green Color Group)

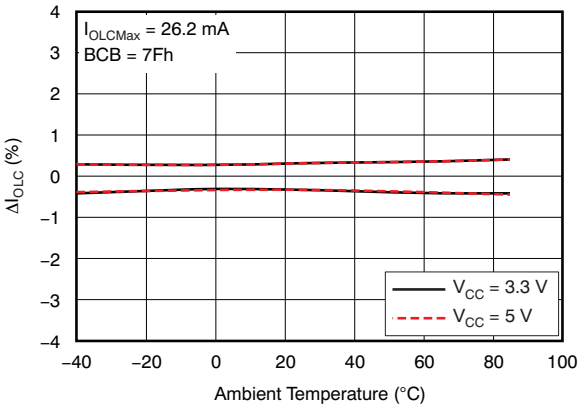


Figure 20. Constant-Current Error vs Ambient Temperature (Channel-to-Channel in Blue Color Group)

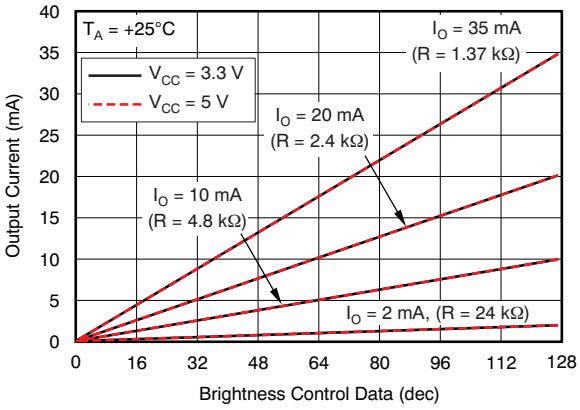


Figure 21. Global Brightness Control Linearity (Red and Green Color Group)

Typical Characteristics (continued)

At T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

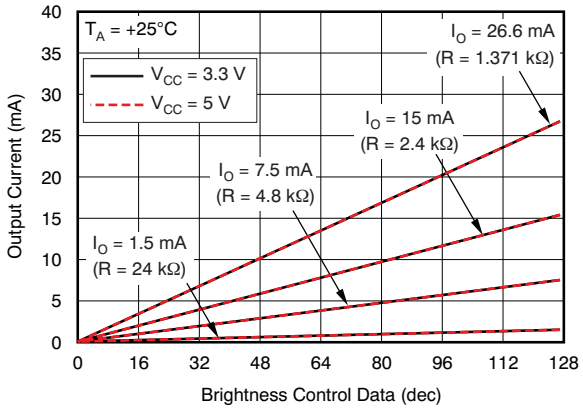


Figure 22. Global Brightness Control Linearity (Blue Color Group)

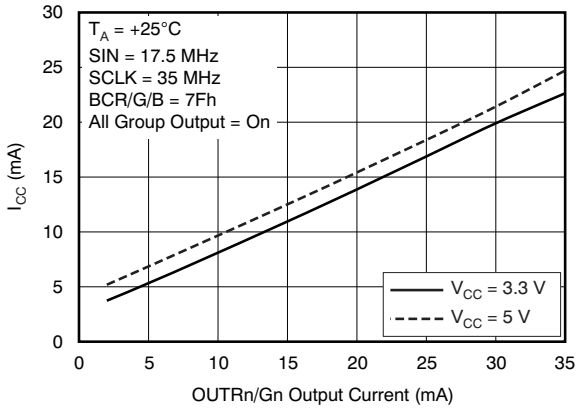


Figure 23. Supply Current vs Output Current (Red and Green Color Group)

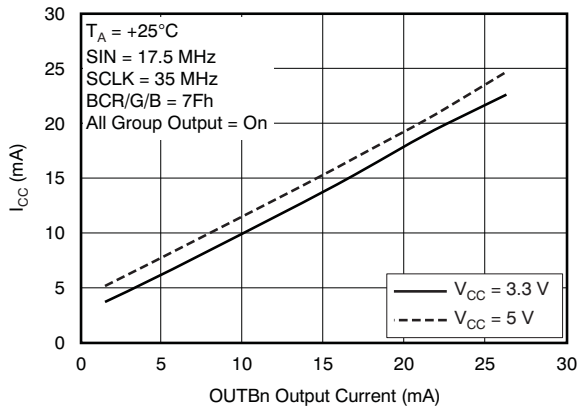


Figure 24. Supply Current vs Output Current (Blue Color Group)

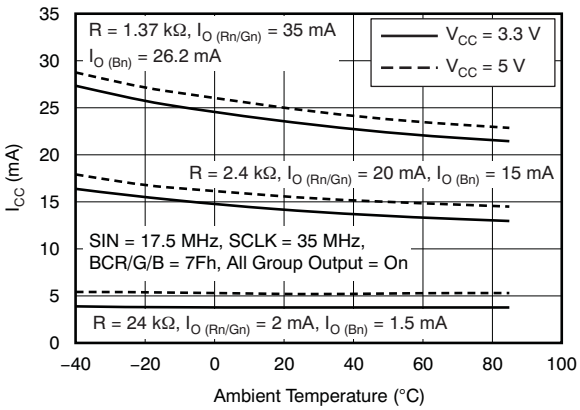


Figure 25. Supply Current vs Ambient Temperature

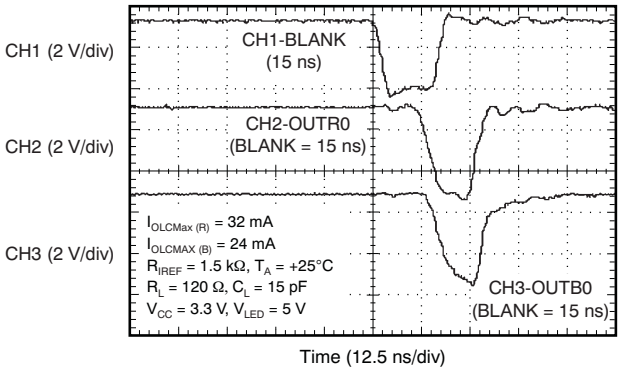


Figure 26. Constant-Current Output-Voltage Waveform

7 Parameter Measurement Information

7.1 Pin Equivalent Input and Output Schematic Diagrams

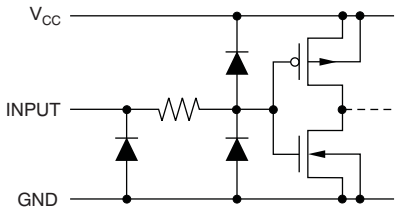


Figure 27. SIN, SCLK, LAT, BLANK

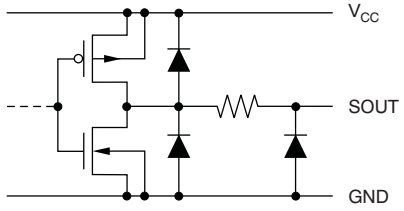


Figure 28. SOUT

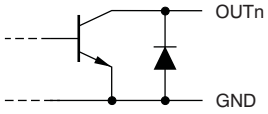


Figure 29. OUTR0, -G0, -B0 Through OUTR7, -G7, -B7

7.2 Test Circuits

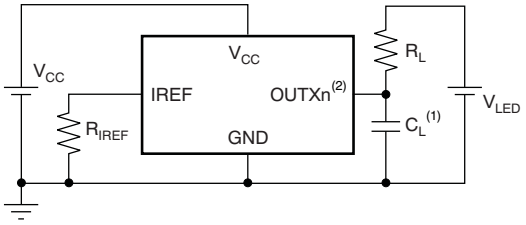


Figure 30. Rise Time and Fall Time Test Circuit for OUTRn, -Gn, -Bn

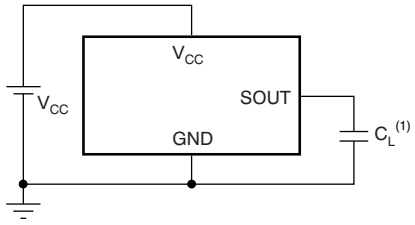
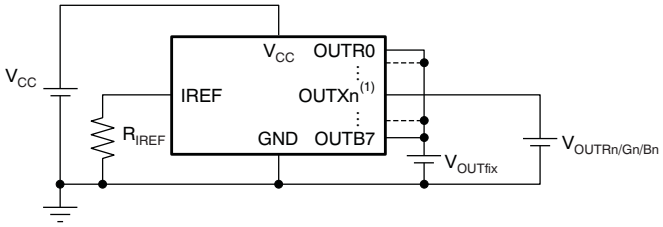


Figure 31. Rise Time and Fall Time Test Circuit for SOUT



X = R, G, or B; n = 0–7.

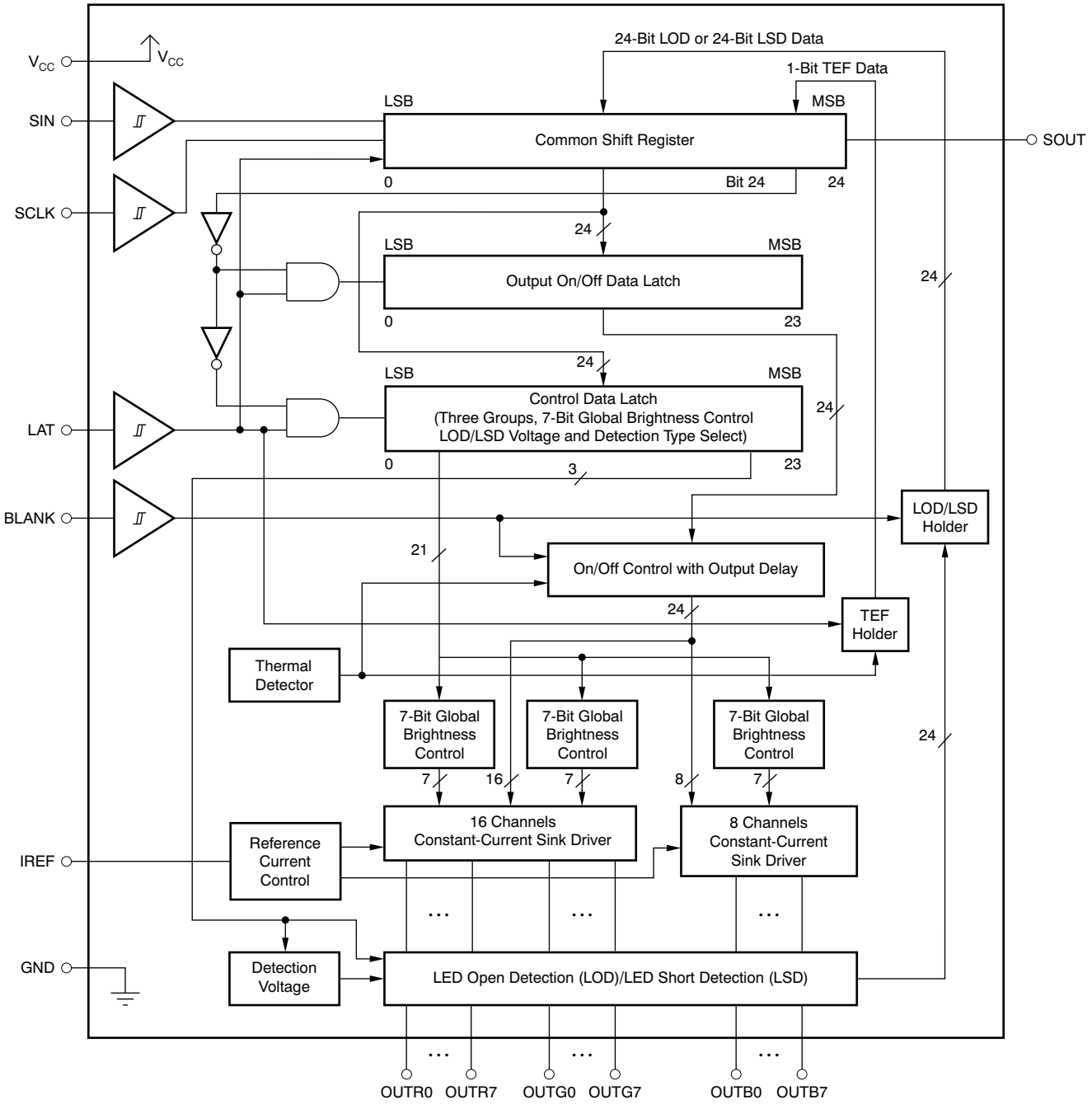
Figure 32. Constant-Current Test Circuit for OUTRn, -Gn, -Bn

8 Detailed Description

8.1 Overview

The TLC5952 device is a 24-channel, constant- current sink driver. Each channel can be turned on or off with internal register data. The output channels are grouped into three groups of eight channels each. Each channel group has a 128-step global brightness control (BC) function. Both on-off data and BC are writable via a serial interface. The maximum current value of all 24 channels is set by a single external resistor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Maximum Constant-Sink-Current Value

The maximum output current per channel, I_{OLCMax}, is programmed by a single resistor, R_{IREF}, which is placed between the IREF and GND pins. The voltage on IREF is set by an internal band-gap V_{IREF}, with a typical value of 1.20 V. The maximum channel current is equivalent to the current flowing through R_{IREF} multiplied by a factor of 40 for OUTRn, -Gn and 30 for OUTBn. The maximum output current per channel can be calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 40 \text{ (for OUTRn/Gn)}$$

$$= \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 30 \text{ (for OUTBn)} \quad (1)$$

where:

- V_{IREF} = the internal reference voltage on IREF (1.20 V, typical)
- I_{OLCMax} = 2 mA to 35 mA at OUTRn, -Gn and 1.5 mA to 26.2 mA at OUTBn

I_{OLCMax} is the largest current for each output. Each output sinks the I_{OLCMax} current when it is turned on and the global brightness control data are set to the maximum value of 7Fh (127d). Each output sink current can be reduced by lowering the output global brightness control (BC) value.

R_{IREF} must be between 1.37 kΩ and 24 kΩ to hold I_{OLCMax} between 35 mA (typ) and 2 mA (typ) for OUTRn, -Gn and between 26.2 mA (typ) and 1.5 mA (typ) for OUTBn. Otherwise, the output may be unstable. Output currents lower than 2 mA (or 1.5 mA for OUTBn) can be achieved by setting I_{OLCMax} to 2 mA or higher and then using global brightness control to lower the output current.

Table 1 shows the characteristics of the constant-current sink versus the external resistor, R_{IREF}.

Table 1. Maximum Constant-Current Output Versus External Resistor Value

I_{OLCMax} (mA)		R_{IREF} (kΩ)
OUTRn, OUTGn	OUTBn	
35	26.28	1.37
30	22.5	1.6
25	18.75	1.92
20	15	2.4
15	11.25	3.2
10	7.5	4.8
5	3.75	9.6
2	1.5	24

8.3.2 Global Brightness Control (BC) Function: Sink-Current Control

The TLC5952 is able to adjust the output current of each of the three color groups OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7. This function is called *global brightness control* (BC). The BC function allows users to adjust the global brightness of LEDs connected to the three output groups (OUTR0–OUTR7, OUTG0–OUTG7, and OUTB0–OUTB7). All color group output currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The brightness control data are entered into the TLC5952 via the serial interface. When the BC data change, the output current also changes immediately. When the device is powered on, the data in the common shift register and the control data latch are not set to any default values. Therefore, BC data must be written to the control data latch before turning on the constant-current output.

Equation 2 determines the output sink current for each color group. Table 2 summarizes the BC data versus current ratio and set current value.

$$I_{OUT}\ (mA) = I_{OLCMax}\ (mA) \times \left[\frac{BCR/G/B}{127d} \right] \quad (2)$$

where:

- I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}
- BCR, -G, -B = the global brightness control value in the control data latch for each output color group

Table 2. BC Data vs Current Ratio and Set-Current Value

BC DATA (Binary)	BC DATA (Decimal)	BC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax} (mA, Typical)	I_{OUT}, mA (I_{OLCMax} = 35 mA, Typical)	I_{OUT}, mA (I_{OLCMax} = 2 mA, Typical)
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.28	0.02
000 0010	2	02	1.6	0.55	0.03
...	...	...	...	...	...
111 1101	125	7D	98.4	34.45	1.97
111 1110	126	7E	99.2	34.72	1.98
111 1111	127	7F	100	35	2

8.3.3 Constant-Current Output On-Off Control

When BLANK is low, each output is controlled by the data in the output on-off data latch. When data corresponding to an output are equal to 1, the output turns on; when the data corresponding to an output are equal to 0, the output turns off. When BLANK is high, all outputs are forced off.

When the device is powered on, the data in the output on-off data latch are not set to any default values. Therefore, on-off data must be written to the output on-off data latch before turning on the constant-current output and pulling BLANK low.

If there are any OUTRn, -Gn, -Bn outputs not connected to an LED, including open for short-to-ground failures, the on-off data corresponding to the unconnected output should be set to 0 before the LED is turned on. Otherwise, the V_{CC} supply current (I_{CC}) increases while the LEDs are on. A truth table for the on-off control data is shown in Table 3.

Table 3. On-Off Control-Data Truth Table

ON-OFF CONTROL DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

8.4 Device Functional Modes

8.4.1 LOD, LSD, and TEF Operation

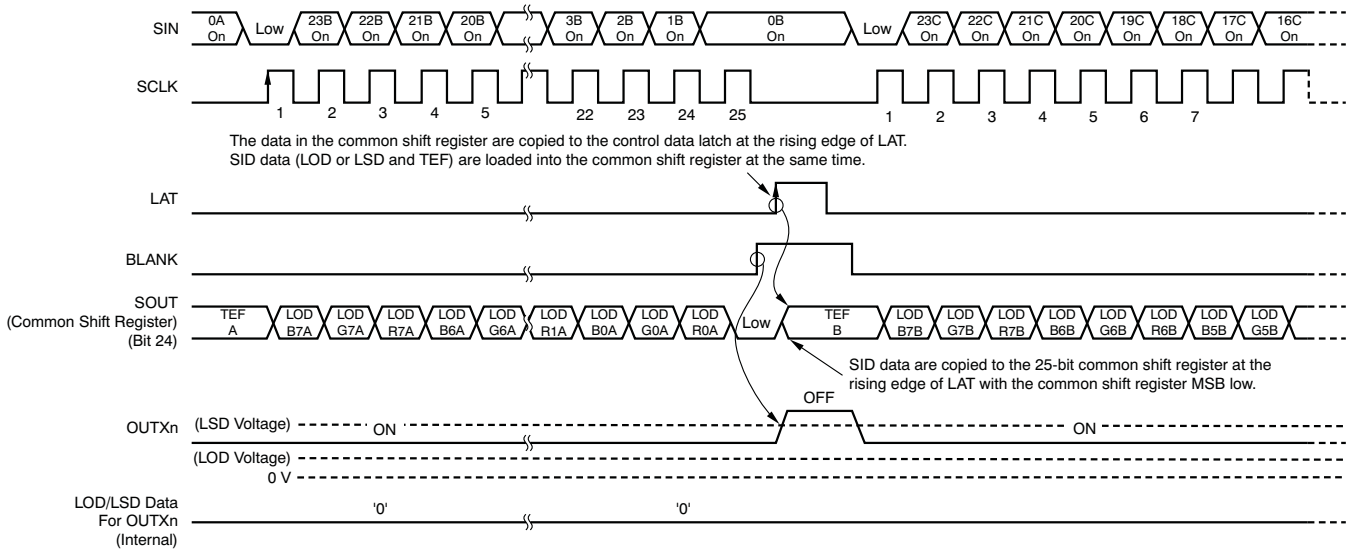


Figure 33. LOD, LSD, and TEF Operation (No LED Error)

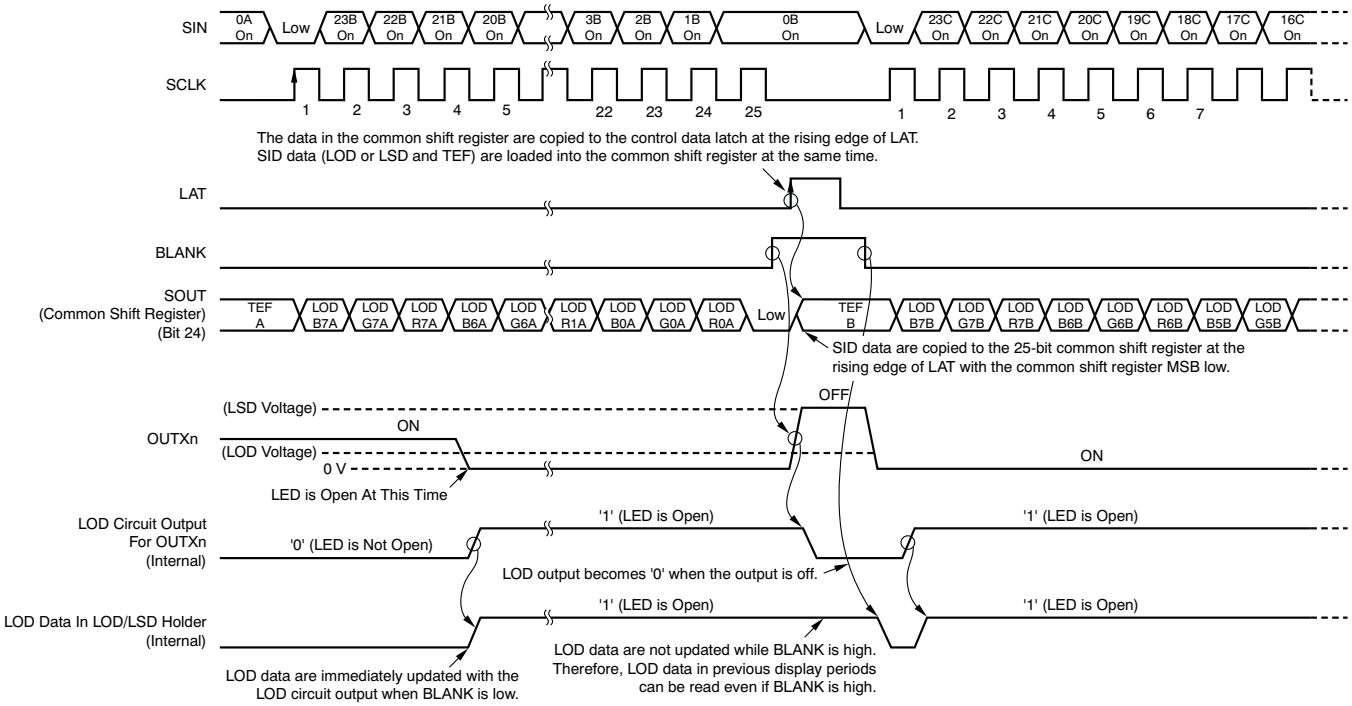


Figure 34. LOD, LSD, and TEF Operation (LED-Open Error)

Device Functional Modes (continued)

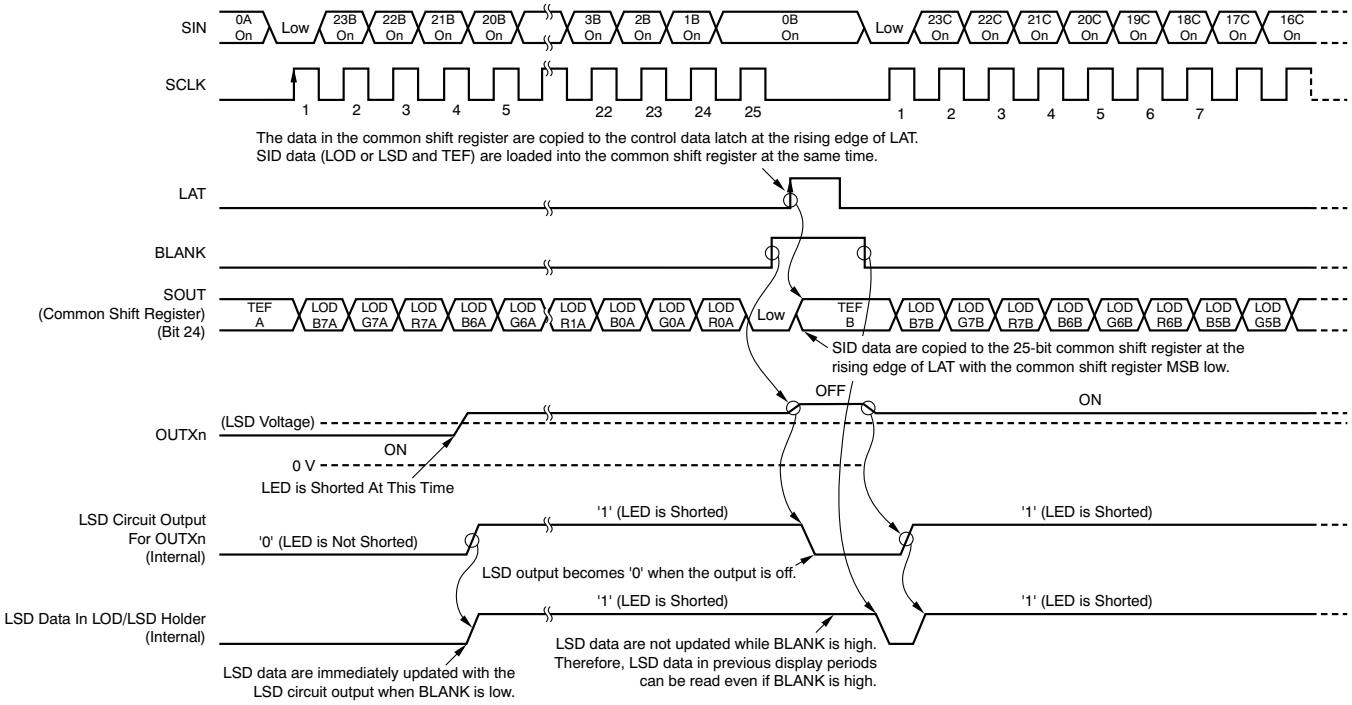


Figure 35. LOD, LSD, and TEF Operation (LED-Short Error)

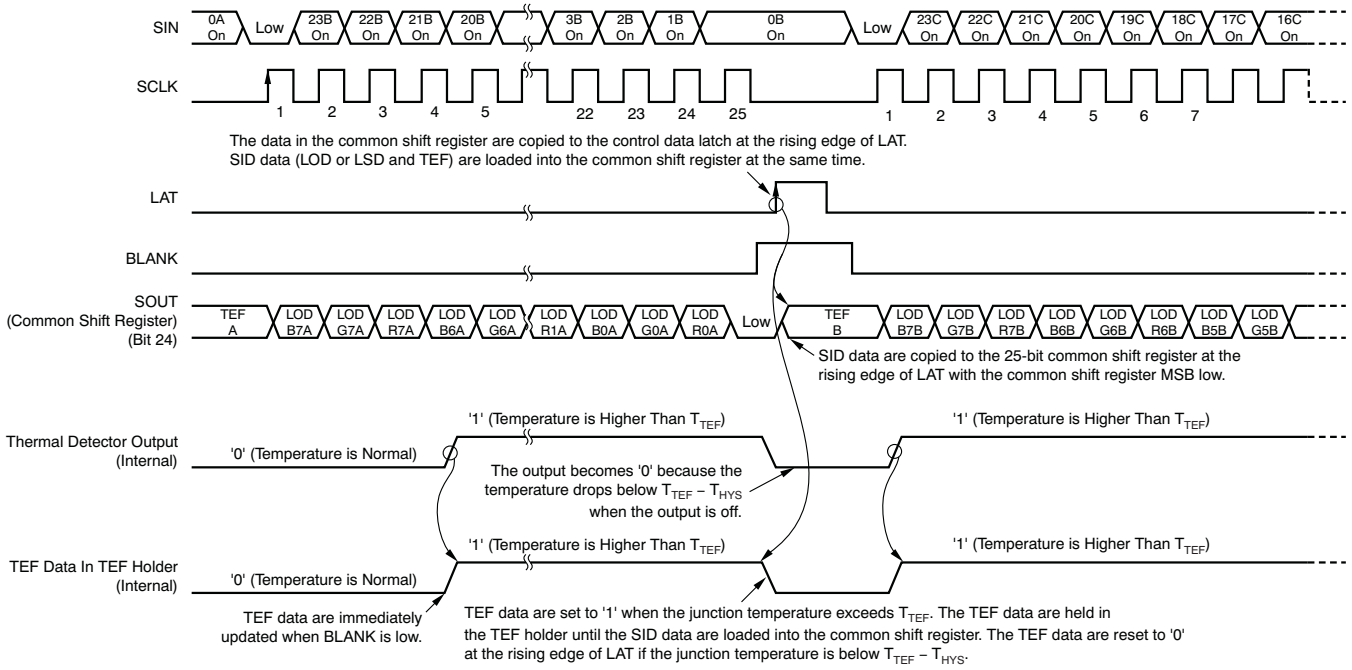


Figure 36. LOD, LSD, and TEF Operation (Thermal Error)

Device Functional Modes (continued)

8.4.2 Register and Data Latch Configuration

The TLC5952 device has two writable data latches: the output on-off data latch and the control data latch. Both data latches are 24 bits in length. If the common shift register MSB is 0, the least significant 24 bits of data from the 25-bit common shift register are latched into the output on-off data latch. If the MSB is 1, the data are latched into the control data latch. Figure 37 shows the common shift register and the control data latch configuration.

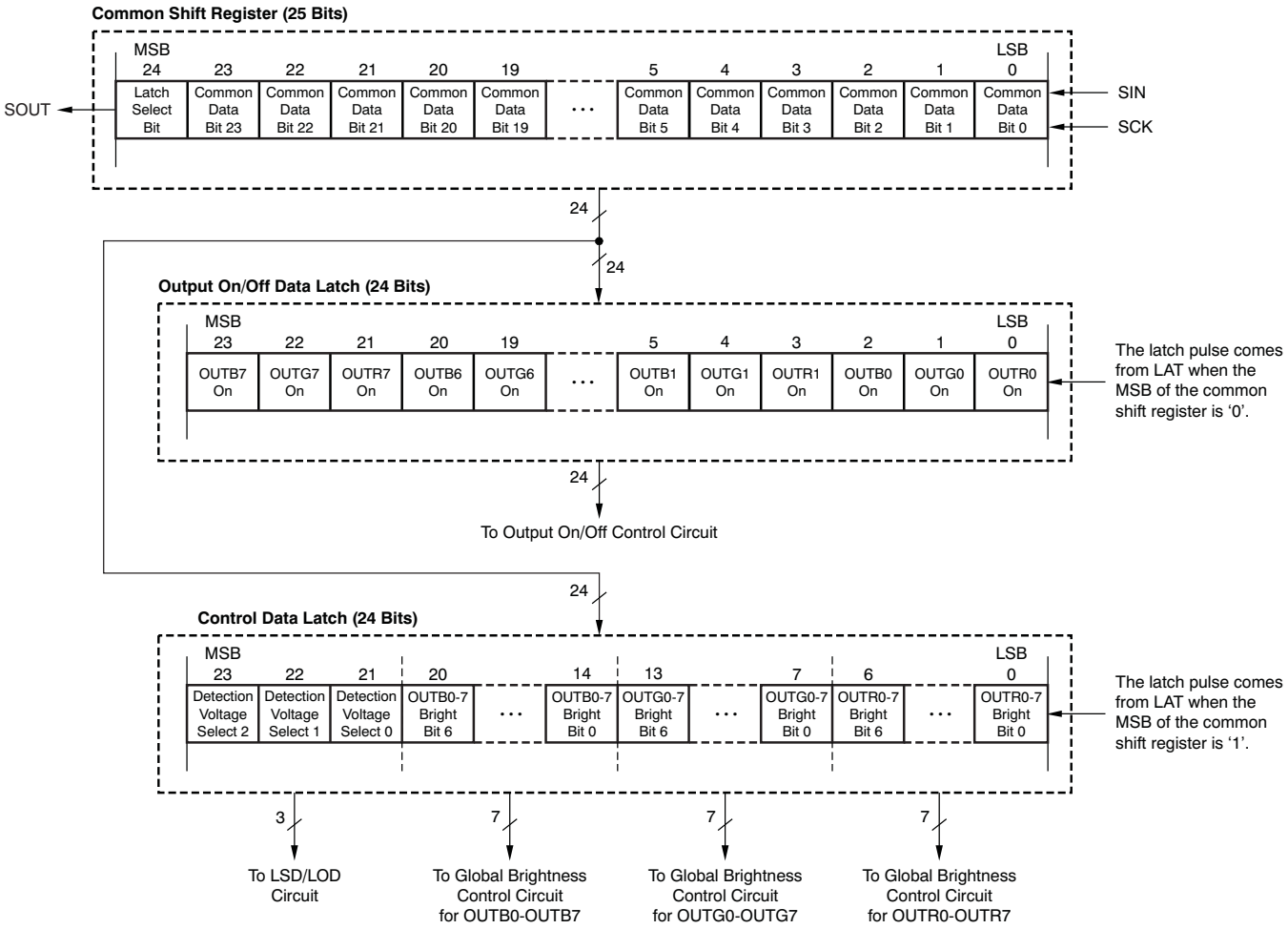


Figure 37. Grayscale Shift Register and Data-Latch Configuration

8.4.2.1 Output On-Off Data Latch

The output on-off data latch is 24 bits long. This latch is used to turn each output current sink (OUTRn, -Gn, -Bn) on or off. When the MSB of the common shift register is set to 0, the lower 24 bits are written to the output on-off data latch on the rising edge of LAT. If the output on-off data latch bit corresponding to an output is 0, the output is turned off; if the bit is a 1, the output is turned on.

When the device is powered on, the data in the output on-off data latch are not set to any default value. Therefore, the on-off control data should be written to the data latch before the constant-current outputs are turned on.

Device Functional Modes (continued)

8.4.2.2 Control-Data Latch

The control data latch is 24 bits long and is used to adjust the LED current for each color group (OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7). The LED current for each group can be adjusted between 0% and 100% of I_{OLCMAX} in 128 steps (7-bit resolution). This data latch is also used to select the error detection type, LED open detection (LOD) or LED short detection (LSD), and the threshold voltage. When the MSB of the common shift register is set to 1, the lower 24 bits are written to the control data latch on the rising edge of LAT. Table 4 shows the control data latch bit assignment.

When the device is powered on, the data in the control data latch are not set to a default value. Therefore, the control data latch data should be written to the latch before the constant-current outputs are turned on.

Table 4. Data Bit Assignment

BITS	DESCRIPTION
6–0	Global brightness control data for RED group (OUTR0-OUTR7, data = 00h to 7Fh)
13–7	Global brightness control data for GREEN group (OUTG0-OUTG7, data = 00h to 7Fh)
20–14	Global brightness control data for BLUE group (OUTB0-OUTB7, data = 00h to 7Fh)
23–21	Detection voltage and type select (data = 0h to 7h) 0 = LED open detection with 0.3 V (typ) threshold 1 = LED open detection with 0.6 V (typ) threshold 2 = LED open detection with 0.9 V (typ) threshold 3 = LED open detection with 1.2 V (typ) threshold 4 = LED short detection with V_{CC} × 60% (typ) threshold 5 = LED short detection with V_{CC} × 70% (typ) threshold 6 = LED short detection with V_{CC} × 80% (typ) threshold 7 = LED short detection with V_{CC} × 90% (typ) threshold

Figure 38 shows the operation to write data into the common shift register and control data latch.

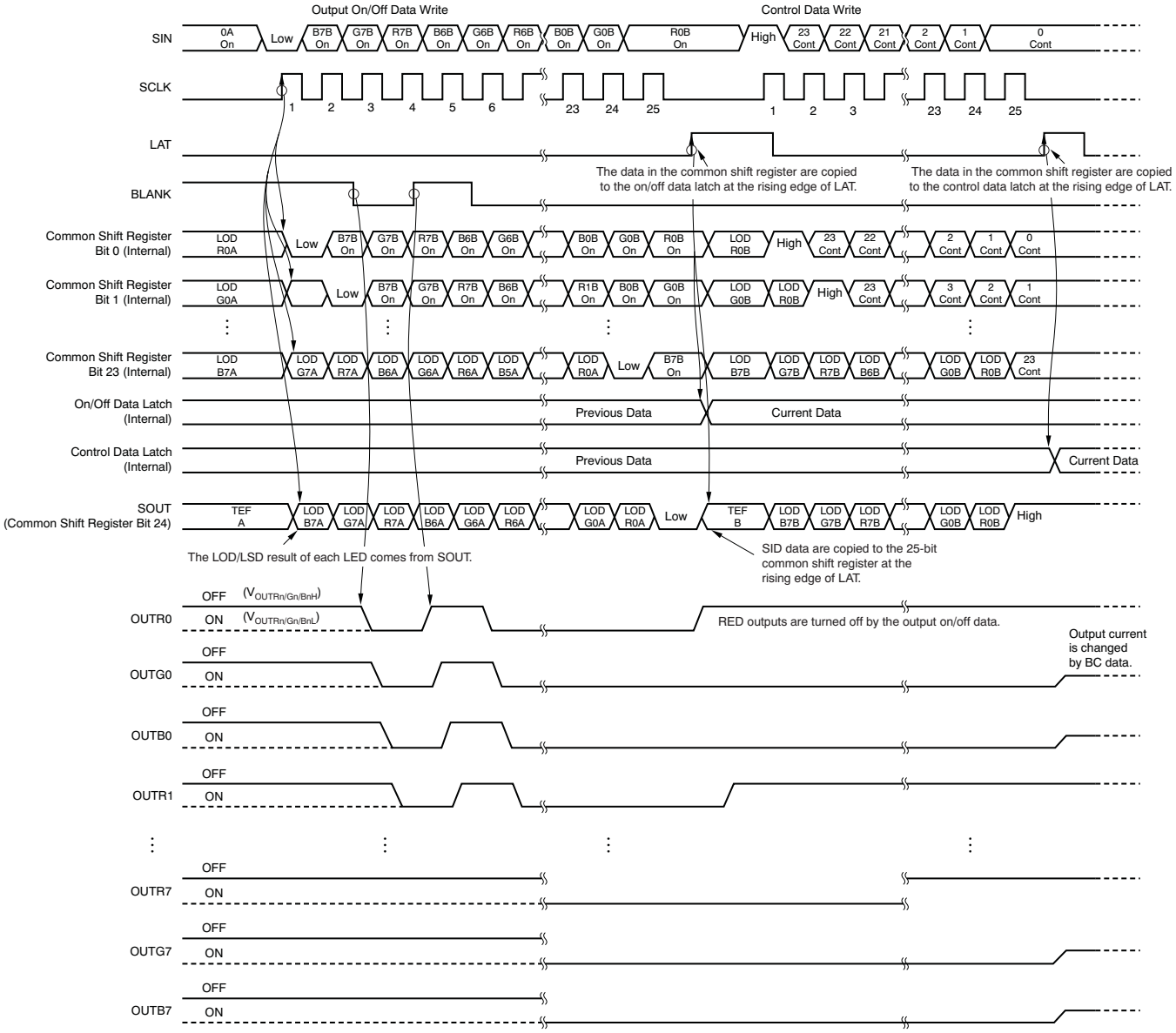


Figure 38. Data Write Operation

8.4.2.3 Status Information Data (SID)

The 25-bit word status information data (SID) contains the status of the LED open detection (LOD) or LED short detection (LSD), and thermal error flag (TEF). When the MSB of the common shift register is set to 0, the SID overwrites the common shift register data at the rising edge of LAT after the data in the common shift register are copied to the output on-off data latch. If the common shift register MSB is 1, the SID data are not copied to the common shift register.

After being copied into the common shift register, new SID data are not available until new data are written into the common shift register. If new data are not written, the LAT signal is ignored. To recheck SID data without changing the constant-current output on-off data, reprogram the common shift register with the same data that are currently programmed into the output on-off data latch. When LAT goes high, the output on-off data do not change, but new SID data are loaded into the common shift register. LOD, LSD, and TEF are shifted out of SOUT with each rising edge of SCLK.

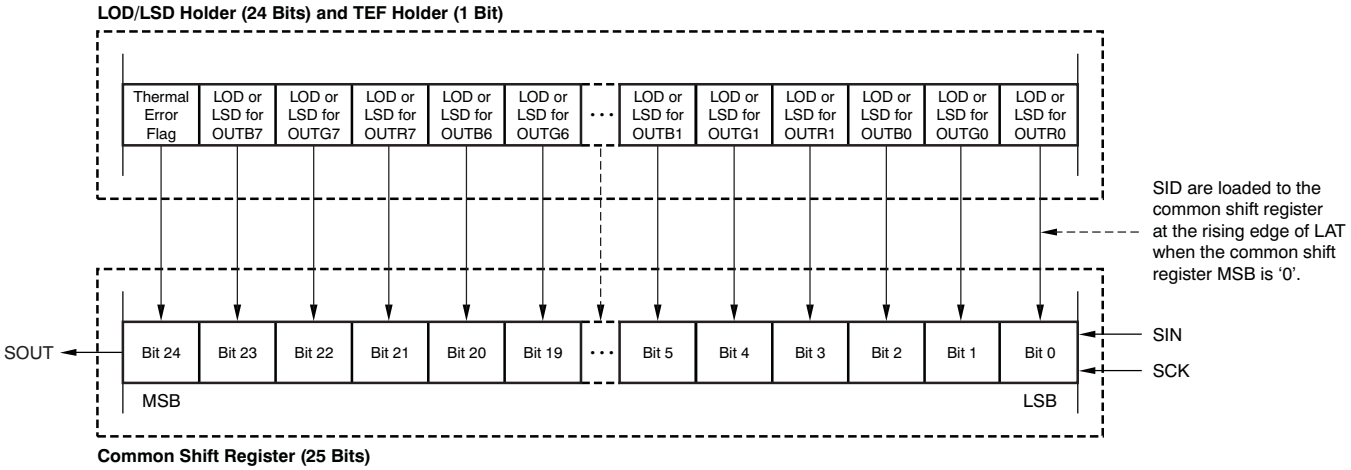


Figure 39. SID Load Assignment

8.4.2.4 LED-Open Detection (LOD), LED-Short Detection (LSD), And Thermal Error Flag (TEF)

LOD detects a fault caused by an LED open circuit or a short from OUTRn, -Gn, -Bn to ground by comparing the OUTRn, -Gn, -Bn voltage to the LOD detection threshold voltage level set in the control data latch (Table 4). If the OUTRn, -Gn, -Bn voltage is lower than the programmed voltage, that output LOD bit is set to 1 to indicate an open LED. Otherwise, the LOD bit is set to 0. LOD data are only valid for outputs programmed to be on. LOD data for outputs programmed to be off are always 0.

LSD data detects a fault caused by a shorted LED by comparing the OUTRn, -Gn, -Bn voltage to the LSD detection threshold voltage level set in the control data latch (Table 4). If the OUTRn, -Gn, -Bn voltage is higher than the programmed voltage, that output LOD bit is set to 1 to indicate a shorted LED. Otherwise, the LSD bit is set to 0. LSD data are only valid for outputs programmed to be on. LSD data for outputs programmed to be off are always 0.

LOD and LSD data are not valid until 1 μs after the falling edge of BLANK. Therefore, BLANK must be low for at least 1 μs before going high. At the rising edge of BLANK, the LOD and LSD detection data are latched in the LOD-LSD holder. Changes in the LOD or LSD data while BLANK is low are directly connected to the output of the LOD-LSD holder, but are only valid 1 μs after the change. The rising edge of LAT transfers the output data of the LOD-LSD holder to the common shift register.

As shown in Table 5, LOD and LSD data cannot be checked simultaneously. LOD and LSD data are not valid when TEF is active because all outputs are forced off.

The TEF bit indicates that the device junction temperature exceeds the temperature threshold (T_{TEF} = 165°C, typ). The TEF bit also indicates that the device has turned off all drivers to avoid overheating. The device automatically turns the drivers back on when the device temperature decreases to less than $T_{TEF} – T_{HYS}$. The TEF data are held in the TEF holder latch until the TEF data are loaded into the common shift register by the rising edge of LAT. If the device temperature falls below $T_{TEF} – T_{HYS}$ when LAT goes high, the TEF data in the TEF holder become 0. If the device temperature is not below $T_{TEF} – T_{HYS}$ when LAT goes high, then the TEF data remain 1. Table 5 shows a truth table for LOD, LSD, and TEF. Figure 33 to Figure 36 show different examples of LOD, LSD, and TEF operation.

Table 5. LOD, LSD, and TEF Truth Table

SID DATA	CONDITION		
	LED OPEN DETECTION (LOD, Voltage Select Data = 0h to 3h)	LED SHORT DETECTION (LSD, Voltage Select Data = 4h to 7h)	THERMAL ERROR FLAG (TEF)
0	LED is not open or the output is off ($V_{OUTRn/Gn/Bn}$ is greater than the voltage selected by the detection voltage select bit in the control data latch)	LED is not shorted or the output is off ($V_{OUTRn/Gn/Bn}$ is less than or equal to the voltage selected by the detection voltage select bit in the control data latch)	Junction temperature is lower than the detect temperature (T_{TEF}) before TEF is undetected or the detect temperature ($T_{TEF} – T_{HYS}$) after TEF is detected
1	LED is open or shorted to GND ($V_{OUTRn/Gn/Bn}$ is less than or equal to the voltage selected by the detection voltage select bit in the control data latch)	LED terminal is short or OUTn is short to higher voltage (V_{OUTn} is greater than The selected voltage by detection voltage select bit in the control data latch)	Junction temperature is higher than the detect temperature (T_{TEF})

8.4.2.5 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs when the device junction temperature (T_J) exceeds the temperature threshold (T_{TEF} = 165°C, typ). The outputs remain disabled as long as the overtemperature condition exists. The outputs are turned on again after the device junction temperature drops below ($T_{TEF} – T_{HYS}$).

8.4.2.6 Noise Reduction

Large surge currents may flow through the device and the board on which the device is mounted if all 24 LED channels turn on simultaneously when BLANK goes low. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5952 turns the LED channels on in a series delay to provide a circuit soft-start feature.

A small delay circuit is implemented between each output. When all bits of the on-off data latch are set to 1, each constant-current output turns on in order (OUTR0, OUTG0, OUTB0, OUTR1, OUTG1, OUTB1, OUTR2–OUTB6, OUTR7, OUTG7, and OUTB7) with a small delay between each output after BLANK goes low or LAT goes high; see Figure 38. Both turnon and turnoff are delayed.

9 Power Supply Recommendations

Connect at least one 10-nF ceramic capacitor as close as possible between the V_{CC} pin and ground. Additional capacitors are needed on the LED power supply to reduce ripple on the LED power supply to a minimum.

10 器件和文档支持

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

10.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

10.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5952DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5952	Samples
TLC5952DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5952	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

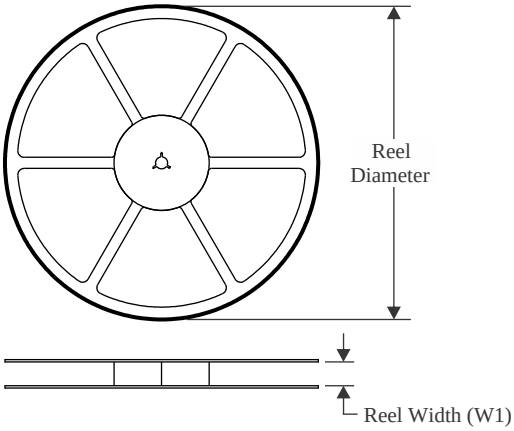
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

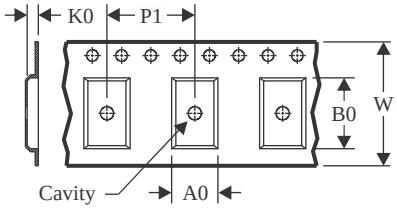
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

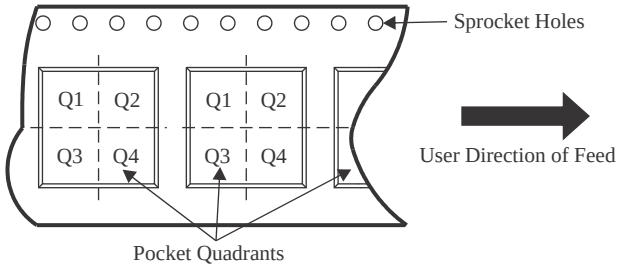


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

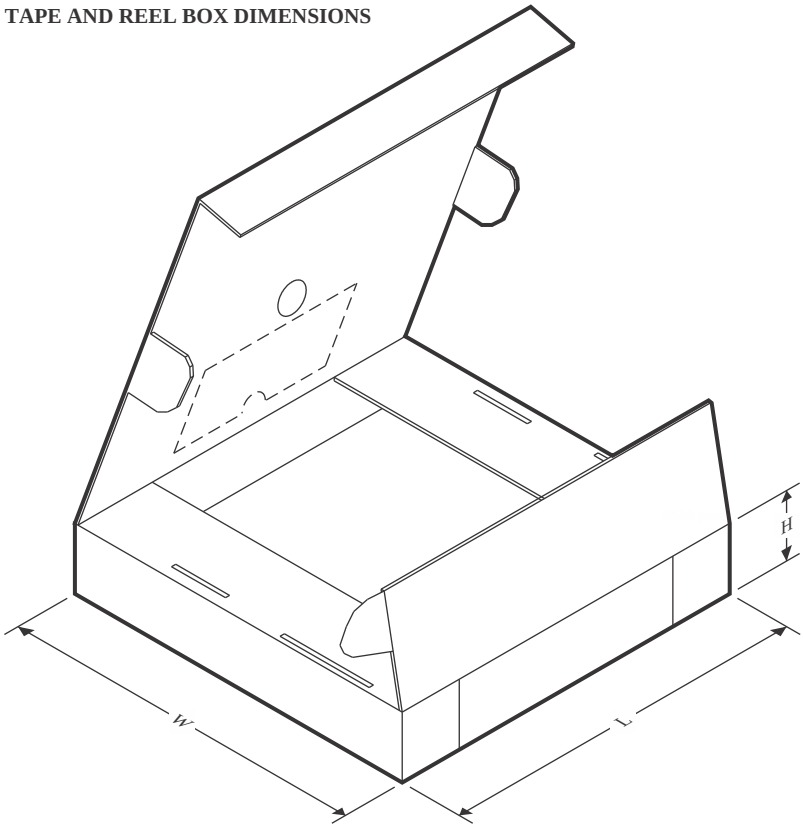
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5952DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

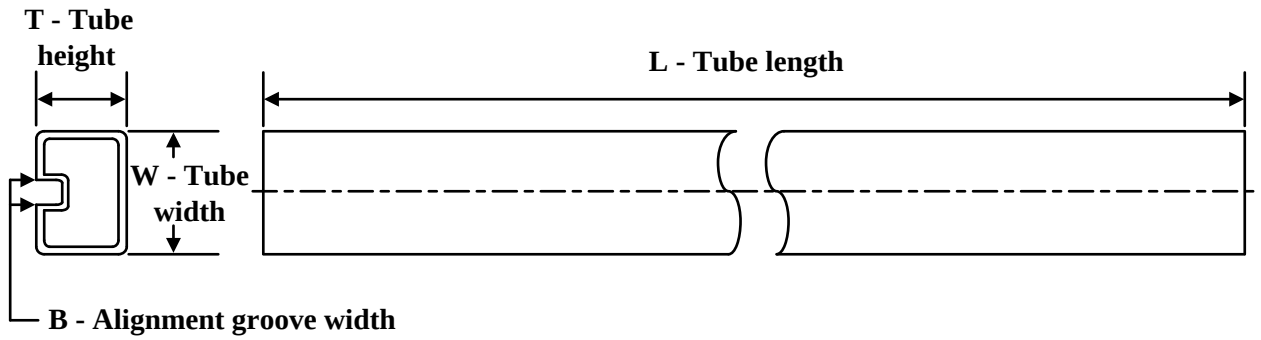
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5952DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5952DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

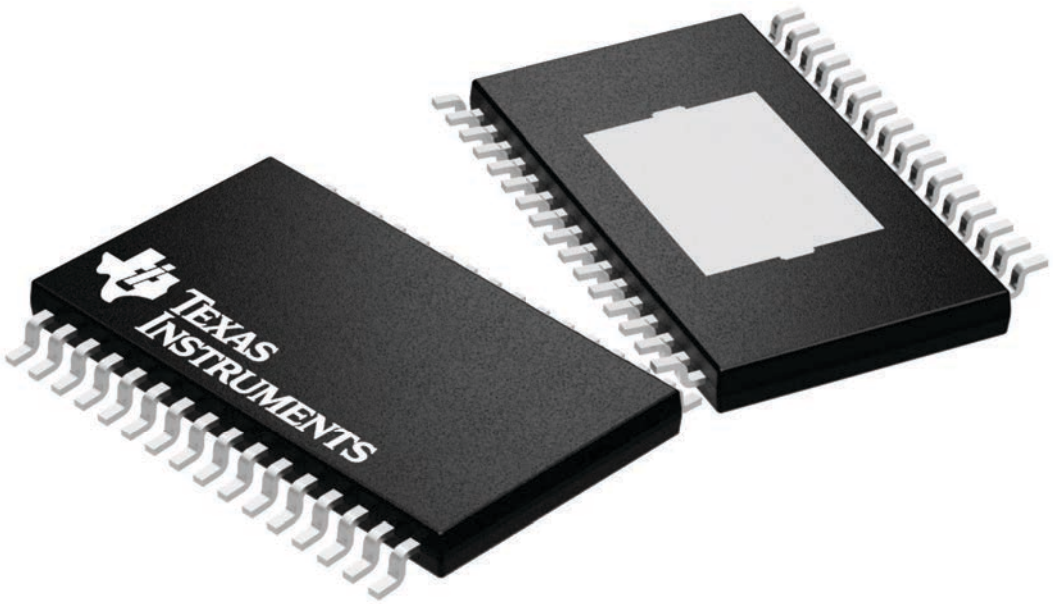
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

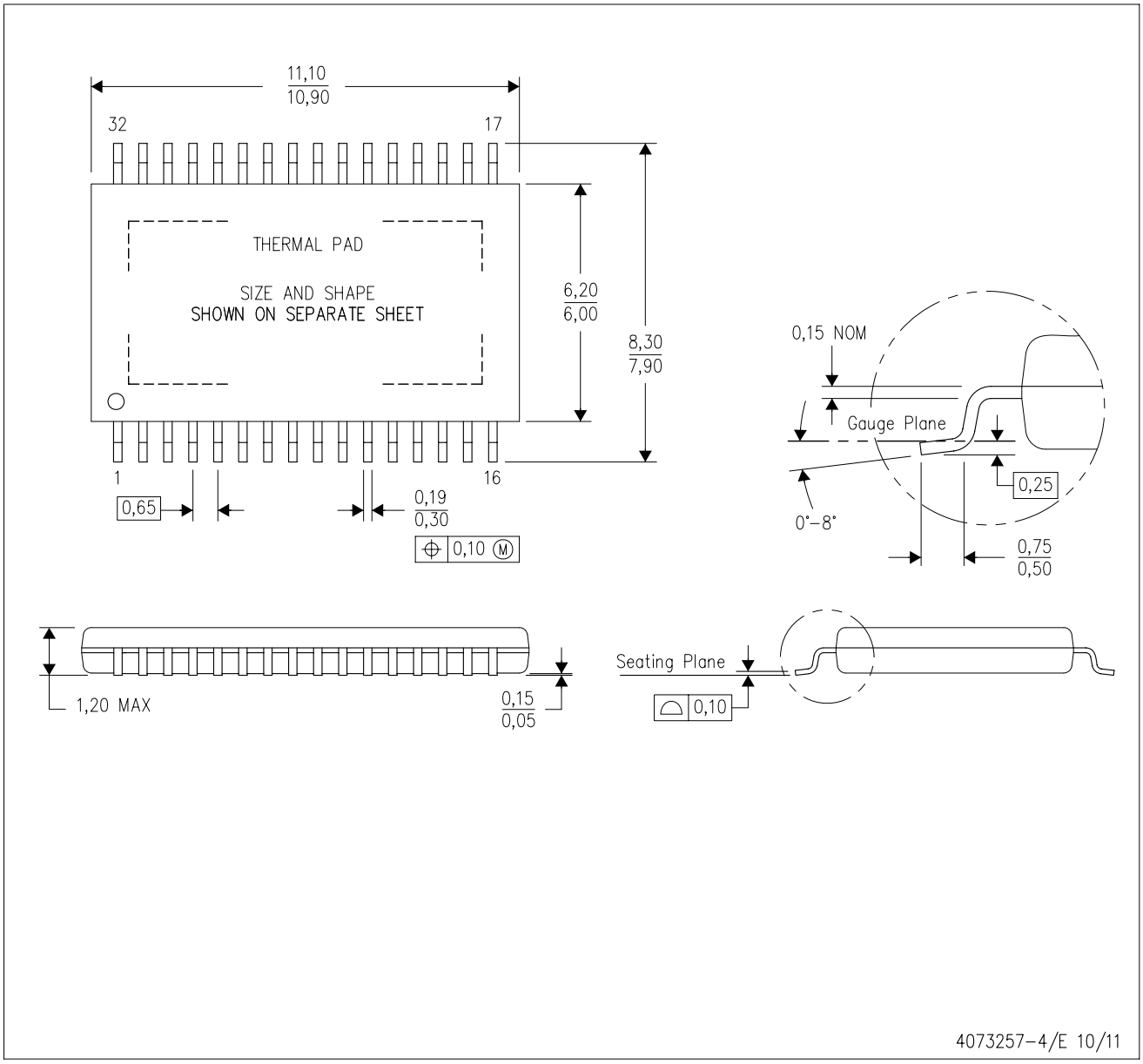
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

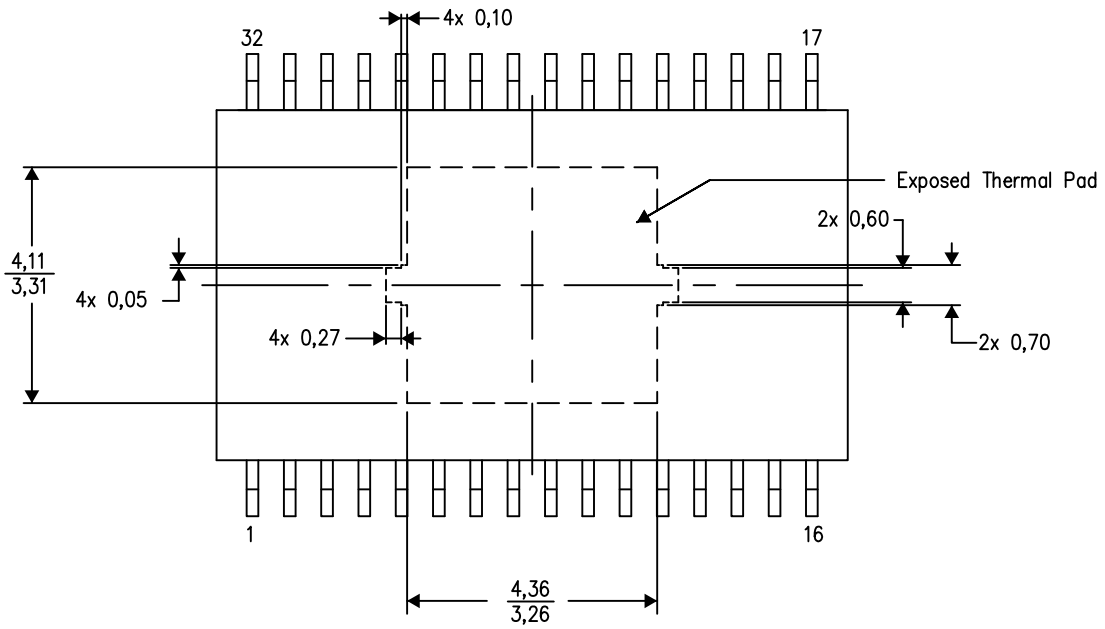
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

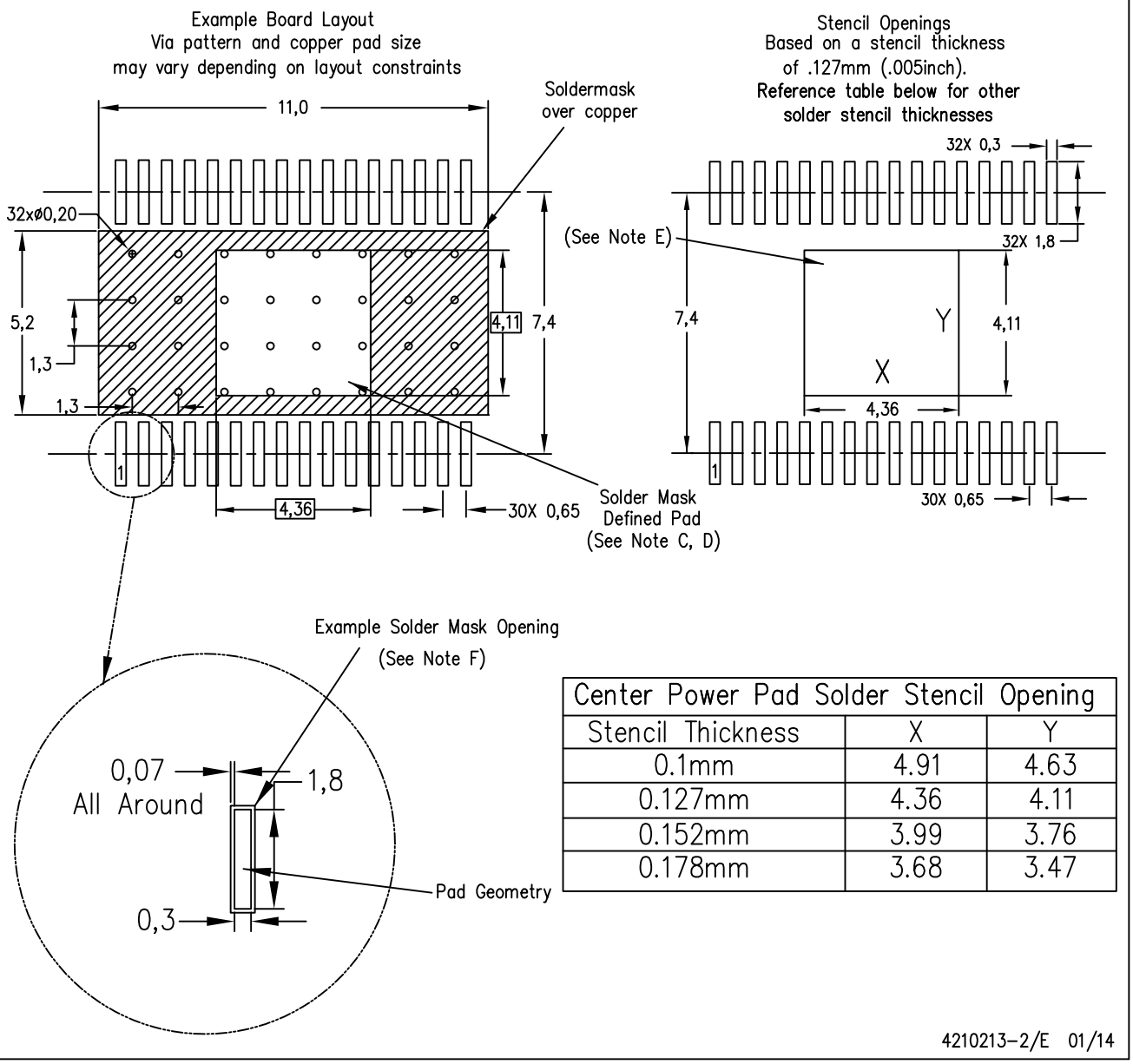
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

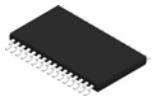
PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

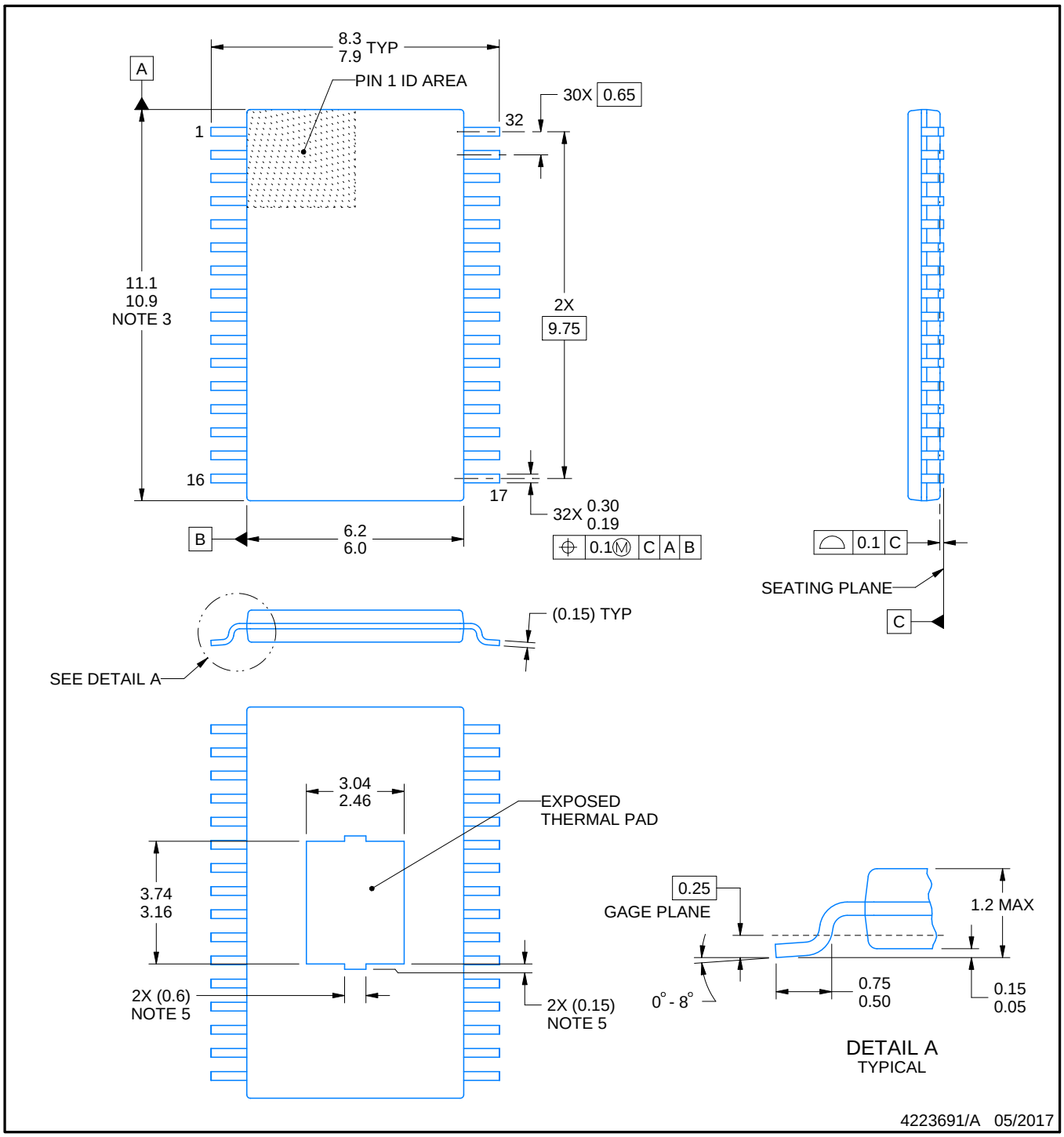


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

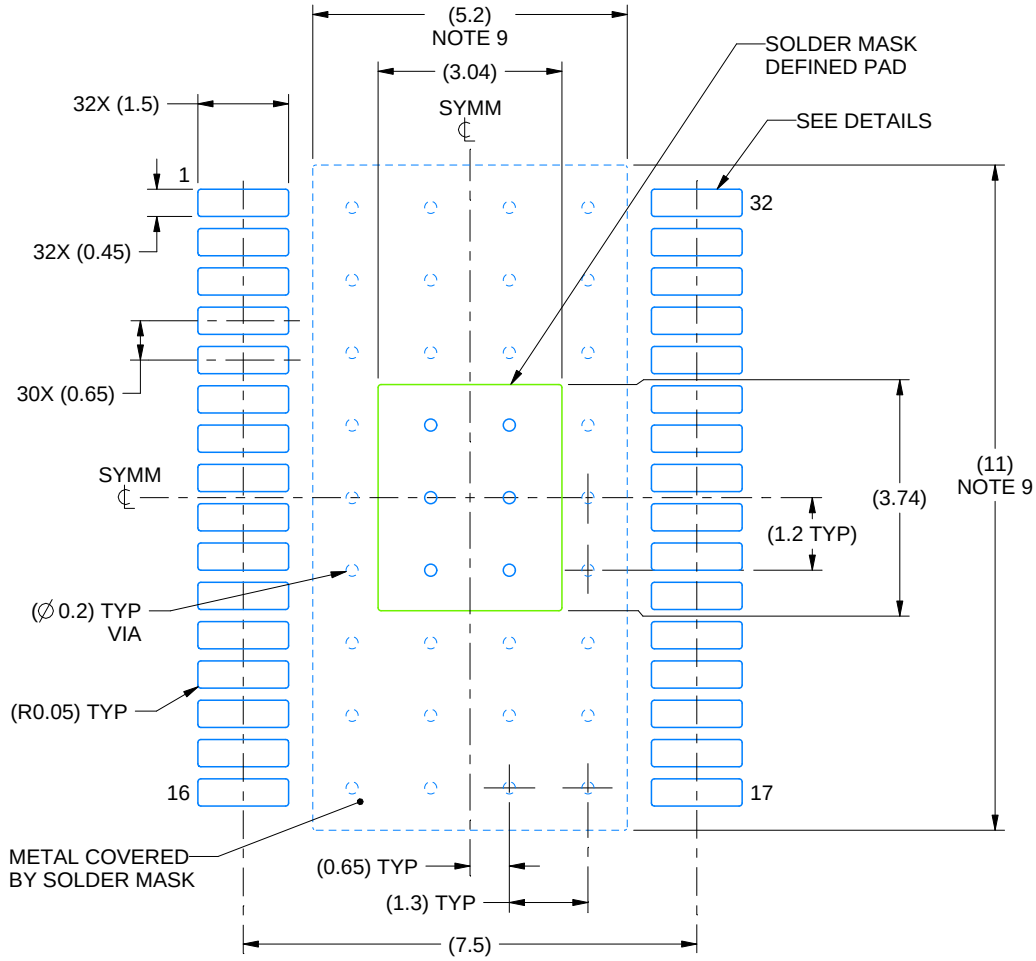
PLASTIC SMALL OUTLINE



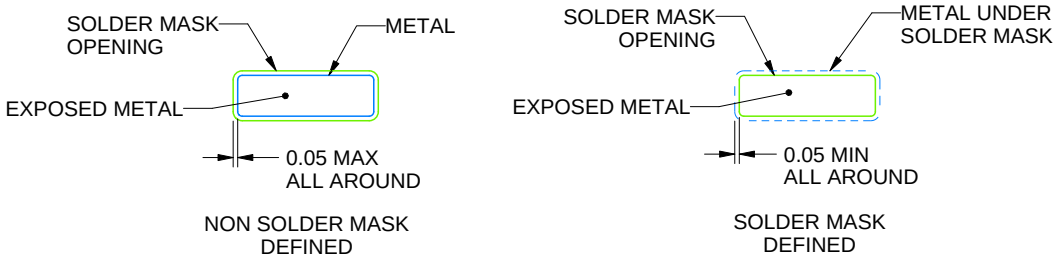
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

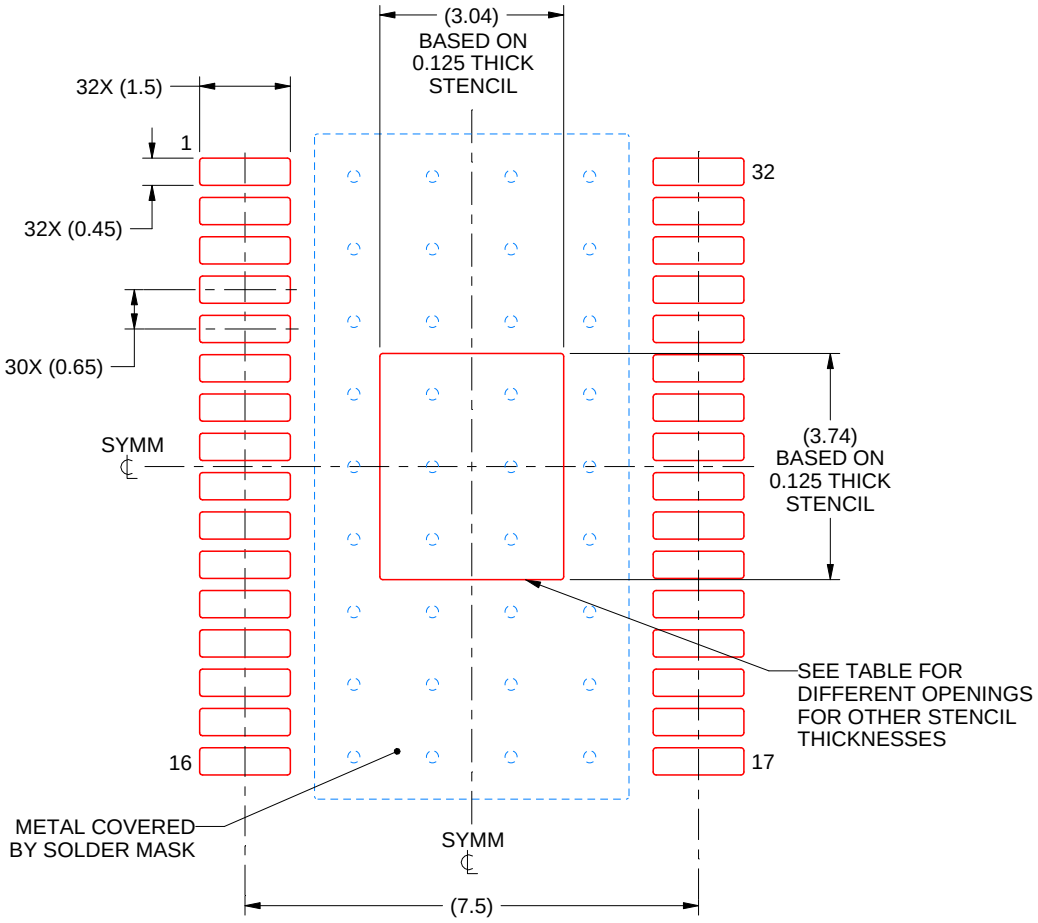


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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