16-CHANNEL LED DRIVER WITH DOT CORRECTION AND PRE-CHARGE FET

FEATURES

- **16 Channels**
- **Drive Capability**
  - **0 to 80 mA (Constant-Current Sink)**
- **Constant Current Accuracy: ±1% (typical)**
- **Serial Data Interface**
- **Fast Switching Output: T_r / T_f = 10ns (typical)**
- **CMOS Level Input/Output**
- **30 MHz Data Transfer Rate**
- **V_{CC} = 3.0 V to 5.5 V**
- **Operating Temperature = –40°C to 85°C**
- **LED Supply Voltage up to 17 V**
- **32-pin HTSSOP(PowerPAD™) and QFN Packages**
- **Dot Correction**
  - **7 bit (128 Steps)**
  - **individual adjustable for each channel**
- **Controlled In-Rush Current**
- **Pre-Charge FET**
- **Error Information**
  - **LOD: LED Open Detection**
  - **TEF: Thermal Error Flag**

APPLICATIONS

- **Monocolor, Multicolor, Fullcolor LED Display**
- **Monocolor, Multicolor LED Signboard**
- **Display Backlighting**
- **Multicolor LED lighting applications**

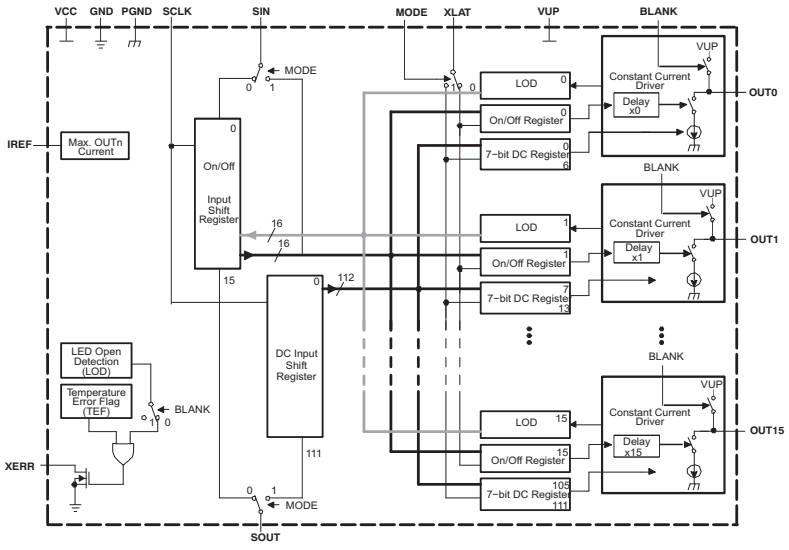
DESCRIPTION

The TLC5924 is a 16 channel constant-current sink driver. Each channel has a On/Off state and a 128-step adjustable constant current sink (dot correction). The dot correction adjusts the brightness variations between LED, LED channels and other LED drivers. Both dot correction and On/Off state are accessible via a serial data interface. A single external resistor sets the maximum current of all 16 channels.

Each constant-current output has a pre-charge FET that enables an improvement in image quality of the dynamic-drive LED display.

The TLC5924 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an over-temperature condition.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	Package	Part Number(1)
–40°C to 85°C	32-pin, HTSSOP, PowerPAD™	TLC5924DAP
	32-pin, 5 mm x 5 mm QFN	TLC5924RHB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)(2)

			TLC5924	UNIT
V_{CC}	Supply voltage(2)		–0.3 to 6	V
V_{UP}	Pre-charge voltage		–0.3 to 16	V
I_O	Output current (dc)	$I_{(OUT0)}$ to $I_{(OUT15)}$	90	mA
V_I	Input voltage range(2)	$V_{(BLANK)}$, $V_{(XLAT)}$, $V_{(SCLK)}$, $V_{(SIN)}$, $V_{(MODE)}$, $V_{(IREF)}$	–0.3 to V_{CC} + 0.3	V
V_O	Output voltage range(2)	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3 to V_{CC} + 0.3	V
		$V_{(OUT0)}$ to $V_{(OUT15)}$	-0.3 to V_{UP}	V
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2	kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	500	V
T_{stg}	Storage temperature range		–40 to 150	°C
	Power dissipation rating at (or above) T_A = 25°C(3)	HTSSOP (DAP)	42.54	mW/°C
		QFN (RHB)	27.86	mW/°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) See SLMA002 for more information about PowerPAD™

RECOMMENDED OPERATING CONDITIONS—DC Characteristics

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{UP}	Pre-charge voltage		3		15	V
V_O	Voltage applied to output, (Out0 - Out15)				V_{UP}	V
V_{IH}	High-level input voltage		0.8 VCC		VCC	V
V_{IL}	Low-level input voltage		GND		0.2 VCC	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15			80	mA
T_A	Operating free-air temperature range		-40		85	°C

RECOMMENDED OPERATING CONDITIONS—AC Characteristics

V_{CC} = 3 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency	SCLK			30	MHz
t_{wh0}, t_{wl0}	CLK pulse duration	SCLK=H/L	16			ns
t_{wh1}	XLAT pulse duration	XLAT=H	20			ns
t_{su0}	Setup time	SIN to SCLK↑(1)	10			ns
t_{su1}		SLCK↑ to XLAT↓(dot correction data)	10			
t_{su1a}		SCLK↑to XLAT↑ (ON/OFF data)	10			
t_{su2}		MODE↑↓ to SCLK↑	10			
t_{su3}		MODE↑↓ to XLAT↑	10			
t_{h0}	Hold time	SCLK↑ to SIN	10			ns
t_{h1}		XLAT↓ to SCLK↑ (dot correction data)	10			
t_{h1a}		XLAT↑ to SCLK↑ (ON/OFF data)	10			
t_{h2}		SCLK↑to MODE↑↓	10			
t_{h3}		XLAT↓ to MODE↑↓	10			

(1) "↑" and "↓" indicates a rising edge, and a falling edge respectively.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC}– 0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, XLAT, SCLK, SIN, MODE	–1		1	µA
I_{CC}	Supply current	No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ			6	mA
		No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			15	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			32	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω		36	65(1)	
I_{OLC}	Constant sink current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω	70	80	90	mA
I_{LO0}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15			0.1	µA
I_{LO1}		V_{XERR} = 5.5 V, No TEF and LOD			10	µA
ΔI_{OLC0}	Constant sink current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1%	± 4%	
ΔI_{OLC1}	Constant sink current error	device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 600 Ω		±4%	±8.5%	
ΔI_{OLC2}	Line regulation	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15, V_{CC} = 3 V to 5.5 V		±1	±4	%/V
ΔI_{OLC3}	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±2	±6	%/V
$R_{(ON)}$	Pre-charge FET on-resistance	V_{UP} = 3 V, V_O = 0 V, OUT0 to OUT15			10	KΩ
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature, rising temperature(2)	150	160	180	°C
$V_{(LOD)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 600 Ω	1.20	1.24	1.28	V

(1) Measured at device start-up temperature. Once the IC is operating (self heating), lower I_{CC} values will be seen. See Figure 20.
(2) Not tested. Specified by design.

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE TA = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
32-pin HTSSOP with PowerPAD(1) soldered	5318 mW	42.54 mW/°C	3403 mW	2765 mW
32-pin HTSSOP with PowerPAD(1) unsoldered	2820 mW	22.56 mW/°C	1805 mW	1466 mW
32-pin QFN	3482 mW	27.86 mW/°C	2228 mW	1811 mW

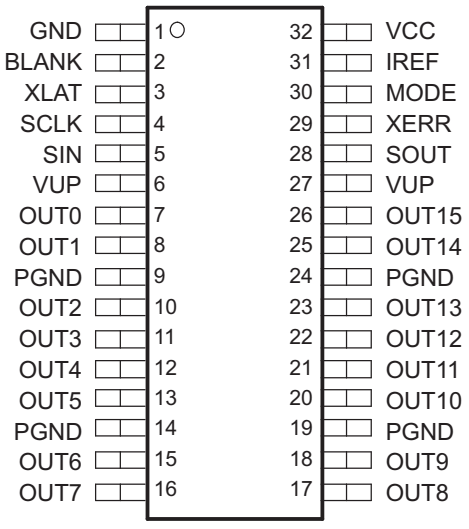
(1) The PowerPAD is soldered to the PCB with a 2 oz. copper trace. See SLMA002 for further information.

SWITCHING CHARACTERISTICS

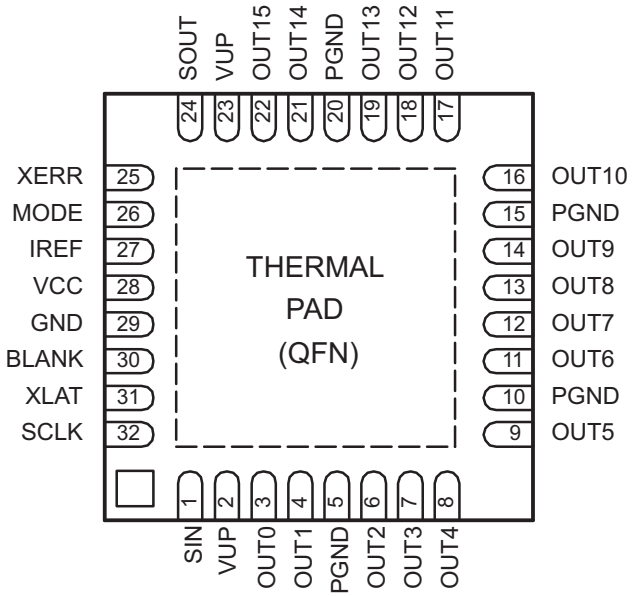
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT(see (1))			16	ns
t_{r1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{f0}	Fall time	SOUT (see (1))			16	ns
t_{f1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{pd0}	Propagation delay time	SCLK↑ to SOUT↑↓ (see (3)(4))			30	ns
t_{pd1}		MODE↑↓ to SOUT↑↓ (see (3))			30	
t_{pd2}		BLANK↑↓ to OUT0↑↓ (see (5)), Sink current On/Off			80	
t_{pd3}		XLAT↑ to OUT0↑↓ (see (5))			60	
t_{pd4}		OUTn↑↓ to XERR↑↓ (see (6))			1000	
t_{pd5}		XLAT↑ to I_{OUT}(dot-correction) (see (7))			1000	
t_d	Output delay time	OUTn↑ to OUT(n+1)↑, OUTn ↓ to OUT(n+1)↓ (see (5))	14	22	30	ns

(1) See Figure 4. Defined as from 10% to 90%
(2) See Figure 5. Defined as from 10% to 90%
(3) See Figure 4, Figure 16
(4) "↑" and "↓" indicates a rising edge, and a falling edge respectively.
(5) See Figure 5 and Figure 16
(6) See Figure 5, Figure 6, and Figure 16
(7) See Figure 5

DAP PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	QFN		
BLANK	2	30	I	Blank (Light OFF). When BLANK=H, All OUTn outputs are forced to VUP level. When BLANK=L, ON/OFF of OUTn outputs are controlled by input data.
GND	1	29		Ground
IREF	31	27	I/O	Reference current terminal
MODE	30	26	I	Mode select. When MODE=L, SIN, SOUT, SCLK, XLAT are connected to ON/OFF control logic. When MODE=H, SIN, SOUT, SCLK, XLAT are connected to dot-correction logic.
OUT0	7	3	O	Constant current output
OUT1	8	4	O	Constant current output
OUT2	10	6	O	Constant current output
OUT3	11	7	O	Constant current output
OUT4	12	8	O	Constant current output
OUT5	13	9	O	Constant current output
OUT6	15	11	O	Constant current output
OUT7	16	12	O	Constant current output
OUT8	17	13	O	Constant current output
OUT9	18	14	O	Constant current output
OUT10	20	16	O	Constant current output
OUT11	21	17	O	Constant current output
OUT12	22	18	O	Constant current output
OUT13	23	19	O	Constant current output
OUT14	25	21	O	Constant current output
OUT15	26	22	O	Constant current output
PGND	9, 14, 19, 24	5, 10, 15, 20		Power ground
VUP	6, 27	2, 23		Pre-charge power supply voltage
SCLK	4	32	I	Data shift clock. Note that the internal connections are switched by MODE (pin #30). At SCLK↑, the shift-registers selected by MODE shift the data.
SIN	5	1	I	Data input of serial I/F
SOUT	28	24	O	Data output of serial I/F
VCC	32	28		Power supply voltage
XERR	29	25	O	Error output. XERR is open drain terminal. XERR transistions from H to L when LOD or TEF detected.
XLAT	3	31	I	Data latch signal. When MODE = L (ON/OFF data mode), XLAT is an edge-triggered latch signal of ON/OFF registers. The serial data in ON/OFF input shift registers is latched into the ON/OFF registers at the rising edge of XLAT. When MODE = H (DC data mode), XLAT is a level-triggered latch signal of dot correction registers. The serial data in DC input shift registers is written into dot correction registers when XLAT = H. The data in dot correction registers is held constant when XLAT = L.

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

(Note: Resistor values are equivalent resistance and not tested).

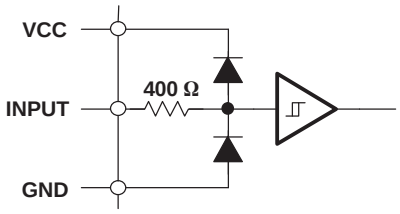


Figure 1. Input Equivalent Circuit (BLANK, XLAT, SCLK, SIN, MODE)

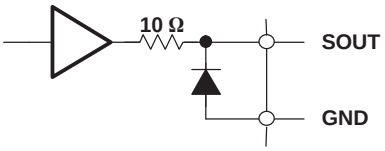


Figure 2. Output Equivalent Circuit

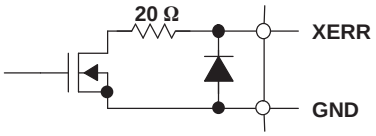


Figure 3. Output Equivalent Circuit (XERR)

PARAMETER MEASUREMENT INFORMATION

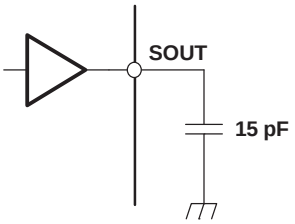


Figure 4. Test Circuit for t_{r0}, t_{f0}, t_{pd0}, t_{pd1}

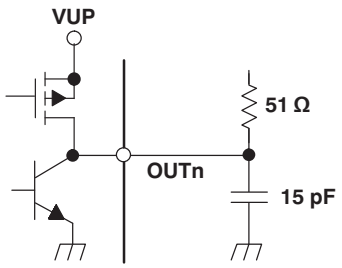


Figure 5. Test Circuit for t_{r1}, t_{f1}, t_{pd2}, t_{pd3}, t_{pd5}, t_{td}

PARAMETER MEASUREMENT INFORMATION (continued)

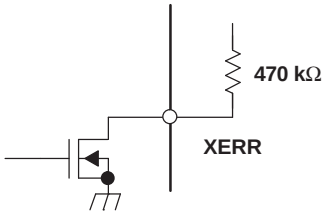


Figure 6. Test Circuit for t_{pd4}

PRINCIPLES OF OPERATION

Setting Maximum Channel Current

The maximum output current per channel is set by a single external resistor, $R_{(IREF)}$, which is placed between IREF and GND. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 40. The maximum output current per channel can be calculated by Equation 1:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 40 \quad (1)$$

where:

V_{IREF} = 1.24V typ.

R_{IREF} = User selected external resistor ®$_{IREF}$ should not be smaller than 600 Ω)

Figure 17 shows the maximum output current, I_{OLC}, versus $R_{(IREF)}$. In Figure 17, $R_{(IREF)}$ is the value of the resistor between IREF terminal to ground, and I_{OLC} is the constant output current of OUT0,.....OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output per channel is 40 times the current flowing out of the IREF pin. The maximum current from IREF equals 1.24V/600Ω.

Setting Dot-Correction

The TLC5924 has the capability to fine adjust the current of each channel, OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LED connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 7-bit word. The channel output can be adjusted in 128 steps from 0% to 100% of the maximum output current I_{MAX}. Dot correction for all channels must be entered at the same time. Equation 2 determines the output current for each OUTn:

$$I_{Outn} = \frac{I_{MAX} \times DC_n}{127} \quad (2)$$

where:

I_{Max} = the maximum programmable current of each output

DCn = the programmed dot-correction value for output n (DCn = 0, 1, 2 ...127)

n = 0, 1, 2 ... 15

Dot correction data are entered for all channels at the same time. The complete dot correction data format consists of 16 x 7-bit words, which forms a 112-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 7 shows the DC data format. The DC15.6 in Figure 7 stands for the 6th most significant bit for output 15.

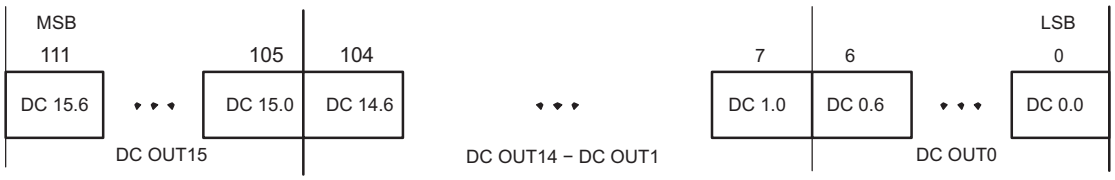


Figure 7. DC Data Format

To input data into dot correction register, MODE must be set to high. The internal input shift register is then set to 112-bit width. After all serial data is clocked in, a high level pulse of XLAT signal connects the serial data to the dot correction register. The dot correction registers are level-triggered latches of XLAT signal. The serial data is latched into the dot correction registers when XLAT goes low. The data in dot correction registers is held constant when XLAT is low. BLANK signal does not need to be high to latch in new data. Since XLAT is a level-triggered signal when MODE is high, SCLK and SIN must not be changed while XLAT is high. (Figure 16).

PRINCIPLES OF OPERATION (continued)

Output Enable

When BLANK = H, TLC5924 switches off the sink current of all OUTn with each output delay, then switches on the pre-charge FET of all OUTn. When BLANK = L, the TLC5924 switches off the pre-charge FETs, and enables the sink current set by input data. See "Delay Between Outputs" section for more detail on the output delay.

Table 1. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	VUP

Setting Channel On/Off Status

All OUTn channels of TLC5924 can be switched on or off independently. Each of the channels can be programmed with a 1-bit word. On/Off data are entered for all channels at the same time. The complete On/Off data format consists of 16 x 1-bit words, which form a 16-bit wide data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 8 shows the On/Off data format.

Figure 8. On/Off Data Format

To input On/Off data into On/Off register MODE must be set to low. The internal input shift register is then set to 16 bit width. After all serial data is clocked in, a rising edge of XLAT is used to latch data into the On/Off register. The ON/OFF register is an edge-triggered latch of XLAT signal. BLANK signal does not need to be high to latch in new data. Figure 16 shows the On/Off data input timing chart.

Delay Between Outputs

The TLC5924 has graduated delay circuits between outputs. These delay circuits can be found in the constant current block of the device (see Functional Block Diagram). The fixed delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20 ns delay, OUT2 has 40 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before BLANK is pulled high will still turn on and off at the determined delayed time regardless of the state of BLANK. Therefore, every LED will be illuminated for the amount of time BLANK is low.

Pre-Charge FET On/Off Timing

The pre-charge FETs turn on at the same time; and, they turn on at the time the last output that is on turns off.

All pre-charge FETs turn off just after BLANK signal becomes low level, regardless of on/off data of each output. Figure 9 shows the example of BLANK and OUTn timing.

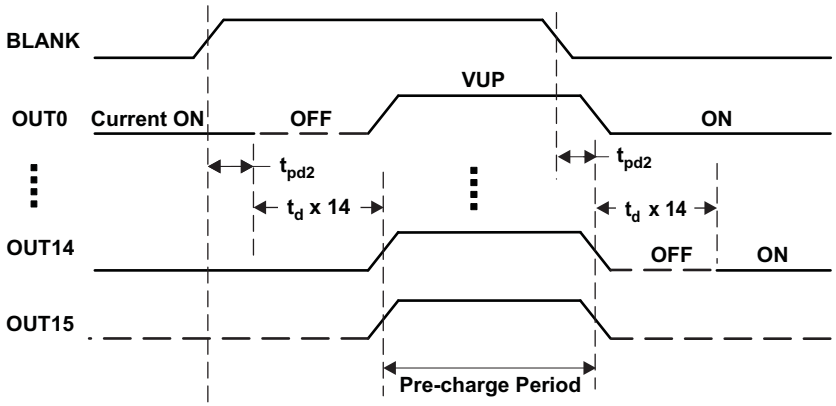


Figure 9. Timing Chart of BLANK and OUTn (On/Off Data Condition: OUT0=H, OUT14=H, OUT15=L)

VUP: Pre-Charge Power Supply

VUP is a pre-charge power supply terminal. The pre-charge voltage should be supplied to this terminal for normal operation. When VUP terminal is open, TLC5924 keeps OUT0-15 open. TLC5924 has two VUP pins as shown in the *Terminal Functions Table*. Both VUP pins should be connected to the pre-charge power supply as shown in Figure 10.

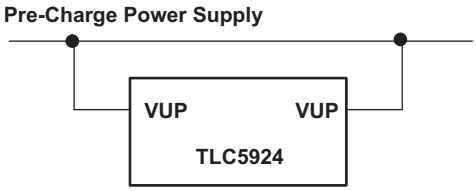


Figure 10. VUP Power Supply

Serial Interface Data Transfer Rate

The TLC5924 includes a flexible serial interface, which can be connected to a microcontroller or digital signal processor. Only 3 pins are required to input data into the device. The rising edge of SCLK signal shifts the data from SIN pin to internal shift register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data is clocked in with MSB first. Multiple TLC5924 devices can be cascaded by connecting SOUT pin of one device with SIN pin of following device. The SOUT pin can also be connected to controller to receive LOD information from TLC5924.

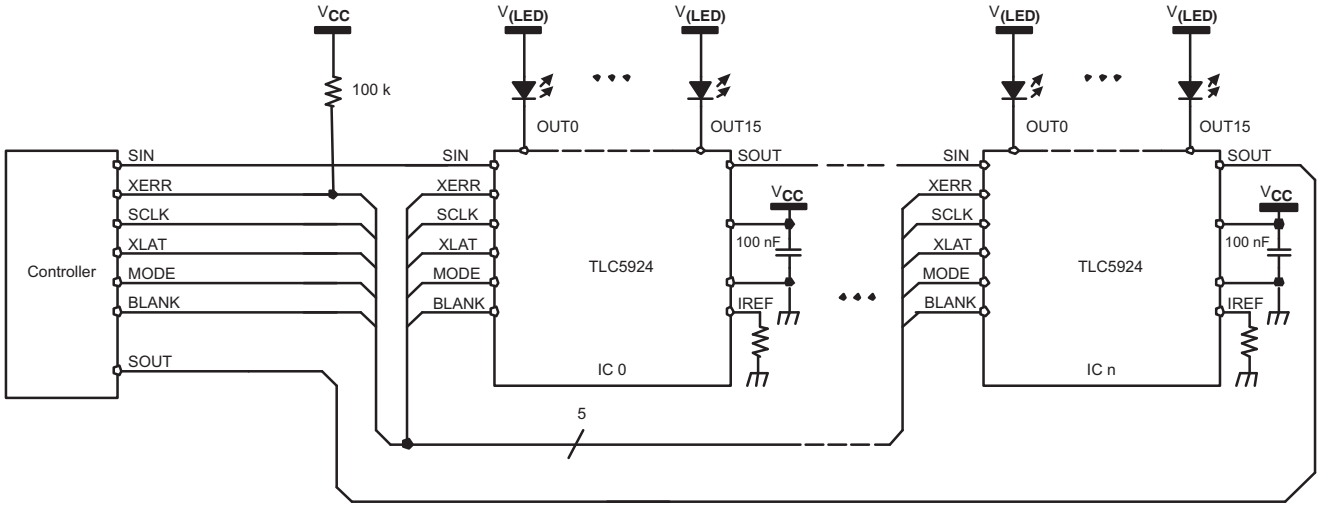


Figure 11. Cascading Devices

Figure 11 shows a example application with *n* cascaded TLC5924 devices connected to a controller. The maximum number of cascaded TLC5924 devices depends on application system and data transfer rate. Equation 3 calculates the minimum data input frequency needed.

$$f\_(SCLK) = 112 \times f\_(update) \times n \quad (3)$$

where:

f_(SCLK): The minimum data input frequency for SCLK and SIN.

f_(update): The update rate of the whole cascaded system.

n: The number of cascaded TLC5924 devices.

Operating Modes

The TLC5924 has different operating modes depending on MODE signal. Table 2 shows the available operating modes. The values in the input shift registers, DC register and On/Off register are unknown just after power on. The DC and On/Off register values should be properly stored through the serial interface before starting the operation.

Table 2. TLC5924 Operating Modes Truth Table

MODE SIGNAL	INPUT SHIFT REGISTER	MODE
LOW	16 bit	On/Off Mode
HIGH	112 bit	Dot Correction Data Input Mode

Error Information Output

The open-drain output XERR is used to report both of the TLC5924 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through a external pull-up resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pull-up resistor. This reduces the number of signals needed to report a system error.

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 3. XERR Truth Table

CONDITION			ERROR INFORMATION		XERR
TEMPERATURE	BLANK	OUTn VOLTAGE	TEF	LODn	
$T_J < T_{(TEF)}$	H	Don't Care	L	L	High-Z(1)
$T_J > T_{(TEF)}$			H		L
$T_J < T_{(TEF)}$	L	$OUTn > V_{(LOD)}$	L	L	High-Z
		$OUTn < V_{(LOD)}$		H	L
$T_J > T_{(TEF)}$		$OUTn > V_{(LOD)}$	H	L	L
		$OUTn < V_{(LOD)}$		H	L

(1) Note: High-Z means high impedance

TEF: Thermal Error Flag

The TLC5924 provides a temperature error flag (TEF) circuit to indicate an over-temperature condition of the IC. If the junction temperature exceeds the threshold temperature $T_{(TEF)}$ (160°C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance.

LOD: LED-Open Detection

The TLC5924 has an LED-open detector to detect broken or disconnected LEDs, which should be connected to the output. The LED-open detector pulls the XERR pin down to GND when the LED open is detected. An open LED is detected when the following three conditions are met:

1. BLANK is low
2. On/Off data is high
3. The voltage of OUTn is less than 0.3 V (typical)

The LOD status of each output can also be read out from the SOUT pin. Figure 12 shows the LOD data format. Table 4 shows the LOD truth table.

Figure 12. LOD Data Format

Table 4. LOD Data Truth Table

LED	ON/OFF	LOD BIT
Good	On	0
Good	Off	0
Bad	On	1
Bad	Off	0

Key Timing Requirements to Reading LOD

- LOD status flag

  The LOD status flag becomes active if the output voltage is <0.3 V (typical) when the output sink current turns on. There is a 1-µs time delay from the time the output sink current turns on until the time the LOD status flag becomes valid. The timing for each channel's LOD status to become valid is shifted by the 30 ns channel-to-channel turn-on time. After BLANK goes low, OUT0 LOD status is valid when tpd2 + tpd4 = 60 ns + 1 µs = 1.06 µs. OUT1 LOD status is valid when tpd2 + tpd4 + td = 60 ns + 1 µs + 30 ns = 1.09 µs. OUT3 LOD status is valid when tpd2 + tpd4 + 2*td = 1.12 µs, and so on.

- LOD internal latch

  The TLC5924 has an internal latch to hold each channel's LOD status flag information, as shown in Figure 13. When MODE is low, the LOD status information is latched into this latch on the rising edge of XLAT. This is an edge-triggered latch. To ensure that a valid LOD status flag is latched, BLANK must be low when XLAT goes high. After the rising edge of XLAT, changes in the status flags do not affect the values in the LOD latch.

- Loading LOD data to the input shift register

  The LOD data must be transferred to the input shift register before it is available to be clocked out of SOUT. The internal shift register has a set/reset function that is controlled by the LOD internal latch. While XLAT is high, the LOD internal latch holds the input shift register in either set or reset, depending on the value in the latch. This effectively puts the LOD data into the input shift register where it remains as long as XLAT is high. The values in the input shift register are unaffected by any other signals, including SIN and SCLK while XLAT is high. During this time, the status of OUT15 is present on SOUT.

- Latching LOD data into the internal shift register

  While XLAT is high, the status of OUT15 is present on SOUT. When XLAT transitions low, all data is latched into the Input shift register, and the LOD internal latch is disconnected from the internal shift register.

- Clocking LOD data out of SOUT

  While XLAT is low and SCLK is low, the status of OUT15 is on SOUT. On the next rising edge of SCLK, the status of OUT14 shifts to SOUT. Each subsequent rising edge of SCLK shifts the LOD data out of SOUT. XLAT must stay low until all LOD data is clocked out of SOUT. See *Shifting the LOD Data Out* section for more details.

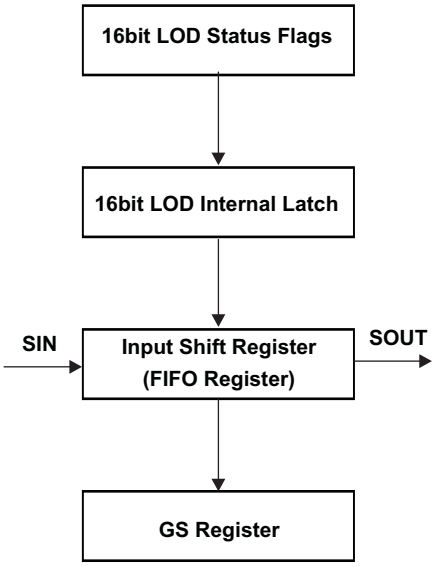


Figure 13. LOD Flags and Latches

Shifting the LOD Data Out

SOUT outputs the LOD data as shown in Figure 14, where:

- XLAT rising edge

  Holds the LOD status flag. SOUT outputs LOD OUT15 data. BLANK must be low.
- XLAT = H

  Sets or resets the input shift register depending on each LOD data.

  Set/Reset function is higher priority than shifting the register value. If XLAT is high and the SCLK pin is pulsed, all LOD data are kept in the shift register and SOUT keeps the LOD OUT15 data.
- XLAT = L

  Ready to shift out LOD data by SCLK. SOUT contains LOD OUT15 data at this time. BLANK can be high or low during this time.
- SCLK rising edge

  SOUT outputs LOD OUT14 at the first SCLK rising edge. SOUT outputs LOD OUT13 at the second SCLK rising edge, and continues to output the next LOD data at each SCLK rising edge.

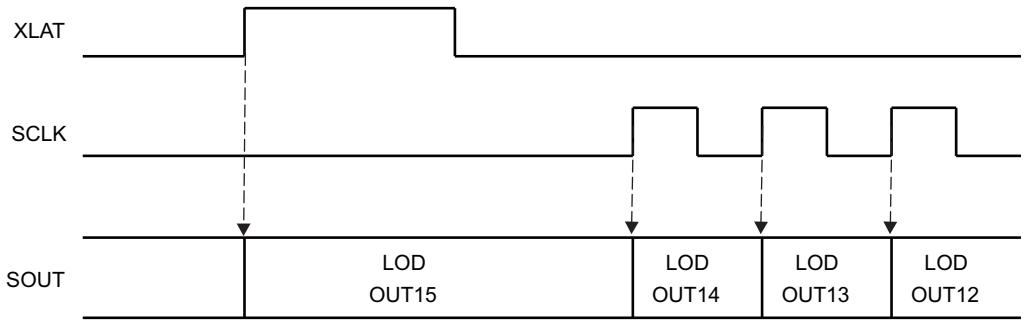


Figure 14. The LOD Data of SOUT

Figure 15 shows the timing chart of reading LOD data.

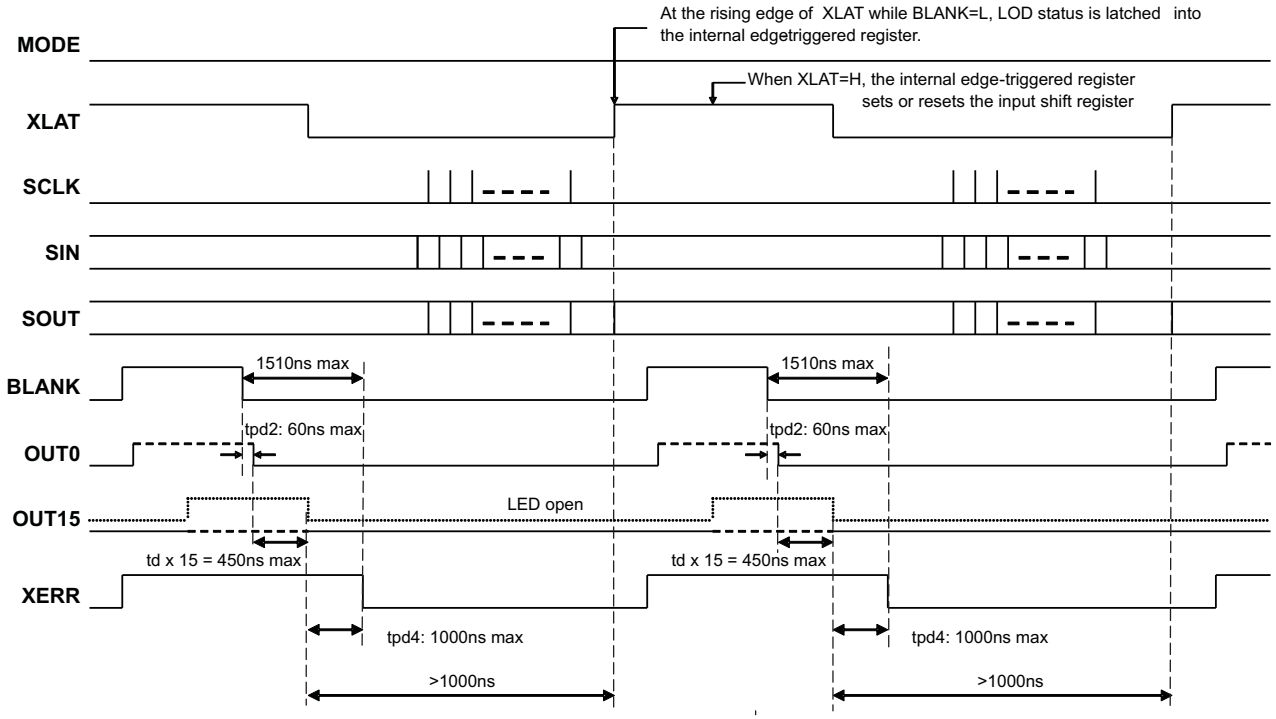


Figure 15. Timing Chart of Reading LOD Data

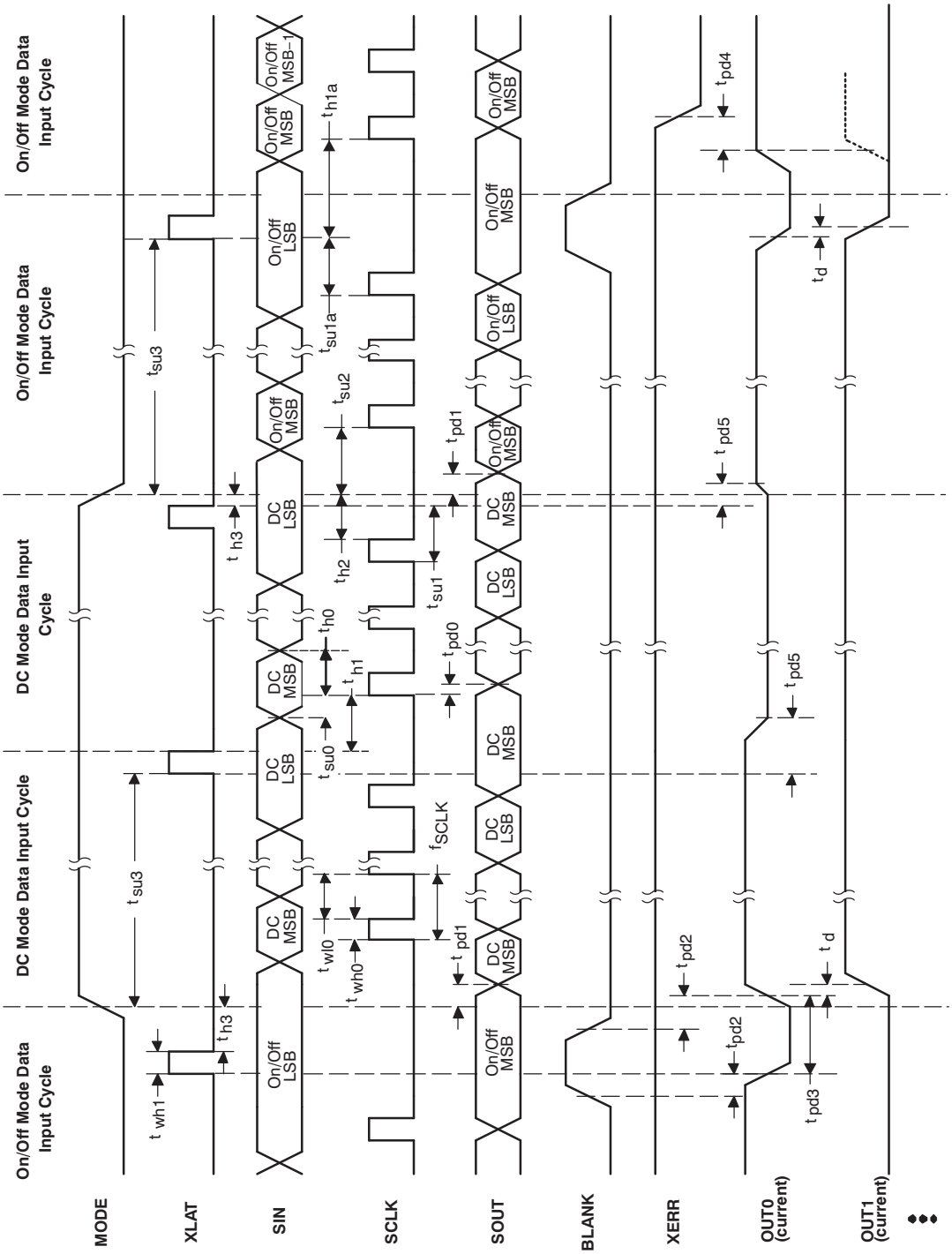


Figure 16. Timing Chart Example for ON/OFF Setting to Dot-Correction

TYPICAL CHARACTERISTICS

REFERENCE RESISTOR
vs
OUTPUT CURRENT

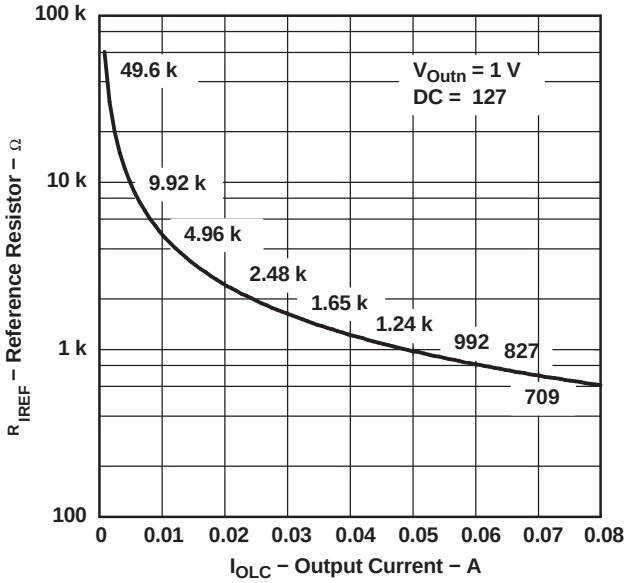


Figure 17.

OUTPUT CURRENT
vs
REQUIRED OUTPUTn VOLTAGE

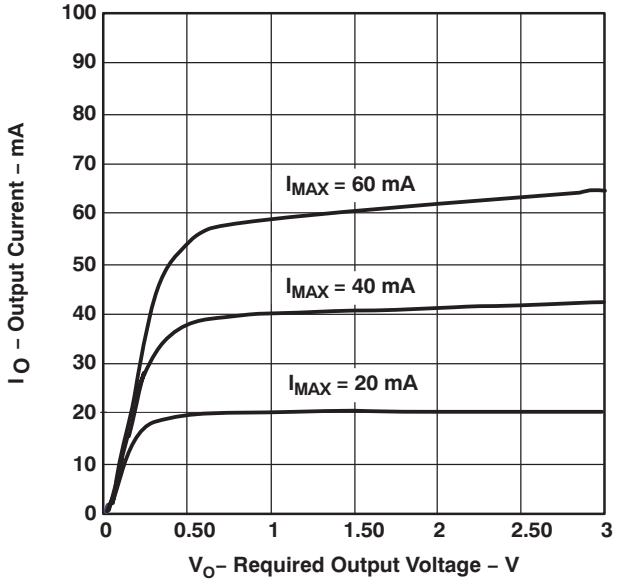


Figure 18.

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

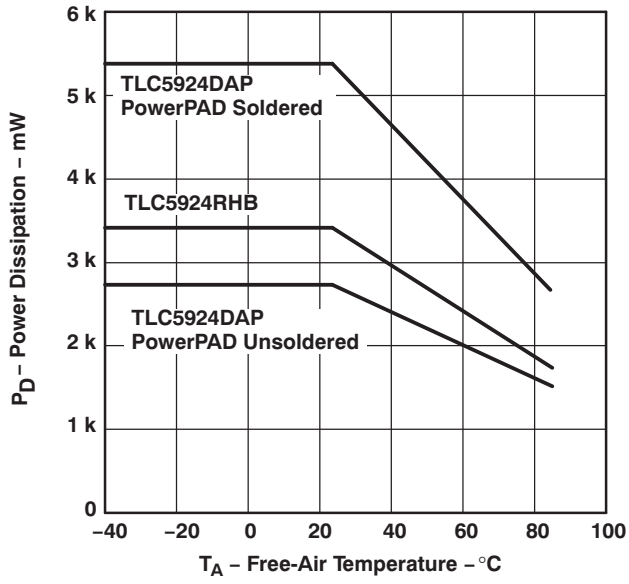
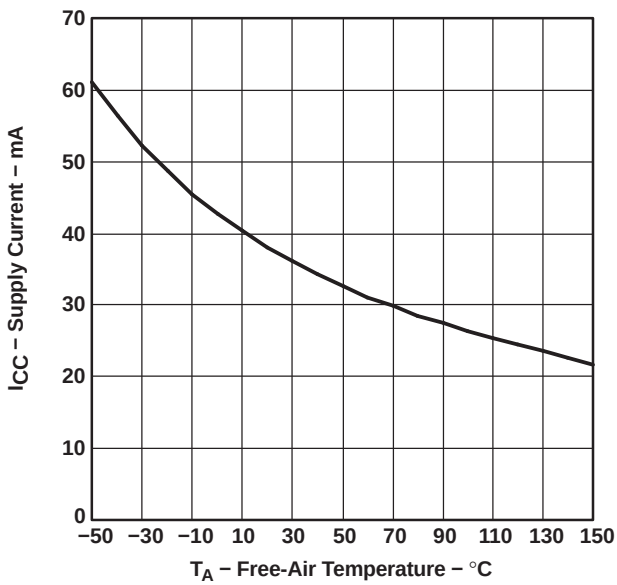


Figure 19.

SUPPLY CURRENT(A)
vs
FREE-AIR TEMPERATURE



A. Data Transfer = 30 MHz / All Outputs, ON/V_O = 1 V / R_{IREF} = 600 Ω / AV_{DD} = 5 V

Figure 20.

Power Rating – Free-Air Temperature

Figure 19 shows total power dissipation. Figure 20 shows supply current versus free-air temperature.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5924DAP	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924DAP.A	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924DAP.B	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924DAPR	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924DAPR.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924DAPR.B	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5924
TLC5924RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5924
TLC5924RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5924

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

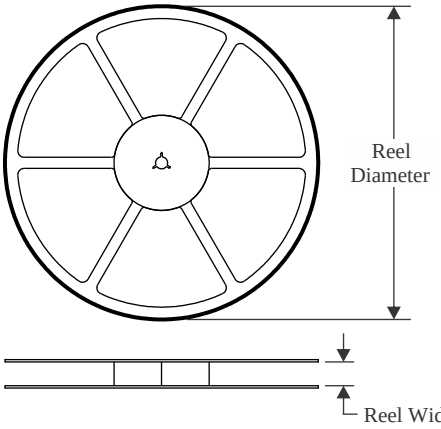
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

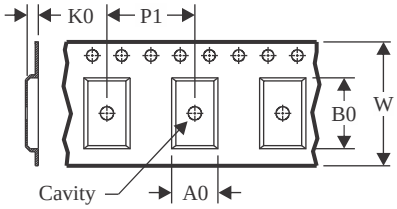
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

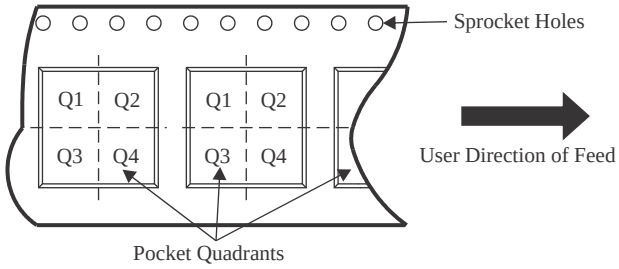


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

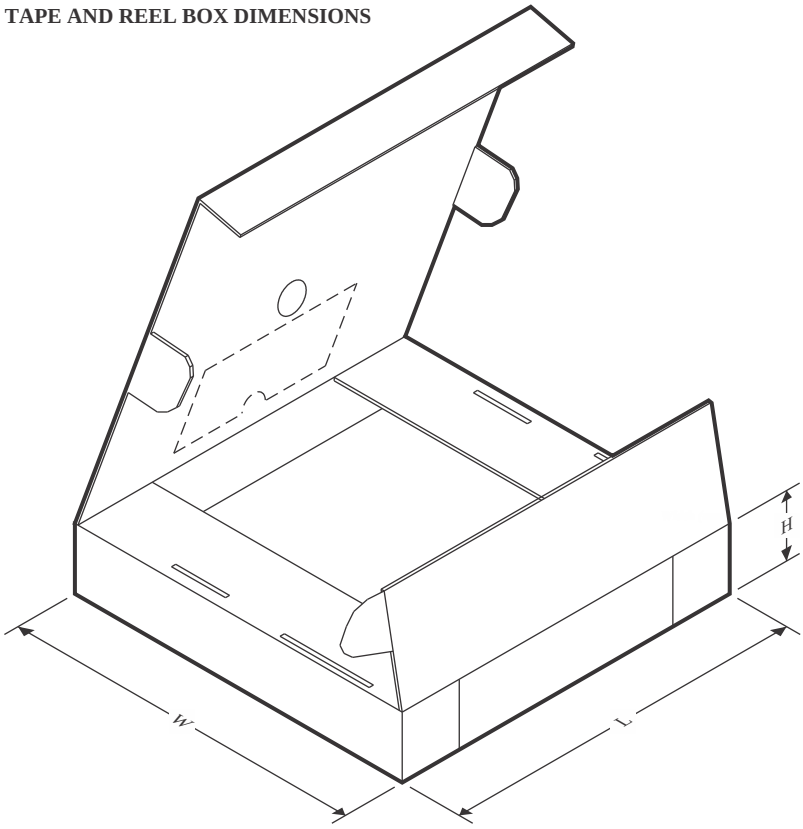
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5924DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TLC5924RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

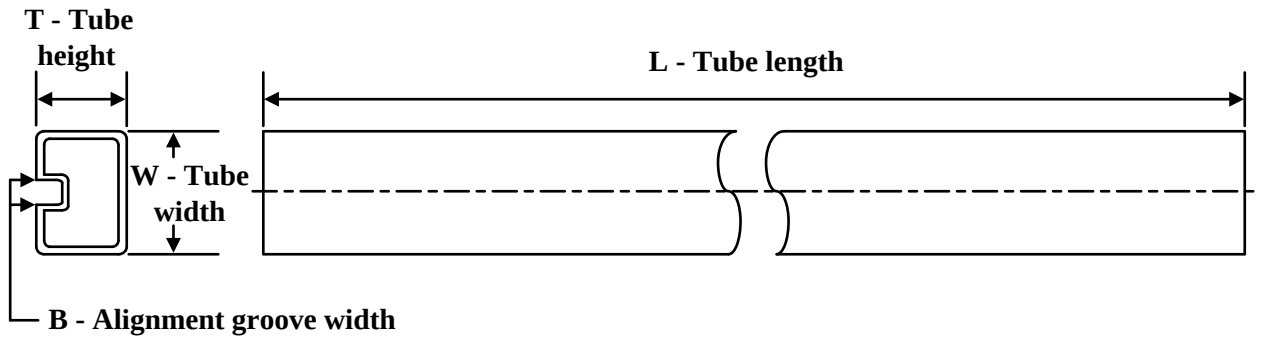
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5924DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TLC5924RHBR	VQFN	RHB	32	3000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5924DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5924DAP.A	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5924DAP.B	DAP	HTSSOP	32	46	530	11.89	3600	4.9

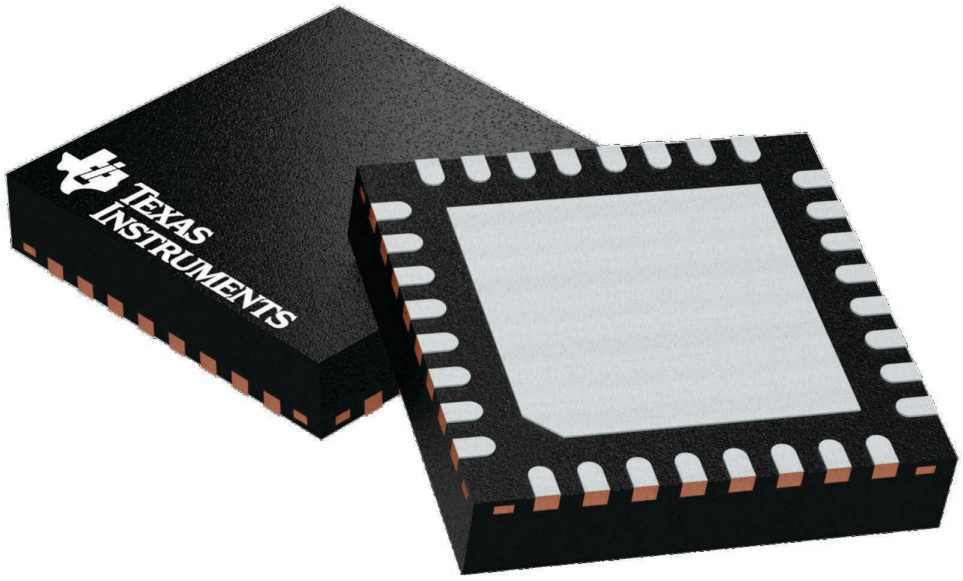
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

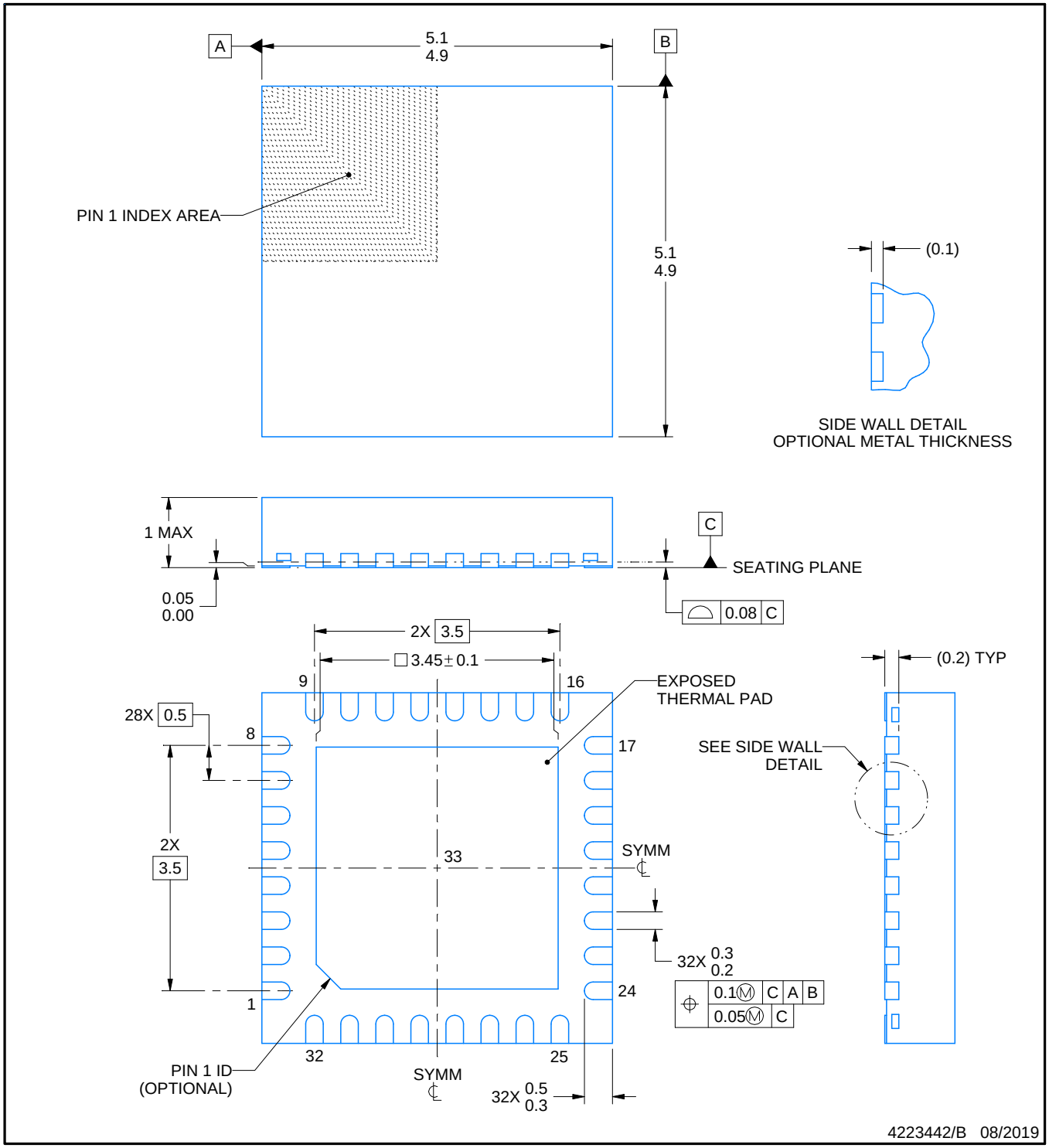
4224745/A

RHB0032E

PACKAGE OUTLINE

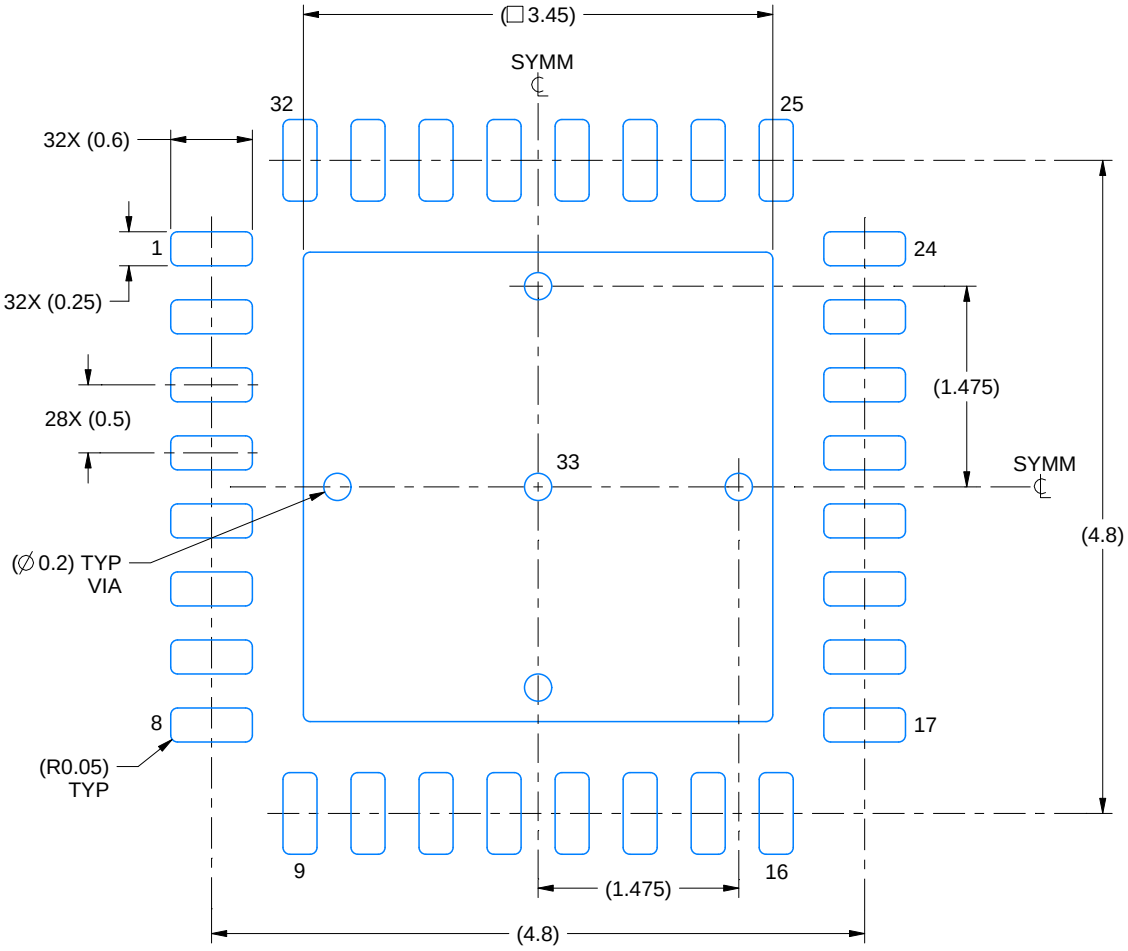
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

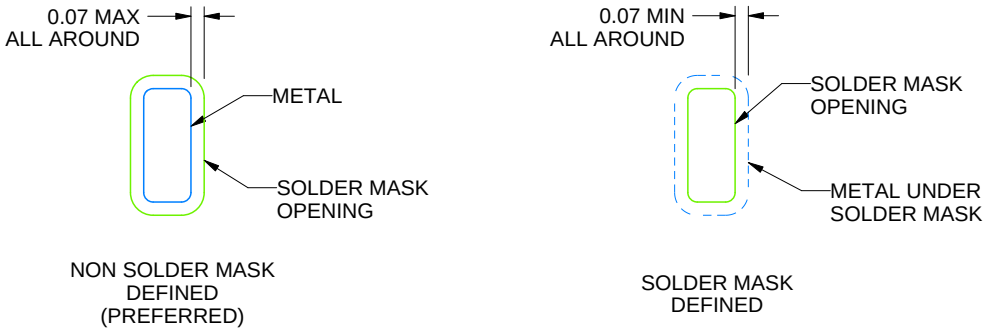


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

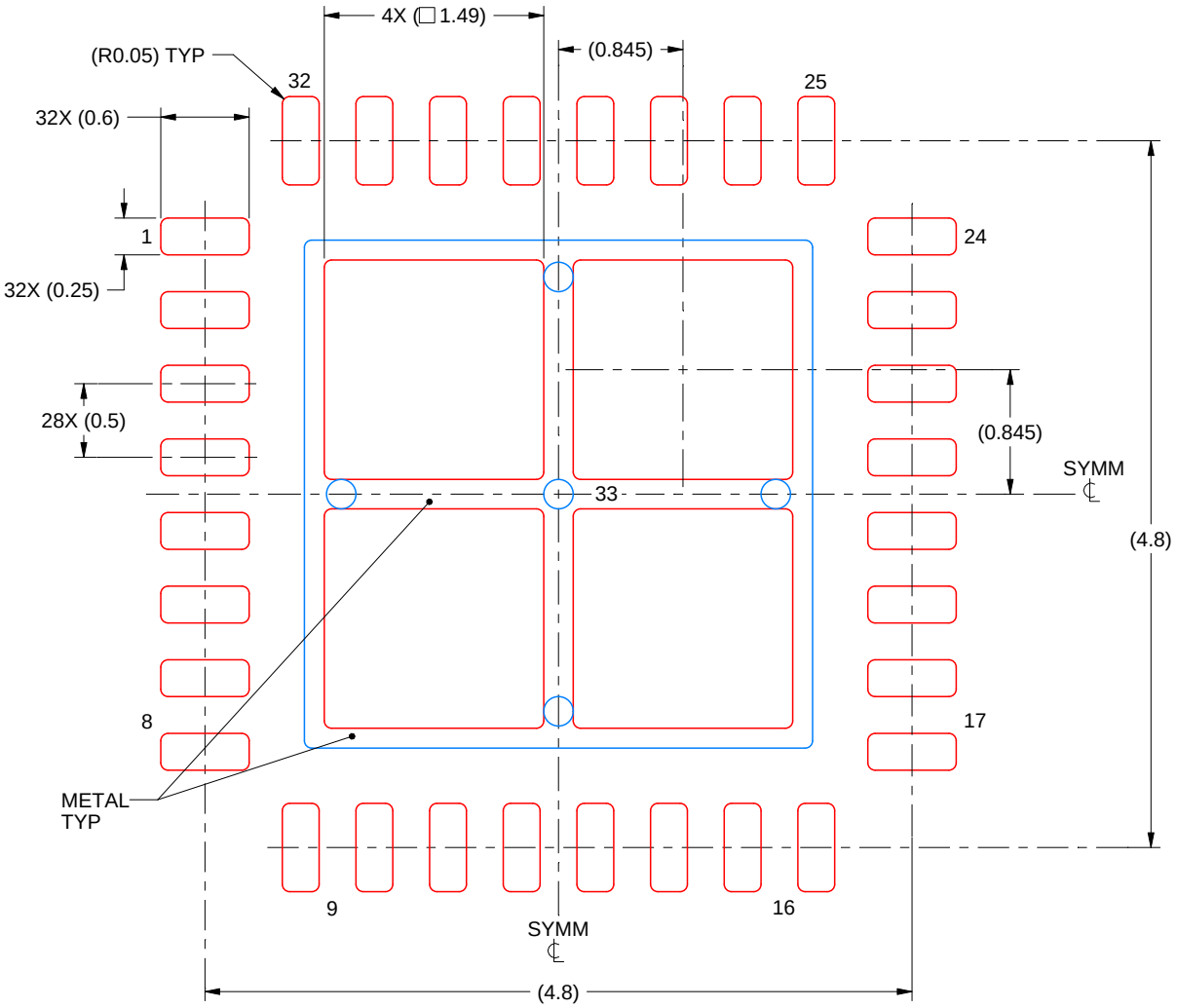


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

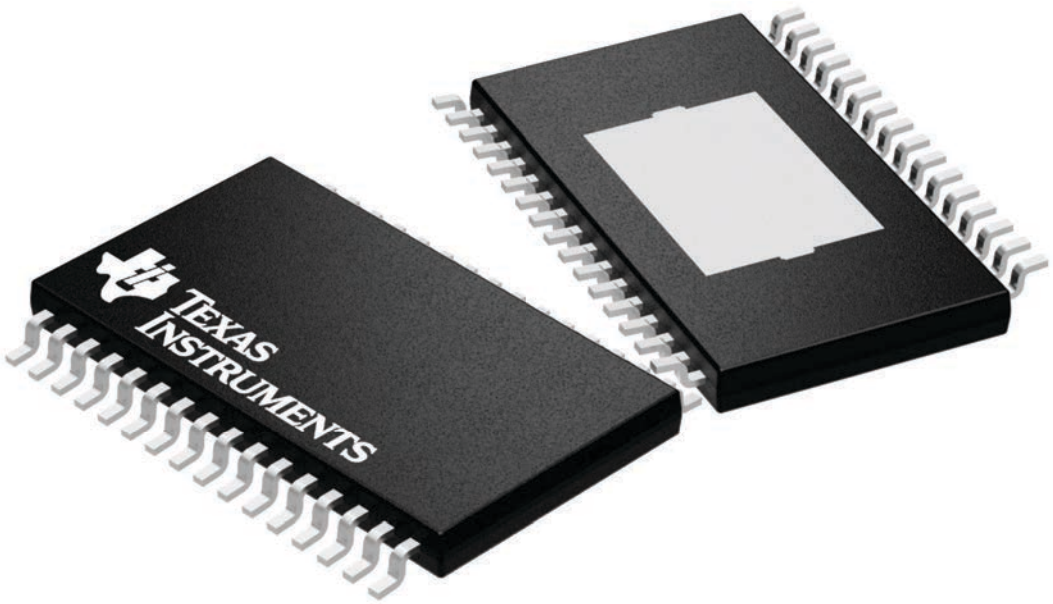
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

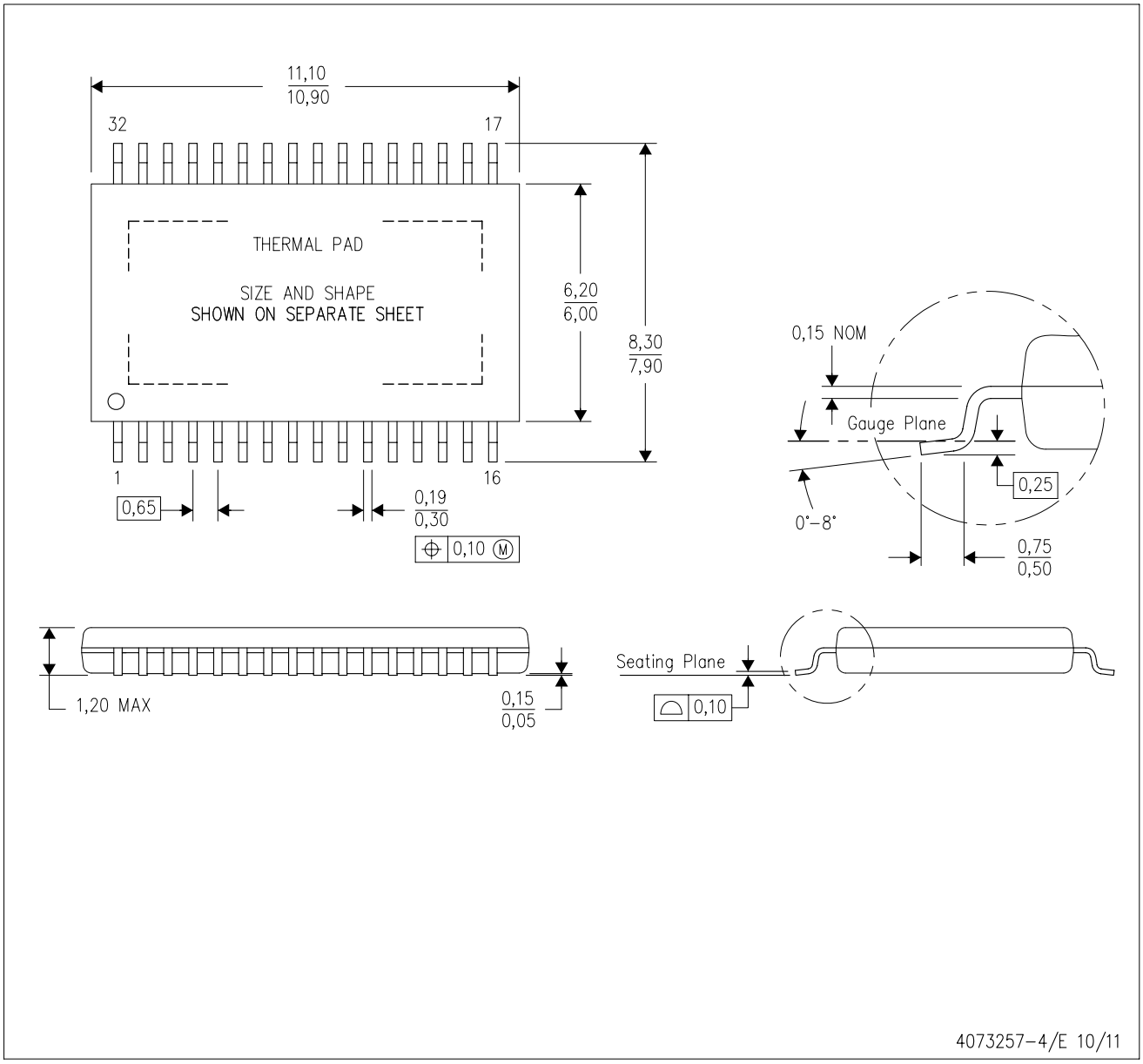
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

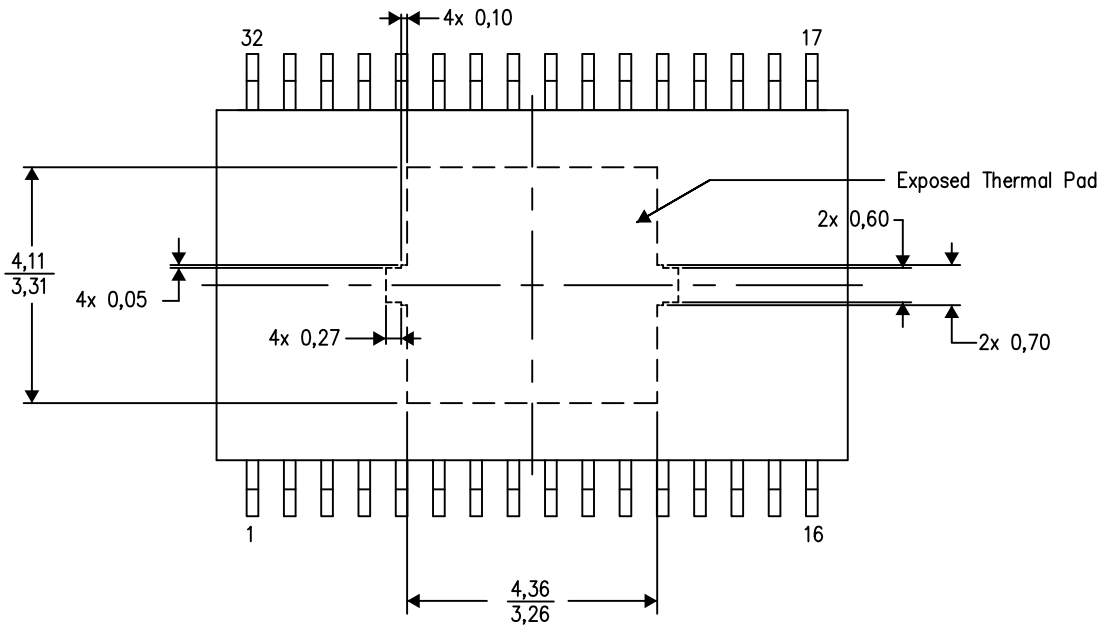
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

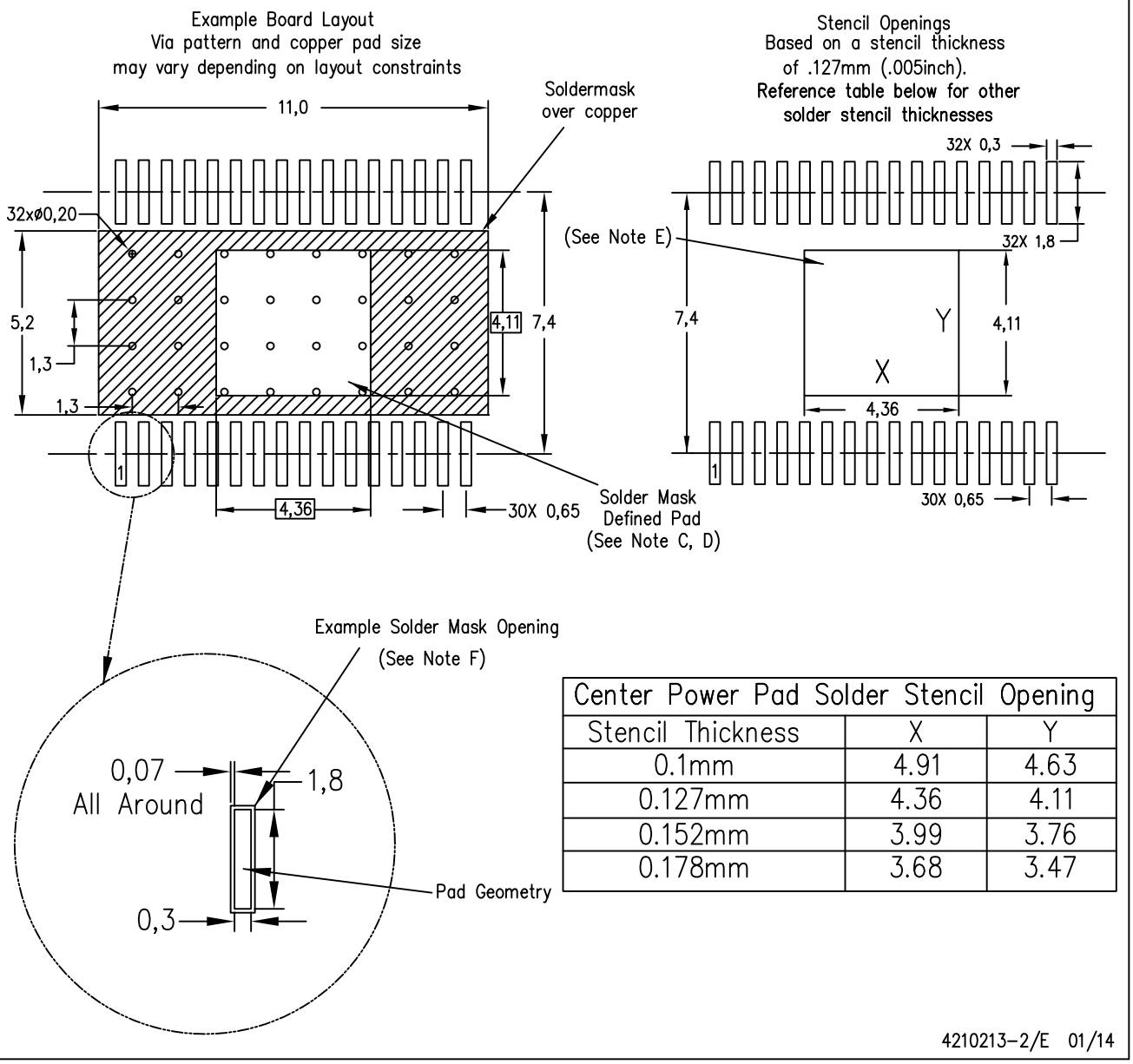
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

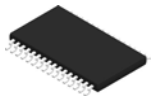
PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

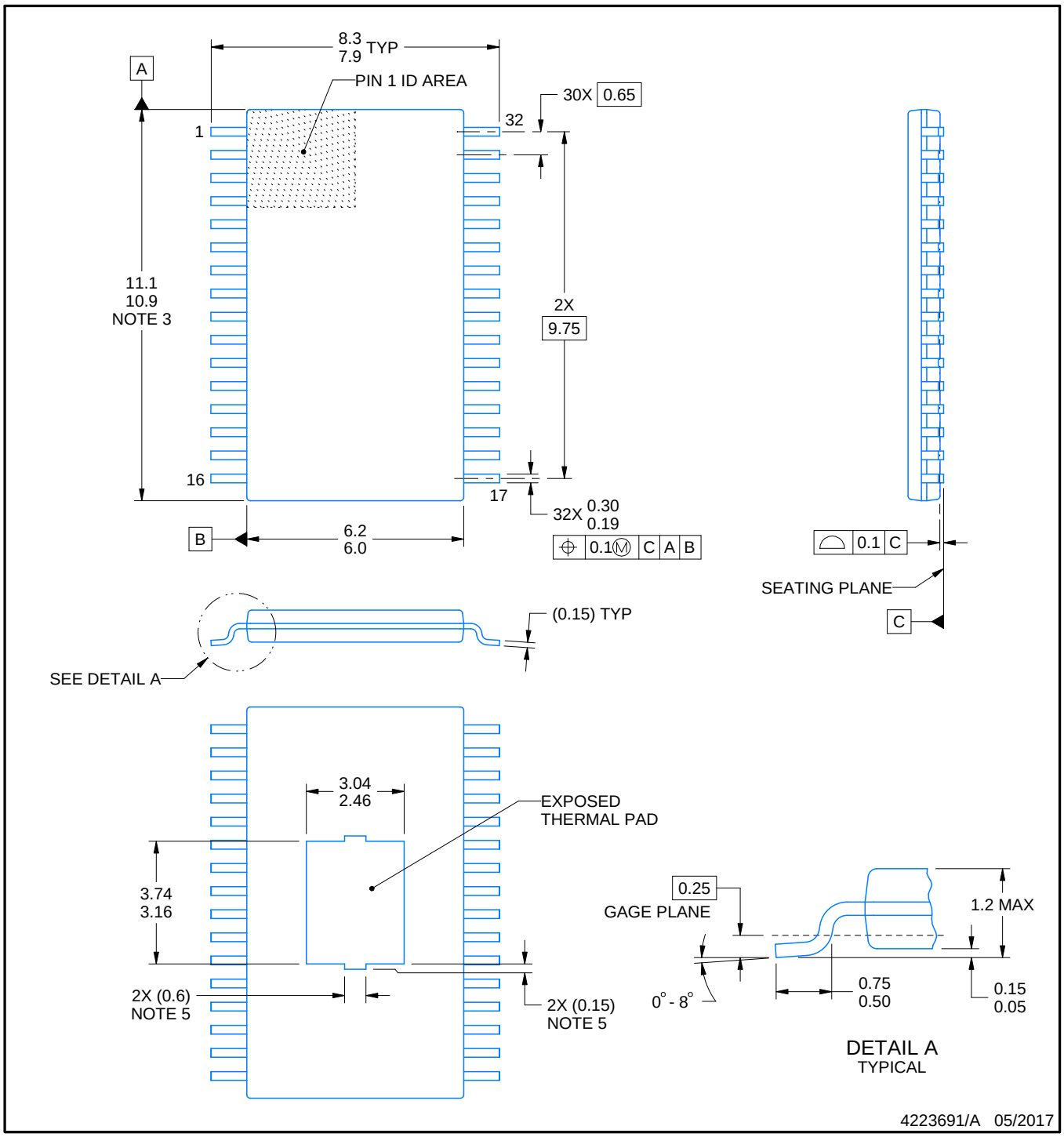


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

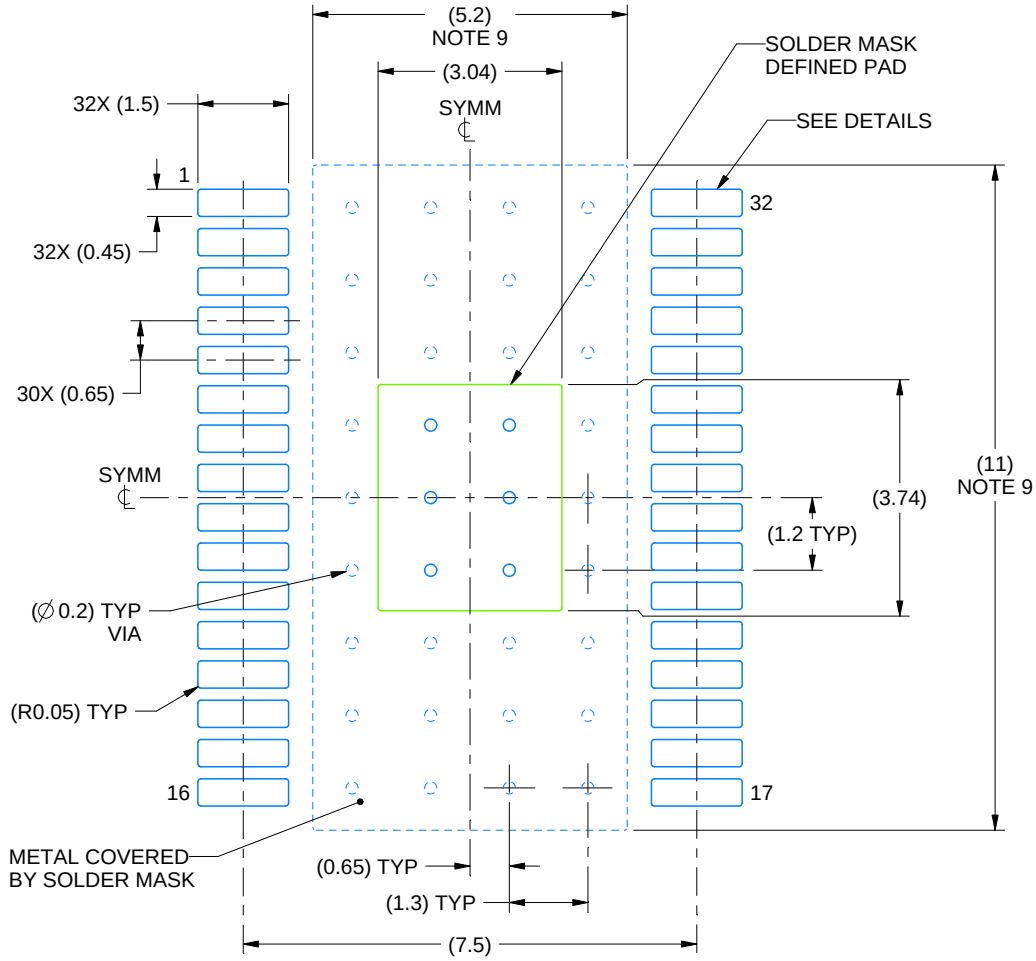
PLASTIC SMALL OUTLINE



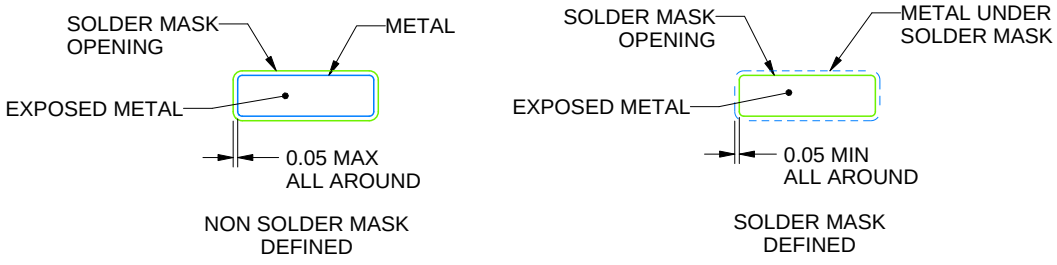
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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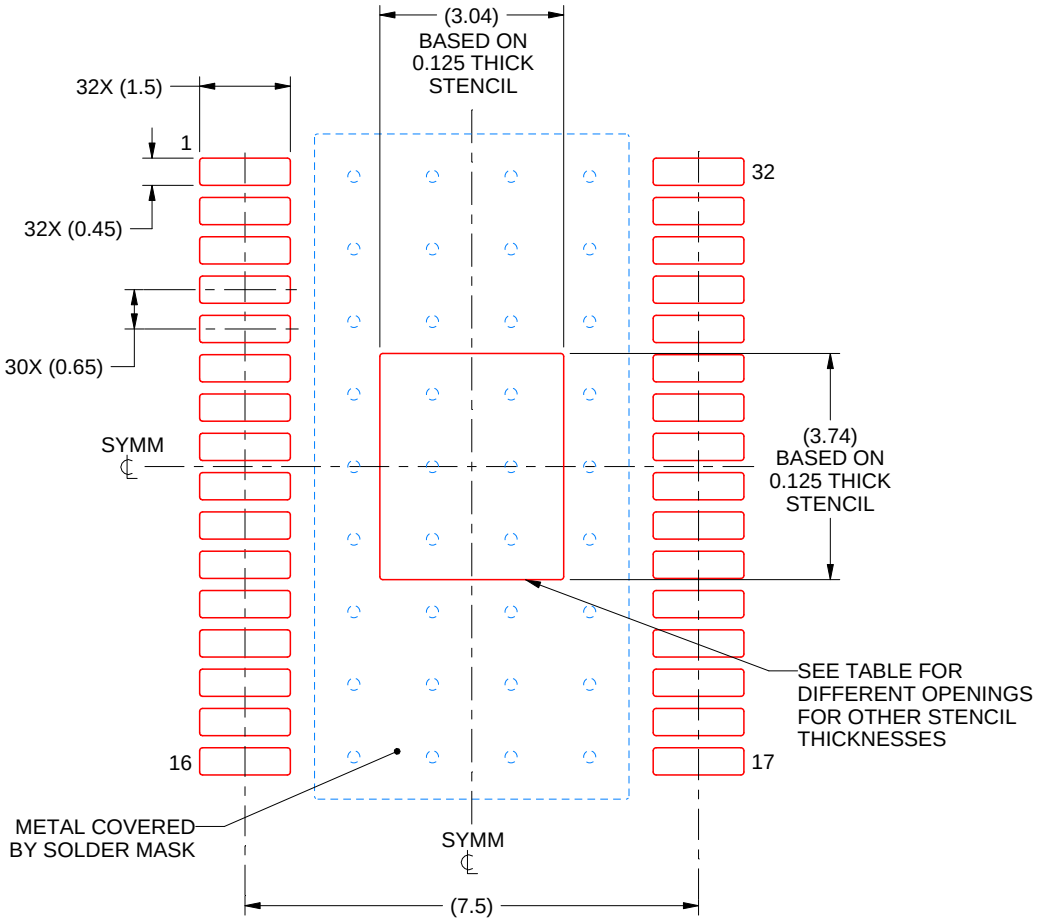
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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