TLC59108F 8-Bit FM+ I²C Bus LED Driver

1 Features

- Eight LED Drivers (Each Output Programmable at OFF, ON, Programmable LED Brightness, Programmable Group Dimming and Blinking Mixed With Individual LED Brightness)
- Eight Open-Drain Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming [Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)]
- 256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle From 0% to 99.6%
- Four Software Programmable I²C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to be Simultaneously Addressed Any Combination (For Example, One Register Used for *All Call* so That All the TLC59108Fs on the I²C Bus Can be Simultaneously Addressed and the Second Register Used for Three Different Addresses so That One Third of All Devices on the Bus Can be Simultaneously Addressed)
- Software Enable and Disable for I²C Bus Address
- Software Reset Feature (SWRST Call) Allows the Device to be Reset Through the I²C Bus
- Up to 14 Hardware Selectable I²C Bus Addresses so That Each Device Can be Programmed Individually
- Output State Change Programmable on the Acknowledge or the STOP Command to Update Outputs Byte-by-Byte or All at the Same Time (Default to Change on STOP)
- Maximum Output Current: 120 mA
- Maximum Output Voltage: 17 V
- 25-MHz Internal Oscillator Requires No External Components
- 1-MHz Fast-Mode Plus (FM+) Compatible I²C Bus Interface With 30 mA High Drive Capability on SDA Output for Driving High Capacitive Buses
- Internal Power-On Reset
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power Up
- Active-Low Reset ($\overline{\text{RESET}}$)
- Supports Hot Insertion

2 Applications

- Gaming
- Small Signage
- Industrial Equipment

3 Description

The TLC59108F device is an I²C bus controlled 8-bit LED driver optimized for red, green, blue, or amber (RGBA) color-mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

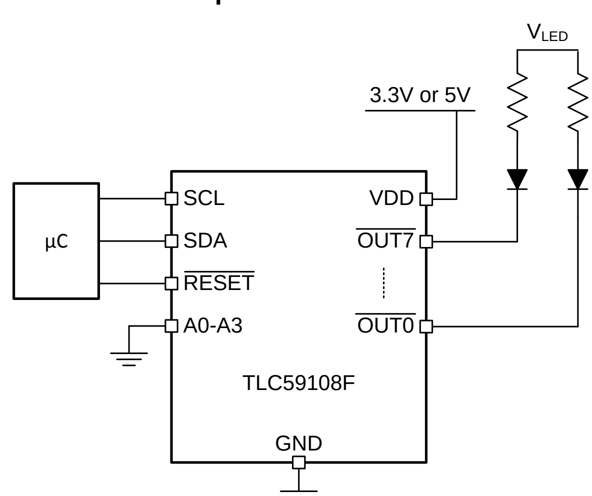
Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The TLC59108F operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17-V tolerant. LEDs can be directly connected to the TLC59108F device outputs.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59108F	VQFN (20)	4.50 mm × 3.50 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

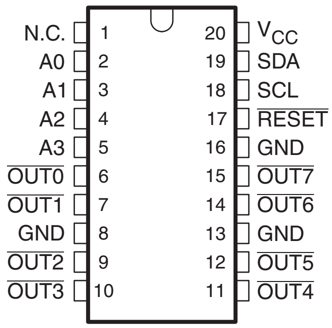
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2011) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Original (November 2011) to Revision A	Page
• Fixed address typo in the Software Reset Section	10
• Changed SLEEP Symbol to OSC and removed the "Low power mode" description to clairify functionality.	19
• Added TLC59108 and TLC59108F Differences section.	23

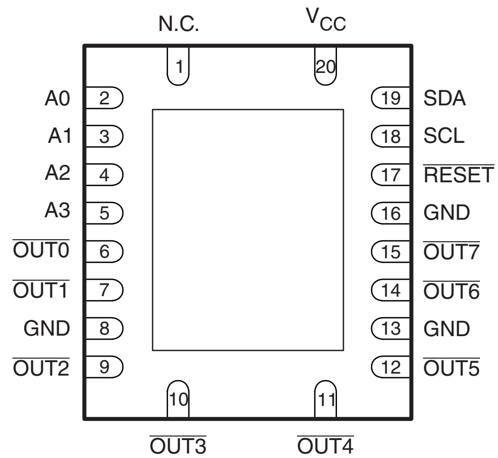
5 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



N.C. – No internal connection

RGY Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NAME	NO.		
A0	2	I	Address input 0
A1	3	I	Address input 1
A2	4	I	Address input 2
A3	5	I	Address input 3
GND	8	–	Ground
	13		
	16		
N.C.	1	I	No internal connection
$\overline{\text{OUT0}}$	6	O	Open-drain output 0 to 7, LED ON at low
$\overline{\text{OUT1}}$	7		
$\overline{\text{OUT2}}$	9		
$\overline{\text{OUT3}}$	10		
$\overline{\text{OUT4}}$	11		
$\overline{\text{OUT5}}$	12		
$\overline{\text{OUT6}}$	14		
$\overline{\text{OUT7}}$	15		
$\overline{\text{RESET}}$	17	I	Active-low reset input
SCL	18	I	Serial clock input
SDA	19	I/O	Serial data input/output
V_{CC}	20	–	Power supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0	7	V
V_I	Input voltage		–0.4	7	V
V_O	Output voltage		–0.5	20	V
I_O	Continuous output current			120	mA
P_D	Power dissipation, T_A = 25 °C, JESD 51-7	PW package		1.2	W
		RGY package		2.2	
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See [(1)].

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{\text{RESET}}$, A0, A1, A2, A3		0.7 × V_{CC}	5.5	V
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{\text{RESET}}$, A0, A1, A2, A3		0	0.3 × V_{CC}	V
V_O	Output voltage	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$			17	V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V		20	mA
			V_{CC} = 4.5 V		30	
I_O	Output current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$		5	120	mA
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6.4 Thermal Information

THERMAL METRIC[(1)]		TLC59108F		UNIT
		PW (TSSOP)	RGY (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.9	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	14.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_I	Input/output leakage current	SCL, SDA, A0, A1, A2, A3, $\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND			±0.3	µA
	Output leakage current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_O = 17 V, T_J = 25°C			0.5	µA
V_{POR}	Power-on reset voltage				2.5		V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V, V_{OL} = 0.4 V	20			mA
			V_{CC} = 5 V, V_{OL} = 0.4 V	30			
V_{OL}	Low-level output voltage	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_{CC} = 3 V, I_{OL} = 120 mA		230	450	mV
			V_{CC} = 4.5 V, I_{OL} = 120 mA		200	400	
r_{ON}	ON-state resistance	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_{CC} = 3 V, I_{OL} = 120 mA		1.92	3.75	Ω
			V_{CC} = 4.5 V, I_{OL} = 120 mA		1.64	3.3	
T_{SD}	Overtemperature shutdown(2)			150	175	200	°C
T_{HYS}	Restart hysteresis				15		°C
C_i	Input capacitance	SCL, A0, A1, A2, A3, $\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND		5		pF
C_{io}	Input/output capacitance	SDA	$V_I = V_{CC}$ or GND		8		pF
I_{CC}	Supply current		V_{CC} = 3 V, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = OFF			6	mA
			V_{CC} = 4.5 V, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = OFF			9	

(1) All typical values are at T_A = 25°C.
(2) Specified by design, not production tested.

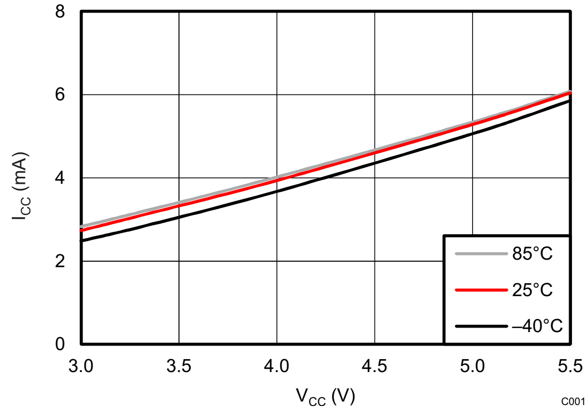
6.6 I²C Interface Timing Requirements

T_A = –40°C to 85°C

		STANDARD-MODE I²C BUS		FAST-MODE I²C BUS		FAST-MODE PLUS I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I²C Interface								
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	I²C bus free time between Stop and Start	4.7		1.3		0.5		μs
$t_{HD;STA}$	Hold time (repeated) for Start condition	4		0.6		0.26		μs
$t_{SU;STA}$	Set-up time (repeated) for Start condition	4.7		0.6		0.26		μs
$t_{SU;STO}$	Set-up time for Stop condition	4		0.6		0.26		μs
$t_{HD;DAT}$	Data hold time	0		0		0		ns
$t_{VD;ACK}$	Data valid acknowledge time[(1)]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{VD;DAT}$	Data valid time[(2)]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{SU;DAT}$	Data set-up time	250		100		50		ns
t_{LOW}	Low period of the SCL clock	4.7		1.3		0.5		μs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		μs
t_f	Fall time of both SDA and SCL signals[(3)] [(4)]		300	20 + $0.1C_b$[(5)]	300		120	ns
t_r	Rise time of both SDA and SCL signals		1000	20 + $0.1C_b$[(5)]	300		120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter[(6)]		50		50		50	ns
Reset								
t_W	Reset pulse width	10		10		10		ns
t_{REC}	Reset recovery time	0		0		0		ns
t_{RESET}	Time to reset[(7)(8)]	400		400		400		ns

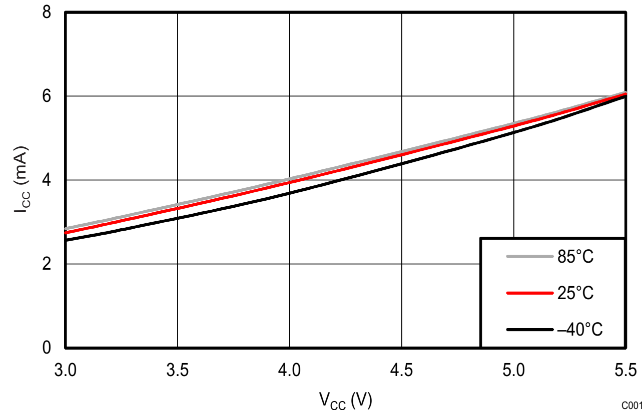
(1) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
(2) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCLs falling edge.
(4) The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(5) C_b = total capacitance of one bus line in pF.
(6) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns
(7) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.
(8) Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

6.7 Typical Characteristics



all LEDs on
Duty Cycle = 100%

Figure 1. I_{CC} vs V_{CC}



all LEDs off

Figure 2. I_{CC} vs V_{CC}

7 Parameter Measurement Information

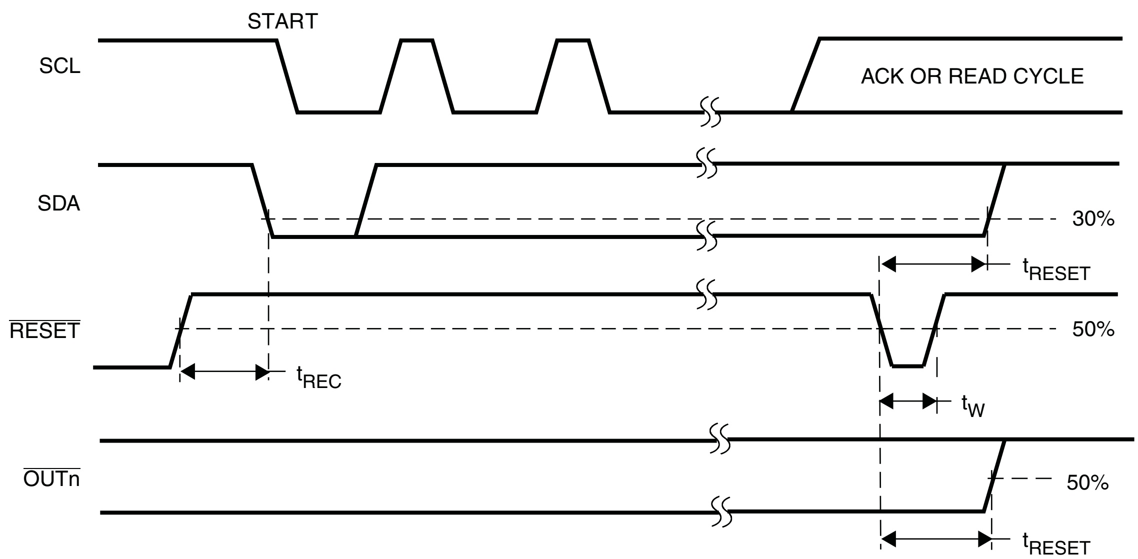


Figure 3. Definition of Reset Timing

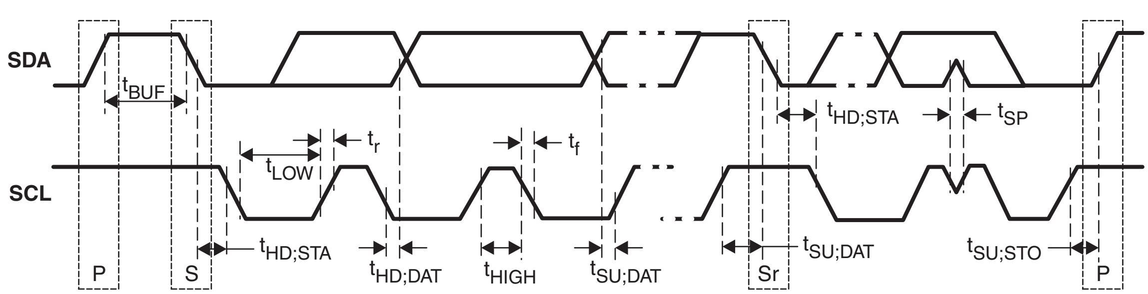
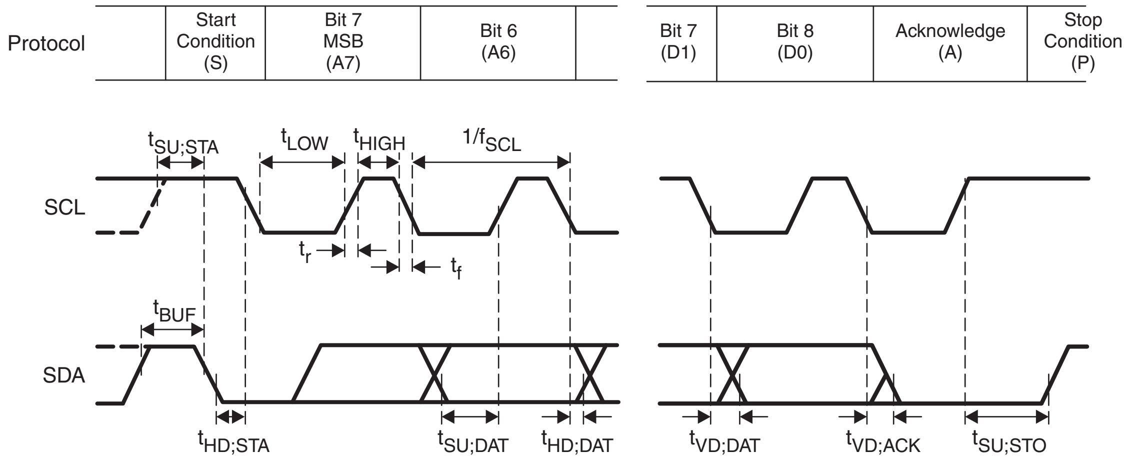


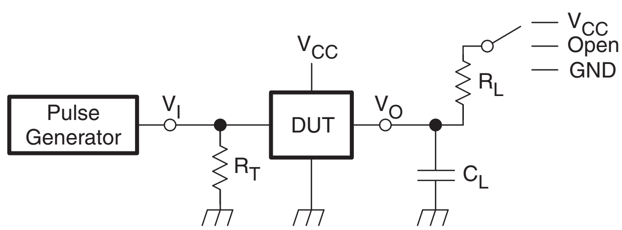
Figure 4. Definition of Timing

Parameter Measurement Information (continued)



Rise and fall times refer to V_{IL} and V_{IH}.

Figure 5. I²C Bus Timing



R_L = Load resistance for SDA and SCL; should be >1 kΩ at 3-mA or lower current.
C_L = Load capacitance; includes jig and probe capacitance.
R_T = Termination resistance; should be equal to the output impedance (Z_O) of the pulse generator.

Figure 6. Test Circuit for Switching Characteristics

8 Detailed Description

8.1 Overview

The TLC59108F is an I^{2}C bus controlled 8-bit LED driver optimized for red, green, blue, or amber (RGBA) color-mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

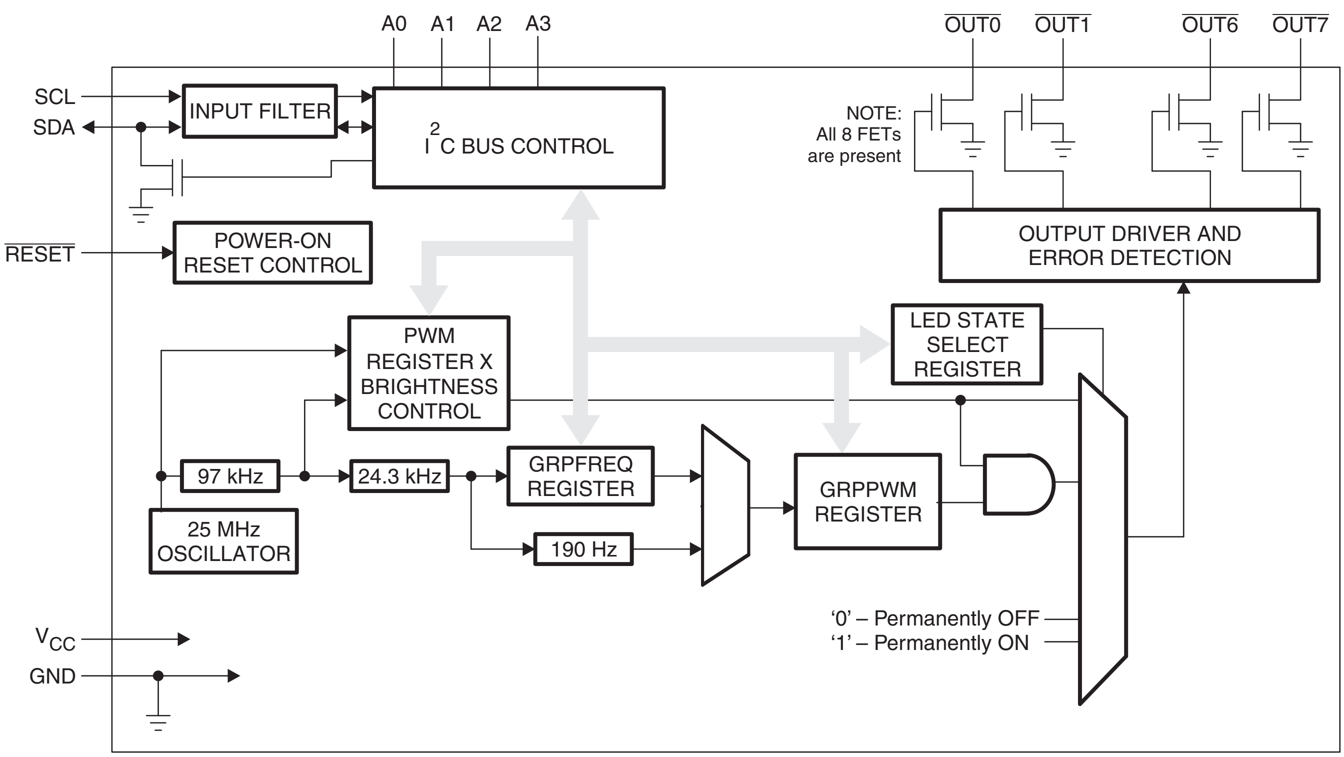
Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The TLC59108F operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17-V tolerant. LEDs can be directly connected to the TLC59108F device outputs.

Software programmable LED group and three sub call I^{2}C bus addresses allow all or defined groups of TLC59108F devices to respond to a common I^{2}C bus address, allowing for example, all the same color LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^{2}C bus commands.

Four hardware address pins allow up to 14 devices on the same bus.

The software reset (SWRST) call allows the master to perform a reset of the TLC59108F through the I^{2}C bus, identical to the power-on reset (POR) that initializes the registers to their default state causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

8.2 Functional Block Diagram



Only one PWM shown for clarity.

8.3 Feature Description

8.3.1 Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the TLC59108F in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released and the TLC59108F registers and I^2C bus state machine are initialized to their default states causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

8.3.2 External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TLC59108F registers and I^2C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high.

This input requires a pullup resistor to V_{CC} if no active connection is used.

8.3.3 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I^2C bus to be reset to the power-up state value through a specific I^2C bus command. To be performed correctly, the I^2C bus must be functional and there must be no device hanging the bus.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I^2C bus master.
2. The reserved SWRST I^2C bus address 1001 011 with the R/$\overline{\text{W}}$ bit set to 0 (write) is sent by the I^2C bus master.
3. The TLC59108F device(s) acknowledge(s) after seeing the SWRST Call address 1001 0110 (96h) only. If the R/$\overline{\text{W}}$ bit is set to 1 (read), no acknowledge is returned to the I^2C bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
   (a) Byte1 = A5h: the TLC59108F acknowledges this value only. If byte 1 is not equal to A5h, the TLC59108F does not acknowledge it.
   (b) Byte 2 = 5Ah: the TLC59108F acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59108F does not acknowledge it.

   If more than two bytes of data are sent, the TLC59108F does not acknowledge any more.
5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59108F then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I^2C bus master may interpret a non-acknowledge from the TLC59108F (at any time) as a SWRST Call Abort. The TLC59108F does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

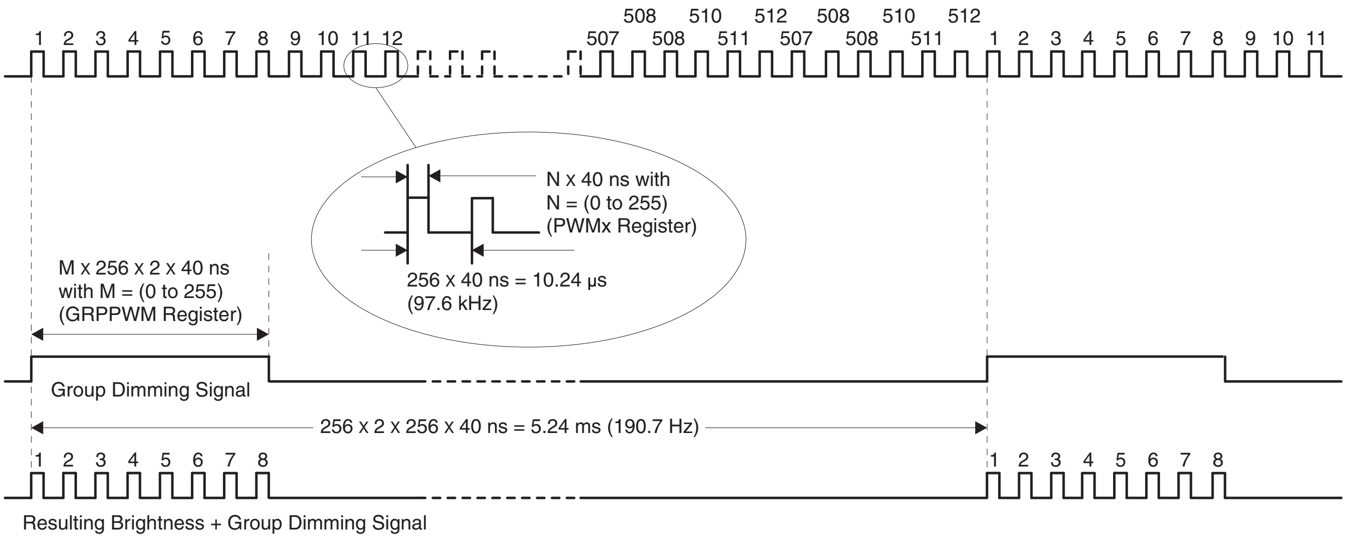
8.3.4 Individual Brightness Control With Group Dimming or Blinking

A 97-kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190-Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) is used to provide a global blinking control.

Feature Description (continued)



A. Minimum pulse width for LEDn brightness control is 40 ns.
B. Minimum pulse width for group dimming is 20.48 µs.
C. When M = 1 (GRPPWM register value), the resulting LEDn brightness control and group dimming signal will have two pulses of the LED brightness control signal (pulse width = N × 40 ns,w ith N defined in the PWMx register).
D. The resulting brightness plus group dimming signal shown above demonstrate a resulting control signal with M = 4 (8 pulses).

Figure 7. Brightness + Group Dimming Signals

8.4 Device Functional Modes

Active - Active mode occurs when one or more of the output channels is enabled.

Standby - Standby mode occurs when all output channels are disabled. Standby mode may be entered either through I^{2}C command or by pulling the $\overline{\text{RESET}}$ pin low.

8.5 Programming

8.5.1 Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

8.5.2 Regular I^{2}C Bus Slave Address

The I^{2}C bus slave address of the TLC59108F is shown in Figure 8. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low. For buffer management purpose, a set of sector information data should be stored.

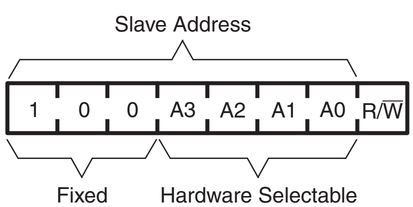


Figure 8. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

Programming (continued)

8.5.3 LED All Call I²C Bus Address

- Default power-up value (ALLCALLADR address register): 90h or 1001 000
- Programmable through I²C bus (volatile programming)
- At power-up, LED All Call I²C bus address is enabled. TLC59108F sends an ACK when 90h ($R/\overline{W}$ = 0) or 91h ($R/\overline{W}$ = 1) is sent by the master.

NOTE

The LED All Call I²C bus address (90h or 1001 000) must not be used as a regular I²C bus slave address since this address is enabled at power-up. All the TLC59108Fs on the I²C bus will acknowledge the address if sent by the I²C bus master.

8.5.4 LED Sub Call I²C Bus Address

- Three different I²C bus address can be used
- Default power-up values:
  - SUBADR1 register: 92h or 1001 001
  - SUBADR2 register: 94h or 1001 010
  - SUBADR3 register: 98h or 1001 100
- Programmable through I²C bus (volatile programming)
- At power-up, Sub Call I²C bus address is disabled. TLC59108F does not send an ACK when 92h ($R/\overline{W}$ = 0) or 93h ($R/\overline{W}$ = 1) or 94h ($R/\overline{W}$ = 0) or 95h ($R/\overline{W}$ = 1) or 98h ($R/\overline{W}$ = 0) or 99h ($R/\overline{W}$ = 1) is sent by the master.

NOTE

The default LED Sub Call I²C bus address may be used as a regular I²C bus slave address as long as they are disabled.

8.5.5 Software Reset I²C Bus Address

The address shown in Figure 9 is used when a reset of the TLC59108F needs to be performed by the master. The software reset address (SWRST Call) must be used with $R/\overline{W}$ = 0. If $R/\overline{W}$ = 1, the TLC59108F does not acknowledge the SWRST. See *Software Reset* for more detail.

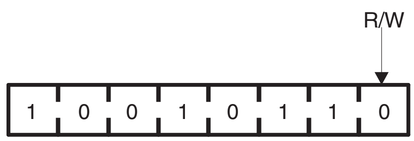


Figure 9. Software Reset Address

NOTE

The Software Reset I²C bus address is a reserved address and cannot be use as a regular I²C bus slave address.

8.5.6 Characteristics of the I²C Bus

The I²C bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Programming (continued)

8.5.6.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

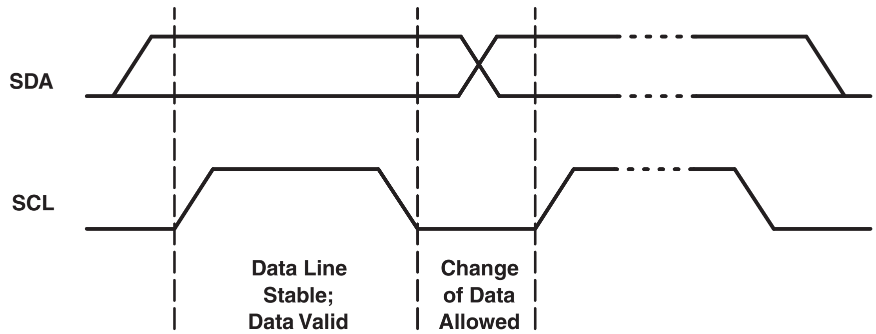


Figure 10. Bit Transfer

8.5.6.2 Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 11).

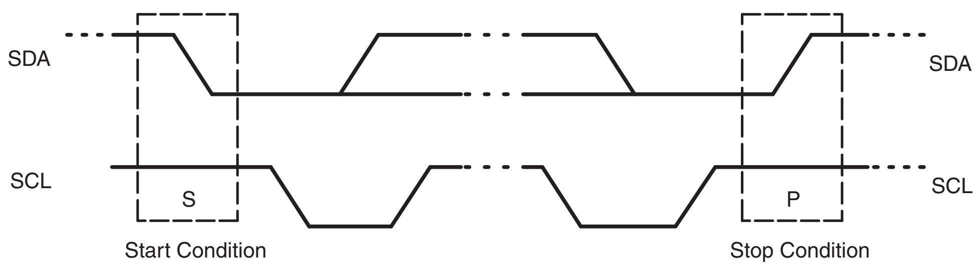


Figure 11. Start and Stop Conditions

8.5.7 System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 12).

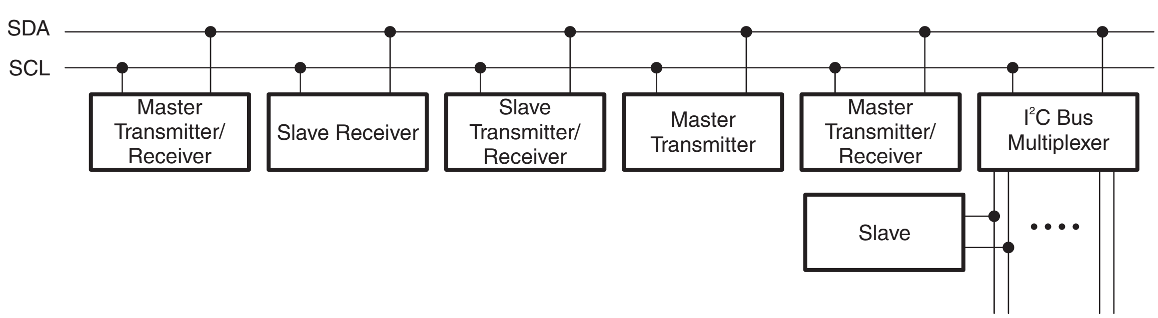


Figure 12. System Configuration

Programming (continued)

8.5.8 Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

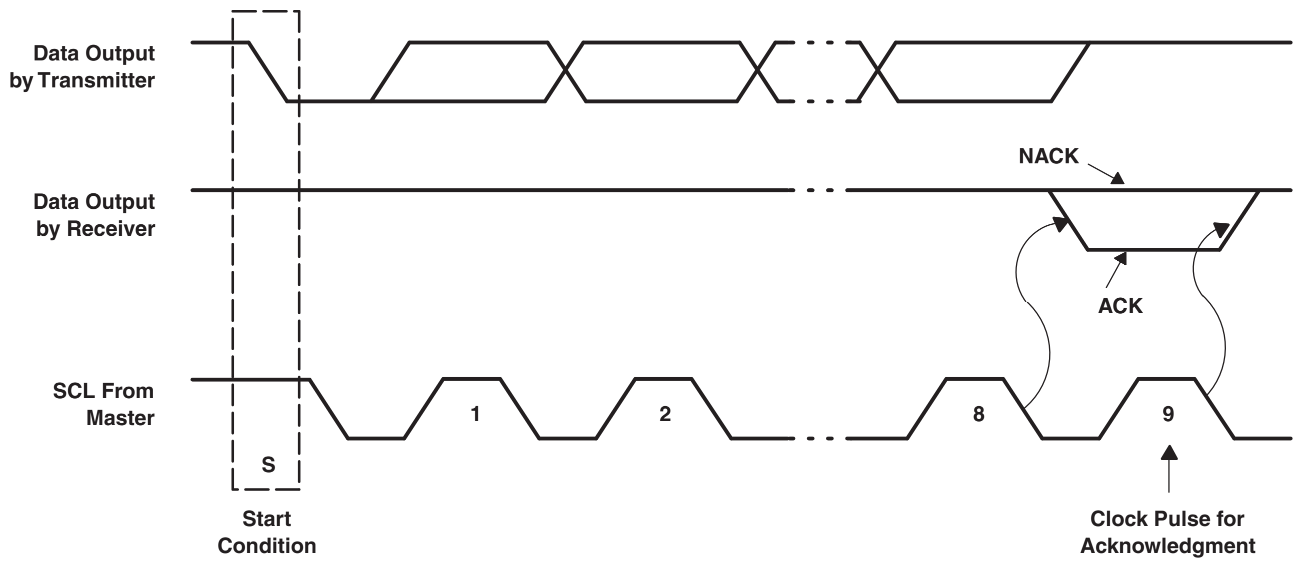


Figure 13. Acknowledge on I^{2}C Bus

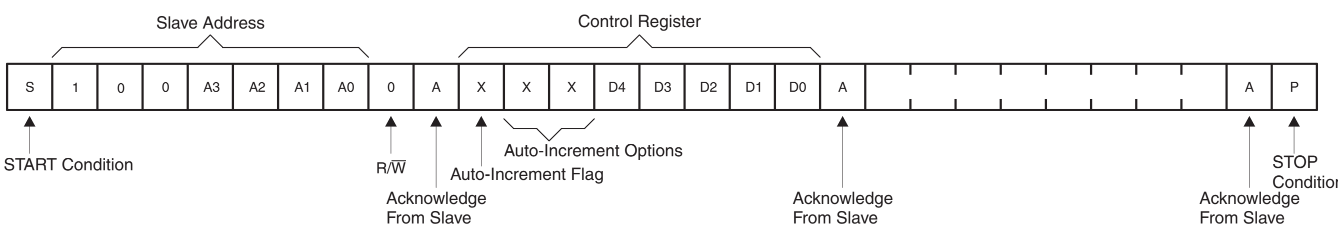


Figure 14. Write to a Specific Register

Programming (continued)

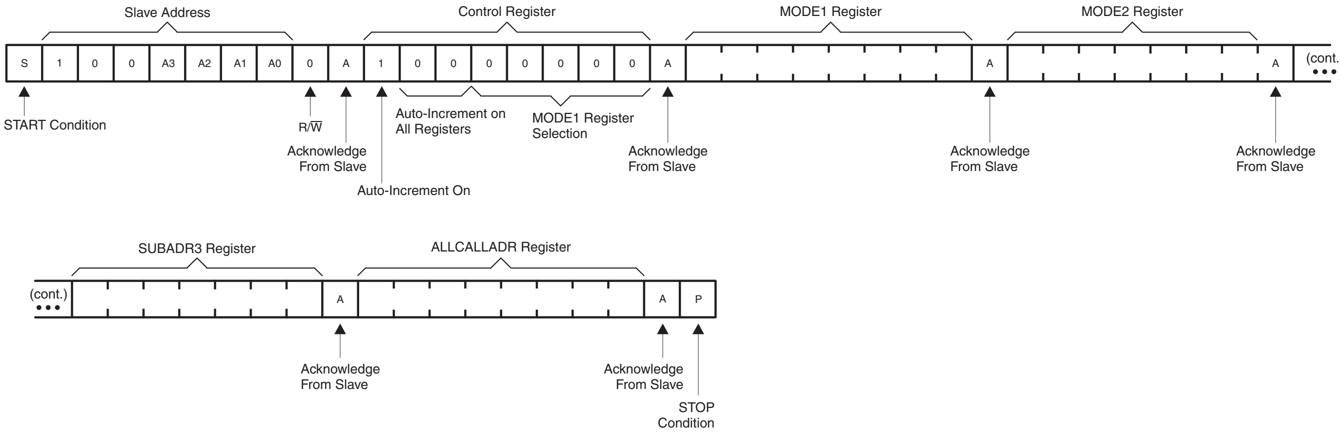


Figure 15. Write to All Registers Using Auto-Increment

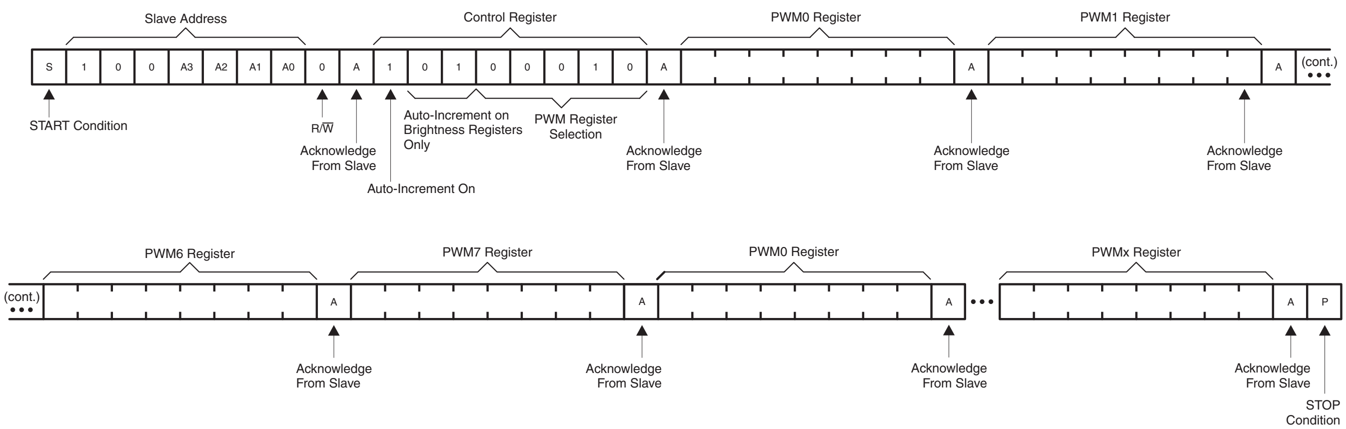


Figure 16. Multiple Writes to Individual Brightness Registers Only Using the Auto-Increment Feature

Programming (continued)

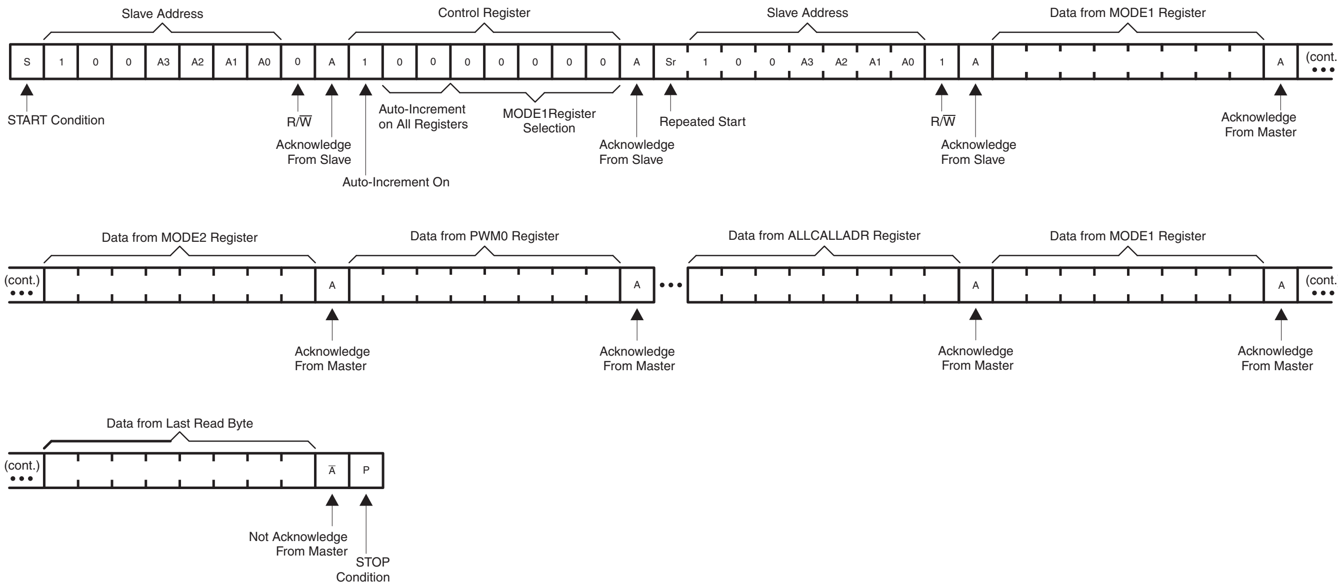
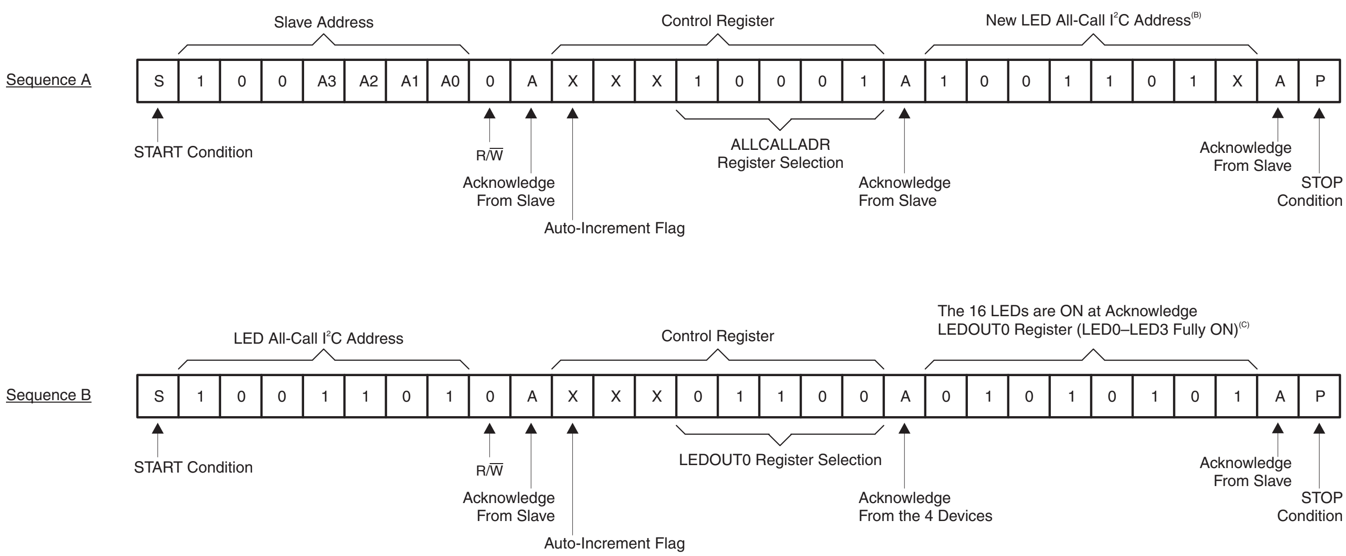


Figure 17. Read All Registers With the Auto-Increment Feature



A. In this example, four TLC59108Fs are used with the same sequence sent to each.

B. ALLCALL bit in MODE1 register is equal to 1 for this example.

C. OCH bit in MODE2 register is equal to 1 for this example.

Figure 18. LED All-Call I²C Bus Address Programming and LED All-Call Sequence Example

8.6 Register Maps

Table 2 describes the registers in the TLC59108F.

Register Maps (continued)

8.6.1 Control Register

Following the successful acknowledgment of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the TLC59108F, which will be stored in the Control register. The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).

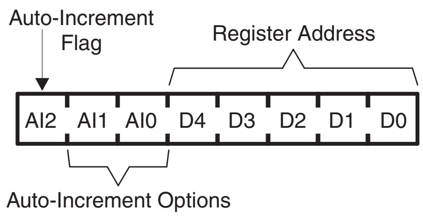


Figure 19. Control Register

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 1. Auto-Increment Options (1)

AI2	AI1	AI0	DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to 0 0000 after the last register (1 0001) is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to 0 0010 after the last register (0 1001) is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to 0 1010 after the last register (0 1011) is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to 0 0010 after the last register (0 1011) is accessed.

(1) Other combinations not shown in Table 1 (A1[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^{2}C bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^{2}C bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^{2}C bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I^{2}C bus communication, for example, changing color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 0001 (as defined in Table 2). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See Table 1 for rollover values. For example, if the Control register = 1110 1100 (ECh), then the register addressing sequence will be (in hex):

04 → … → 11 → 02 → ... → 11 → 02 → … as long as the master keeps sending or reading data.

Table 2. Register Descriptions

REGISTER NUMBER (HEX)	NAME	ACCESS (1)	DESCRIPTION
00	MODE1	R/W	Mode register 1
01	MODE2	R/W	Mode register 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	GRPPWM	R/W	Group duty cycle control
0B	GRPFREQ	R/W	Group frequency
0C	LEDOUT0	R/W	LED output state 0
0D	LEDOUT1	R/W	LED output state 1
0E	SUBADR1	R/W	I^2C bus sub-address 1
0F	SUBADR2	R/W	I^2C bus sub-address 2
10	SUBADR3	R/W	I^2C bus sub-address 3
11	ALLCALLADR	R/W	LED all call I^2C bus address

(1) R = read, W = write

8.6.2 Mode Register 1 (MODE1)

Table 3 describes Mode Register 1.

Table 3. MODE1 – Mode Register 1 (Address 00h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	AI2	R	0 (2)	Register auto-increment disabled
			1	Register auto-increment enabled
6	AI1	R	0 (2)	Auto-increment bit 1 = 0
			1	Auto-increment bit 1 = 1
5	AI0	R	0 (2)	Auto-increment bit 0 = 0
			1	Auto-increment bit 0 = 1
4	OSC	R/W	0	Normal mode (3)
			1 (2)	Oscillator off (4).
3	SUB1	R/W	0 (2)	Device does not respond to I^2C bus sub-address 1.
			1	Device responds to I^2C bus sub-address 1.
2	SUB2	R/W	0 (2)	Device does not respond to I^2C bus sub-address 2.
			1	Device responds to I^2C bus sub-address 2.
1	SUB3	R/W	0 (2)	Device does not respond to I^2C bus sub-address 3.
			1	Device responds to I^2C bus sub-address 3.
0	ALLCALL	R/W	0	Device does not respond to LED All Call I^2C bus address.
			1 (2)	Device responds to LED All Call I^2C bus address.

(1) R = read, W = write
(2) Default value
(3) It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set from logic 1 to 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 500 μs window.
(4) No LED control (on, off, blinking, or dimming) is possible when the oscillator is off. Write to a register cannot be accepted during SLEEP mode. When you change the LED condition, SLEEP bit must be set to logic 0.

8.6.3 Mode Register 2 (MODE2)

Table 4 describes Mode Register 2.

Table 4. MODE2 – Mode Register 2 (Address 01h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7:6		R	0 (2)	Reserved
5	DMBLNK	R/W	0 (2)	Group control = dimming
			1	Group control = blinking
4		R	0 (2)	Reserved
3	OCH	R/W	0 (2)	Outputs change on Stop command (3).
			1	Outputs change on ACK.
2:0		R	000 (2)	Reserved

(1) R = read, W = write
(2) Default value
(3) Change of the outputs at the STOP command allows synchronizing outputs of more than one TLC59108F. Applicable to registers from 02h (PWM0) to 0Dh (LEDOUT) only.

8.6.4 Individual Brightness Control Registers (PWM0–PWM7)

Table 5 describes the Individual Brightness Control Registers.

Table 5. PWM0–PWM7 – Individual Brightness Control Registers (Addresses 02h–09h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000 (2)	PWM0 individual duty cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000 (2)	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000 (2)	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000 (2)	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000 (2)	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000 (2)	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000 (2)	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000 (2)	PWM7 individual duty cycle

(1) R = read, W = write
(2) Default value

A 97-kHz fixed-frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 and LEDOUT1 registers).

$$\text{duty cycle} = \frac{\text{IDCx[7:0]}}{256}$$

8.6.5 Group Duty Cycle Control Register (GRPPWM)

Table 6 describes the Group Duty Cycle Control Register .

Table 6. GRPPWM – Group Duty Cycle Control Register (Address 0Ah) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Ah	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111 (2)	GRPPWM register

(1) R = read, W = write
(2) Default value

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190-Hz fixed frequency signal is superimposed with the 97-kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a *Don't care*.

General brightness for the 8 outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$\text{Duty cycle} = \frac{\text{GDC[7:0]}}{256} \quad (1)$$

8.6.6 Group Frequency Register (GRPFREQ)

Table 7 describes the Group Frequency Register.

Table 7. GRPFREQ – Group Frequency Register (Address 0Bh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Bh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000 (2)	GRPFREQ register

(1) R = read, W = write
(2) Default value

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a *Don't care* when DMBLNK = 0. Applicable to LED output programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$\text{globalblinkingperiod} = \frac{\text{GFRQ[7:0]} + 1}{24}(\text{s}) \quad (2)$$

8.6.7 LED Driver Output State Registers (LEDOUT0, LEDOUT1)

Table 8 describes the LED Driver Output State Registers.

Table 8. LEDOUT0 and LEDOUT1 – LED Driver Output State Registers (Address 0Ch and 0Dh) Bit Descriptions

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Ch	LEDOUT0	7:6	LDR3[1:0]	R/W	00 (2)	LED3 output state control
		5:4	LDR2[1:0]		00 (2)	LED2 output state control
		3:2	LDR1[1:0]		00 (2)	LED1 output state control
		1:0	LDR0[1:0]		00 (2)	LED0 output state control
0Dh	LEDOUT1	7:6	LDR7[1:0]	R/W	00 (2)	LED7 output state control
		5:4	LDR6[1:0]		00 (2)	LED6 output state control
		3:2	LDR4[1:0]		00 (2)	LED5 output state control
		1:0	LDR4[1:0]		00 (2)	LED4 output state control

(1) R = read, W = write
(2) Default value

LDRx = 00 : LED driver x is off (default power-up state).

LDRx = 01 : LED driver x is fully on (individual brightness and group dimming and blinking not controlled).

LDRx = 10 : LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11 : LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

8.6.8 I^2C Bus Sub-Address Registers 1 to 3 (SUBADR1–SUBADR3)

Table 9 describes the Output Gain Control Register.

Table 9. SUBADR1–SUBADR3 – I^2C Bus Sub-Address Registers 1 to 3 (Addresses 0Eh–10h) Bit Descriptions

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Eh	SUBADR1	7:5	A1[7:5]	R	100 (2)	Reserved
		4:1	A1[4:1]	R/W	1001 (2)	I^2C bus sub-address 1
		0	A1[0]	R	0 (2)	Reserved
0Fh	SUBADR2	7:5	A2[7:5]	R	100 (2)	Reserved
		4:1	A2[4:1]	R/W	1010 (2)	I^2C bus sub-address 2
		0	A2[0]	R	0 (2)	Reserved
10h	SUBADR3	7:5	A3[7:5]	R	100 (2)	Reserved
		4:1	A3[4:1]	R/W	1100 (2)	I^2C bus sub-address 3
		0	A3[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

Sub-addresses are programmable through the I^{2}C bus. Default power-up values are 92h, 94h, 98h and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once sub-addresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I^{2}C bus sub-address are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I^{2}C bus sub-address can be used during either an I^{2}C bus read or write sequence.

8.6.9 LED All Call I^{2}C Bus Address Register (ALLCALLADR)

Table 10 describes the LED All Call I^{2}C Bus Address Register.

Table 10. ALLCALLADR – LED All Call I^{2}C Bus Address Register Addresses 11h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
11h	ALLCALLADR	7:5	AC[7:5]	R	100 (2)	Reserved
		4:1	AC[4:1]	R/W	1000 (2)	ALLCALL I^{2}C bus address
		0	AC[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

The LED All Call I^{2}C-bus address allows all the TLC59108Fs in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I^{2}C-bus and can be used during either an I^{2}C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I^{2}C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0 (MODE1 register), the device does not acknowledge the address programmed in register ALLCALLADR.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Setting LED Current

The LED current is primarily dependent on the supply voltage, the forward voltage of the LED, and the series resistor (R_{SET}). In many applications the supply voltage and LED forward voltage cannot be adjusted. Hence, R_{SET} is used to adjust the LED current. This calculation is discussed in detail in the typical application example.

9.1.2 PWM Brightness Dimming

The perceived brightness of the LEDs can be adjusted by use of PWM dimming. For example, an LED driven at 50% duty cycle will appear less bright than it would at 100% duty cycle. The TLC59116F offers duty cycle control for each individual channel and also offers group duty cycle control. Refer to the *Register Maps* for details regarding programmable duty cycle.

9.1.3 TLC59108 and TLC59108F Differences

The TLC59108 and TLC59108F are similar devices with the difference being the output structure. The TLC59108 has 8 constant-current outputs while the TLC59108F has 8 open-drain outputs. The REXT is used to program the current on the TLC59108 for all channels. The in-line resistors on the OUT pins are used in conjunction with the VLED to set the currents on each TLC59108F channel. Because the resistors are unique for each output, the currents can be set by output by changing the resistor value.

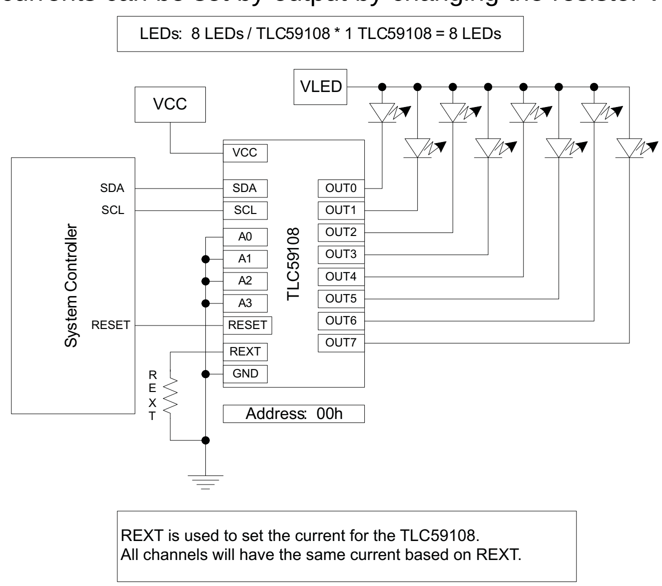


Figure 20. TLC59108 One Driver

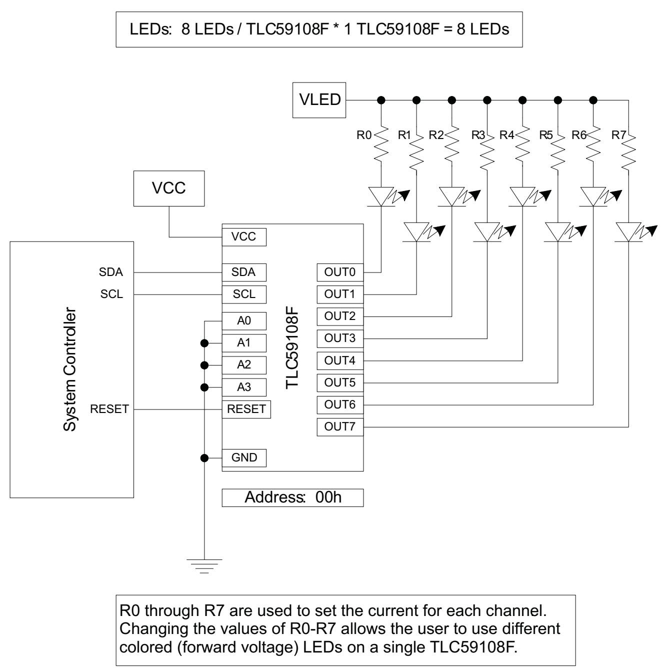


Figure 21. TLC59108F One Driver

Application Information (continued)

9.1.4 Connecting Multiple Devices

This drawing is an example of using the TLC59108F in a system requiring up to 48 LED strings. The TLC59108F drivers share a single I^2C bus. The address pins are set high or low to enable the drivers to be independently accessed (all can be written in parallel through the ALLCALLADR function). The resistors in series with the LEDs along with the VLED voltage will set the current for each string independently. Changing the resistor values allows for multi-color displays.

Application Information (continued)

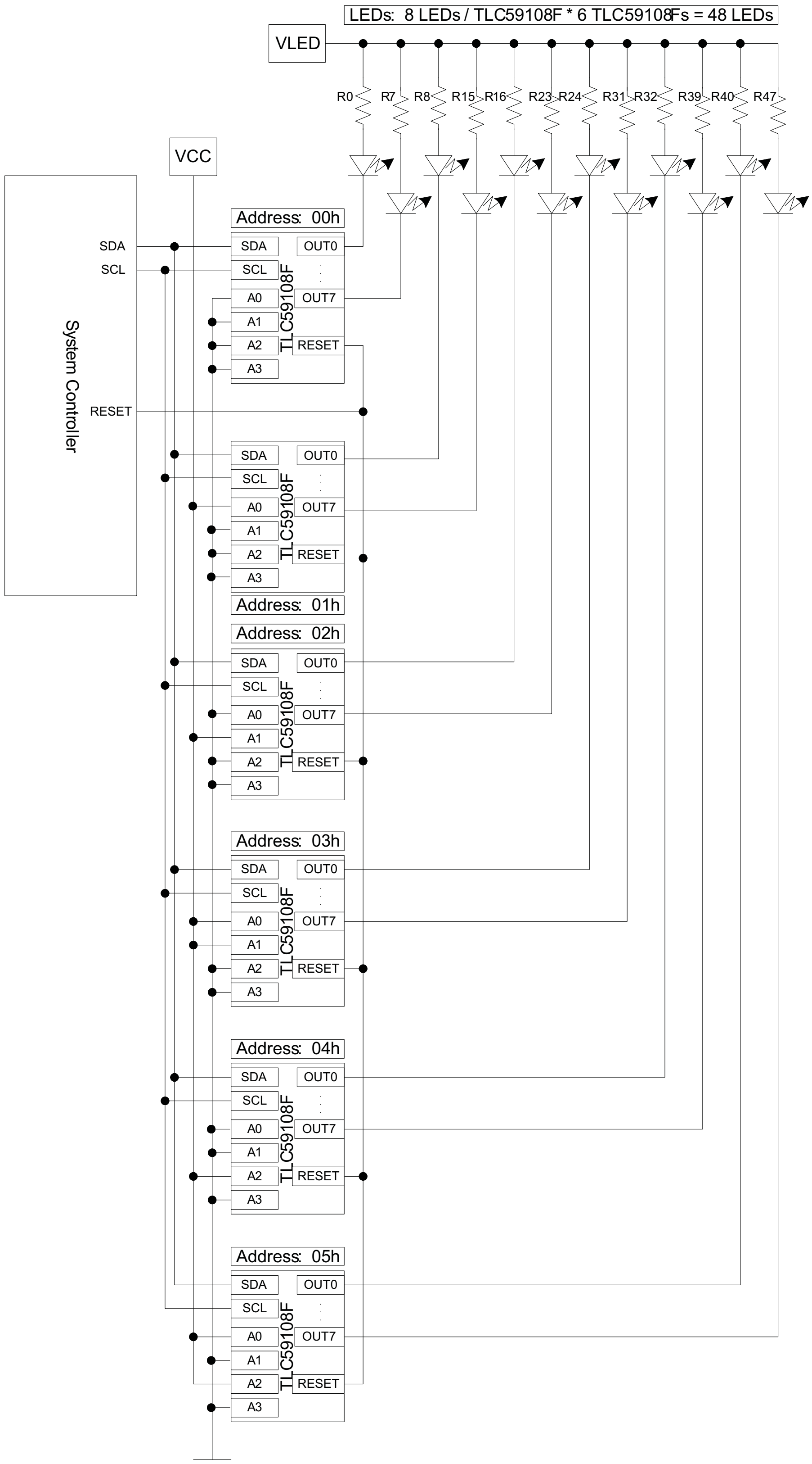


Figure 22. Six Drivers

9.2 Typical Application

This application example provides guidance on how to set the LED current using the TLC59108F.

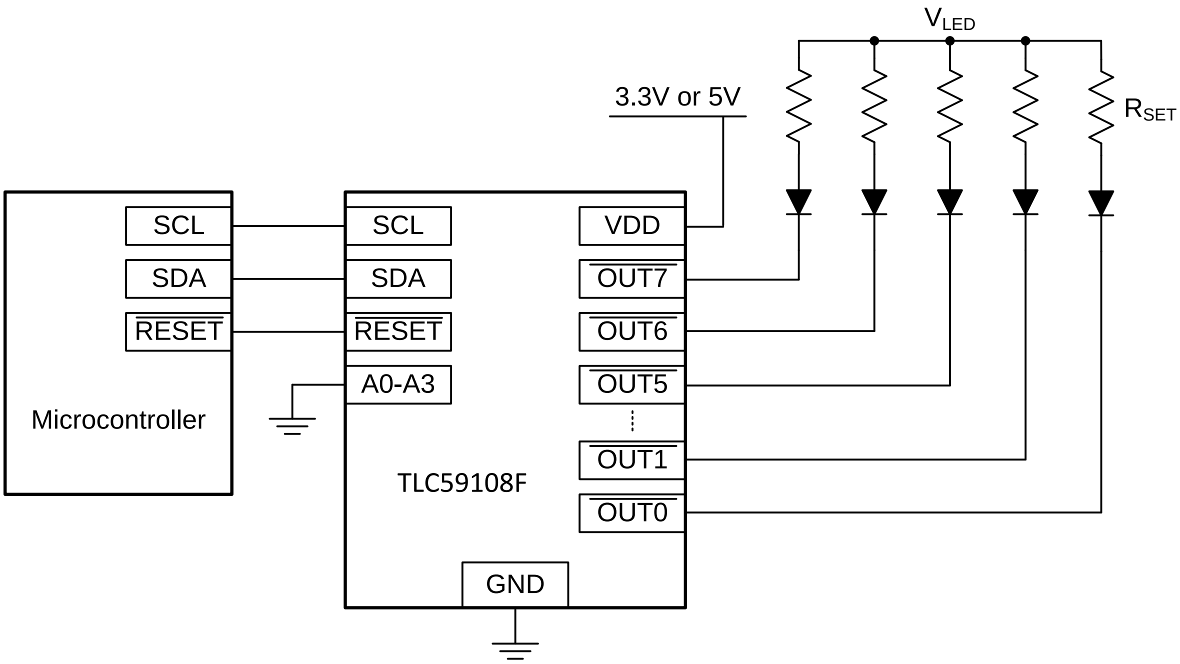


Figure 23. Typical Application

9.2.1 Design Requirements

For this design example, use the following as the input parameters listed in Table 11.

Table 11. Design Parameters

DESIGN PARAMETERS		EXAMPLE VALUE
V_{LED}	Supply voltage that powers LED	5 V
V_F	Forward voltage across the LED	3 V
I_{LED}	Current flowing through the LED	6 mA
R_{ON}	Resistance across open-drain output	1.5 Ω

9.2.2 Detailed Design Procedure

In the LED current path, there are three voltage drops that must be considered:

- Drop across the series resistor (V_{RSET})
- Drop across the LED (V_F)
- Drop across the open-drain output channel (V_O)

The drop across the LED is defined above as V_F = 3 V. The drop across the open-drain output is calculated as $R_{ON} \times I_{LED}$ (1.5 × 0.006 = 0.009 V). The remaining voltage must be across the series resistor:

$$5\ \text{V} = 3\ \text{V} + 0.009\ \text{V} + V_{RSET} \quad (3)$$

$$V_{RSET} = 1.991\ \text{V} \quad (4)$$

After calculating V_{RSET}, we can calculate R_{SET} using Equation 5, Equation 6, and Equation 7 :

$$V_{RSET} = I_{LED} \times R_{SET} \quad (5)$$

$$1.991\ \text{V} = 0.006\ \text{mA} \times R_{SET} \quad (6)$$

$$R_{SET} = 332\ \Omega \quad (7)$$

9.2.3 Application Curve

The following graph shows the typical LED Current as a function of R_{SET} and V_F. The graph assumes that V_{LED} = 5 V.

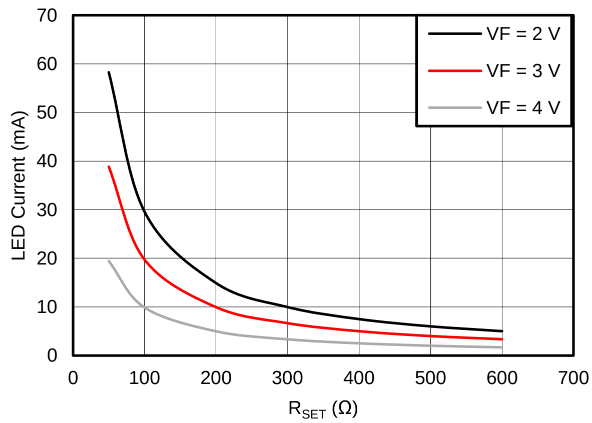


Figure 24. LED Current vs R_{SET}

10 Power Supply Recommendations

TLC59108F is designed to operate from a V_{CC} range of 3 V to 5.5 V. The system will also require a power supply for the LEDs. The supply voltage for the LEDs must be greater than the forward voltage of the LED plus the V_{OL} of the channel.

11 Layout

11.1 Layout Guidelines

The I^2C signals (SDA / SCL) should be kept away from potential noise sources.

The traces carrying power through the LEDS should be wide enough to handle the necessary current.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground. For the RGY package, the thermal pad should be connected to ground to help dissipate heat.

11.2 Layout Example

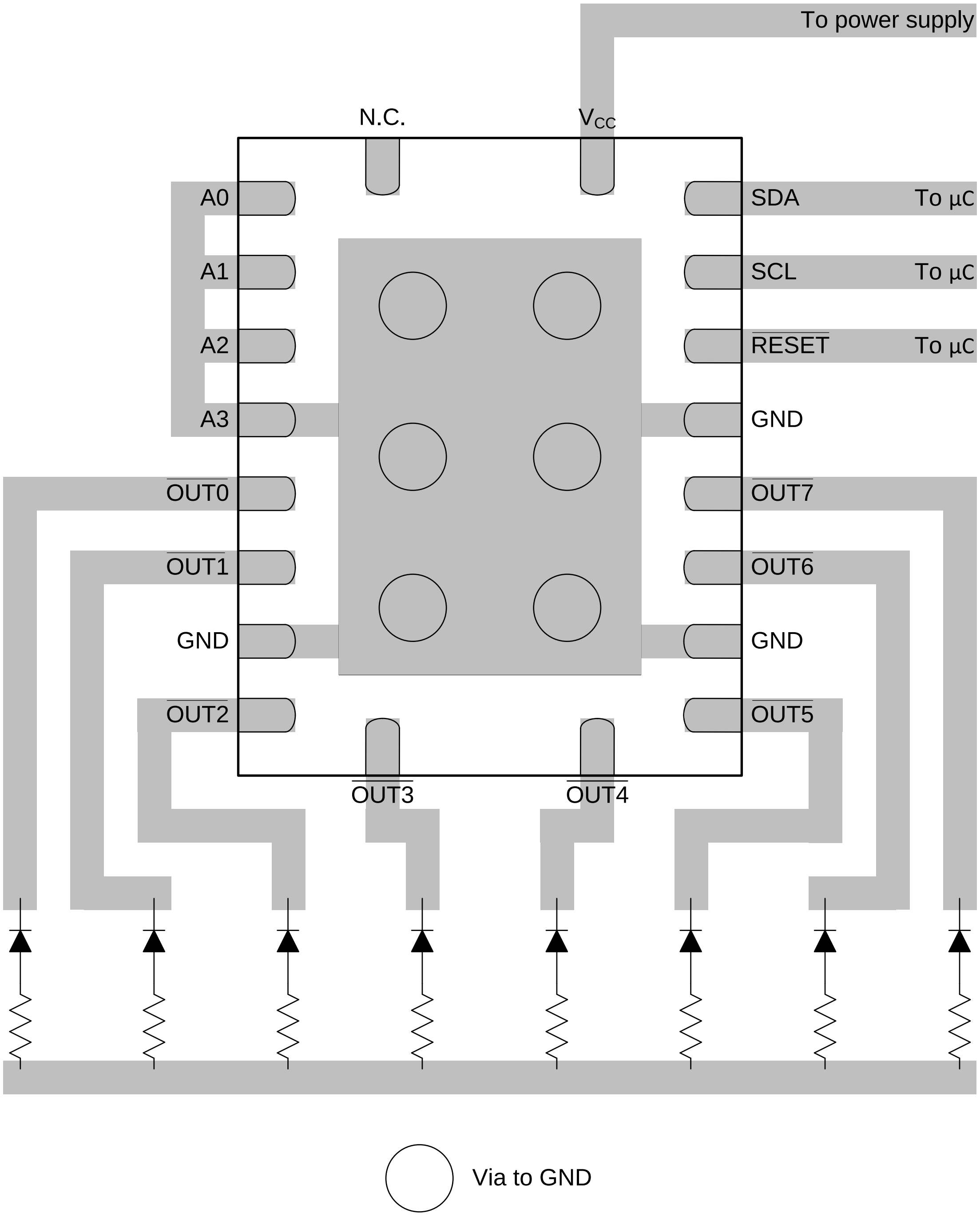


Figure 25. RGY Layout Example

Layout Example (continued)

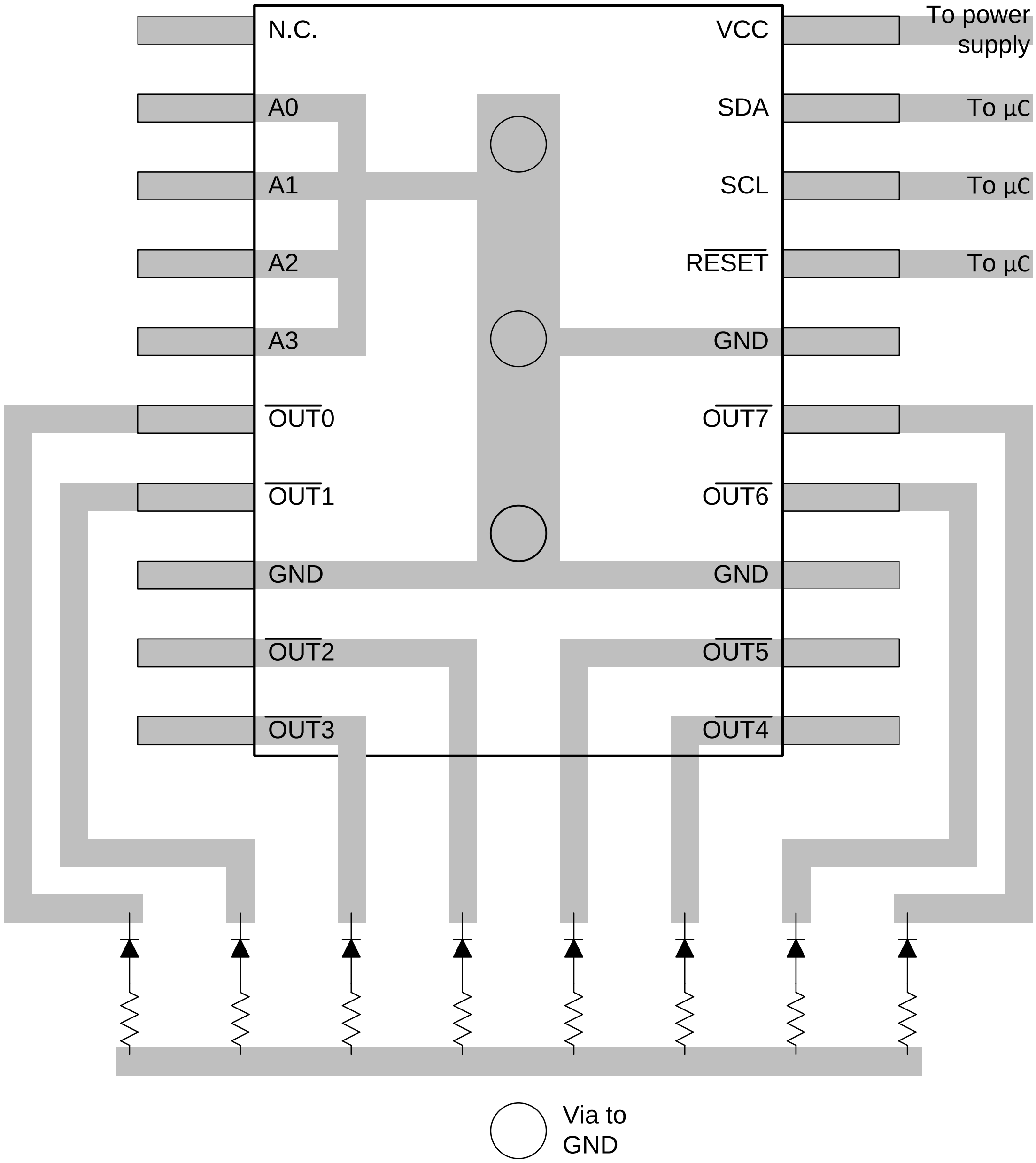


Figure 26. PW Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC59108FIPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59108F
TLC59108FIPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59108F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

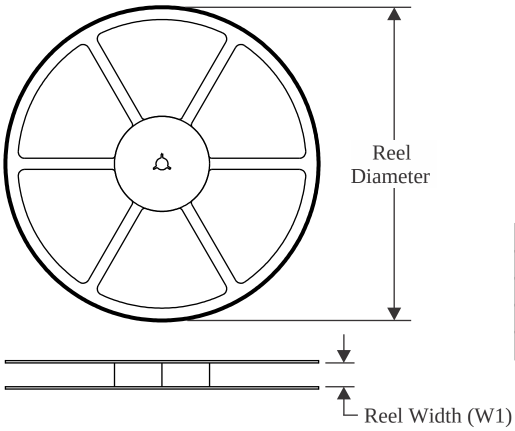
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

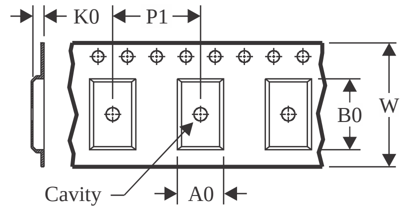
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

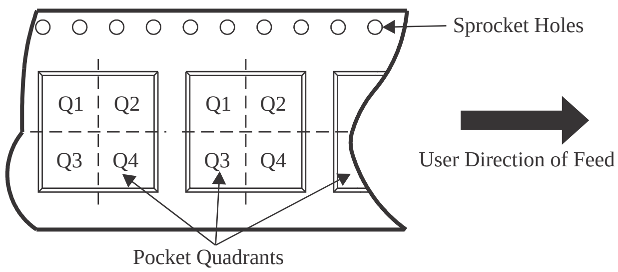


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

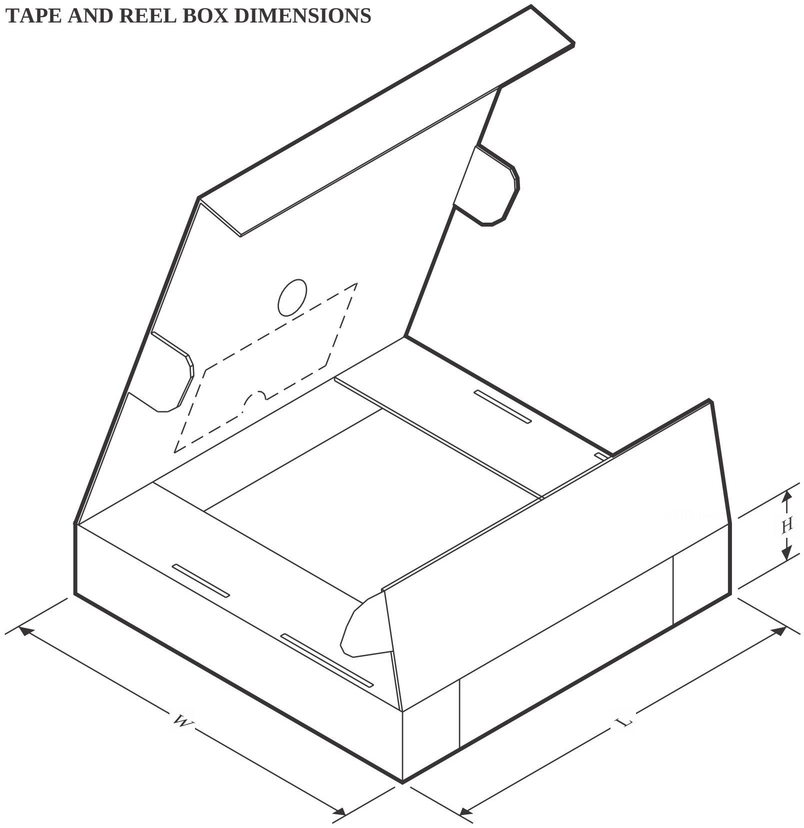
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

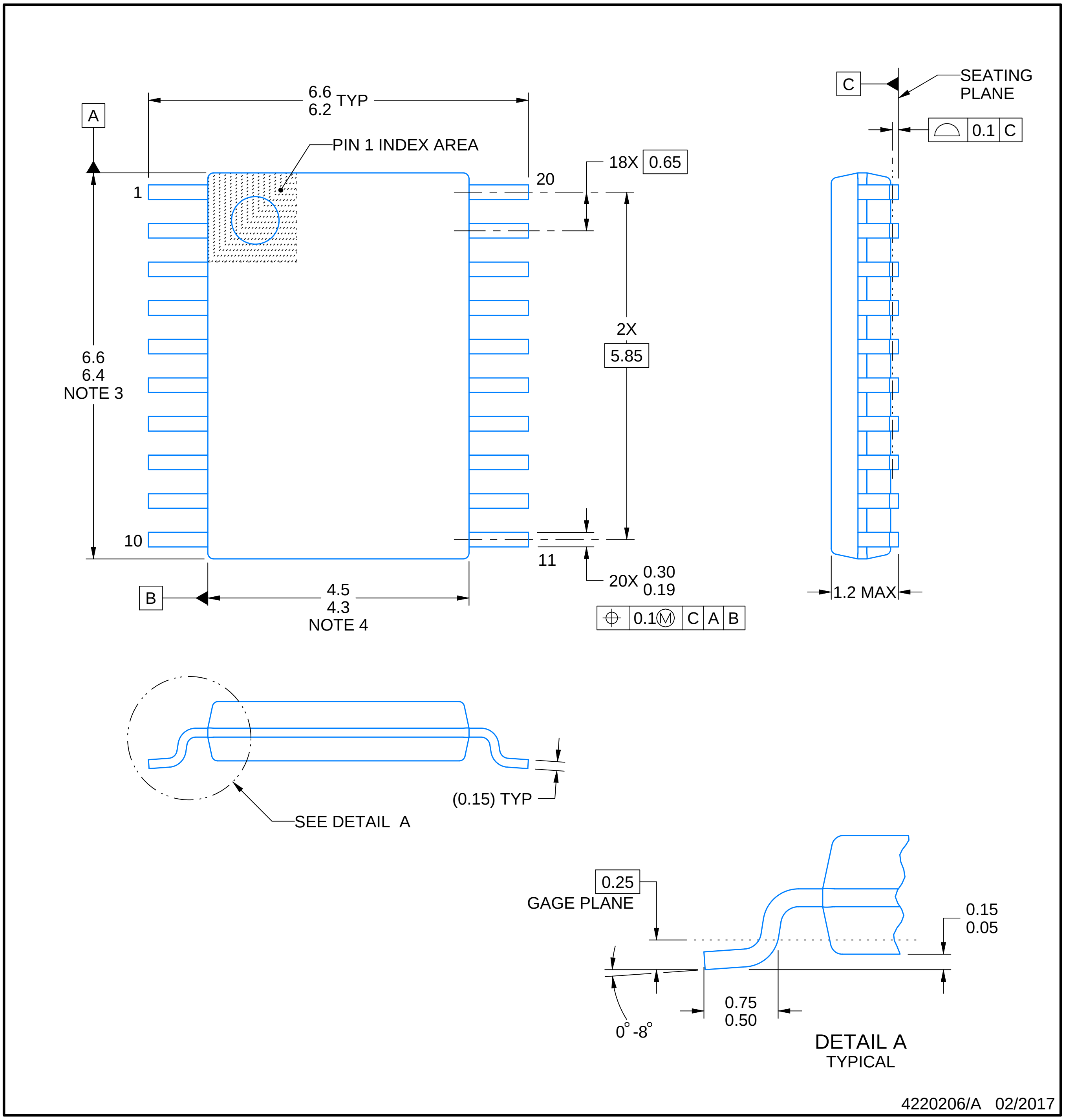
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59108FIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



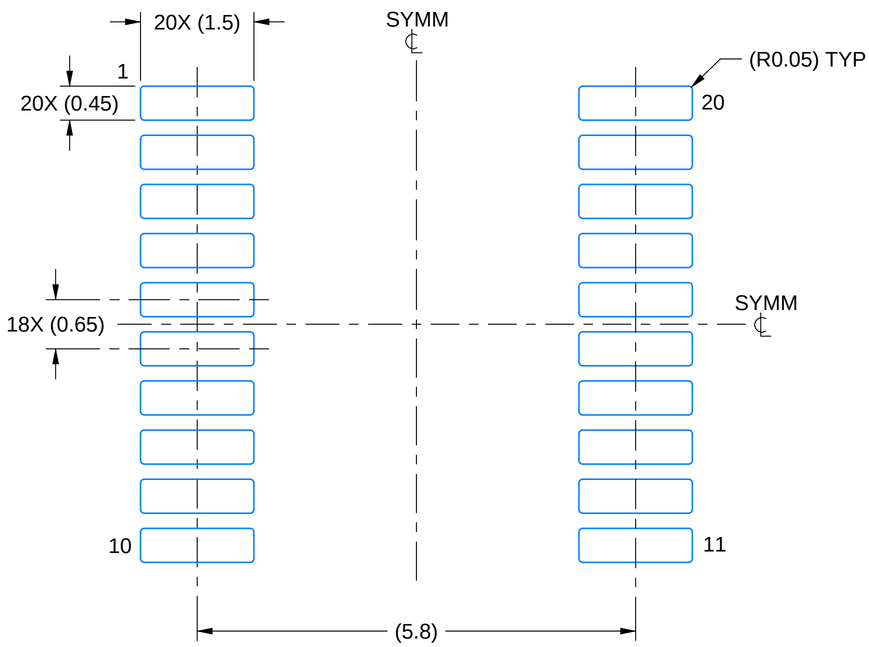
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59108FIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

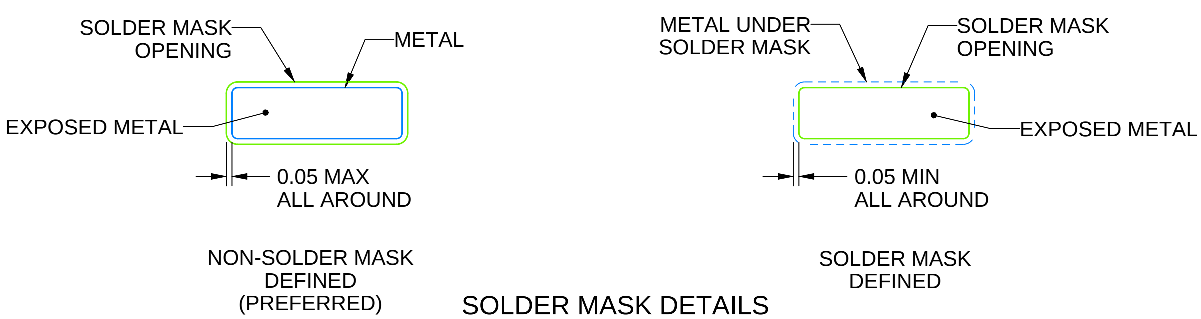


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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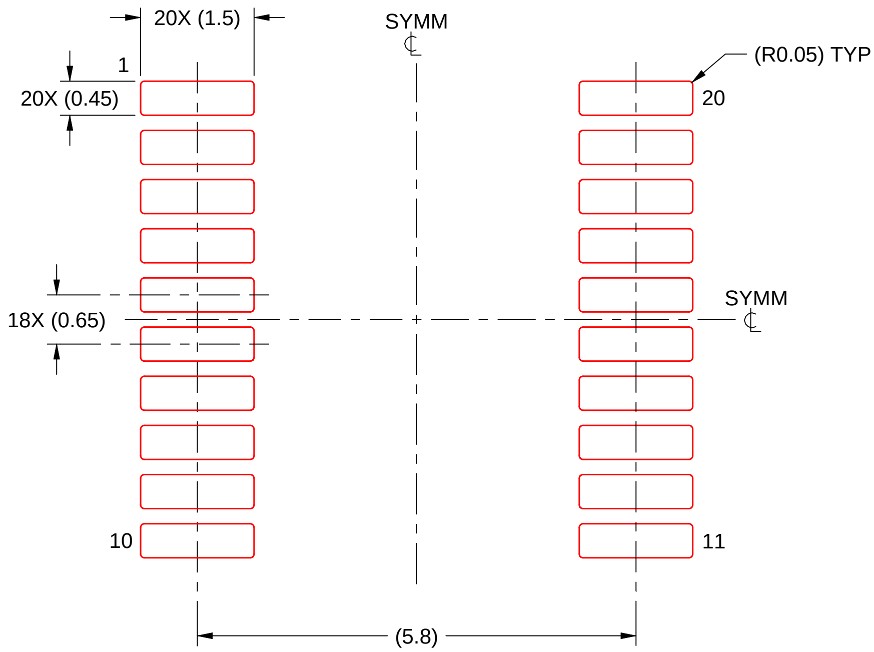
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.