

TLC555 LinCMOS™ 技术计时器

1 特性

- 极低功耗：
 - $V_{DD} = 5V$ 时为 1mW (典型值)
- 能够在非稳态模式下正常工作
- 支持轨到轨摆动的 CMOS 输出
- 高输出电流能力
 - 灌电流：100mA (典型值)
 - 拉电流：10mA (典型值)
- 输出与 CMOS、TTL 和 MOS 完全兼容
- 低电源电流在输出转换期间降低了尖峰
- 2V 至 15V 单电源运行
- 在功能上可与 NE555 互换；具有相同的引脚
- ESD 保护超出 ANSI/ESDA/JEDEC JS-001 规定的 1000V
- 可用于 Q 级温度汽车
 - 高可靠性汽车应用
 - 配置控制和打印支持
 - 通过汽车标准鉴定

2 应用

- 精确计时
- 脉冲发生
- 顺序计时
- 延时时间生成
- 脉宽调制
- 脉冲位置调制
- 线性斜坡发生器

3 说明

TLC555 是一款采用 TI LinCMOS™ 技术制造的单片定时电路。该计时器与 CMOS、TTL 和 MOS 逻辑器件完全兼容，可在最高 2MHz 的频率下运行。由于输入阻抗较高，此器件可支持比 NE555 或 LM555 所支持的计时电容器更小的计时电容器。因此，可实现更加准确的延时时间和振荡。在整个电源电压范围内可保持较低功耗。

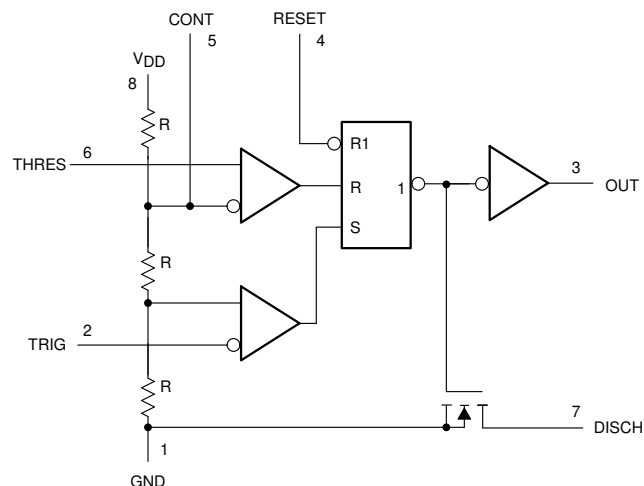
与 NE555 类似，TLC555 有一个约等于电源电压三分之一的触发电平以及一个约等于电源电压三分之二的阈值电平。可使用控制电压端子 (CONT) 来改变这些电平。当触发输入 (TRIG) 下降至低于触发电平的时候，触发器被设定并且输出变为高电平。如果 TRIG 高于触发电平并且阈值输入 (THRES) 在阈值电平之上的话，触发器被复位并且输出为低电平。复位输入 (RESET) 的优先级高于所有其它输入并且可被用来启动一个新的定时周期。如果 RESET 为低电平，触发器被复位并且输出为低电平。只要当输出为低电平，在放电端子 (DISCH) 和接地 (GND) 之间提供一个低阻抗路径。所有未用输入端必须接入合适的逻辑电平以免发生误触发。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ |
|---------|-------------------|---------------------|
| TLC555C | SOIC (8) | 4.9mm × 6.0mm |
| | PDIP (8) | 9.81mm × 9.43mm |
| | SOP (8) | 6.2mm × 7.8mm |
| | TSSOP (14) | 5.0mm × 6.4mm |
| TLC555I | SOIC (8) | 4.9mm × 6.0mm |
| | PDIP (8) | 9.81mm × 9.43mm |
| TLC555M | LCCC (20) | 8.89mm × 8.89mm |
| | CDIP (8) | 9.6mm × 9.0mm |
| TLC555Q | SOIC (8) | 4.9mm × 6.0mm |

(1) 有关详细信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



简化版原理图



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4 Pin Configuration and Functions

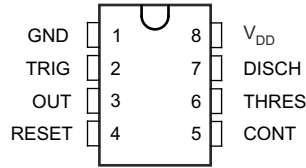


图 4-1. D, P, PS, and JG Packages, 8-Pin SOIC, PDIP, SOP, and CDIP (Top View)

表 4-1. Pin Functions: D, P, PS, and JG Packages

| PIN | | TYPE | DESCRIPTION |
|----------|-----|--------|----------------------------------------------------------------------------------------------|
| NAME | NO. | | |
| CONT | 5 | Input | Controls comparator thresholds. Outputs $2/3 V_{DD}$ and allows bypass capacitor connection. |
| DISCH | 7 | Output | Open collector output to discharge timing capacitor. |
| GND | 1 | — | Ground. |
| NC | — | — | No internal connection. |
| OUT | 3 | Output | High current timer output signal. |
| RESET | 4 | Input | Active low reset input forces output and discharge low. |
| THRES | 6 | Input | End of timing input. $THRES > CONT$ sets output low and discharge low. |
| TRIG | 2 | Input | Start of timing input. $TRIG < 1/2 CONT$ sets output high and discharge open. |
| V_{DD} | 8 | — | Power-supply voltage. |

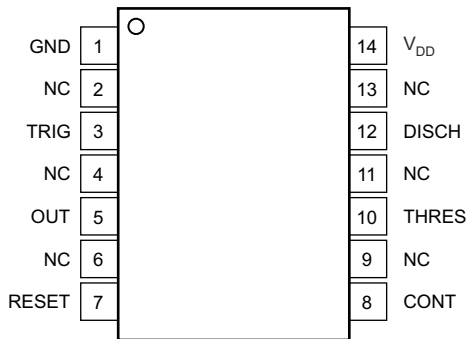


图 4-2. PW Package, 14-Pin TSSOP (Top View)

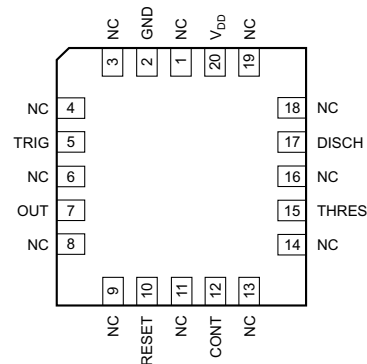


图 4-3. FK Package, 20-Pin LCCC (Top View)

表 4-2. Pin Functions: PW and FK

| NAME | PIN NO. | | TYPE | DESCRIPTION |
|-------|--------------------|------------------------------------------|--------|----------------------------------------------------------------------------------------------|
| | PW (TSSOP) | FK (LCCC) | | |
| CONT | 8 | 12 | Input | Controls comparator thresholds. Outputs $2/3 V_{DD}$ and allows bypass capacitor connection. |
| DISCH | 12 | 17 | Output | Open-collector output to discharge timing capacitor. |
| GND | 1 | 2 | — | Ground. |
| NC | 2, 4, 6, 9, 11, 13 | 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19 | — | No internal connection. |
| OUT | 5 | 7 | Output | High current timer output signal. |
| RESET | 7 | 10 | Input | Active low reset input forces output and discharge low. |
| THRES | 10 | 15 | Input | End of timing input. $THRES > CONT$ sets output low and discharge low. |
| TRIG | 3 | 5 | Input | Start of timing input. $TRIG < 1/2 CONT$ sets output high and discharge open. |

表 4-2. Pin Functions: PW and FK (续)

| NAME | PIN | | TYPE | DESCRIPTION |
|-----------------|------------|-----------|------|-----------------------|
| | NO. | | | |
| | PW (TSSOP) | FK (LCCC) | | |
| V _{DD} | 14 | 20 | — | Power-supply voltage. |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|----------------------------------|----------------------------------------|-------|-----------------|------|
| | Voltage | Supply, V _{DD} ⁽²⁾ | - 0.3 | 18 | V |
| | | Input, any input | - 0.3 | V _{DD} | |
| | | Discharge | - 0.3 | 18 | |
| | Current | Sink, discharge or output | | 150 | mA |
| | | Source, output, I _O | | 15 | |
| T _A | Operating temperature | C-suffix | 0 | 70 | °C |
| | | I-suffix | - 40 | 85 | |
| | | Q-suffix | - 40 | 125 | |
| | | M-suffix | - 55 | 125 | |
| | Case temperature, for 60 seconds | FK package | - 65 | 150 | °C |
| T _{stg} | Storage temperature | | - 65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network GND.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|----------------------------------------|-----------------------------------------------------------------------|-------|------|
| V _(ESD) | Electrostatic discharge ⁽³⁾ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1000 | |
| | | Machine model (MM) | ±200 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) See 节 7.2.5 for application guidance on protecting the device against ESD.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|---------|------|-----|------|
| V _{DD} | Supply voltage | TLC555C | 2 | 15 | V |
| | | TLC555I | 3 | 15 | |
| | | TLC555M | 5 | 15 | |
| | | TLC555Q | 5 | 15 | |
| T _A | Operating free-air temperature | TLC555C | 0 | 70 | °C |
| | | TLC555I | - 40 | 85 | |
| | | TLC555M | - 55 | 125 | |
| | | TLC555Q | - 40 | 125 | |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TLC555 | | | | | | UNIT |
|-------------------------------|----------------------------------------------|-------------|--------------|--------------|-------------|-------------|---------------|------|
| | | D (SOIC) | FK (LCCC) | JG (CDIP) | P (PDIP) | PS (SOP) | PW (TSSOP) | |
| | | 8 PINS | 20 PINS | 8 PINS | 8 PINS | 8 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 138.9 | N/A | 120 | 93.1 | 120 | 135 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 78.8 | 37 | 81 | 82.5 | 72 | 61 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 87.9 | 36 | 110 | 69.6 | 69 | 77 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 23.2 | N/A | 45 | 52.0 | 32 | 12 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 86.9 | N/A | 103 | 69.2 | 68 | 77 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 4.3 | 31 | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics: $V_{DD} = 2\text{ V}$ for TLC555C, $V_{DD} = 3\text{ V}$ for TLC555I

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|----------------|------------------------------------------------------------------|-------------------------------------|---------|------|-------|-------|------|
| V_{IT} | Threshold voltage | 25°C | TLC555C | 0.95 | 1.33 | 1.65 | V |
| | | | TLC555I | 1.6 | | 2.4 | |
| | | Full range | TLC555C | 0.85 | | 1.75 | |
| | | | TLC555I | 1.5 | | 2.5 | |
| I_{IT} | Threshold current | 25°C | TLC555C | | 10 | | pA |
| | | | TLC555I | | 10 | | |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| $V_{I(TRIG)}$ | Trigger voltage | 25°C | TLC555C | 0.4 | 0.67 | 0.95 | V |
| | | | TLC555I | 0.71 | 1 | 1.29 | |
| | | Full range | TLC555C | 0.3 | | 1.05 | |
| | | | TLC555I | 0.61 | | 1.39 | |
| $I_{I(TRIG)}$ | Trigger current | 25°C | TLC555C | | 10 | | pA |
| | | | TLC555I | | 10 | | |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| $V_{I(RESET)}$ | Reset voltage | 25°C | TLC555C | 0.4 | 1.1 | 1.5 | V |
| | | | TLC555I | 0.4 | 1.1 | 1.5 | |
| | | Full range | TLC555C | 0.3 | | 2 | |
| | | | TLC555I | 0.3 | | 1.8 | |
| | Control voltage (open-circuit) as a percentage of supply voltage | Max | TLC555C | | 66.7% | | |
| | | | TLC555I | | 66.7% | | |
| | Discharge switch on-stage voltage | $I_{OL} = 1\text{ mA}$, 25°C | TLC555C | | 0.03 | 0.2 | V |
| | | | TLC555I | | 0.03 | 0.2 | |
| | | $I_{OL} = 1\text{ mA}$, Full range | TLC555C | | | 0.25 | |
| | | | TLC555I | | | 0.375 | |
| | Discharge switch off-stage current | 25°C | TLC555C | | 0.1 | | nA |
| | | | TLC555I | | 0.1 | | |
| | | Max | TLC555C | | 0.5 | | |
| | | | TLC555I | | 120 | | |

5.5 Electrical Characteristics: $V_{DD} = 2\text{ V}$ for TLC555C, $V_{DD} = 3\text{ V}$ for TLC555I (续)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------------------------|-------------------------------------------|---------|-----|------|------|---------------|
| V_{OH} | High-level output voltage | $I_{OH} = -300\ \mu\text{A}$, 25°C | TLC555C | 1.5 | 1.9 | | V |
| | | | TLC555I | 2.5 | 2.85 | | |
| | | $I_{OH} = -300\ \mu\text{A}$, Full range | TLC555C | 1.5 | | | |
| | | | TLC555I | 2.5 | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 1\ \text{mA}$, 25°C | TLC555C | | 0.07 | 0.3 | V |
| | | | TLC555I | | 0.07 | 0.3 | |
| | | $I_{OL} = 1\ \text{mA}$, Full range | TLC555C | | | 0.35 | |
| | | | TLC555I | | | 0.4 | |
| I_{DD} | Supply current ⁽²⁾ | 25°C | TLC555C | | | 250 | μA |
| | | | TLC555I | | | 250 | |
| | | Full range | TLC555C | | | 400 | |
| | | | TLC555I | | | 500 | |
| C_{PD} | Power dissipation capacitance ⁽³⁾ (4) | 25°C | TLC555C | | 80 | | pF |
| | | | TLC555I | | 90 | | |

- (1) Full range is 0°C to 70°C the for TLC555C, and -40°C to +85°C for the TLC555I. For conditions shown as MAX, use the appropriate value specified in the [§ 5.3](#).
- (2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
- (3) C_{PD} is used to determine the dynamic power consumption.
- (4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.

5.6 Electrical Characteristics: $V_{DD} = 5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|----------------|-------------------------------------------|--------------------------------|------------------------------------|------|------|------|------|
| V_{IT} | Threshold voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 2.8 | 3.3 | 3.8 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 2.7 | | 3.9 | |
| I_{IT} | Threshold current | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | | TLC555M, TLC555Q | | 5000 | | | |
| $V_{I(TRIG)}$ | Trigger voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 1.36 | 1.66 | 1.96 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 1.26 | | 2.06 | |
| $I_{I(TRIG)}$ | Trigger current | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | | TLC555M, TLC555Q | | 5000 | | | |
| C_1 | Trigger, threshold capacitance (each pin) | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 2.1 | | pF |
| $V_{I(RESET)}$ | Reset voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 0.4 | 1.1 | 1.5 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 0.3 | | 1.8 | |

5.6 Electrical Characteristics: $V_{DD} = 5\text{ V}$ (续)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|-----------------------|------------------------------------------------------------------|-------------------------------------------------|---------------------------------------|-----|-------|------|----------------|
| $I_{I(\text{RESET})}$ | Reset current | 25°C, $V_{\text{RESET}} = 0\text{ V}$ | TLC555C, TLC555I, TLC555M, TLC555Q | | 5.9 | | $\mu\text{ A}$ |
| | | 25°C, $V_{\text{RESET}} = V_{\text{DD}}$ | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | Max, $V_{\text{RESET}} = V_{\text{DD}}$ | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | | | TLC555M, TLC555Q | | 5000 | | |
| | Control voltage (open circuit) as a percentage of supply voltage | Max | TLC555C, TLC555I, TLC555M, TLC555Q | | 66.7% | | |
| | Discharge switch on-stage voltage | $I_{\text{OL}} = 10\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.14 | 0.5 | V |
| | | $I_{\text{OL}} = 10\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | | | 0.6 | |
| | Discharge switch off-stage current | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.1 | | nA |
| | | | TLC555C | | 0.5 | | |
| | | Max | TLC555I | | 120 | | |
| | | | TLC555M, TLC555Q | | 120 | | |
| V_{OH} | High-level output voltage | $I_{\text{OH}} = -1\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 4.1 | 4.8 | | V |
| | | $I_{\text{OH}} = -1\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 4.1 | | | |
| V_{OL} | Low-level output voltage | $I_{\text{OL}} = 8\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.21 | 0.4 | V |
| | | | TLC555C | | | 0.5 | |
| | | $I_{\text{OL}} = 8\text{ mA}$, Full range | TLC555I | | | 0.5 | |
| | | | TLC555M, TLC555Q | | | 0.6 | |
| V_{OL} | Low-level output voltage | $I_{\text{OL}} = 5\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.13 | 0.3 | V |
| | | | TLC555C | | | 0.4 | |
| | | $I_{\text{OL}} = 5\text{ mA}$, Full range | TLC555I | | | 0.4 | |
| | | | TLC555M, TLC555Q | | | 0.45 | |
| | | $I_{\text{OL}} = 3.2\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.08 | 0.3 | |
| | | | TLC555C | | | 0.35 | |
| | | $I_{\text{OL}} = 3.2\text{ mA}$, Full range | TLC555I | | | 0.35 | |
| | | | TLC555M, TLC555Q | | | 0.4 | |
| I_{DD} | Supply current ⁽²⁾ | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 180 | 350 | $\mu\text{ A}$ |
| | | | TLC555C | | | 500 | |
| | | Full range | TLC555I | | | 600 | |
| | | | TLC555M, TLC555Q | | | 700 | |
| C_{PD} | Power dissipation capacitance ⁽³⁾ (4) | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 115 | | pF |

- (1) Full range is 0°C to 70°C the for TLC555C, -40°C to 85°C for the TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for the TLC555M. For conditions shown as MAX, use the appropriate value specified in the [# 5.3](#) table.
- (2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
- (3) C_{PD} is used to determine the dynamic power consumption.
- (4) $P_{\text{D}} = V_{\text{DD}}^2 f_{\text{o}} (C_{\text{PD}} + C_{\text{L}})$ where f_{o} = output frequency, C_{L} = output load capacitance, V_{DD} = supply voltage.

5.7 Electrical Characteristics: $V_{DD} = 15\text{ V}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------|-------------------------------------------|---------------------------------------|---------------------------------------|-------|------|-------|---------------|
| V_{IT} | Threshold voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 9.45 | 10 | 10.55 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 9.35 | | 10.65 | |
| I_{IT} | Threshold current | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | TLC555M, TLC555Q | | 5000 | | | | |
| $V_{I(TRIG)}$ | Trigger voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 4.65 | 5 | 5.35 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 4.55 | | 5.45 | |
| $I_{I(TRIG)}$ | Trigger current | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | Max | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | TLC555M, TLC555Q | | 5000 | | | | |
| C_I | Trigger, threshold capacitance (each pin) | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 1.8 | | pF |
| $V_{I(RESET)}$ | Reset voltage | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 0.4 | 1.1 | 1.5 | V |
| | | Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 0.3 | | 1.8 | |
| $I_{I(RESET)}$ | Reset current | 25°C, $V_{RESET} = 0\text{ V}$ | TLC555C, TLC555I, TLC555M, TLC555Q | | 17.8 | | μA |
| | | 25°C, $V_{RESET} = V_{DD}$ | TLC555C, TLC555I, TLC555M, TLC555Q | | 10 | | pA |
| | | | TLC555C | | 75 | | |
| | | | TLC555I | | 150 | | |
| | | | TLC555M, TLC555Q | | 5000 | | |
| Control voltage (open circuit) as a percentage of supply voltage | Max | TLC555C, TLC555I, TLC555M, TLC555Q | | 66.7% | | | |
| Discharge switch on-stage voltage | | $I_{OL} = 100\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.77 | 1.7 | V |
| | | $I_{OL} = 100\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | | | 1.8 | |
| Discharge switch off-stage current | | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.1 | | nA |
| | | Max | TLC555C | | 0.5 | | |
| | | | TLC555I | | 120 | | |
| | TLC555M, TLC555Q | | 120 | | | | |
| V_{OH} | High-level output voltage | $I_{OH} = -10\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | 12.5 | 14.2 | | V |
| | | $I_{OH} = -10\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 12.5 | | | |
| | | | TLC555C, TLC555I, TLC555M, TLC555Q | 13.5 | 14.6 | | |
| | | $I_{OH} = -5\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 13.5 | | | |
| | | | TLC555C, TLC555I, TLC555M, TLC555Q | 14.2 | 14.9 | | |
| | | $I_{OH} = -1\text{ mA}$, Full range | TLC555C, TLC555I, TLC555M, TLC555Q | 14.2 | | | |

5.7 Electrical Characteristics: $V_{DD} = 15\text{ V}$ (续)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT | |
|-----------|-----------------------------------------------------|------------------------------------------|---------------------------------------|-----|------|------|------|-----|
| V_{OL} | Low-level output voltage | $I_{OL} = 100\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 1.28 | 3.2 | V | |
| | | | TLC555C | | | 3.6 | | |
| | | $I_{OL} = 100\text{ mA}$, Full range | TLC555I | | | 3.7 | | |
| | | | TLC555M, TLC555Q | | | 3.8 | | |
| | | | TLC555C, TLC555I, TLC555M, TLC555Q | | 0.63 | 1 | | |
| | | $I_{OL} = 50\text{ mA}$, Full range | TLC555C | | | 1.3 | | |
| | | | TLC555I | | | 1.4 | | |
| | | | TLC555M, TLC555Q | | | 1.5 | | |
| | | $I_{OL} = 10\text{ mA}$, 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | | 0.12 | | 0.3 |
| | | | TLC555C | | | | | 0.4 |
| TLC555I | | | | | 0.4 | | | |
| | | $I_{OL} = 10\text{ mA}$, Full range | TLC555M, TLC555Q | | | 0.45 | | |
| | | | TLC555C, TLC555I, TLC555M, TLC555Q | | 360 | 600 | | |
| | | | TLC555C | | | 800 | | |
| I_{DD} | Supply current ⁽²⁾ | Full range | TLC555I | | | 900 | | |
| | | | TLC555M, TLC555Q | | | 1000 | | |
| | | | TLC555C, TLC555I, TLC555M, TLC555Q | | 140 | | | |
| C_{PD} | Power dissipation capacitance ⁽³⁾ (4) | 25°C | TLC555C, TLC555I, TLC555M, TLC555Q | | 140 | | pF | |

(1) Full range is 0°C to 70°C for TLC555C, -40°C to 85°C for TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for TLC555M. For conditions shown as MAX, use the appropriate value specified in the [# 5.3](#) table.

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

(3) C_{PD} is used to determine the dynamic power consumption.

(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.

5.8 Timing Characteristics

$V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted). Characteristic values are specified by design, characterization, or both.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| | Supply voltage sensitivity of timing interval | $V_{DD} = 5\text{ V to }15\text{ V}$, $C_T = 0.1\ \mu\text{F}$ $R_A = R_B = 1\text{ k}\Omega\text{ to }100\text{ k}\Omega$ ⁽¹⁾ | | 0.1 | 0.5 | %/V |
| t_r | Output pulse rise time | $R_L = 10\text{ M}\Omega$, $C_L = 10\text{ pF}$ | | 20 | 75 | ns |
| t_f | Output pulse fall time | $R_L = 10\text{ M}\Omega$, $C_L = 10\text{ pF}$ | | 15 | 60 | ns |
| f_{max} | Maximum frequency in a-stable mode | $R_A = 470\ \Omega$, $C_T = 200\text{ pF}$, $R_B = 200\ \Omega$ ⁽¹⁾ | 1.2 | 2.1 | | MHz |

(1) R_A , R_B , and C_T are as defined in [图 6-5](#).

5.9 Typical Characteristics

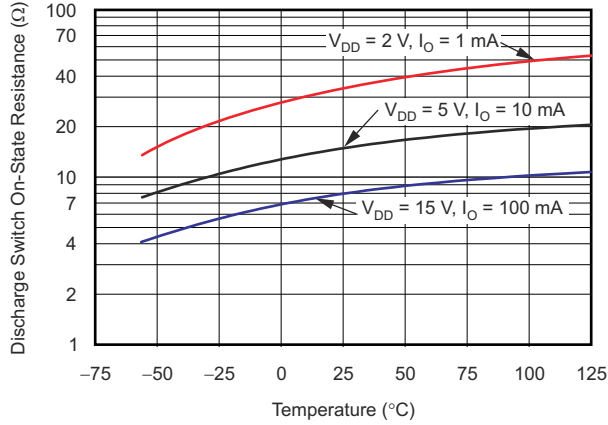
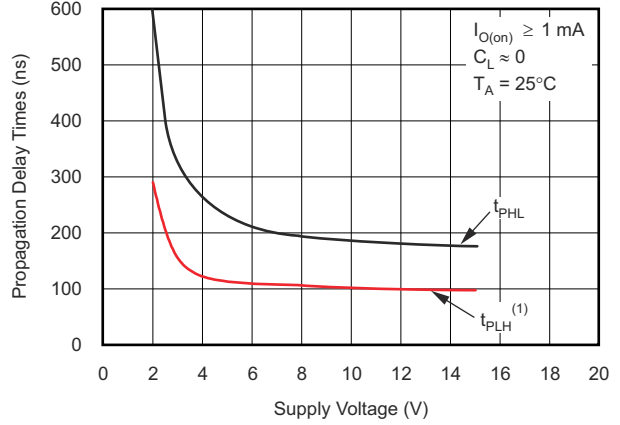


图 5-1. Discharge Switch On-State Resistance vs Free-Air Temperature



(1) The effects of the load resistance on these values must be taken into account separately.

图 5-2. Propagation Delay Times to Discharge Output From Trigger and Threshold Shorted Together vs Supply Voltage

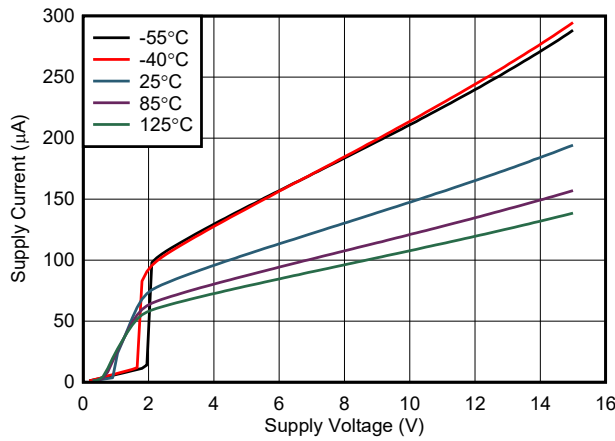


图 5-3. Supply Current vs Supply Voltage, Unit 1

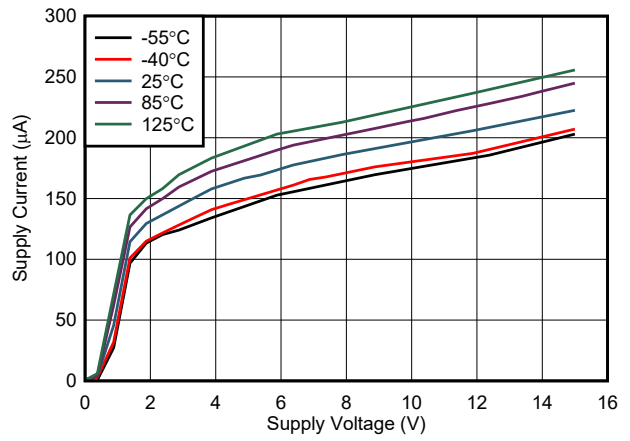


图 5-4. Supply Current vs Supply Voltage, Unit 2

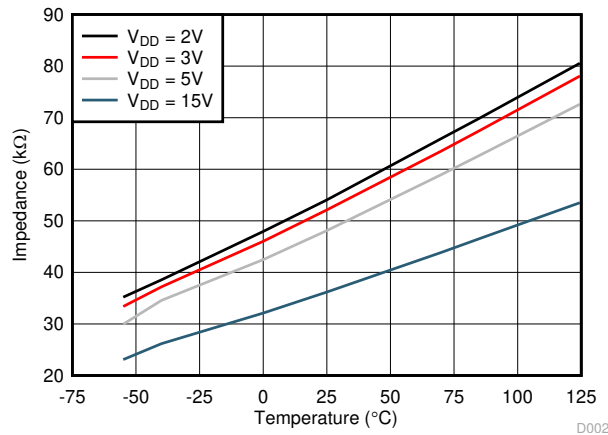


图 5-5. Control Impedance vs Temperature

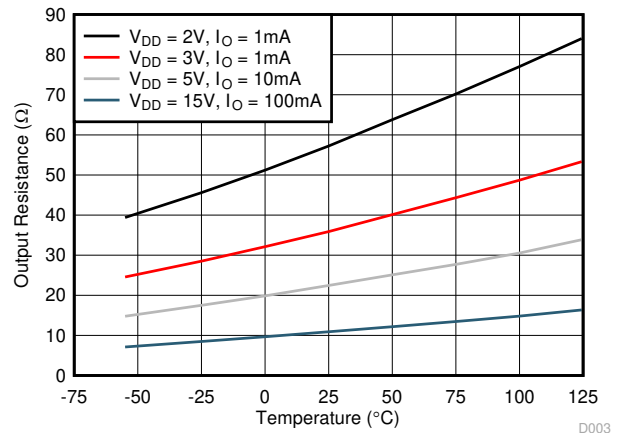
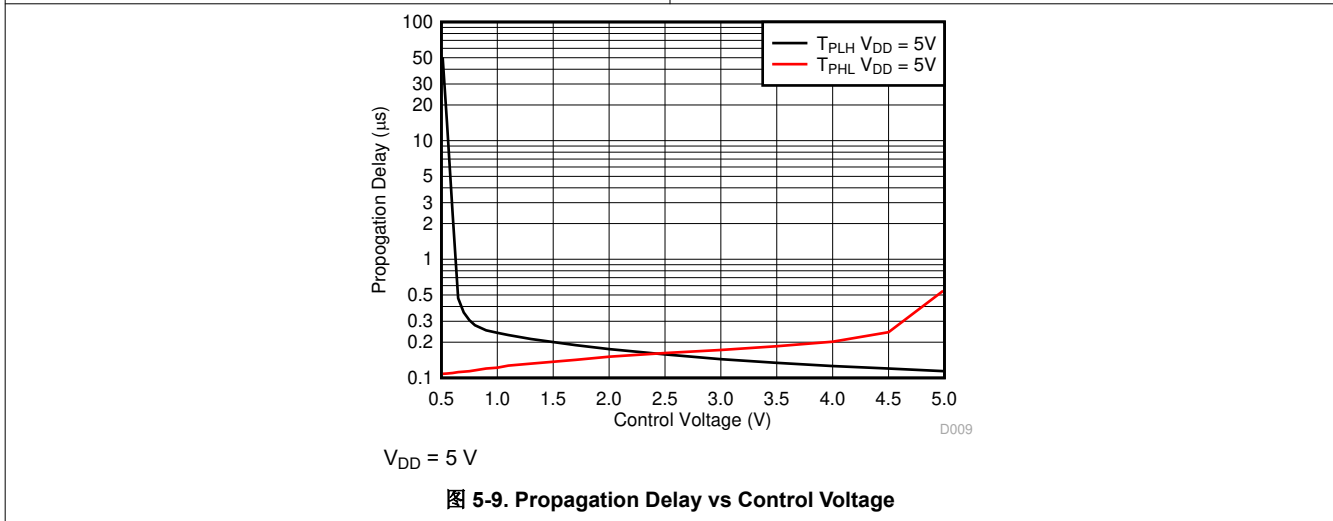
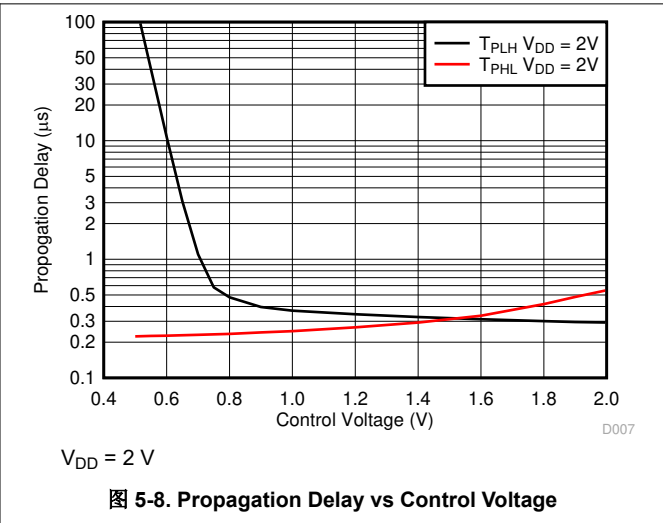
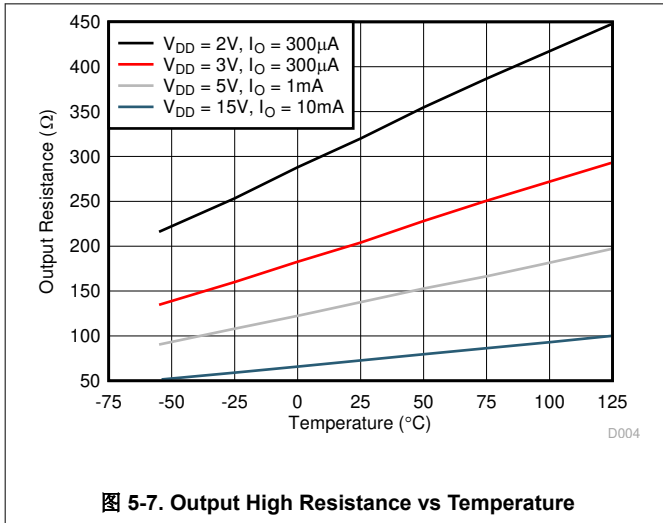


图 5-6. Output Low Resistance vs Temperature

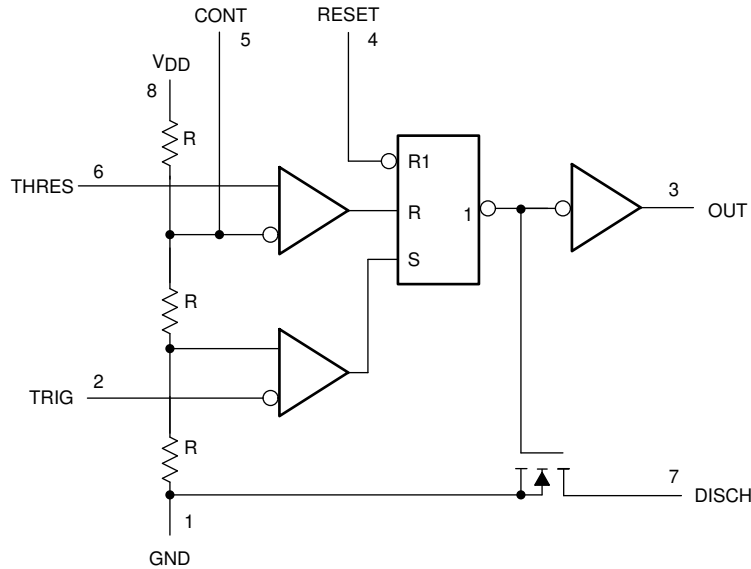
5.9 Typical Characteristics (continued)



6 Detailed Description

6.1 Overview

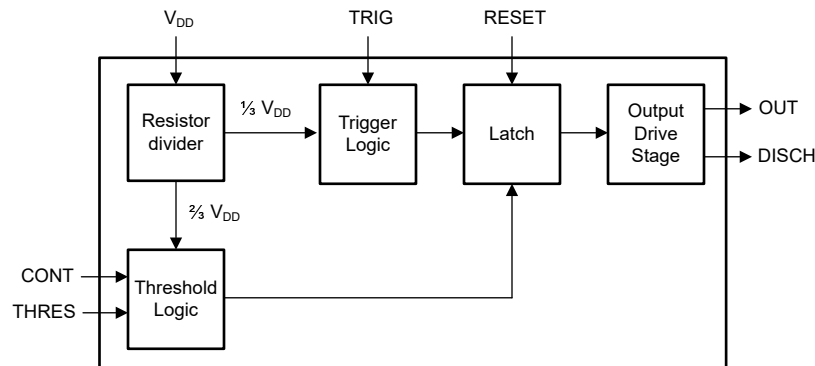
The TLC555 is a precision timing device used for general-purpose timing applications up to 2.1 MHz. All inputs are level sensitive, not edge-triggered inputs.



Pin numbers are for all packages except PW and FK. RESET overrides TRIG, which overrides THRES (when CONT pin is $2/3 V_{DD}$). The resistance of R resistors vary with V_{DD} and temperature. The resistors match each other very well across V_{DD} and temperature for a temperature-stable control-voltage ratio.

图 6-1. Simplified Schematic

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, 图 6-2 shows how any of these timers can be connected. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low, which quickly discharges capacitor C.

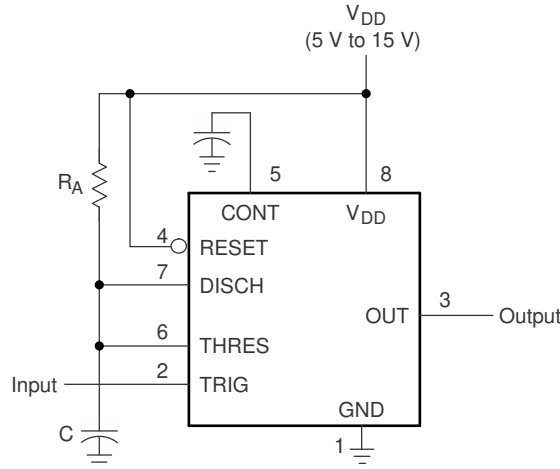


图 6-2. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage is less than the trigger threshold. If initiated, the sequence ends only if TRIG is high for at least 1 μ s before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 1 μ s, which limits the minimum monostable pulse duration to 1 μ s. The output pulse duration is approximately $t_w = 1.1 \times R_A C$. 图 6-4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{DD} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not asserted low, RESET must be connected to V_{DD} . If the RESET function is required and the pin is driven by external logic or a microcontroller, use a pullup resistor to V_{DD} (such as 10 k Ω) to prevent the RESET pin from floating. If the RESET function is not required, short the RESET pin directly to the V_{DD} pin.

In monostable applications, set the trip point of the trigger input by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage, from a resistor divider with at least 500- μ A bias, provides good results.

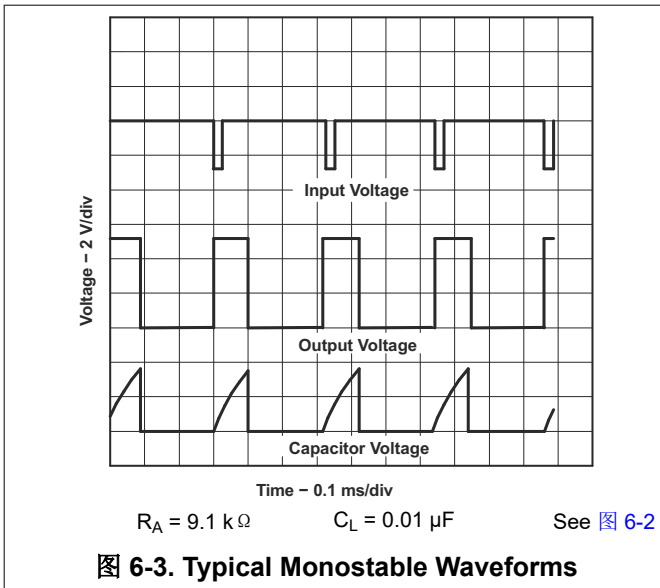


图 6-3. Typical Monostable Waveforms

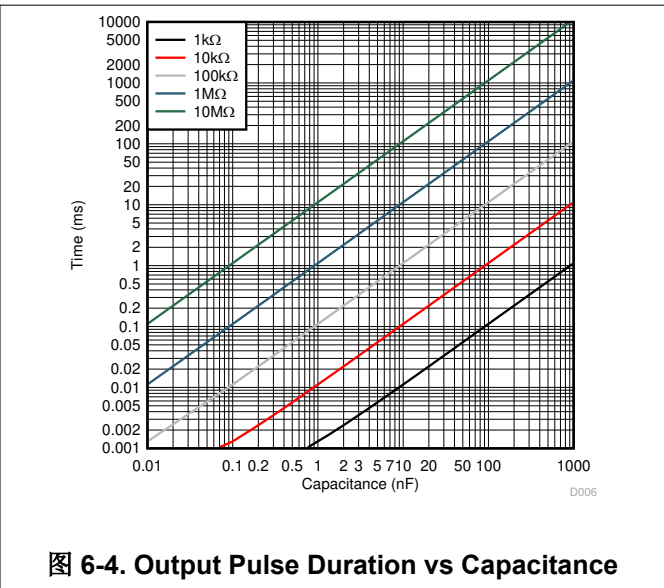


图 6-4. Output Pulse Duration vs Capacitance

6.3.2 Astable Operation

As shown in [图 6-5](#), adding a second resistor, R_B , to the circuit of [图 6-2](#) and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

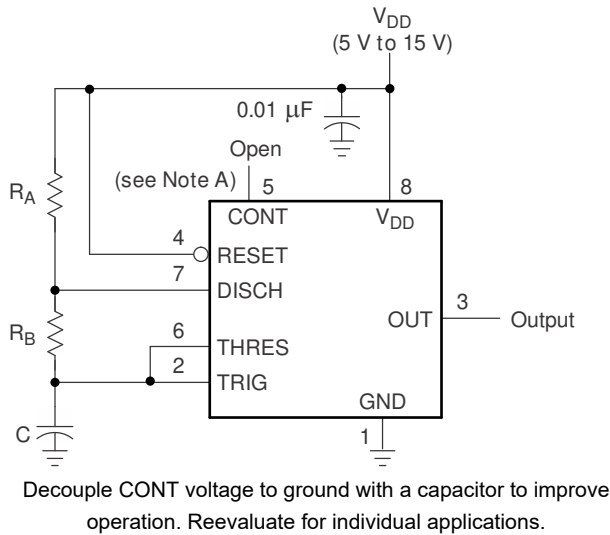


图 6-5. Circuit for Astable Operation

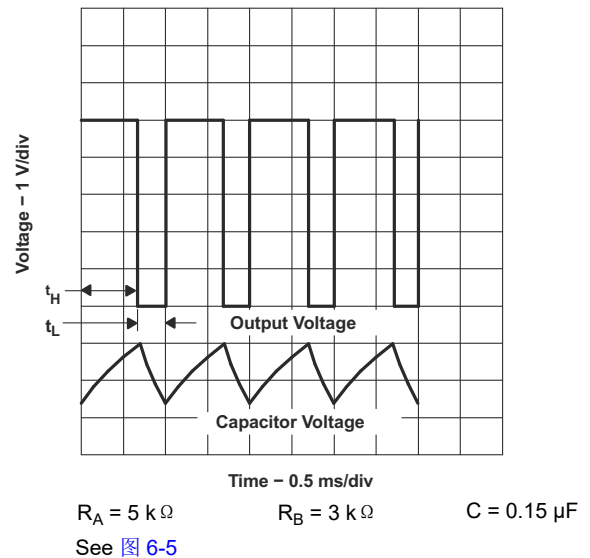


图 6-6. Typical Astable Waveforms

[图 6-6](#) shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L for frequencies below 100 kHz can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

方程式 1 到 方程式 7 并不考虑从 TRIG 和 THRES 输入到 DISCH 输出的任何传播延迟时间。这些延迟时间直接添加到周期并给电容器充电，这造成了计算值和实际值之间的差异，且随着频率的增加而增加。此外，放电期间的内部导通电阻 r_{on} 添加到 R_B 中，为计算提供了另一个时间误差源，当 R_B 非常低时。以下方程提供了与测量值更好的吻合。方程式 8 中的公式代表了在更高频率（超过 100 kHz）使用时，因为传播延迟和放电电阻被添加到公式中，实际的低时间和高时间。 C_T 的值包括标称或故意定时电容，以及 PCB 上的寄生电容。CONT 上的去耦电容也会影响占空比，其误差贡献取决于电容器的漏电阻。对于进一步讨论，请参阅 [Design low-duty-cycle timer circuits article](#)。

$$t_{c(H)} = C_T (R_A + R_B) \ln \left[3 - \exp \left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PLH}$$

$$t_{c(L)} = C_T (R_B + r_{on}) \ln \left[3 - \exp \left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PHL} \tag{8}$$

这些方程和之前给出的方程类似，因为它们都涉及将时间常数乘以对数项。对数项的极限值必须在低频时为 $\ln(2)$ ，在极高频时为 $\ln(3)$ 。对于接近 50% 占空比的占空比，适当的对数项常数可以代入，结果良好。占空比小于 50% 的输出波形要求 $t_{c(H)} / t_{c(L)} < 1$ ，且可能 $R_A \leq r_{on}$ 。这些条件可能难以实现。图 6-8 显示了与各种 C_T 和 $R_A + 2 \times R_B$ 组合相关的标称自由运行频率。

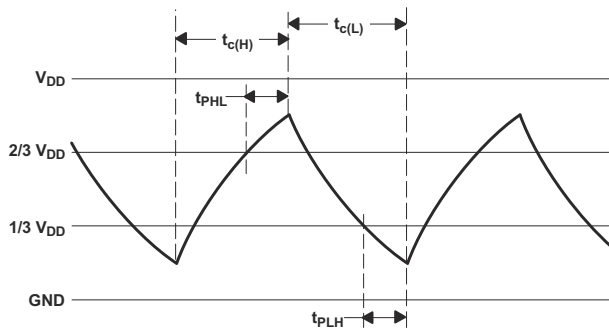


图 6-7. Trigger and Threshold Voltage Waveform

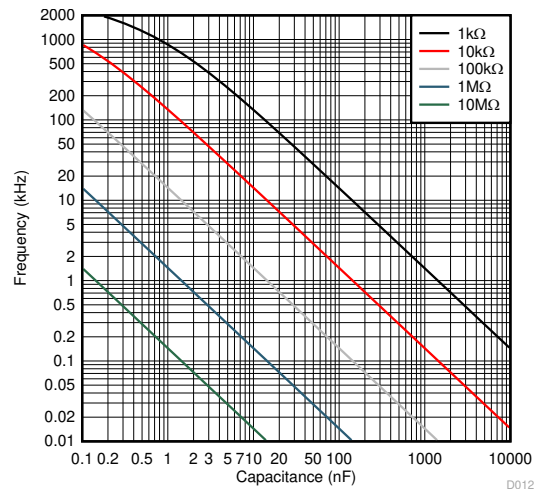


图 6-8. Nominal Free-Running Frequency vs Timing Capacitance
Resistance = $R_A + 2 \times R_B$

6.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of 图 6-2 can be made to operate as a frequency divider. 图 6-9 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

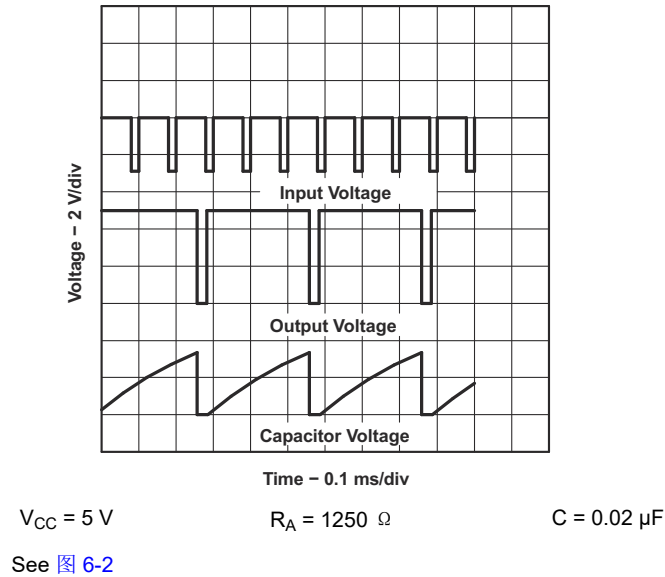


图 6-9. Divide-by-Three Circuit Waveforms

6.4 Device Functional Modes

表 6-1 shows the device truth table. For a valid reset voltage condition, use an external pullup resistor to V_{DD} (if using the RESET functionality), or short the RESET pin directly to V_{DD} (if the RESET functionality is not used).

表 6-1. Function Table

| RESET VOLTAGE ⁽¹⁾ | TRIGGER VOLTAGE ⁽¹⁾ | THRESHOLD VOLTAGE ⁽¹⁾ | OUTPUT | DISCHARGE SWITCH |
|------------------------------|--------------------------------|----------------------------------|---------------------------|------------------|
| < MIN | Irrelevant | Irrelevant | L | On |
| > MAX | < MIN | Irrelevant ⁽²⁾ | H | Off |
| > MAX | > MAX | > MAX | L | On |
| > MAX | > MAX | < MIN | As previously established | |

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under 节 5.6.
 (2) CONT pin open or $2/3 V_{DD}$.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TLC555 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. 节 7.2 presents a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in 图 7-1 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in 图 7-2.

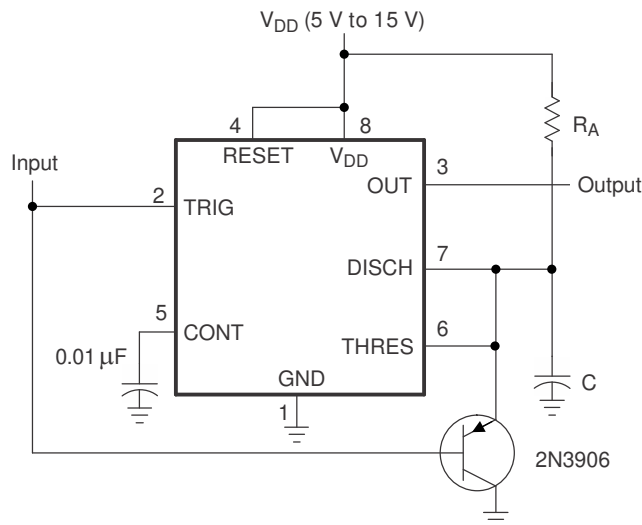


图 7-1. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. An input stuck low cannot be detected because the timing capacitor (C) remains discharged.

7.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [\text{maximum normal input high time}]$.

7.2.1.3 Application Curve

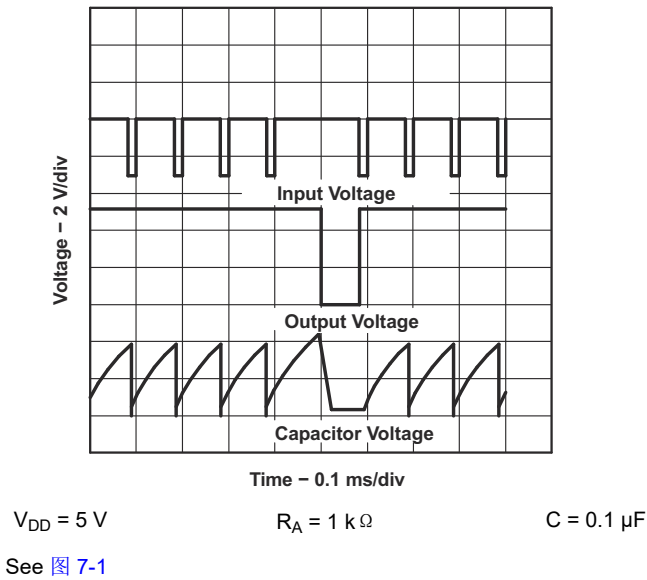
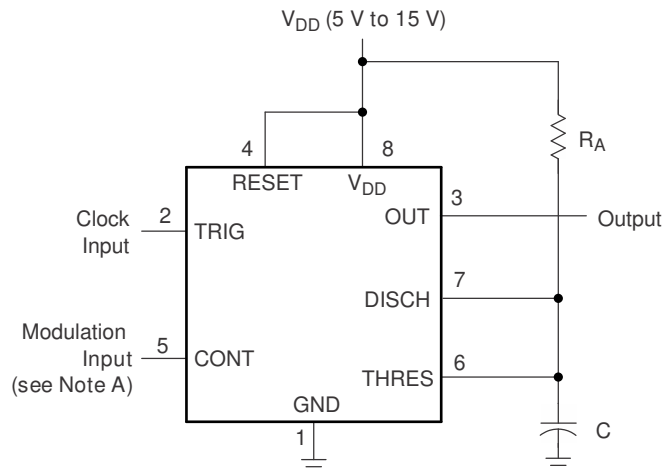


图 7-2. Timing Waveforms for Missing-Pulse Detector

7.2.2 Pulse-Width Modulation

To modify timer operation, apply an external voltage (or current) to CONT to modulate the internal threshold and trigger voltages. [图 7-3](#) shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. [图 7-4](#) shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle can result in inconsistent output pulses. Attempting to run close to 100% duty cycle results in frequency division by 2, then 3, then 4.



- A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

图 7-3. Circuit for Pulse-Width Modulation

7.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than $1/3 V_{DD}$, respectively. Clock input V_{OL} time must be less than minimum output high time; therefore, a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1 V. Lower CONT voltage can greatly increase threshold comparator propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC-based with an negative exponential curve.

7.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C$ is same or less than clock input period. 图 7-4 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

7.2.2.3 Application Curve

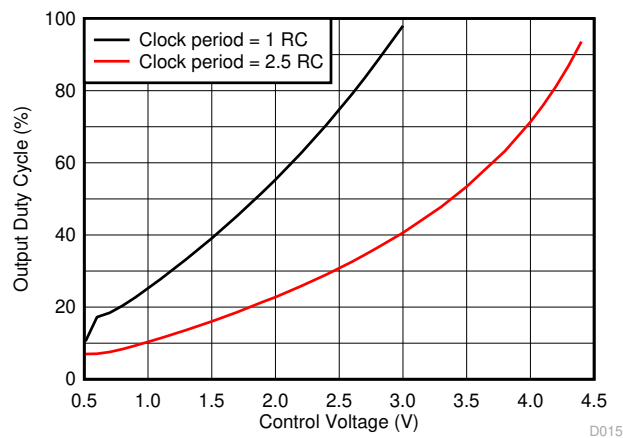
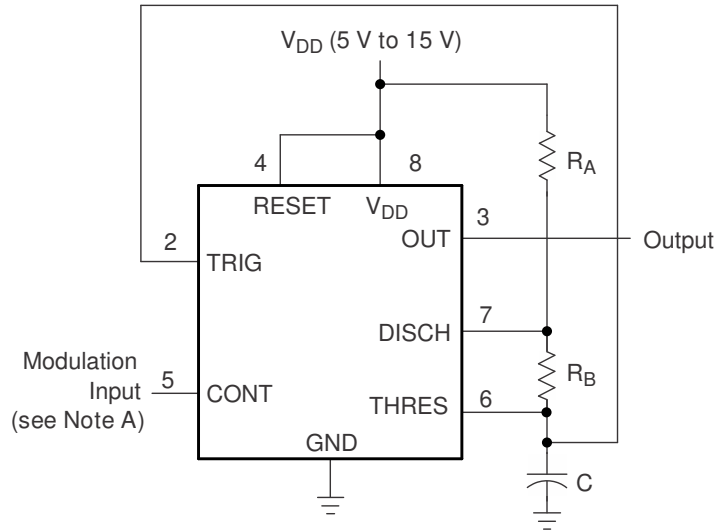


图 7-4. Pulse-Width-Modulation vs Control Voltage
Clock Duty Cycle 98%, $V_{DD} = 5 V$

7.2.3 Pulse-Position Modulation

As shown in 图 7-5, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. 图 7-6 and 图 7-7 shows the output frequency and duty cycle versus control voltage.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

$$R_A = 3 \text{ k}\Omega$$

$$R_B = 309 \text{ k}\Omega$$

$$C = 1 \text{ nF}$$

图 7-5. Circuit for Pulse-Position Modulation

7.2.3.1 Design Requirements

Both dc- and ac-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage less than 1 V can result in output glitches instead of a steady-output pulse stream

7.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of V_{DD} can be determined using formulas in 节 6.3.2 section.

7.2.3.3 Application Curves

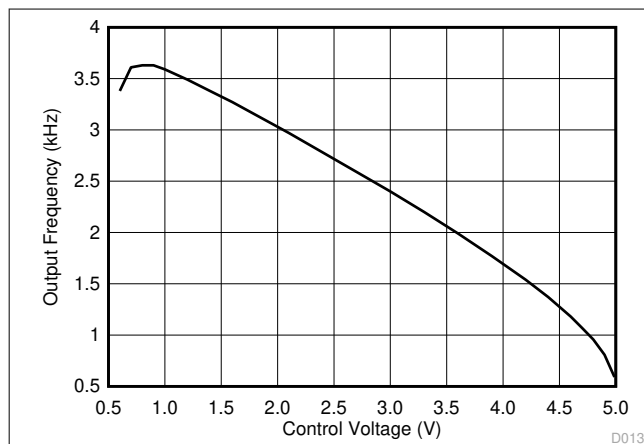


图 7-6. Pulse-Position-Modulation Frequency vs Control Voltage, $V_{DD} = 5 \text{ V}$

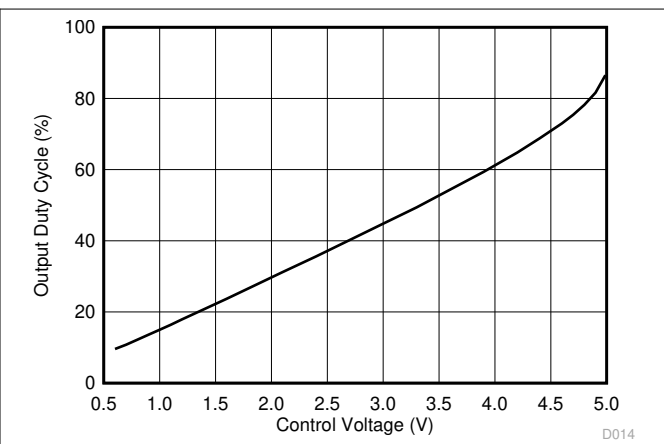
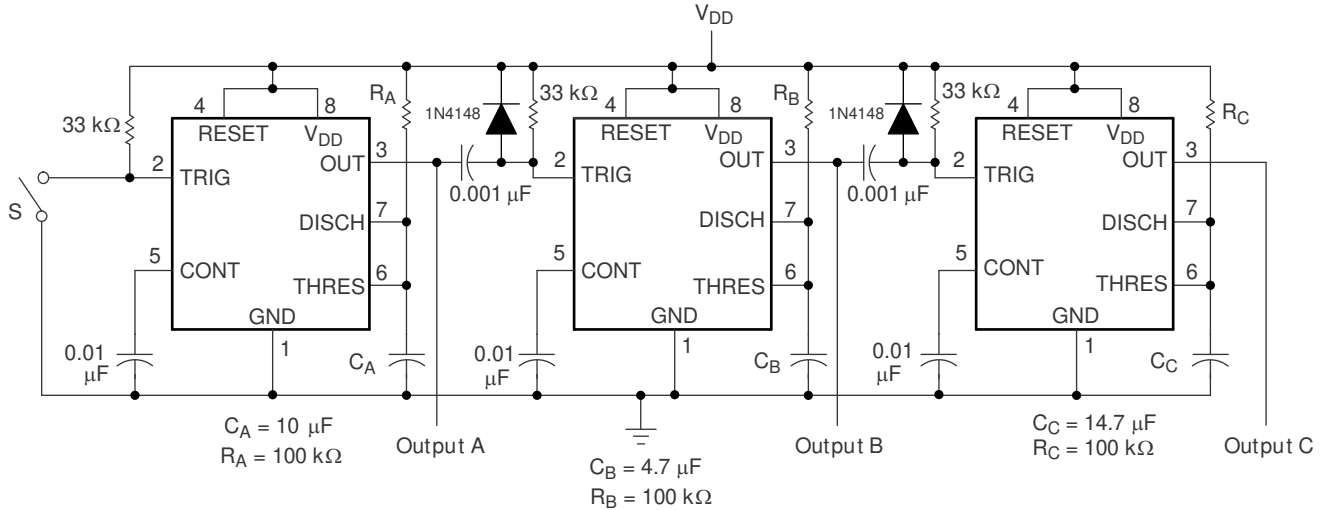


图 7-7. Pulse-Position-Modulation Duty Cycle vs Control Voltage, $V_{DD} = 5 \text{ V}$

7.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. 图 7-8 shows a sequencer circuit with possible applications in many systems, and 图 7-9 shows the output waveforms.



S closes momentarily at $t = 0$.

图 7-8. Sequential Timer Circuit

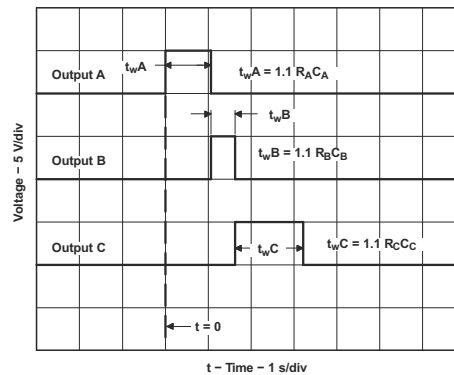
7.2.4.1 Design Requirements

The sequential-timer application chains together multiple monostable timers. The joining components are the 33-kΩ resistors and 0.001-μF capacitors. The output high-to-low edge passes a 10-μs start pulse to the next monostable. A diode is required to prevent overvoltage on the trigger input when on the previous output low-to-high edge.

7.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula: $t_w = 1.1 \times R \times C$.

7.2.4.3 Application Curve



See 图 7-8

图 7-9. Sequential Timer Waveforms

7.3 Power Supply Recommendations

The TLC555 requires a voltage supply greater than or equal to 2 V, 3 V, or 5 V based the coldest ambient temperature supported and a supply voltage less than or equal to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry and provide stable output pulses. Minimum recommended is 0.1- μ F ceramic in parallel with 1- μ F electrolytic. Place the bypass capacitors as close as possible to the TLC555 and minimize the trace length.

7.4 Layout

7.4.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555. The 0.1- μ F ceramic capacitor in parallel with a 1- μ F electrolytic capacitor must be as close as possible to the TLC555. The capacitor used for the time delay must also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

图 7-11 is the basic layout for various applications.

- C1—based on time delay calculations
- C2—0.01- μ F bypass capacitor for control voltage pin
- C3—0.1- μ F bypass ceramic capacitor
- C4—1- μ F electrolytic bypass capacitor
- R1—based on time-delay calculations

7.4.2 Layout Example

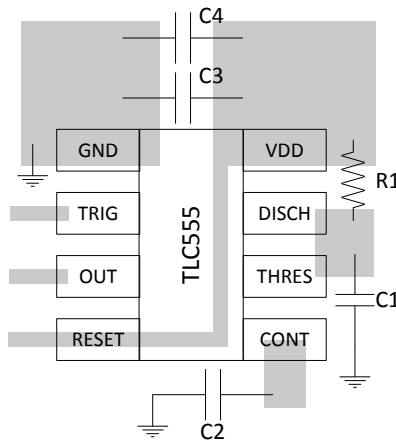


图 7-11. Layout Example

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.3 Trademarks

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (July 2019) to Revision J (November 2023) | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • 将 <i>特性</i> 中的 ESD 保护规格从 MIL-STD-883C 方法 3015.2 规定的 2000V 更改为 ANSI/ESDA/JEDEC JS-001 规定的 1000V..... | 1 |
| • 将 <i>说明</i> 部分中的 <i>器件信息</i> 表更改为 <i>封装信息</i> ，并将 <i>封装尺寸 (标称值)</i> 更改为 <i>封装尺寸</i> | 1 |
| • Added <i>ESD Ratings</i> table and HBM, CDM, and MM specifications..... | 5 |
| • Changed thermal resistance and characterization parameter values for SOIC and PDIP packages in <i>Thermal Information</i> table..... | 6 |
| • Changed reset current (I_{RESET}) test conditions to $V_{\text{RESET}} = V_{\text{DD}}$, in <i>Electrical Characteristics: $V_{\text{DD}} = 5 \text{ V}$</i> and <i>Electrical Characteristics: $V_{\text{DD}} = 15 \text{ V}$</i> | 7 |
| • Added new reset current (I_{RESET}) typical specification, for test condition $V_{\text{RESET}} = 0 \text{ V}$, to <i>Electrical Characteristics: $V_{\text{DD}} = 5 \text{ V}$</i> and <i>Electrical Characteristics: $V_{\text{DD}} = 15 \text{ V}$</i> | 7 |
| • Changed supply current (I_{DD}) typical value from 170 μA to 180 μA in <i>Electrical Characteristics: $V_{\text{DD}} = 5 \text{ V}$</i> . | 7 |
| • Changed title of <i>Operating Characteristics</i> section to <i>Timing Characteristics</i> and clarified that values are specified by design or characterization..... | 10 |
| • Deleted Initial error of timing interval specification in <i>Timing Characteristics</i> | 10 |
| • Added Figure 5-4, <i>Supply Current vs Supply Voltage, Unit 2</i> | 11 |
| • Changed Figure 5-3, <i>Supply Current vs Supply Voltage</i> , to add "Unit 1" to title, and deleted 0°C and 70°C curves..... | 11 |
| • Changed functional block diagram to simplified schematic and moved to <i>Overview</i> | 13 |
| • Updated <i>Functional Block Diagram</i> | 13 |
| • Added guidance for RESET pin pullup resistance and CONT pin voltage range to <i>Monostable Operation</i> ... | 13 |
| • Added clarity regarding nominal operating frequency and parasitic terms in <i>Astable Operation</i> | 15 |
| • Deleted link to deprecated TLC555 Design Calculator in <i>Astable Operation</i> | 15 |

- Deleted Figure 17, *Equivalent Schematic*, and added guidance concerning the RESET pin in *Device Functional Modes* 17

Changes from Revision H (August 2016) to Revision I (July 2019) Page

- Added MIN value for input voltage in *Absolute Maximum Ratings* 5
- Added discharge pin in *Absolute Maximum Ratings* 5
- Changed MIN supply voltage based on part number in *Recommended Operating Conditions* 5
- Added power dissipation capacitance TYP value in *Electrical Characteristics: $V_{DD} = 2\text{ V}$ for TLC555C, $V_{DD} = 3\text{ V}$ for TLC555I* 6
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: $V_{DD} = 5\text{ V}$* 7
- Changed V_{OH} test condition current to -1 mA in *Electrical Characteristics: $V_{DD} = 5\text{ V}$* 7
- Added power dissipation capacitance TYP value in *Electrical Characteristics: $V_{DD} = 5\text{ V}$* 7
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: $V_{DD} = 15\text{ V}$* 9
- Added power dissipation capacitance TYP value in *Electrical Characteristics: $V_{DD} = 15\text{ V}$* 9
- Added *Operating Characteristics* to the *Specifications* section 10
- Added Supply Current vs Supply Voltage chart to the *Typical Characteristics* section 11
- Added Control Impedance vs Temperature chart to the *Typical Characteristics* section 11
- Added Output Low Resistance vs Temperature chart to the *Typical Characteristics* section 11
- Added Output High Resistance vs Temperature chart to the *Typical Characteristics* section 11
- Added Propagation Delay vs Control Voltage chart, $V_{DD} = 2\text{ V}$ to the *Typical Characteristics* section 11
- Added Propagation Delay vs Control Voltage chart, $V_{DD} = 5\text{ V}$ to the *Typical Characteristics* section 11
- Changed trigger high hold time to $1\text{ }\mu\text{s}$ in *Monostable Operation* 13
- Changed minimum monostable pulse width to $1\text{ }\mu\text{s}$ in *Monostable Operation* 13
- Changed Output Pulse Duration vs Capacitance chart scale down to 0.001 ms in *Monostable Operation* 13
- Added more astable frequency formulas to the *Astable Operation* section 15
- Changed scale on Free-Running Frequency vs Timing Capacitance chart up to 2 MHz in the *Astable Operation* section 15
- Added CONT pin table note to the Table 6-1, *Function Table* in the *Device Functional Modes* 17
- Changed the application curve chart in the *Pulse-Width Modulation* section 20
- Changed the application curve charts in the *Pulse-Position Modulation* section 21
- Added clamping diodes to Sequential Timer Circuit in the *Sequential Timer* section 22
- Added *Designing for Improved ESD Performance* section to the *Application Information* section 23

Changes from Revision G (November 2008) to Revision H (August 2016) Page

- 添加了特性说明部分、器件功能模式、应用和实现部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 1
- Changed values in the *Thermal Information* table to align with JEDEC standards 6
- Deleted *Dissipation Ratings* table 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TLC555CD | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | 0 to 70 | TL555C | |
| TLC555CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL555C | Samples |
| TLC555CP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TLC555CP | Samples |
| TLC555CPS | ACTIVE | SO | PS | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P555 | Samples |
| TLC555CPSR | ACTIVE | SO | PS | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P555 | Samples |
| TLC555CPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P555 | Samples |
| TLC555CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P555 | Samples |
| TLC555ID | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | TL555I | |
| TLC555IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL555I | Samples |
| TLC555IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TLC555IP | Samples |
| TLC555QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL555Q | Samples |
| TLC555QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TL555Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC555 :

- Automotive : [TLC555-Q1](#)
- Military : [TLC555M](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC555CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC555CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TLC555CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC555IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC555QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC555QDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC555CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC555CPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| TLC555CPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLC555IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC555QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC555QDRG4 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TLC555CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLC555CD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLC555CDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLC555CDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLC555CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TLC555CPS | PS | SOP | 8 | 80 | 530 | 10.5 | 4000 | 4.1 |
| TLC555CPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLC555ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLC555ID | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLC555IDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLC555IDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLC555IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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