单路差分比较器

查询样品: TL331-EP

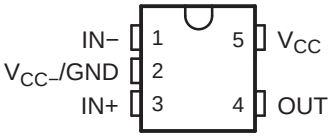
特性

- 单电源或双电源
- 宽电源电压范围：**2V** 至 **36V**
- 独立于电源电压的低电源电流漏极：**0.4mA**（典型值）
- 低输入偏置电流：**25nA**（典型值）
- 低输入偏移电压：**2mV**（典型值）
- 共模输入电压范围包括接地
- 差分输入电压范围等于最大额定电源电压：**±36V**
- 低输出饱和电压
- 输出与 **TTL**，**MOS** 和 **CMOS** 兼容

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

DBV PACKAGE
(TOP VIEW)



说明/订购信息

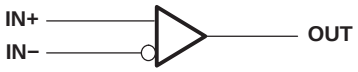
这个器件包含一个单电压比较器，此比较器被设计成在宽范围电压上由一个单电源供电运行。 如果两个电源之间的电压差在 2V 和 36V 之间且 V_{CC}比输入共模电压的正值至少高 1.5V，也可使用双电源供电运行。 电流漏极与电源电压无关。 为了实现线与关系，用户可将输出连接至另外一个集电极开路输出。

ORDERING INFORMATION(1)

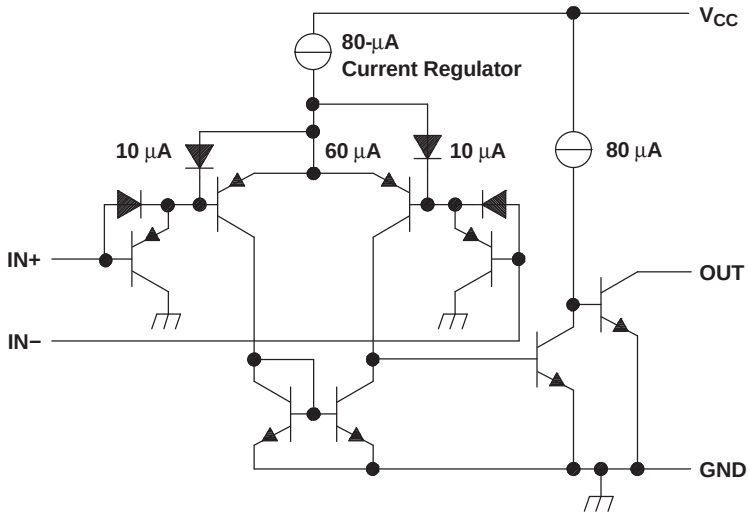
T_A	$V_{IO(MAX)}$ at 25°C	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	5 mV	SOT-23 (DBV)	Reel of 3000	TL331MDBVREP	TEPU	V62/13611-01XE
			Reel of 250	TL331MDBVTEP		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM



SCHEMATIC



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Note: Current values shown are nominal.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage(2)	36 V
V_{ID}	Differential input voltage(3)	±36 V
V_I	Input voltage range (either input)	–0.3 V to 36 V
V_O	Output voltage	36 V
I_O	Output current	20 mA
	Duration of output short-circuit to ground(4)	Unlimited
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

THERMAL INFORMATION

THERMAL METRIC(1)		TL331-EP DBV 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	299	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	65.4	
θ_{JB}	Junction-to-board thermal resistance(4)	97.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	95.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
			–55°C to 125°C			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			–55°C to 125°C			250	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–25	–250	nA
			–55°C to 125°C			–400	
V_{ICR}	Common-mode input voltage range(2)		25°C	0 to V_{CC} – 1.5			V
			–55°C to 125°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}	25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V, V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = 30 V, V_{ID} = 1 V	–55°C to 125°C			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, V_{ID} = –1 V	25°C		150	400	mV
			–55°C to 125°C			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V, V_{ID} = –1 V	25°C	6			mA
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 5 V	25°C		0.4	0.7	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either or both inputs can go to 30 V without damage.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF(1) (2)	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL331MDBVTEP	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU
TL331MDBVTEP.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU
V62/13611-01XE	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TL331-EP :

- Catalog : TL331

- Automotive : TL331-Q1

NOTE: Qualified Version Definitions:

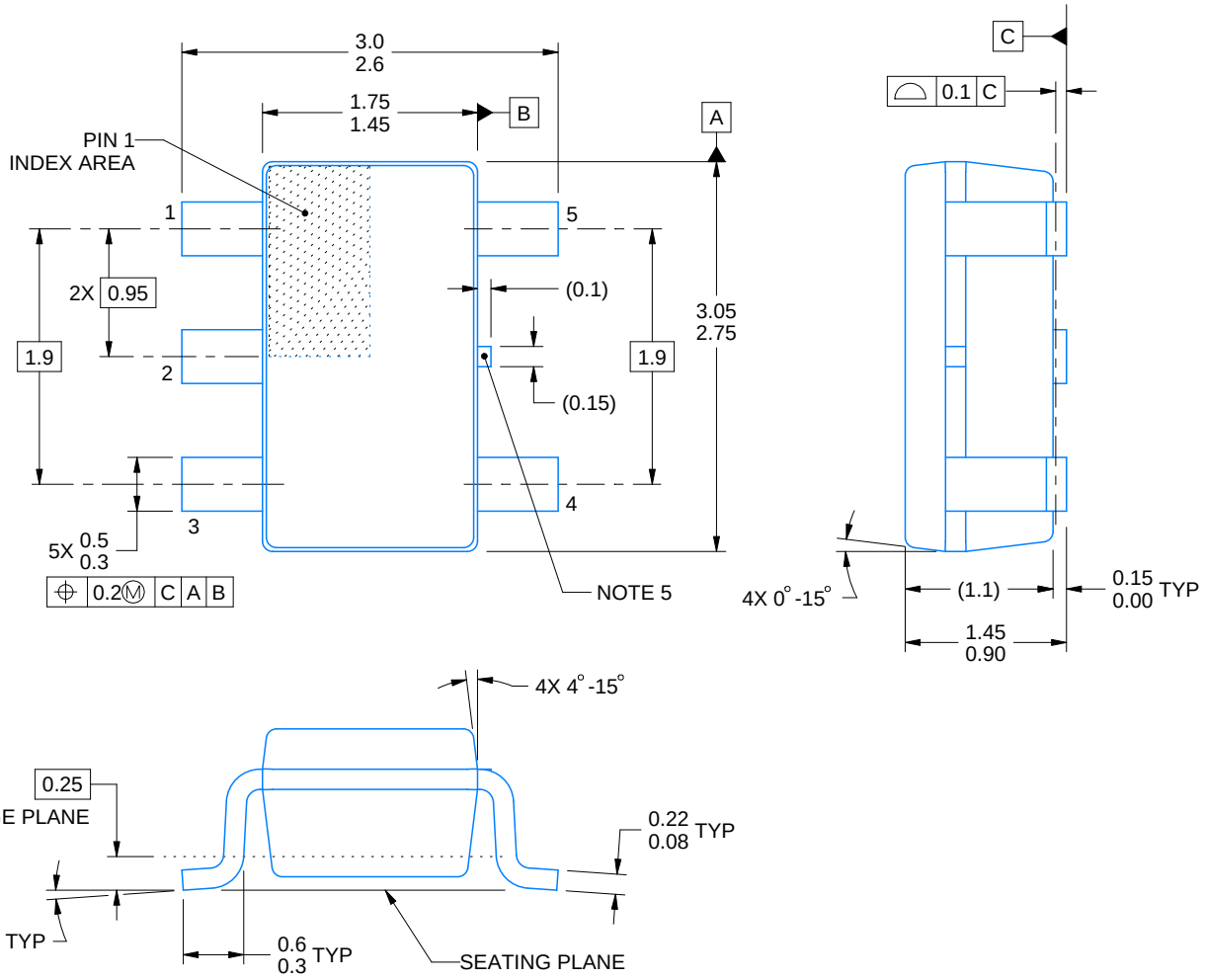
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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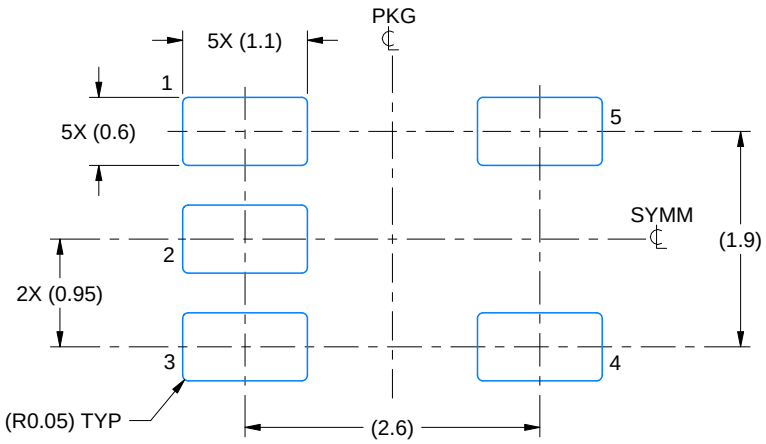
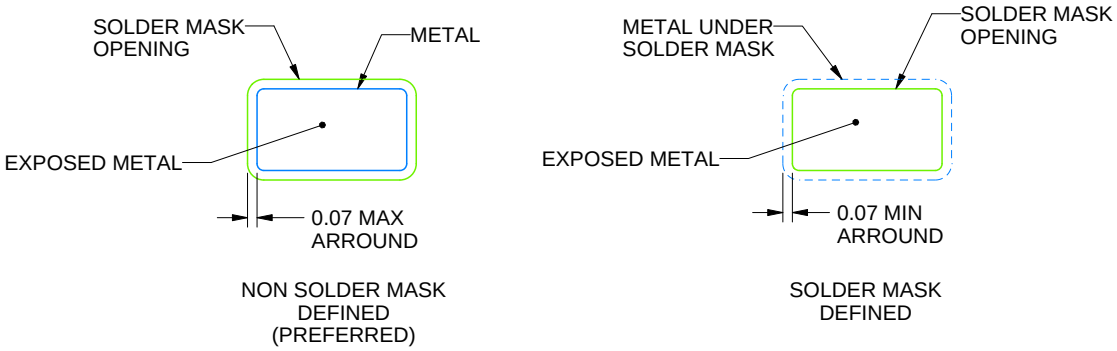
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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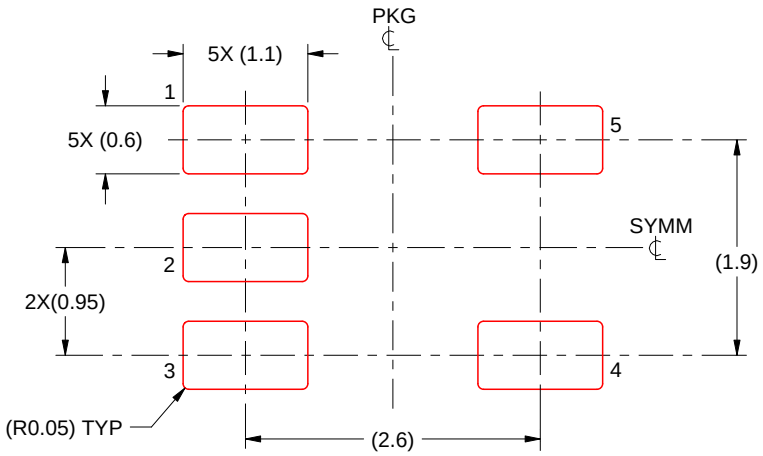
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月