

TL06xx 低功耗 JFET 输入运算放大器

1 特性

- 极低功耗
- 典型电源电流：每个放大器 200µA
- 宽共模和差分电压范围
- 低输入偏置和失调电流
- 共模输入电压范围包括 V_{CC+}
- 输出短路保护
- 高输入阻抗：JFET 输入级
- 内部频率补偿
- 无闩锁操作
- 高压摆率：3.5 V/µs (典型值)
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 平板电脑
- 白色家电
- 个人电子产品
- 计算机

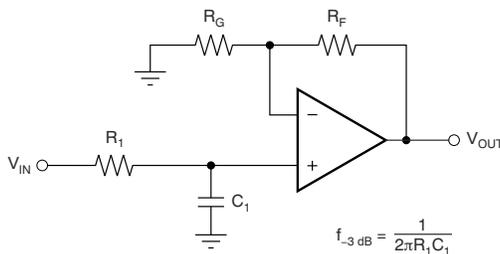
3 说明

TL06x (TL061、TL062 和 TL064) 系列业界通用运算放大器以较低功耗镜像 TL07x 和 TL08x 系列运算放大器。这些器件为成本敏感型应用提供了卓越的价值，具有高输入阻抗、宽带宽、高压摆率以及低输入失调电压和输入偏置电流。高 ESD (1.5kV, HBM)、集成 EMI 和射频滤波器以及宽工作温度范围可支持将 TL06x 器件用于条件严苛、环境严苛的应用。

器件信息

| 器件型号 | 通道数 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ |
|--------|-----|-------------------|---------------------|
| TL061x | 单通道 | D (SOIC, 8) | 4.90mm × 6.00mm |
| | | P (PDIP, 8) | 9.59 mm × 7.94 mm |
| | | PS (SO, 8) | 6.20 mm × 7.80 mm |
| TL062x | 双通道 | D (SOIC, 8) | 4.90mm × 6.00mm |
| | | P (PDIP, 8) | 9.59 mm × 7.94 mm |
| | | PS (SO, 8) | 6.20 mm × 7.80 mm |
| | | JG (CDIP, 8) | 9.58 mm × 7.62 mm |
| | | PW (TSSOP, 8) | 3.00mm × 6.40mm |
| | | FK (LCCC, 20) | 8.89 mm × 8.80 mm |
| TL064x | 四通道 | D (SOIC, 14) | 8.65mm × 6.00mm |
| | | J (CDIP, 14) | 19.4 mm × 7.90 mm |
| | | N (PDIP, 14) | 19.31 mm × 7.94 mm |
| | | NS (SO, 14) | 10.20 mm × 7.80 mm |
| | | PW (TSSOP, 14) | 5.00mm × 6.40mm |
| | | W (CFP, 14) | 21.78 mm × 9.21 mm |
| | | FK (LCCC, 20) | 8.89 mm × 8.80 mm |

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G} \right) \left(\frac{1}{1 + sR_1C_1} \right)$$

单极低通滤波器



Table of Contents

| | | | |
|--|----|--|----|
| 1 特性 | 1 | 8 Detailed Description | 15 |
| 2 应用 | 1 | 8.1 Overview..... | 15 |
| 3 说明 | 1 | 8.2 Functional Block Diagram..... | 15 |
| 4 Revision History | 2 | 8.3 Feature Description..... | 15 |
| 5 Pin Configuration and Functions | 4 | 8.4 Device Functional Modes..... | 15 |
| 6 Specifications | 6 | 9 Applications and Implementation | 16 |
| 6.1 Absolute Maximum Ratings..... | 6 | 9.1 Application Information..... | 16 |
| 6.2 ESD Ratings..... | 6 | 9.2 Typical Applications..... | 16 |
| 6.3 Recommended Operating Conditions..... | 6 | 9.3 System Examples..... | 17 |
| 6.4 Thermal Information (TL061)..... | 7 | 9.4 Power Supply Recommendations..... | 19 |
| 6.5 Thermal Information (TL062)..... | 7 | 9.5 Layout..... | 20 |
| 6.6 Thermal Information (TL064)..... | 7 | 10 Device and Documentation Support | 21 |
| 6.7 Electrical Characteristics for TL06xC and TL06xxC..... | 8 | 10.1 Documentation Support..... | 21 |
| 6.8 Electrical Characteristics for TL06xxC and TL06xl..... | 9 | 10.2 支持资源..... | 21 |
| 6.9 Electrical Characteristics for TL06xM..... | 10 | 10.3 Trademarks..... | 21 |
| 6.10 Operating Characteristics..... | 10 | 10.4 静电放电警告..... | 21 |
| Typical Characteristics..... | 11 | 10.5 术语表..... | 21 |
| 7 Parameter Measurement Information | 14 | 11 Mechanical, Packaging, and Orderable Information | 21 |

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision M (June 2023) to Revision N (August 2023) | Page |
|--|------|
| • Added typical specification for Unity-Gain Bandwidth in <i>Electrical Characteristics for TL06xM</i> | 10 |
| • Changed Equivalent Input Noise Voltage vs Frequency curve in <i>Typical Characteristics</i> section..... | 11 |

| Changes from Revision L (May 2015) to Revision M (June 2023) | Page |
|--|------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式..... | 1 |
| • 更新了 <i>器件信息</i> 中的封装尺寸和通道数，并根据通道数重新排列了封装..... | 1 |
| • Updated TL061 pinout diagram in <i>Pin Configuration and Functions</i> | 4 |
| • Changed Charged Device Model (CDM) ESD from 2 kV to 1.5 kV in <i>ESD Ratings</i> | 6 |
| • Added table note for input bias current and input offset current on <i>Electrical Characteristics for TL06xC and TL06xxC</i> | 8 |
| • Added table note for input bias current and input offset current on <i>Electrical Characteristics for TL06xxC and TL06xl</i> | 9 |
| • Changed name of <i>Electrical Characteristics for TL06xM and TL064M</i> to <i>Electrical Characteristics for TL06xM</i> | 10 |
| • Added table note for input bias current and input offset current on <i>Electrical Characteristics for TL06xM</i> | 10 |
| • Changed typical input voltage noise density at 1 kHz from $42 \text{ nV}/\sqrt{\text{Hz}}$ to $30 \text{ nV}/\sqrt{\text{Hz}}$ | 10 |
| • Updated description in <i>Overview</i> | 15 |
| • Updated image in <i>Functional Block Diagram</i> | 15 |

| Changes from Revision K (January 2014) to Revision L (May 2015) | Page |
|--|------|
| • 添加了 <i>应用</i> | 1 |
| • 添加了 <i>引脚配置和功能</i> 部分、 <i>ESD</i> 等级表、 <i>特性说明</i> 部分、 <i>器件功能模式</i> 、 <i>应用和实施</i> 部分、 <i>电源相关建议</i> 部分、 <i>布局</i> 部分、 <i>器件和文档支持</i> 部分以及 <i>机械、封装和可订购信息</i> 部分..... | 1 |

| Changes from Revision J (September 2004) to Revision K (January 2014) | Page |
|---|------|
| • 将文档更新为新的 TI 数据表格式 - 无规格变化..... | 1 |

- 删除了 *订购信息表*..... 1
- 更新了 *特性* 中的“军用免责声明”。..... 1

5 Pin Configuration and Functions

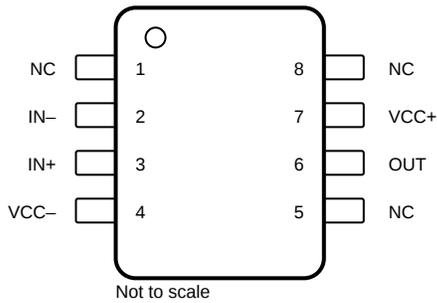


图 5-1. TL061x D, P, and PS Package, 8-Pin SOIC, PDIP, and SO (Top View)

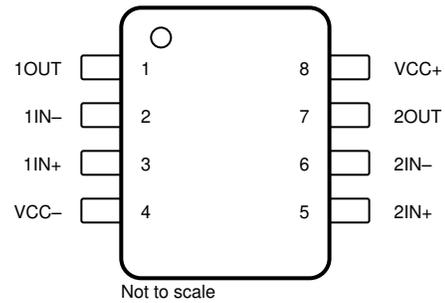


图 5-2. TL062x D, JG, P, PS, and PW Package, 8-Pin SOIC, CDIP, PDIP, SO, and TSSOP (Top View)

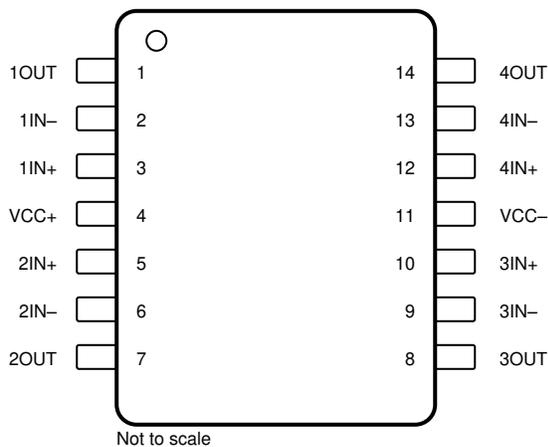


图 5-3. TL064x D, J, N, NS, PW, and W Package, 14-Pin SOIC, CDIP, PDIP, SO, TSSOP and CFP (Top View)

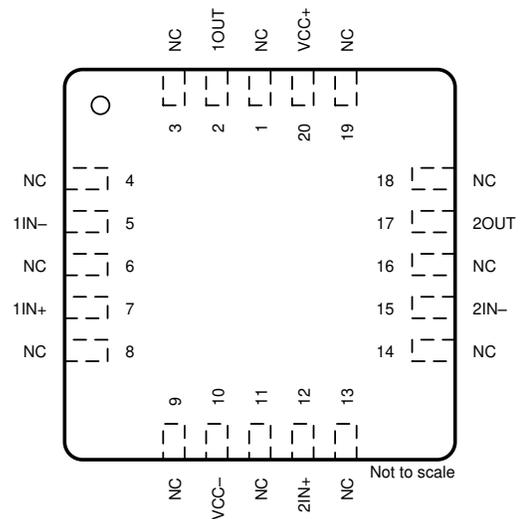


图 5-4. TL062 FK Package, 20-Pin LCCC (Top View)

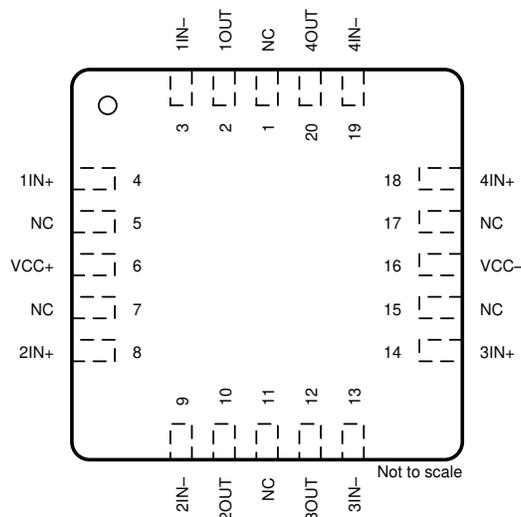


图 5-5. TL064 FK Package, 20-Pin LCCC (Top View)

表 5-1. Pin Functions

| NAME | PIN | | | | | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|----------|------------------|----|--------------------|----|---------------------|-------------------------|
| | TL061 | TL062 | | TL064 | | | |
| | D, P, PS | D, JG, P, PS, PW | FK | D, J, N, NS, PW, W | FK | | |
| 1IN - | — | 2 | 5 | 2 | 3 | I | Negative input |
| 1IN+ | — | 3 | 7 | 3 | 4 | I | Positive input |
| 1OUT | — | 1 | 2 | 1 | 2 | O | Output |
| 2IN - | — | 6 | 15 | 6 | 9 | I | Negative input |
| 2IN+ | — | 5 | 12 | 5 | 8 | I | Positive input |
| 2OUT | — | 7 | 17 | 7 | 10 | O | Output |
| 3IN - | — | — | — | 9 | 13 | I | Negative input |
| 3IN+ | — | — | — | 10 | 14 | I | Positive input |
| 3OUT | — | — | — | 8 | 12 | O | Output |
| 4IN - | — | — | — | 13 | 19 | I | Negative input |
| 4IN+ | — | — | — | 12 | 18 | I | Positive input |
| 4OUT | — | — | — | 14 | 20 | O | Output |
| IN - | 2 | — | — | — | — | I | Negative input |
| IN+ | 3 | — | — | — | — | I | Positive input |
| NC | 8 | — | 1 | — | 1 | — | Do not connect |
| | | | 3 | | 5 | | |
| | | | 4 | | 7 | | |
| | | | 6 | | 11 | | |
| | | | 8 | | 15 | | |
| | | | 9 | | 17 | | |
| | | | 11 | | | | |
| | | | 13 | | | | |
| | | | 14 | | | | |
| | | | 16 | | | | |
| 18 | | | | | | | |
| 19 | | | | | | | |
| OFFSET N1 | 1 | — | — | — | — | — | Input offset adjustment |
| OFFSET N2 | 5 | — | — | — | — | — | Input offset adjustment |
| OUT | 6 | — | — | — | — | O | Output |
| V _{CC-} | 4 | 4 | 10 | 11 | 16 | — | Power supply |
| V _{CC+} | 7 | 8 | 20 | 4 | 6 | — | Power supply |

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|--|--------------------------------|------|------|
| V _{CC+} | Supply voltage ⁽²⁾ | | 18 | V |
| V _{CC-} | | | - 18 | |
| V _{ID} | Differential input voltage ⁽³⁾ | | ±30 | V |
| V _I | Input voltage ^{(2) (4)} | | ±15 | V |
| | Duration of output short circuit ⁽⁵⁾ | Unlimited | | |
| T _J | Operating virtual junction temperature | | 150 | °C |
| | Case temperature for 60 seconds | FK package | 260 | °C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds | J, JG, U, or W package | 300 | °C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | D, N, NS, P, PS, or PW package | 260 | °C |
| T _{stg} | Storage temperature | - 65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
- (3) Differential voltages are at IN+, with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either supply. Temperature or supply voltages must be limited so that the dissipation rating is not exceeded.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---------------------|----------------------|----------------------|------|
| V _{CC+} | Supply voltage | 5 | 15 | V |
| V _{CC-} | Supply voltage | - 5 | - 15 | V |
| V _{CM} | Common-mode voltage | V _{CC-} + 4 | V _{CC+} - 4 | V |
| T _A | Ambient temperature | TL06xM | - 55 | 125 |
| | | TL06xQ | - 40 | 125 |
| | | TL06xI | - 40 | 85 |
| | | TL06xC | 0 | 70 |

6.4 Thermal Information (TL061)

| THERMAL METRIC ⁽¹⁾ | | TL061 | | UNIT |
|-------------------------------|--|----------|----------|------|
| | | D (SOIC) | P (PDIP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ^{(2) (3)} | 97 | 85 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance ^{(4) (5)} | — | — | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.5 Thermal Information (TL062)

| THERMAL METRIC ⁽¹⁾ | | TL062 | | | | | UNIT | |
|-------------------------------|--|----------|----------|---------|------------|-----------|------|-----------|
| | | D (SOIC) | P (PDIP) | PS (SO) | PW (TSSOP) | FK (LCCC) | | JG (CDIP) |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 20 PINS | | 8 PINS |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ^{(2) (3)} | 97 | 85 | 95 | 149 | — | — | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance ^{(4) (5)} | — | — | — | — | 5.61 | 14.5 | °C/W |

6.6 Thermal Information (TL064)

| THERMAL METRIC ⁽¹⁾ | | TL064 | | | | | | | UNIT | |
|-------------------------------|--|----------|----------|---------|---------|------------|-----------|----------|-------|---------|
| | | D (SOIC) | N (PDIP) | NS (SO) | PS (SO) | PW (TSSOP) | FK (LCCC) | J (CDIP) | | W (CFP) |
| | | 14 PINS | 14 PINS | 14 PINS | 8 PINS | 14 PINS | 20 PINS | 14 PINS | | 14 PINS |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ^{(2) (3)} | 86 | 80 | 76 | 95 | 113 | — | — | — | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance ^{(2) (3)} | — | — | — | — | — | 5.61 | 15.05 | 14.65 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.7 Electrical Characteristics for TL06xC and TL06xxC

$V_{CC\pm} = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to $(V_{CC+} + V_{CC-}) / 2$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | TL061C, TL062C, TL064C | | | TL061AC, TL062AC, TL064AC | | | UNIT |
|-----------------|---|---------------------------|------------|----------|---------------------------|--------------------------|-----|-------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} | Input offset voltage $V_O = 0$, $R_S = 50\ \Omega$ | $T_A = 25^\circ\text{C}$ | | 3 | 15 | $T_A = 25^\circ\text{C}$ | | mV |
| | | $T_A = \text{Full range}$ | | 20 | | 7.5 | | |
| α_{VIO} | Temperature coefficient of input offset voltage $V_O = 0$, $R_S = 50\ \Omega$, $T_A = \text{Full range}$ | 10 | | | 10 | | | $\mu\text{ V}/^\circ\text{C}$ |
| $I_{IO}^{(3)}$ | Input offset current $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 5 | 200 | $T_A = 25^\circ\text{C}$ | | pA |
| | | $T_A = \text{Full range}$ | | 5 | | 3 | | |
| $I_{IB}^{(3)}$ | Input bias current ⁽²⁾ $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 30 | 400 | $T_A = 25^\circ\text{C}$ | | pA |
| | | $T_A = \text{Full range}$ | | 10 | | 7 | | |
| V_{ICR} | Common-mode input voltage range $T_A = 25^\circ\text{C}$ | ± 11 | - 12 to 15 | ± 11 | - 12 to 15 | | | V |
| V_{OM} | Maximum peak output voltage swing $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | ± 10 | ± 13.5 | ± 10 | ± 13.5 | | | V |
| | $R_L \geq 10\text{ k}\Omega$, $T_A = \text{Full range}$ | ± 10 | | ± 10 | | | | |
| A_{VD} | Large-signal differential voltage amplification $V_O = \pm 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$ | $T_A = 25^\circ\text{C}$ | | 3 | 6 | $T_A = 25^\circ\text{C}$ | | V/mV |
| | | $T_A = \text{Full range}$ | | 3 | | 4 | | |
| B_1 | Unity-gain bandwidth $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | 1 | | | 1 | | | MHz |
| r_i | Input resistance $T_A = 25^\circ\text{C}$ | 10^{12} | | | 10^{12} | | | Ω |
| CMRR | Common-mode rejection ratio $V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | 70 | 86 | 80 | 86 | | | dB |
| k_{SVR} | Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$) $V_{CC} = \pm 9\text{ V}$ to $\pm 15\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | 70 | 95 | 80 | 95 | | | dB |
| P_D | Total power dissipation (each amplifier) $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | 6 | | 7.5 | 6 | | 7.5 | mW |
| I_{CC} | Supply current (each amplifier) $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | 200 | | 250 | 200 | | 250 | μA |
| V_{O1}/V_{O2} | Crosstalk attenuation $A_{VD} = 100$, $T_A = 25^\circ\text{C}$ | 120 | | | 120 | | | dB |

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and -40°C to 85°C for TL06xI.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Fig 6-12](#). Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
- (3) Specified by design and characterization; not production tested.

6.8 Electrical Characteristics for TL06xxC and TL06xI

 $V_{CC\pm} = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to $(V_{CC+} + V_{CC-}) / 2$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | | TL061BC, TL062BC, TL064BC | | | TL061I, TL062I, TL064I | | | UNIT |
|---|---|---------------------------|------------------------------|------------------|-----|------------------------|------------------|-----|-------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_O = 0$, $R_S = 50\ \Omega$ | $T_A = 25^\circ\text{C}$ | | 2 | 3 | | 3 | 6 | mV |
| | | $T_A = \text{Full range}$ | | | 5 | | | 9 | |
| α_{VIO} Temperature coefficient of input offset voltage | $V_O = 0$, $R_S = 50\ \Omega$, $T_A = \text{Full range}$ | | | 10 | | | 10 | | $\mu\text{ V}/^\circ\text{C}$ |
| $I_{IO}^{(3)}$ Input offset current | $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 5 | 100 | | 5 | 100 | pA |
| | | $T_A = \text{Full range}$ | | | 3 | | | 10 | nA |
| $I_{IB}^{(3)}$ Input bias current ⁽²⁾ | $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 30 | 200 | | 30 | 200 | pA |
| | | $T_A = \text{Full range}$ | | | 7 | | | 20 | nA |
| V_{ICR} Common-mode input voltage range | $T_A = 25^\circ\text{C}$ | | ± 11 | - 12 to 15 | | ± 11 | - 12 to 15 | | V |
| V_{OM} Maximum peak output voltage swing | $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | | ± 10 | ± 13.5 | | ± 10 | ± 13.5 | | V |
| | $R_L \geq 10\text{ k}\Omega$, $T_A = \text{Full range}$ | | ± 10 | | | ± 10 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_O = \pm 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$ | $T_A = 25^\circ\text{C}$ | 4 | 6 | | 4 | 6 | | V/mV |
| | | $T_A = \text{Full range}$ | 4 | | | 4 | | | |
| B_1 Unity-gain bandwidth | $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | | | 1 | | | 1 | | MHz |
| r_i Input resistance | $T_A = 25^\circ\text{C}$ | | | 10^{12} | | | 10^{12} | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | | 80 | 86 | | 80 | 86 | | dB |
| k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$) | $V_{CC} = \pm 9\text{ V}$ to $\pm 15\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | | 80 | 95 | | 80 | 95 | | dB |
| P_D Total power dissipation (each amplifier) | $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | | | 6 | 7.5 | | 6 | 7.5 | mW |
| I_{CC} Supply current (each amplifier) | $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | | | 200 | 250 | | 200 | 250 | μA |
| V_{O1}/V_{O2} Crosstalk attenuation | $A_{VD} = 100$, $T_A = 25^\circ\text{C}$ | | | 120 | | | 120 | | dB |

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and -40°C to 85°C for TL06xI.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Fig 6-12](#). Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
- (3) Assured by design and characterization; not production tested.

6.9 Electrical Characteristics for TL06xM

$V_{CC\pm} = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to $(V_{CC+} + V_{CC-}) / 2$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽²⁾ | TL061M, TL062M | | | TL064M | | | UNIT |
|-------------------------|---|---|-----------|-------------------|-----------|--------------------------|-----|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} | Input offset voltage $V_O = 0$, $R_S = 50\ \Omega$ | $T_A = 25^\circ\text{C}$ | | 3 | 6 | $T_A = 25^\circ\text{C}$ | | mV |
| | | $T_A = -55^\circ\text{C}$ to 125°C | | | | 9 | | |
| αV_{IO} | Temperature coefficient of input offset voltage $V_O = 0$, $R_S = 50\ \Omega$, $T_A = -55^\circ\text{C}$ to 125°C | 10 | | | 10 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IO} ⁽⁴⁾ | Input offset current $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 5 | 100 | $T_A = 25^\circ\text{C}$ | | pA |
| | | $T_A = -55^\circ\text{C}$ | | 20 ⁽¹⁾ | | 20 ⁽¹⁾ | | nA |
| | | $T_A = 125^\circ\text{C}$ | | 20 | | 20 | | |
| I_{IB} ⁽⁴⁾ | Input bias current ⁽³⁾ $V_O = 0$ | $T_A = 25^\circ\text{C}$ | | 30 | 200 | $T_A = 25^\circ\text{C}$ | | pA |
| | | $T_A = -55^\circ\text{C}$ | | 50 ⁽¹⁾ | | 50 ⁽¹⁾ | | nA |
| | | $T_A = 125^\circ\text{C}$ | | 50 | | 50 | | |
| V_{ICR} | Common-mode input voltage range $T_A = 25^\circ\text{C}$ | ± 11 | -12 to 15 | ± 11 | -12 to 15 | | | V |
| V_{OM} | Maximum peak output voltage swing $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | ± 10 | | | ± 10 | | | V |
| | | $R_L \geq 10\text{ k}\Omega$, $T_A = -55^\circ\text{C}$ to 125°C | | ± 10 | | | | |
| A_{VD} | Large-signal differential voltage amplification $V_O = \pm 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$ | $T_A = 25^\circ\text{C}$ | | 4 | 6 | $T_A = 25^\circ\text{C}$ | | V/mV |
| | | $T_A = -55^\circ\text{C}$ to 125°C | | 4 | | 4 | | |
| B_1 | Unity-gain bandwidth $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | 1 | | | 1 | | | MHz |
| r_i | Input resistance $T_A = 25^\circ\text{C}$ | 10^{12} | | | 10^{12} | | | Ω |
| CMRR | Common-mode rejection ratio $V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | 80 | 86 | 80 | 86 | | | dB |
| k_{SVR} | Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$) $V_{CC} = \pm 9\text{ V}$ to $\pm 15\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ | 80 | 95 | 80 | 95 | | | dB |
| P_D | Total power dissipation (each amplifier) $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | 6 | | 7.5 | 6 | | 7.5 | mW |
| I_{CC} | Supply current (each amplifier) $V_O = 0$, No load, $T_A = 25^\circ\text{C}$ | 200 | | 250 | 200 | | 250 | μA |
| V_{O1}/V_{O2} | Crosstalk attenuation $A_{VD} = 100$, $T_A = 25^\circ\text{C}$ | 120 | | | 120 | | | dB |

- (1) This parameter is not production tested.
- (2) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Fig 6-12](#). Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
- (4) Specified by design and characterization; not production tested.

6.10 Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $(V_{CC+} + V_{CC-}) / 2$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----|-----|-----|------------------------|
| SR | Slew rate at unity gain ⁽¹⁾ $V_i = 10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, see Fig 7-1 | 1.5 | 3.5 | | V/ μs |
| t_r | Rise-time $V_i = 20\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, see Fig 7-1 | | 0.2 | | μs |
| | Overshoot factor | | 10% | | |
| V_n | Equivalent input noise voltage $R_S = 20\ \Omega$, $f = 1\text{ kHz}$ | | 30 | | nV/ $\sqrt{\text{Hz}}$ |

- (1) Slew rate at -55°C to 125°C is $0.7\text{ V}/\mu\text{s min}$.

Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

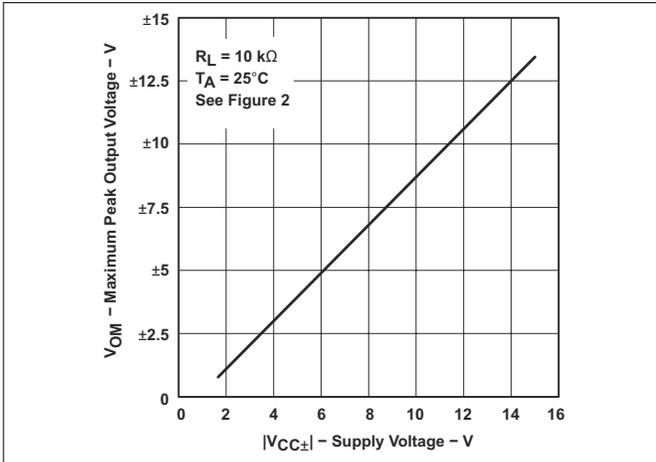


图 6-1. Maximum Peak Output Voltage vs Supply Voltage

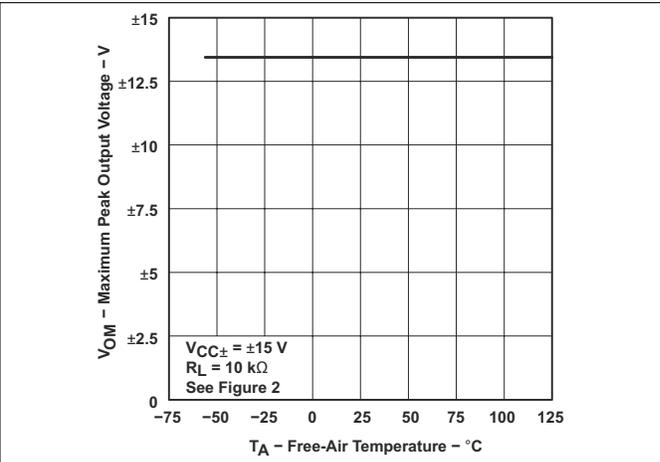


图 6-2. Maximum Peak Output Voltage vs Free-Air Temperature

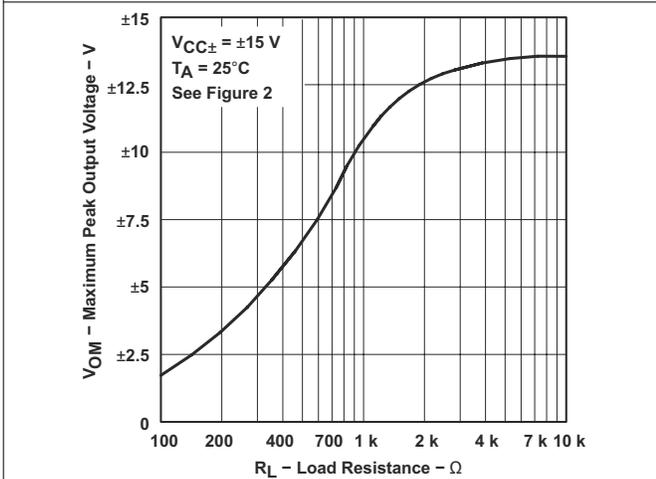


图 6-3. Maximum Peak Output Voltage vs Load Resistance

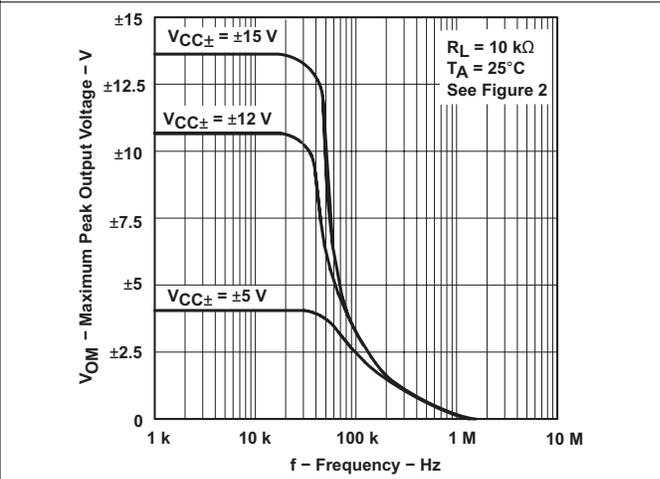


图 6-4. Maximum Peak Output Voltage vs Frequency

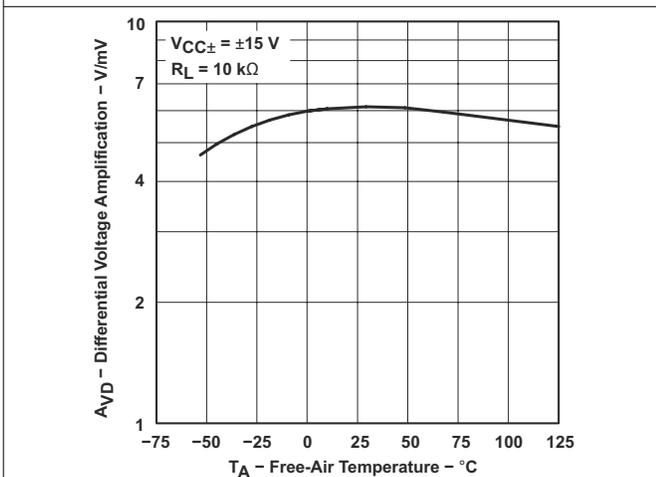


图 6-5. Differential Voltage Amplification vs Free-Air Temperature

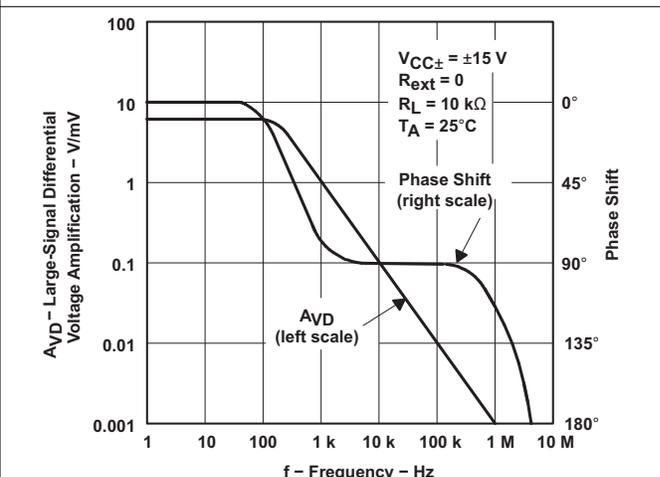
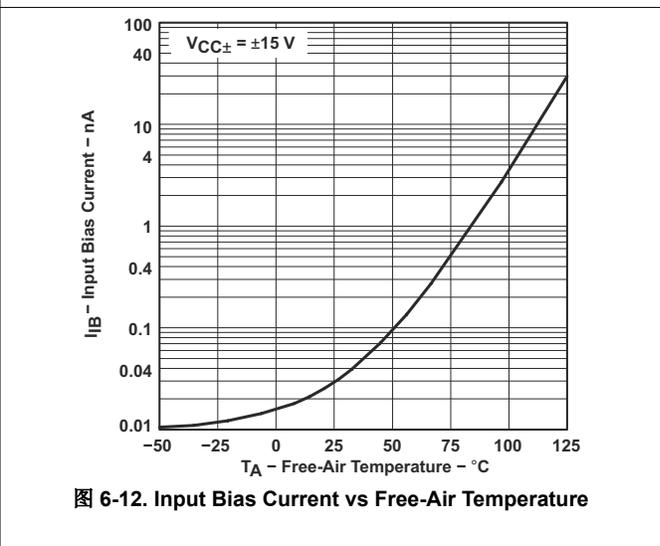
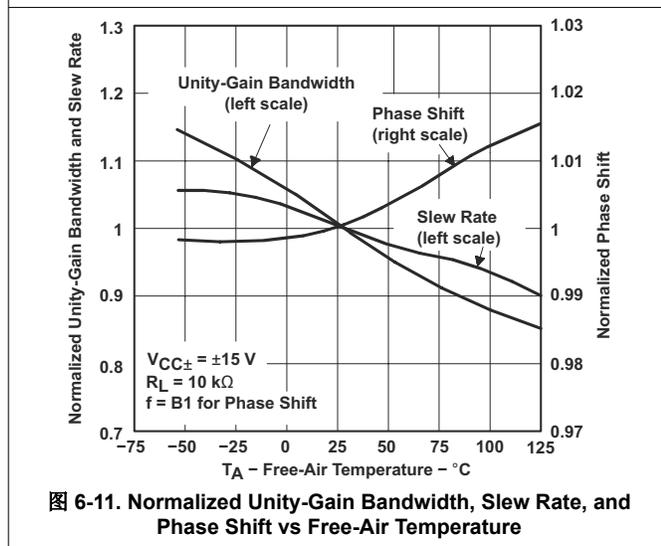
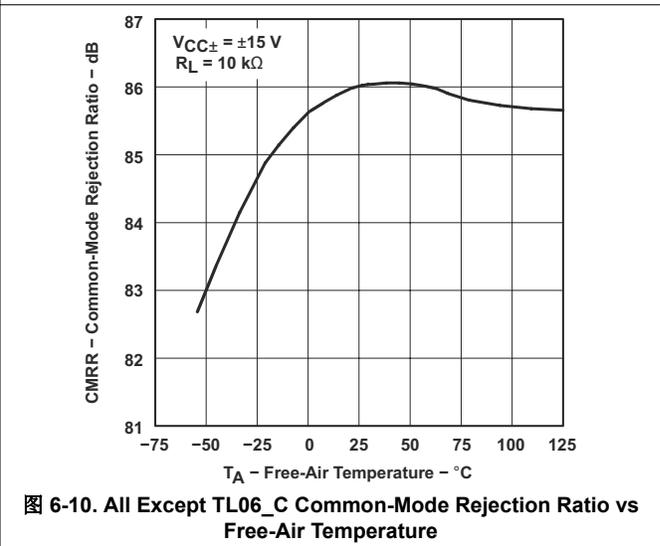
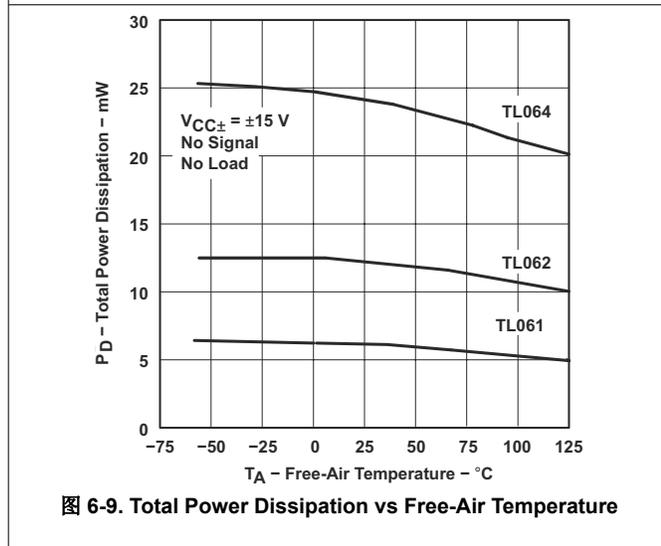
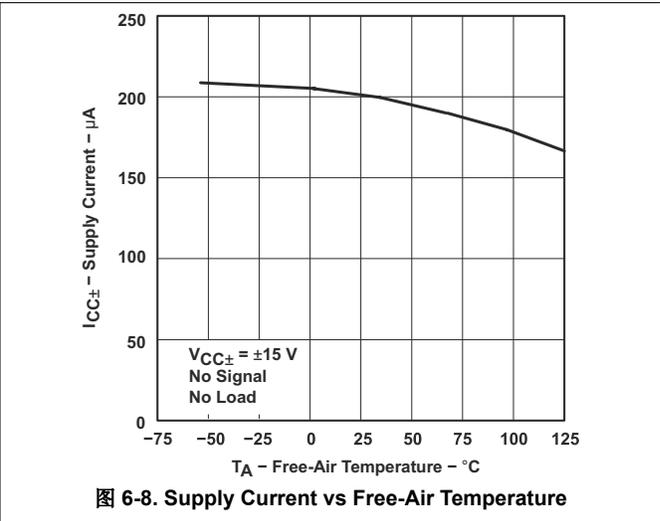
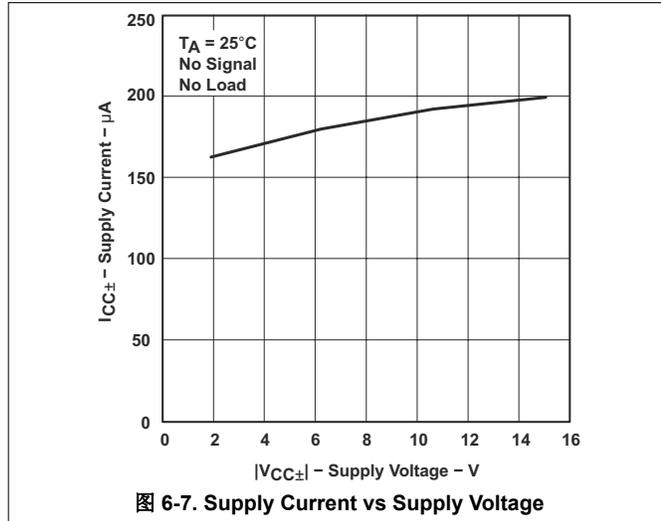


图 6-6. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.



Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

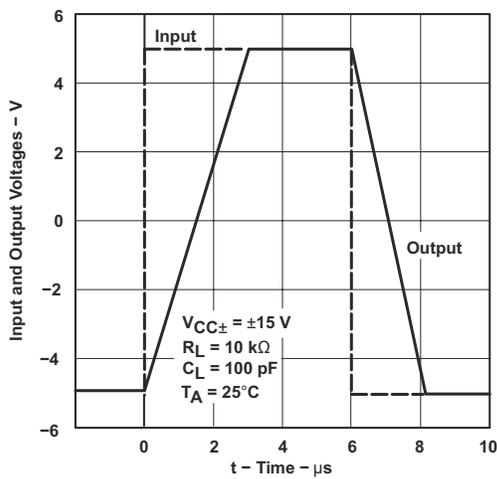


图 6-13. Voltage-Follower Large-Signal Pulse Response vs Time

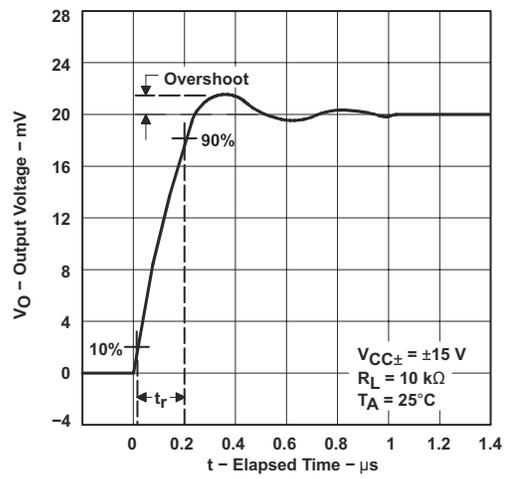


图 6-14. Output Voltage vs Elapsed Time

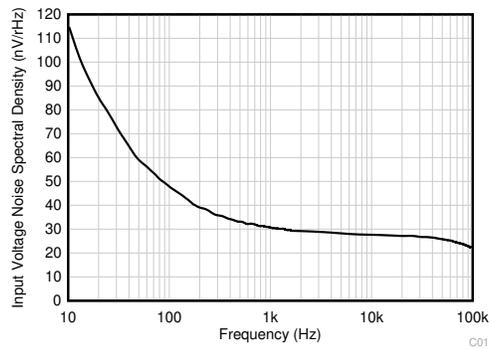


图 6-15. Equivalent Input Noise Voltage vs Frequency

7 Parameter Measurement Information

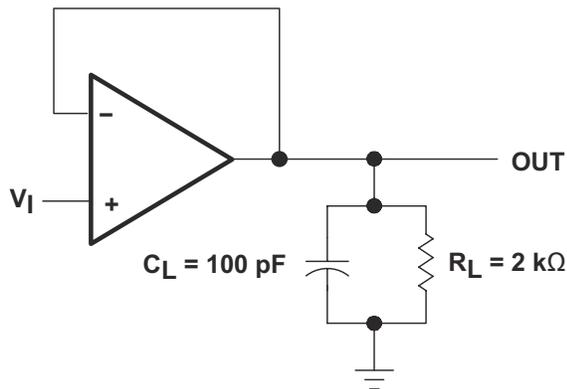


图 7-1. Unity-Gain Amplifier

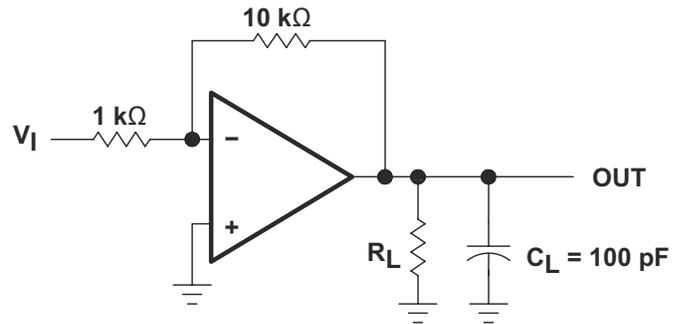


图 7-2. Gain-of-10 Inverting Amplifier

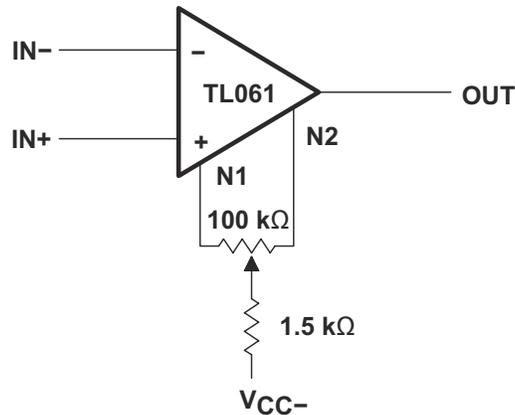


图 7-3. Input Offset-Voltage Null Circuit

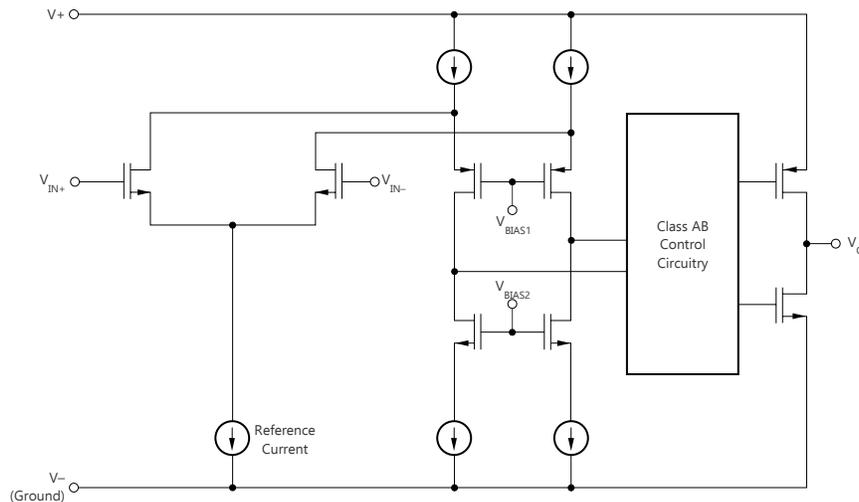
8 Detailed Description

8.1 Overview

The TL06x (TL061, TL062, and TL064) family of industry-standard operational amplifiers (op amps) mirror the TL07x and TL08x family of op amps with lower power consumption. These devices provide outstanding value for cost-sensitive applications, featuring high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and wide temperature operation enable the TL06x devices to be used in rugged and environmentally-demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of this device is 86 dB.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 3.5-V/ μ s slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TL06x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

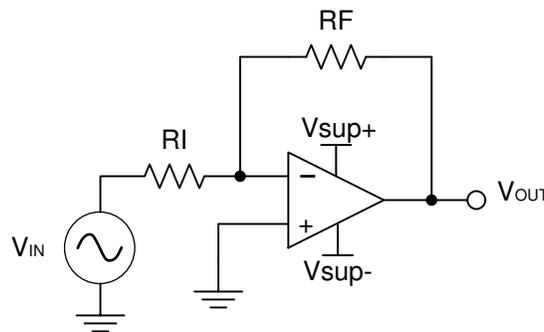


图 9-1. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choose a value in the $k\Omega$ range to limit currents in the amplifier circuit to the mA range. This example will choose $10 k\Omega$ for R_I which means $36 k\Omega$ will be used for R_F . This was determined by Equation 3.

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

9.2.1.3 Application Curve

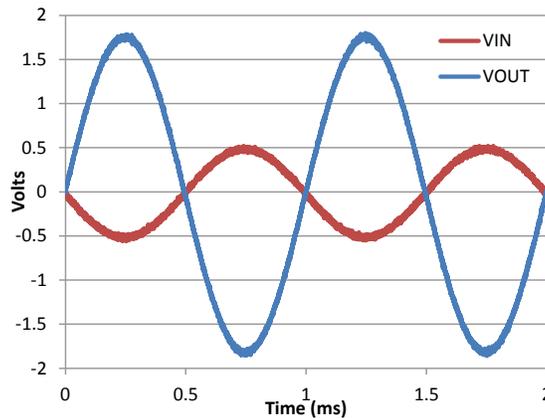


图 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

9.3.1 General Applications

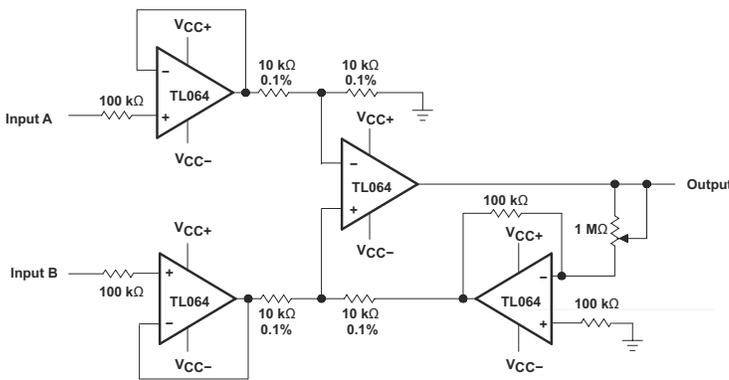


图 9-3. Instrumentation Amplifier

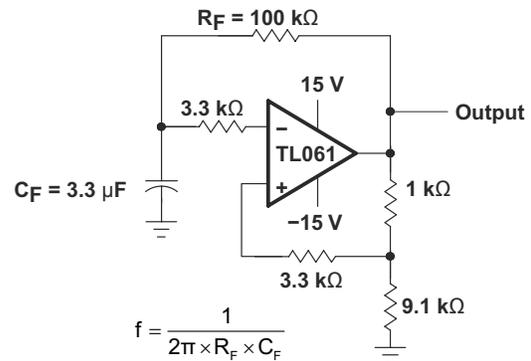


图 9-4. 0.5-Hz Square-Wave Oscillator

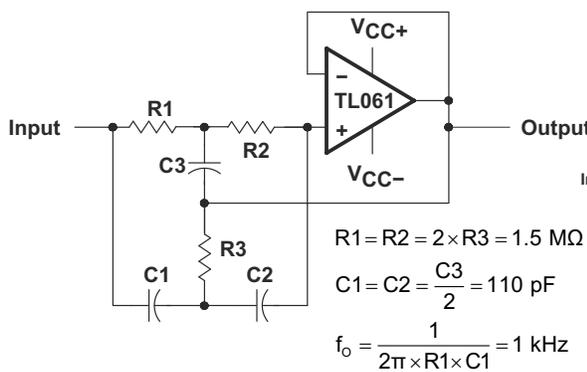


图 9-5. High-Q Notch Filter

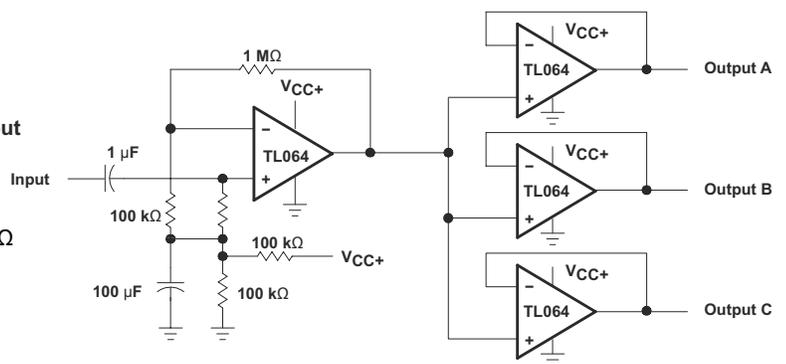


图 9-6. Audio-Distribution Amplifier

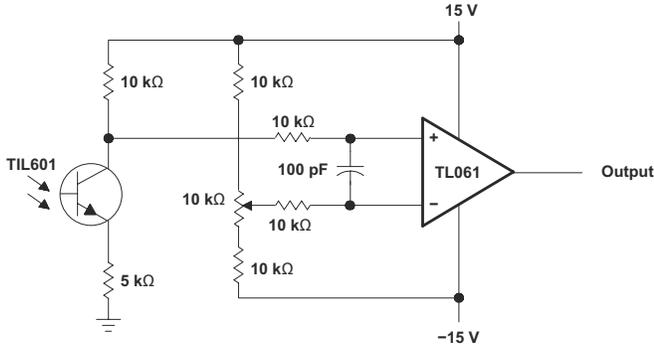


图 9-7. Low-Level Light Detector Preamp

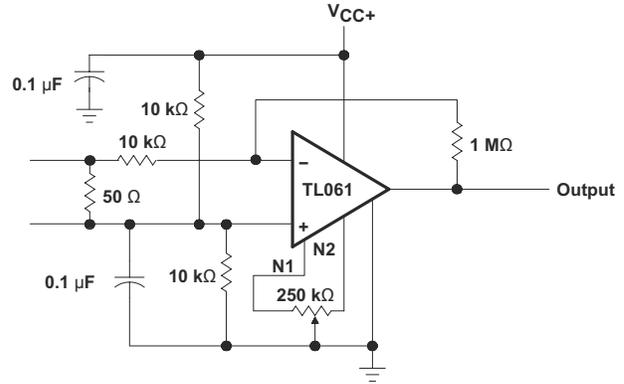


图 9-8. AC Amplifier

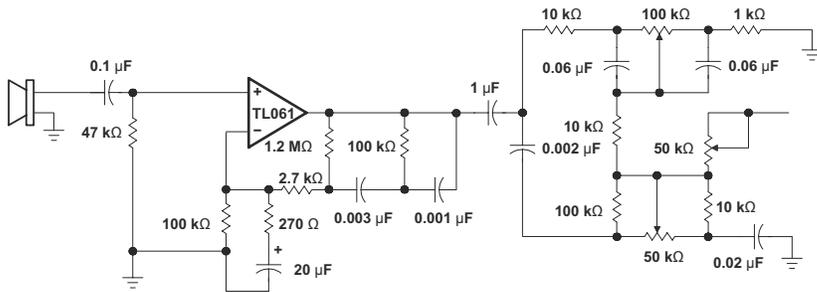


图 9-9. Microphone Preamp With Tone Control

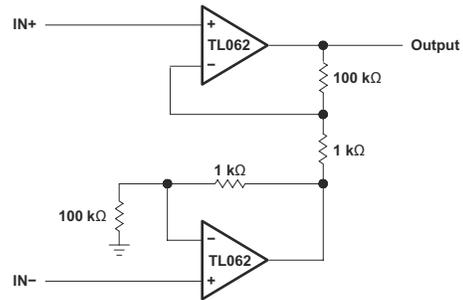


图 9-10. Instrumentation Amplifier

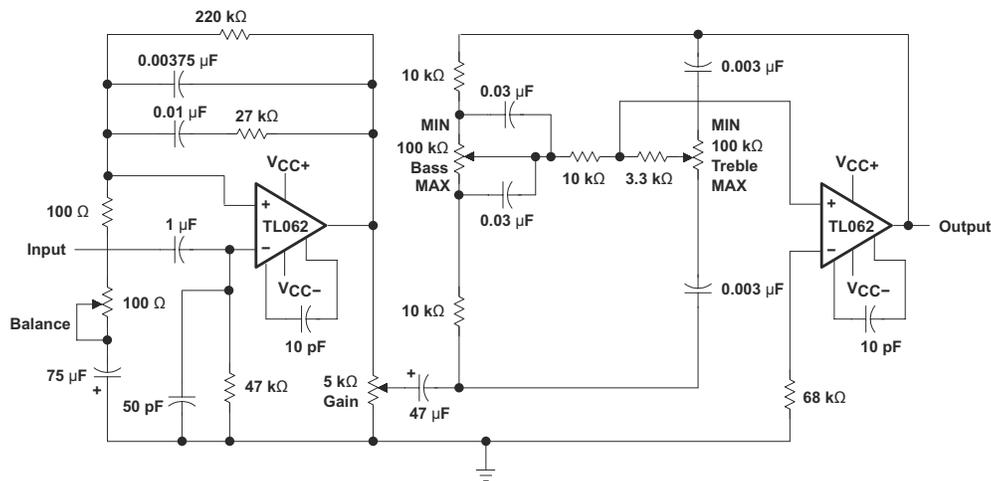
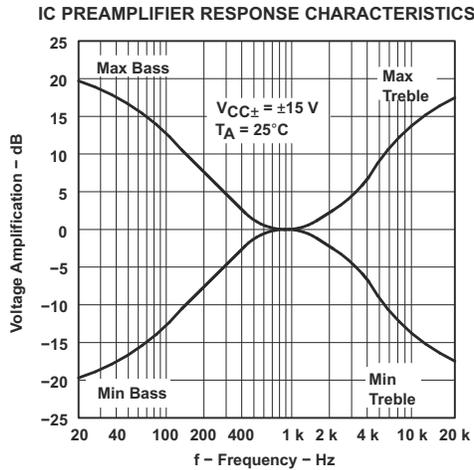


图 9-11. IC Preamplifier

9.4 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single supply, or outside the range of $\pm 18\text{ V}$ for a dual supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.

9.5 Layout

9.5.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.5.2 Layout Examples

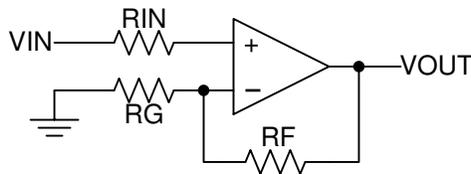


图 9-12. Operational Amplifier Schematic for Noninverting Configuration

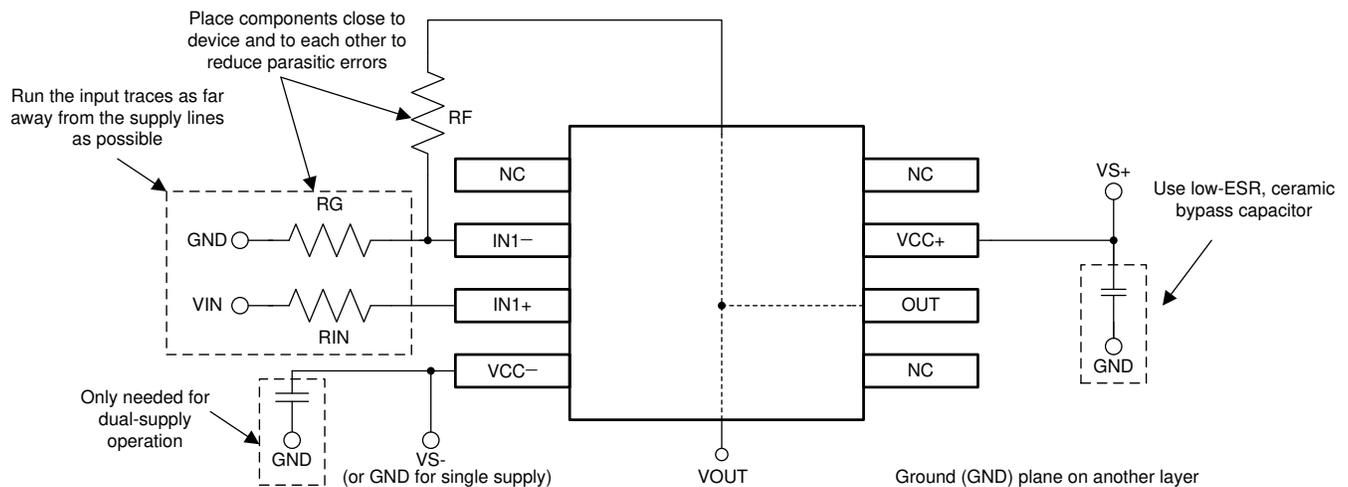


图 9-13. Operational Amplifier Board Layout for Noninverting Configuration

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Circuit Board Layout Techniques chapter extracts](#)

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------|
| 81023022A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023022A TL062MFKB |
| 8102302PA | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102302PA TL062M |
| 81023032A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023032A TL064MFKB |
| 8102303CA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303CA TL064MJB |
| 8102303DA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303DA TL064MWB |
| TL061ACD | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | 061AC |
| TL061ACDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 061AC |
| TL061ACDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 061AC |
| TL061ACP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061ACP |
| TL061ACP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061ACP |
| TL061BCP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061BCP |
| TL061BCP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061BCP |
| TL061BCPE4 | Active | Production | PDIP (P) 8 | 50 TUBE | - | Call TI | Call TI | 0 to 70 | |
| TL061CD | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | TL061C |
| TL061CDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL061C |
| TL061CDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL061C |
| TL061CP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061CP |
| TL061CP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL061CP |
| TL061CPSR | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T061 |
| TL061CPSR.A | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T061 |
| TL061ID | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -40 to 85 | TL061I |
| TL061IDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL061I |
| TL061IDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL061I |
| TL061IDRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | - | Call TI | Call TI | -40 to 85 | |
| TL061IP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL061IP |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TL061IP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL061IP |
| TL061IPE4 | Active | Production | PDIP (P) 8 | 50 TUBE | - | Call TI | Call TI | -40 to 85 | |
| TL062ACD | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | 062AC |
| TL062ACDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 062AC |
| TL062ACDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 062AC |
| TL062ACDRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 062AC |
| TL062ACP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062ACP |
| TL062ACP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062ACP |
| TL062ACPSR | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062A |
| TL062ACPSR.A | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062A |
| TL062BCD | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | 062BC |
| TL062BCDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 062BC |
| TL062BCDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 062BC |
| TL062BCP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062BCP |
| TL062BCP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062BCP |
| TL062CD | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | TL062C |
| TL062CDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL062C |
| TL062CDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL062C |
| TL062CDRE4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL062C |
| TL062CDRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL062C |
| TL062CP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062CP |
| TL062CP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL062CP |
| TL062CPE4 | Active | Production | PDIP (P) 8 | 50 TUBE | - | Call TI | Call TI | 0 to 70 | |
| TL062CPS | Active | Production | SO (PS) 8 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPS.A | Active | Production | SO (PS) 8 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPSR | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPSR.A | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPW | Obsolete | Production | TSSOP (PW) 8 | - | - | Call TI | Call TI | 0 to 70 | T062 |
| TL062CPWR | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPWR.A | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T062 |
| TL062CPWRG4 | Obsolete | Production | TSSOP (PW) 8 | - | - | Call TI | Call TI | 0 to 70 | T062 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------|
| TL062ID | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -40 to 85 | TL062I |
| TL062IDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL062I |
| TL062IDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL062I |
| TL062IP | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL062IP |
| TL062IP.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL062IP |
| TL062IPWR | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Z062 |
| TL062IPWR.A | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Z062 |
| TL062IPWRG4 | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | - | Call TI | Call TI | -40 to 85 | |
| TL062MFKB | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023022A TL062MFKB |
| TL062MFKB.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023022A TL062MFKB |
| TL062MJG | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TL062MJG |
| TL062MJG.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TL062MJG |
| TL062MJGB | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102302PA TL062M |
| TL062MJGB.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102302PA TL062M |
| TL064ACD | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | TL064AC |
| TL064ACDR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064AC |
| TL064ACDR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064AC |
| TL064ACN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064ACN |
| TL064ACN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064ACN |
| TL064BCD | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | TL064BC |
| TL064BCDR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064BC |
| TL064BCDR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064BC |
| TL064BCN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064BCN |
| TL064BCN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064BCN |
| TL064CD | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | TL064C |
| TL064CDR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064C |
| TL064CDR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064C |
| TL064CN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064CN |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------|
| TL064CN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | TL064CN |
| TL064CNSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064 |
| TL064CNSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL064 |
| TL064CPW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | 0 to 70 | T064 |
| TL064CPWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | 0 to 70 | T064 |
| TL064CPWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T064 |
| TL064CPWRG4 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | T064 |
| TL064ID | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | TL064I |
| TL064IDR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064IDR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064IDRG4 | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | TL064I |
| TL064IN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL064IN |
| TL064IN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TL064IN |
| TL064INE4 | Active | Production | PDIP (N) 14 | 25 TUBE | - | Call TI | Call TI | -40 to 85 | |
| TL064INS | Active | Production | SOP (NS) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064INS.A | Active | Production | SOP (NS) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064INSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064INSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL064I |
| TL064IPWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Z064 |
| TL064IPWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Z064 |
| TL064MFKB | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023032A TL064MFKB |
| TL064MFKB.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 81023032A TL064MFKB |
| TL064MJ | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TL064MJ |
| TL064MJ.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TL064MJ |
| TL064MJB | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303CA TL064MJB |
| TL064MJB.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303CA TL064MJB |
| TL064MWB | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303DA TL064MWB |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------|
| TL064MWB.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8102303DA TL064MWB |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL062, TL062M, TL064, TL064M :

● Catalog : [TL062](#), [TL064](#)

● Military : [TL062M](#), [TL064M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL061ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL061CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL061CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TL061IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL062ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL062ACPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TL062BCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL062CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL062CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TL062CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL062IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL062IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL064ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL064BCDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL064CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL064CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

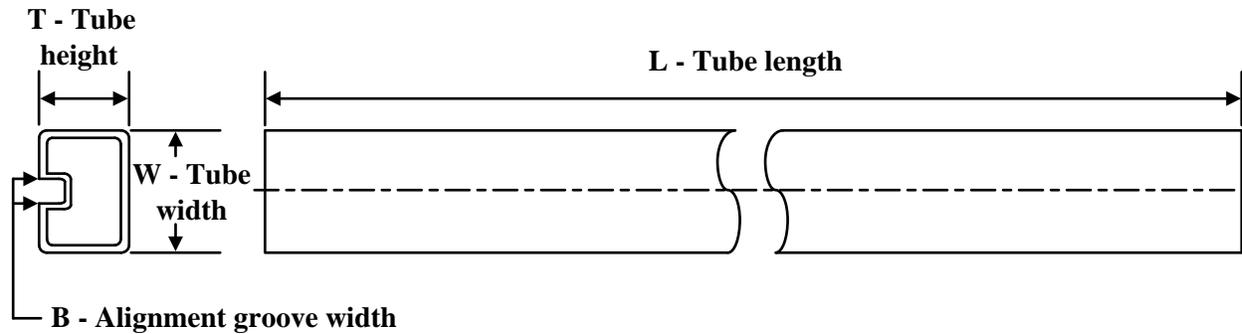
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL064CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL064CNSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| TL064CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL064CPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL064CPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL064IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL064INSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| TL064IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL064IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL061ACDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL061CDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL061CPSR | SO | PS | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| TL061IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL062ACDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL062ACPSR | SO | PS | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| TL062BCDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL062CDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL062CPSR | SO | PS | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| TL062CPWR | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| TL062IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TL062IPWR | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| TL064ACDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TL064BCDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TL064CDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TL064CDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL064CDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TL064CNSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL064CPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TL064CPWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TL064CPWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TL064IDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TL064INSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| TL064IPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| TL064IPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 81023022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 81023032A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8102303DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| TL061ACP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061ACP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061BCP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061BCP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061CP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL061IP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062ACP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062ACP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062BCP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062BCP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062CP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062CPS | PS | SOP | 8 | 80 | 530 | 10.5 | 4000 | 4.1 |
| TL062CPS.A | PS | SOP | 8 | 80 | 530 | 10.5 | 4000 | 4.1 |
| TL062IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062IP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL062MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TL062MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TL064ACN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064ACN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064BCN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064BCN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064CN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064CN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

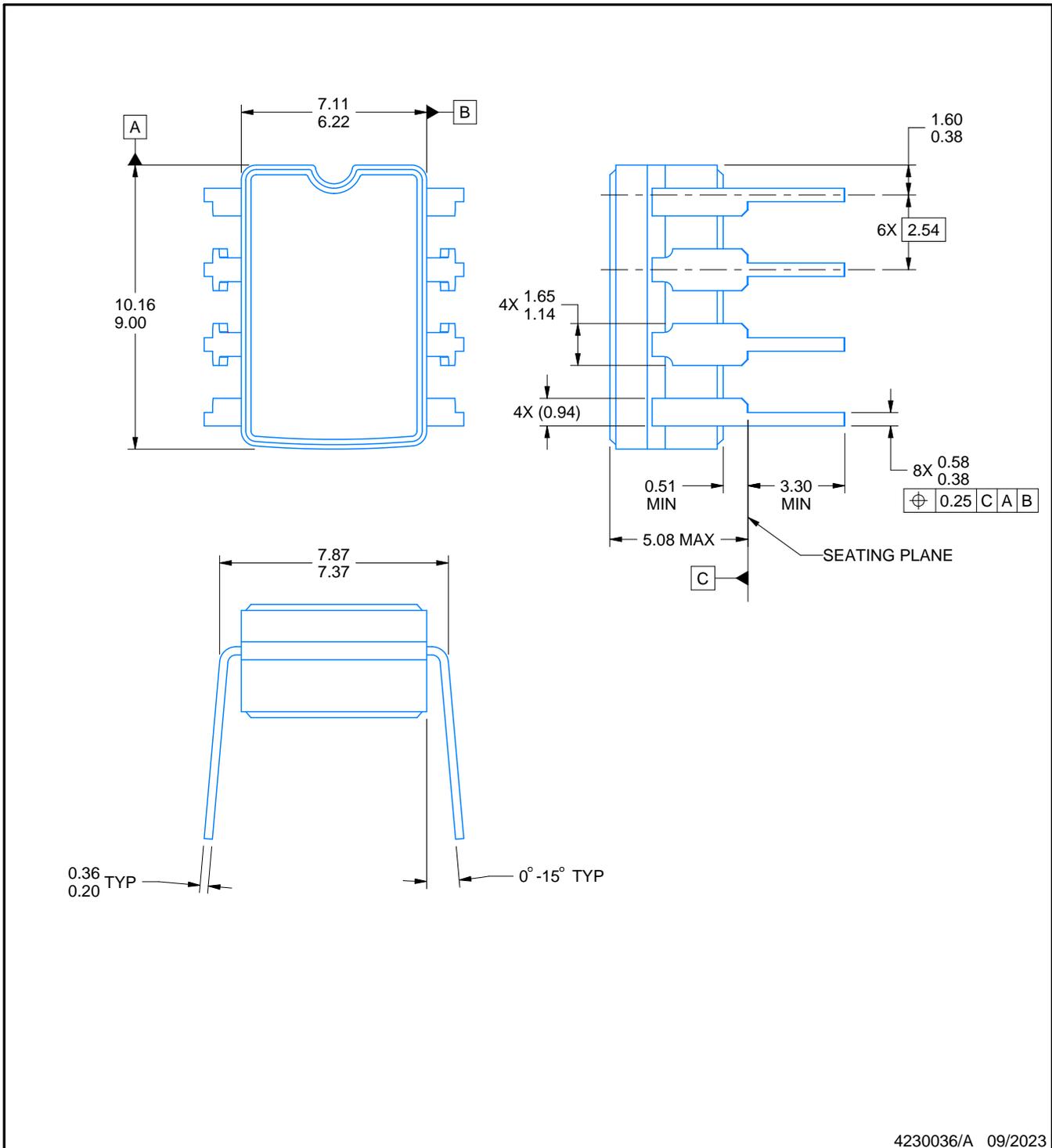
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL064IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064IN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL064INS | NS | SOP | 14 | 50 | 530 | 10.5 | 4000 | 4.1 |
| TL064INS.A | NS | SOP | 14 | 50 | 530 | 10.5 | 4000 | 4.1 |
| TL064MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TL064MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TL064MWB | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| TL064MWB.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



NOTES:

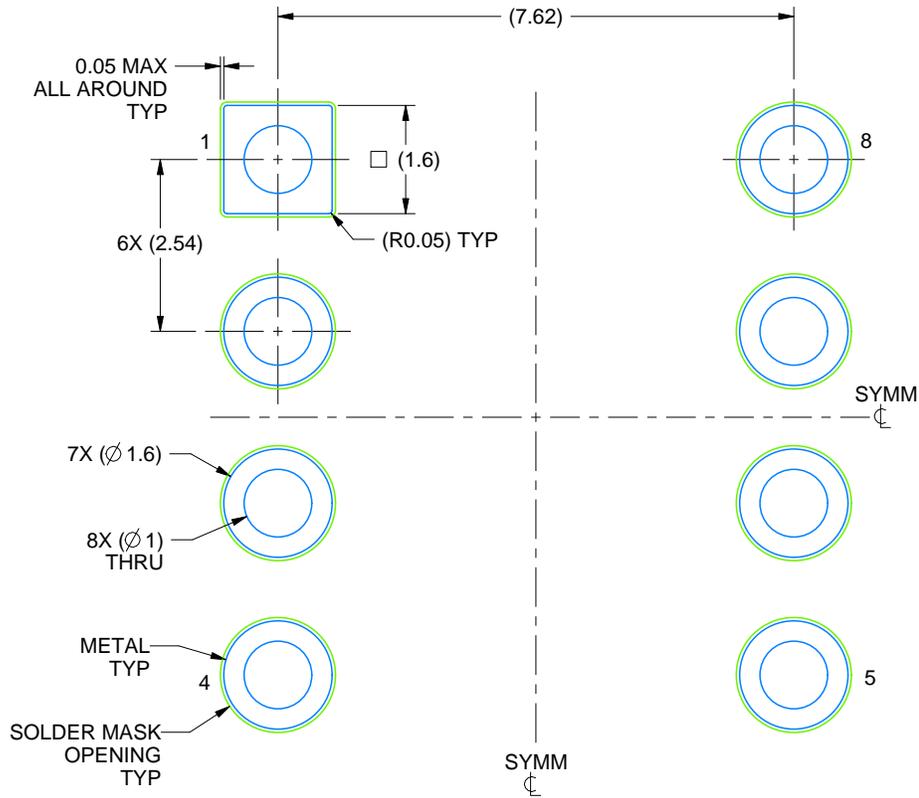
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

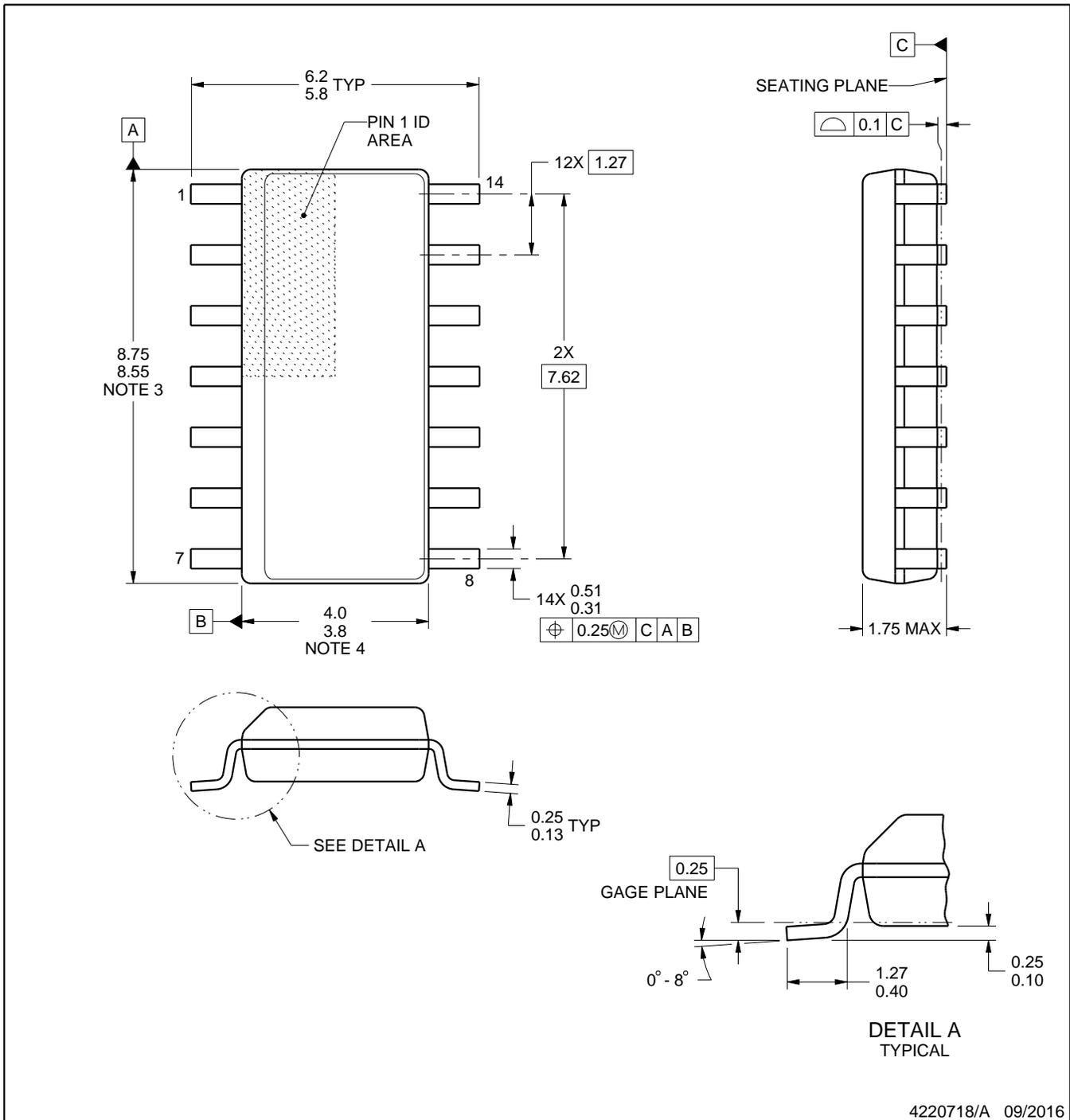
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

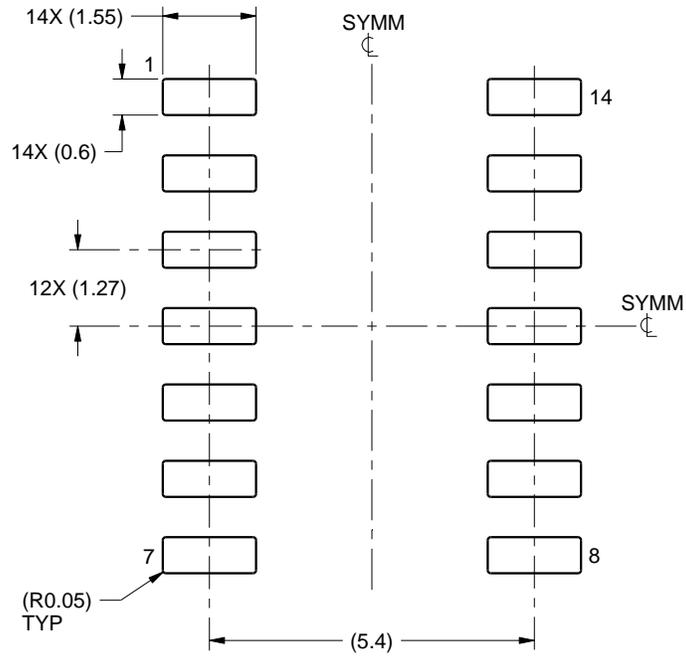
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

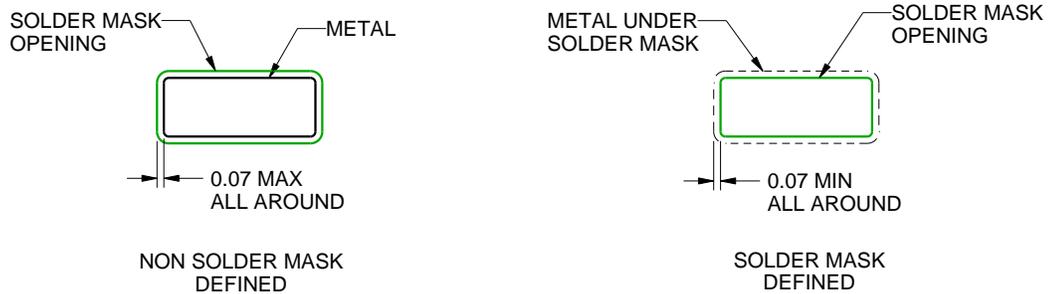
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

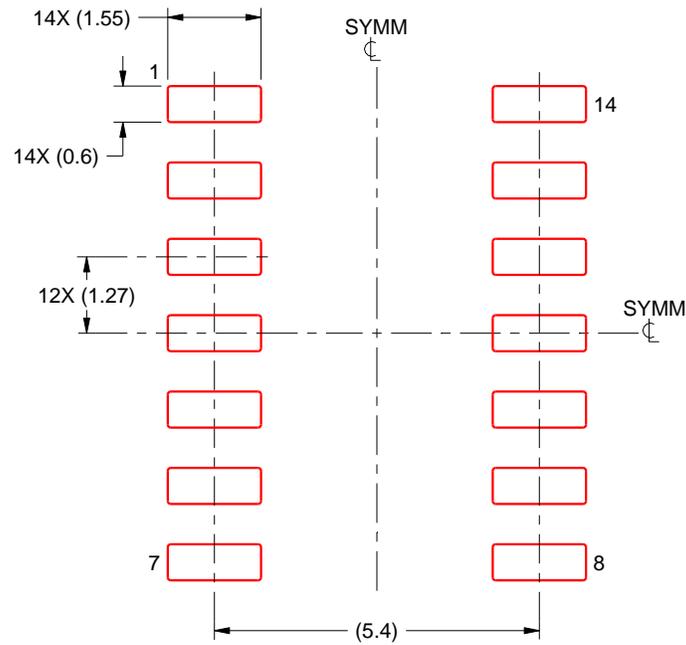
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

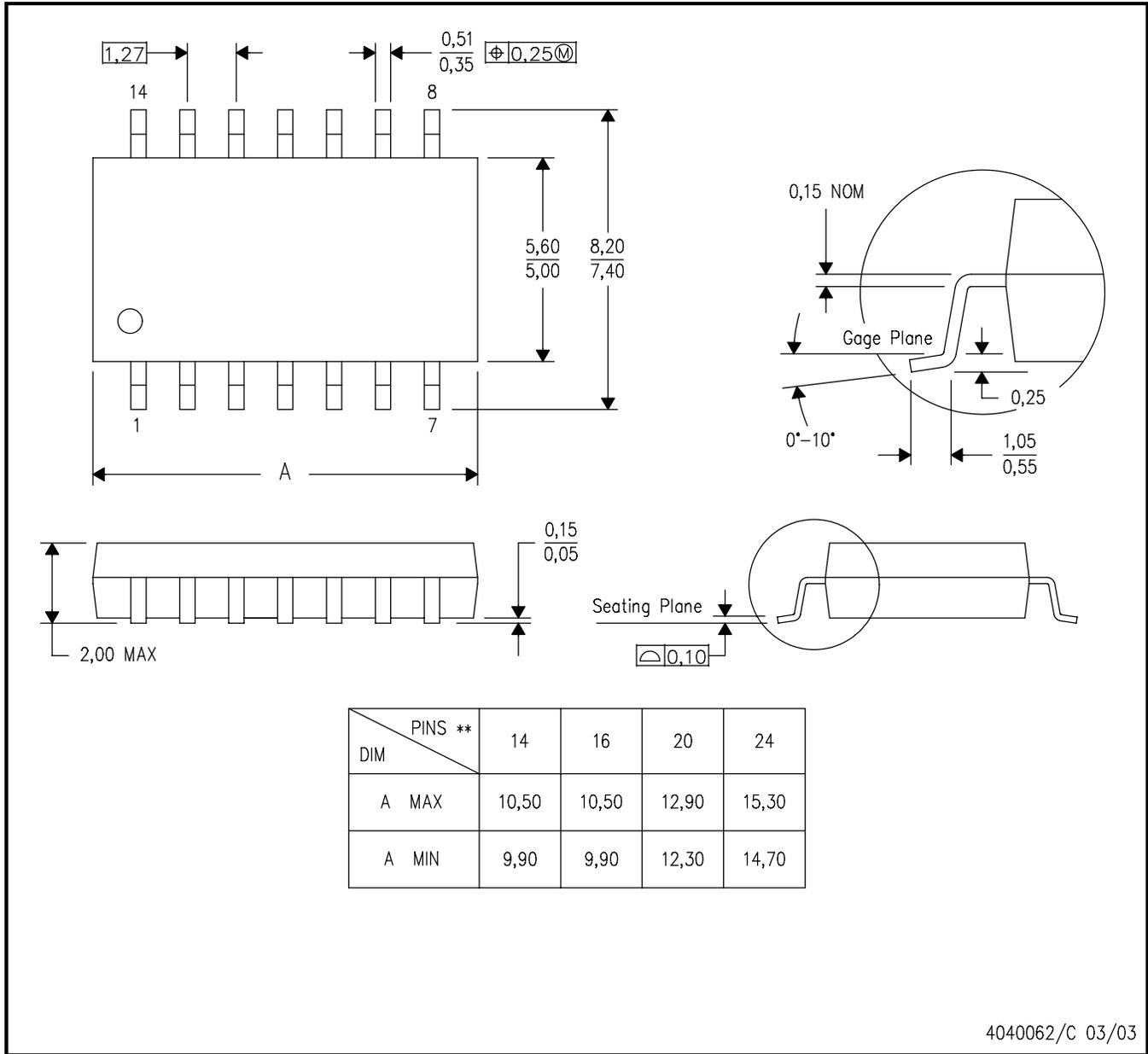
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

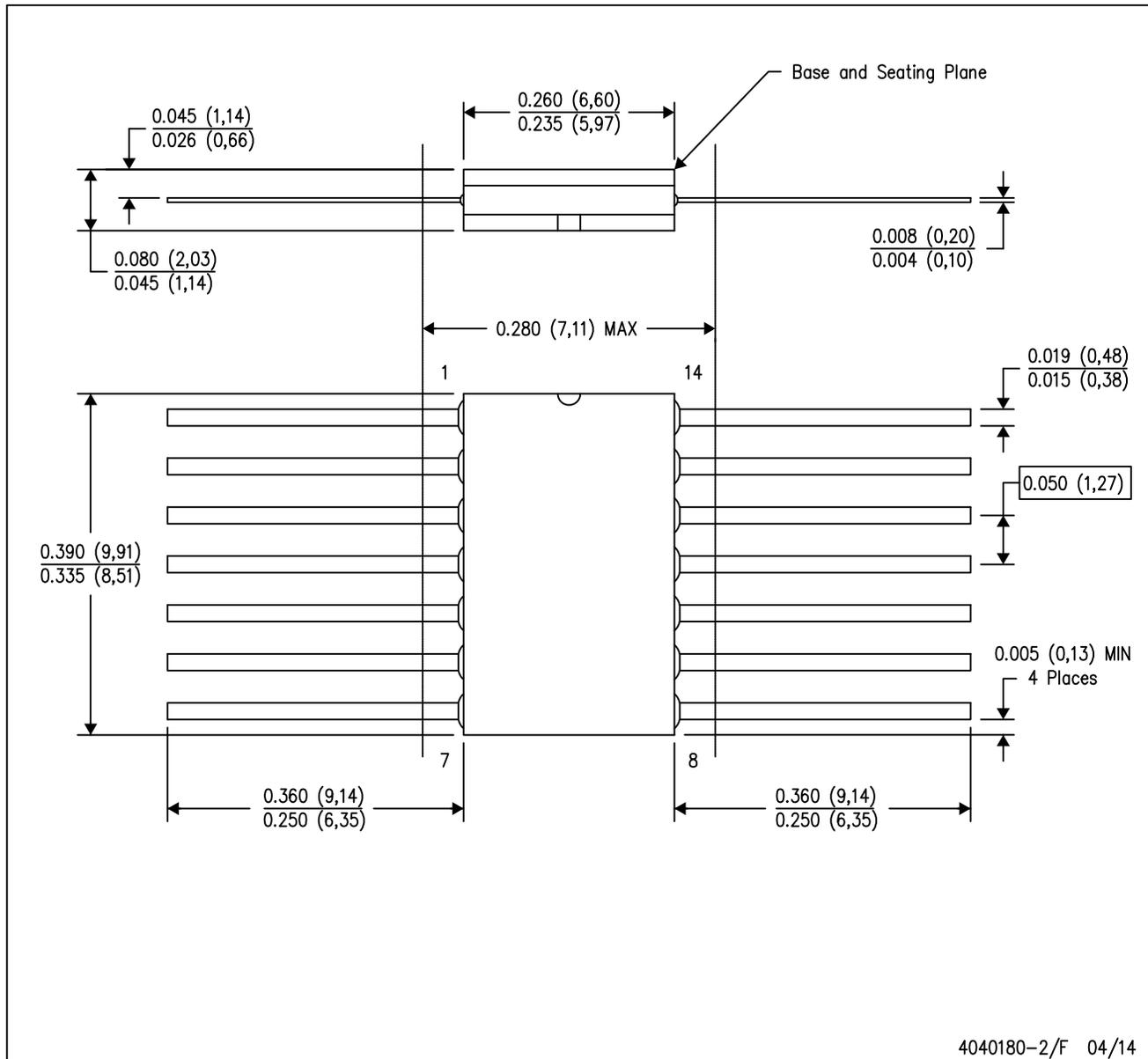
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

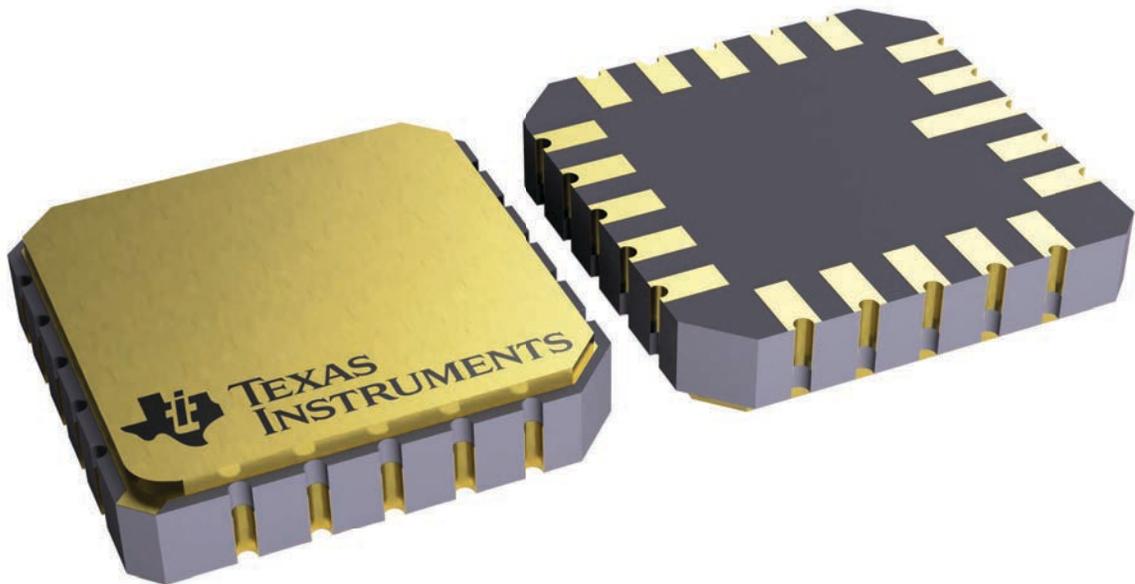
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

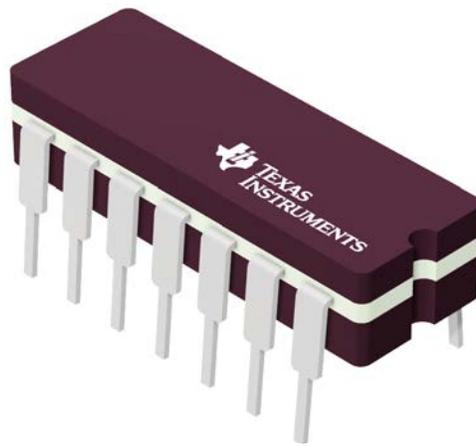
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

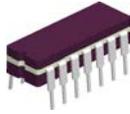
GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

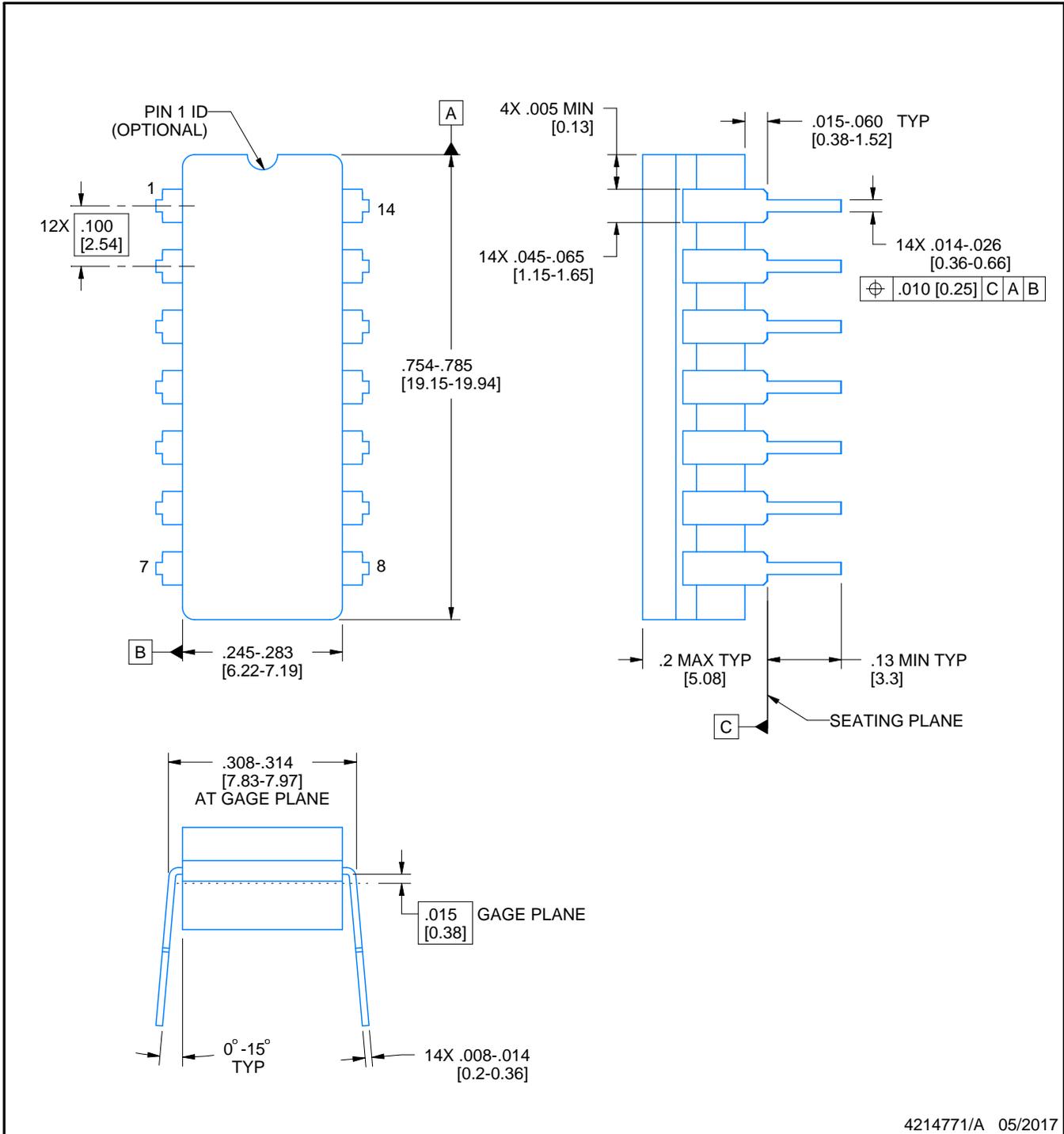
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

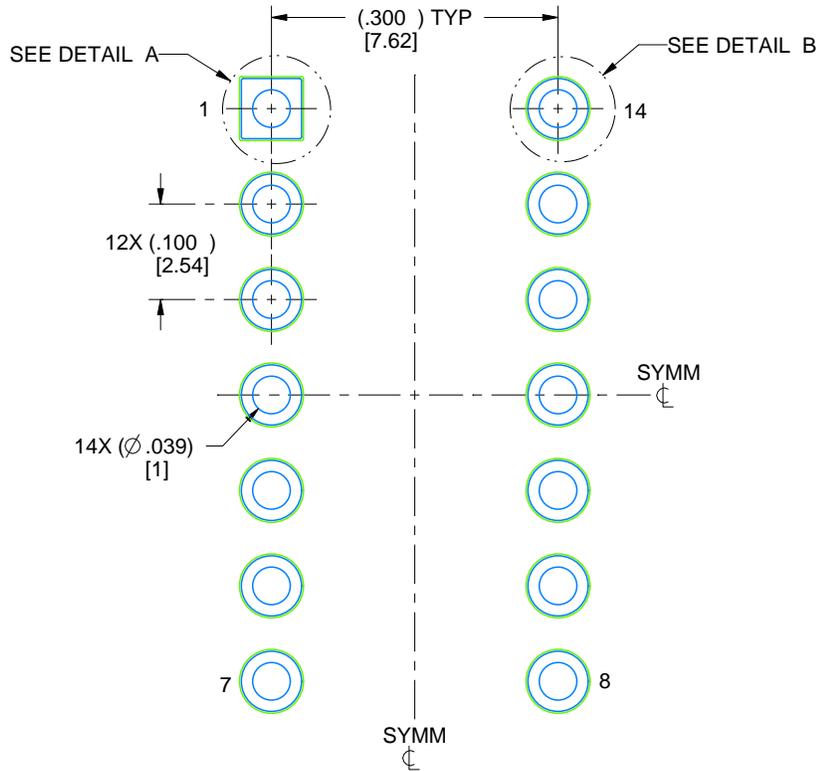
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

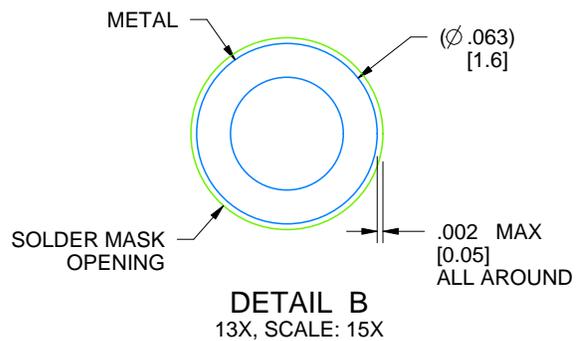
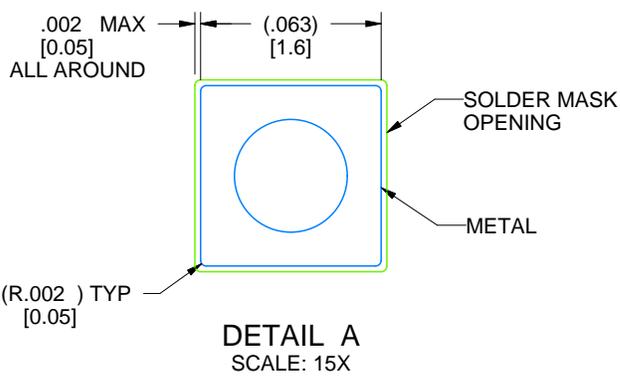
J0014A

CDIP - 5.08 mm max height

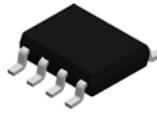
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

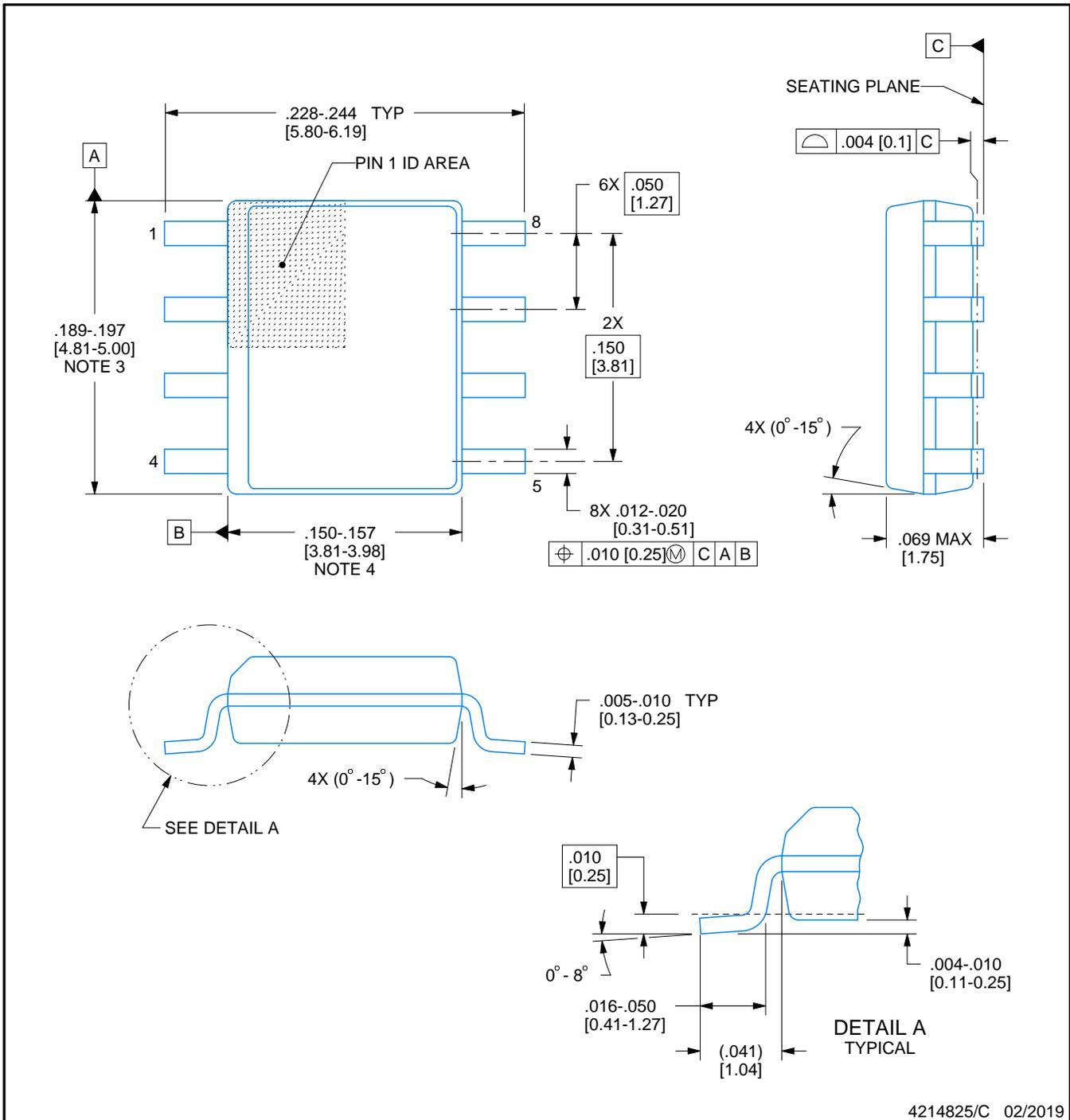


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

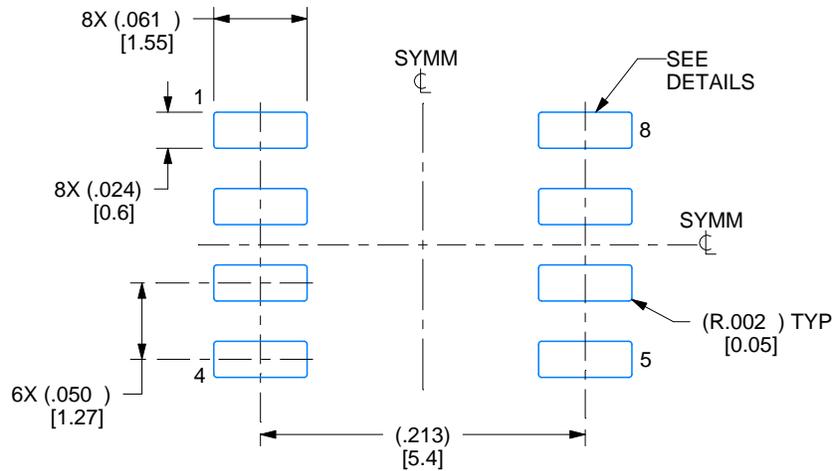
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

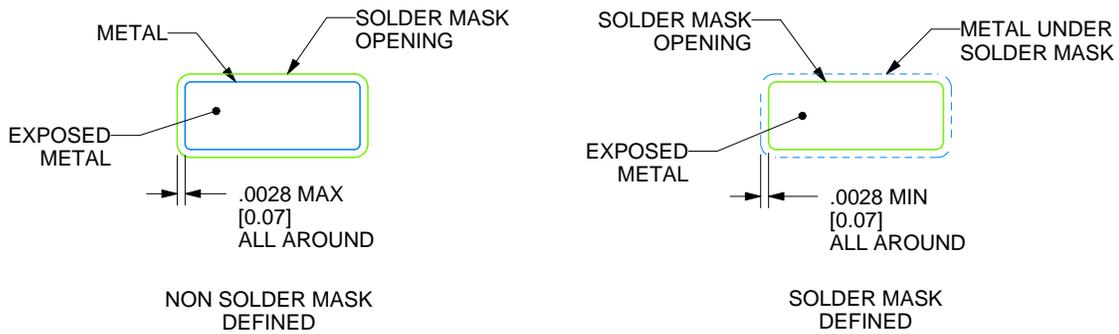
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

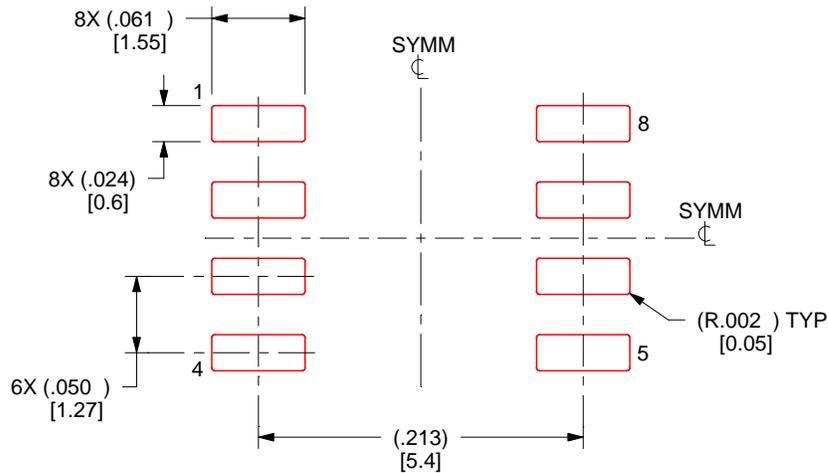
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

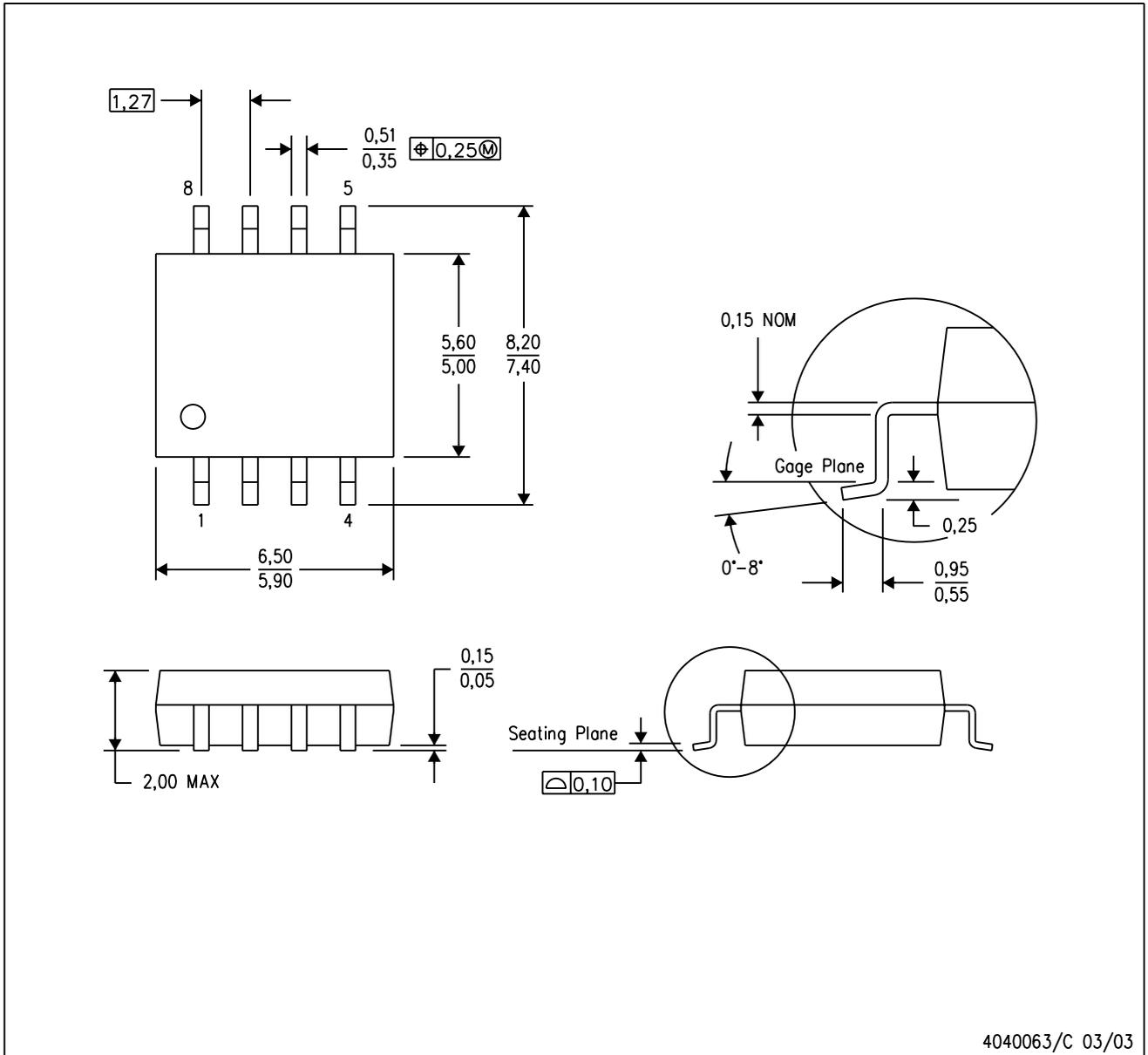
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

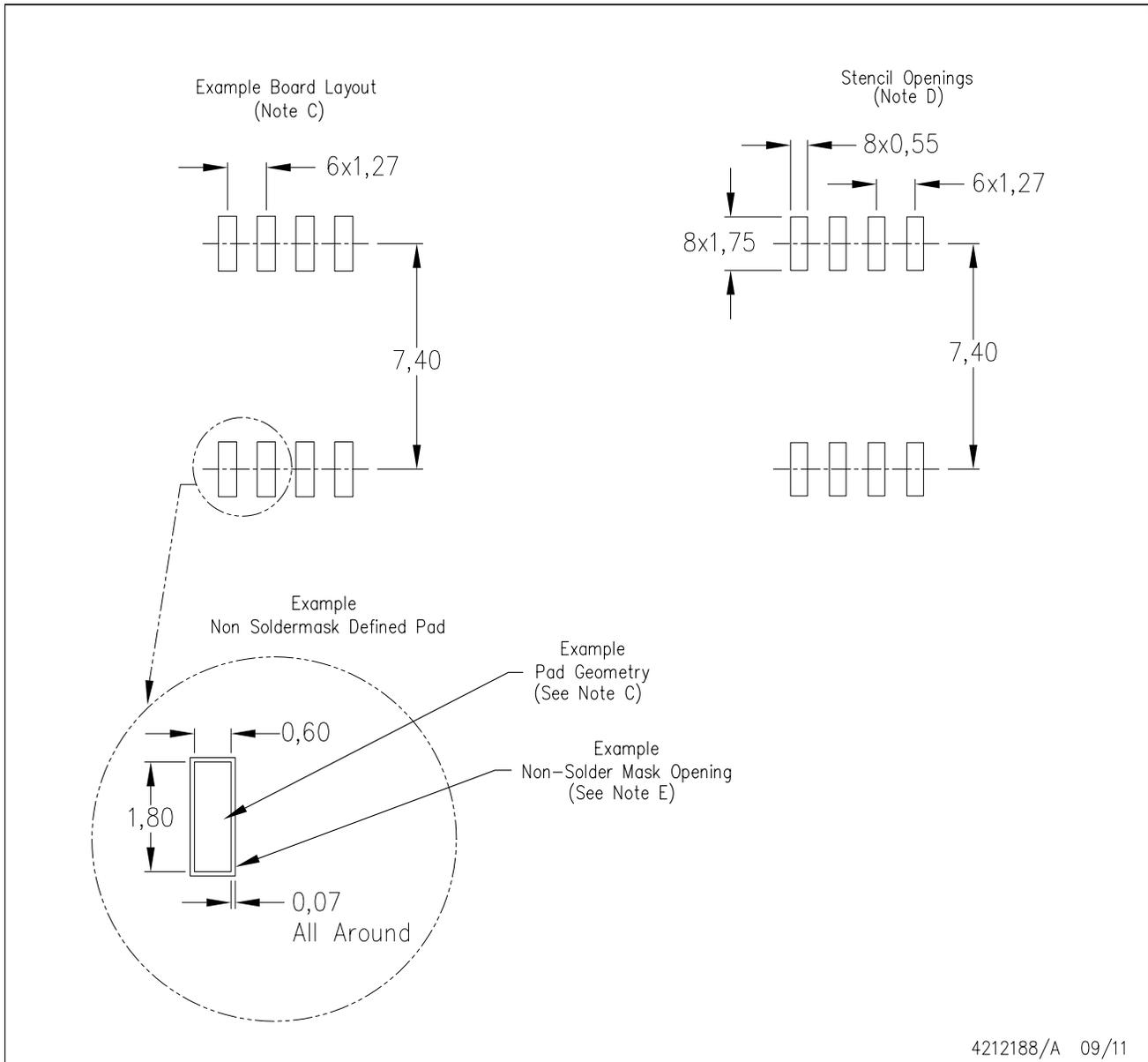
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

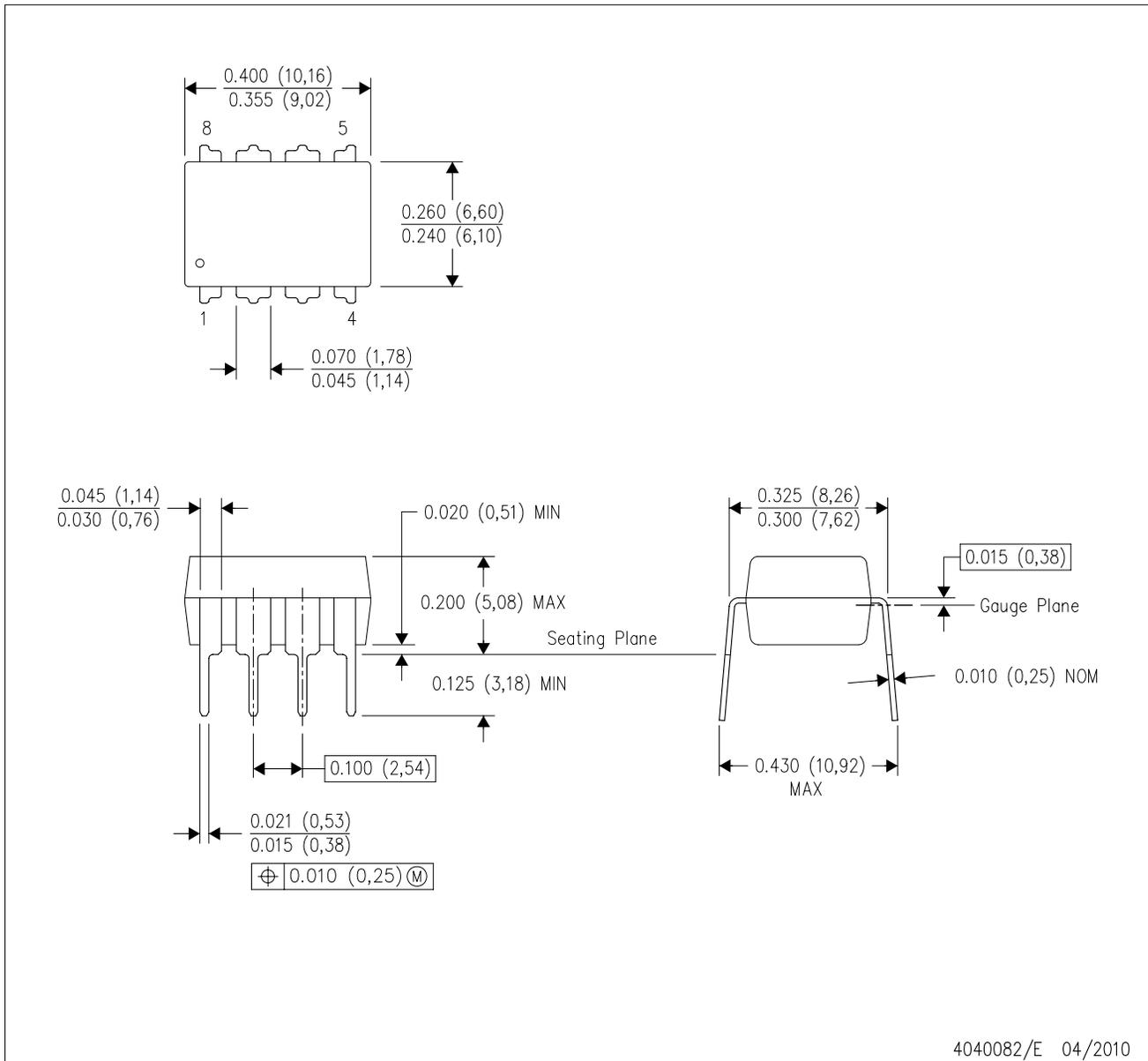
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

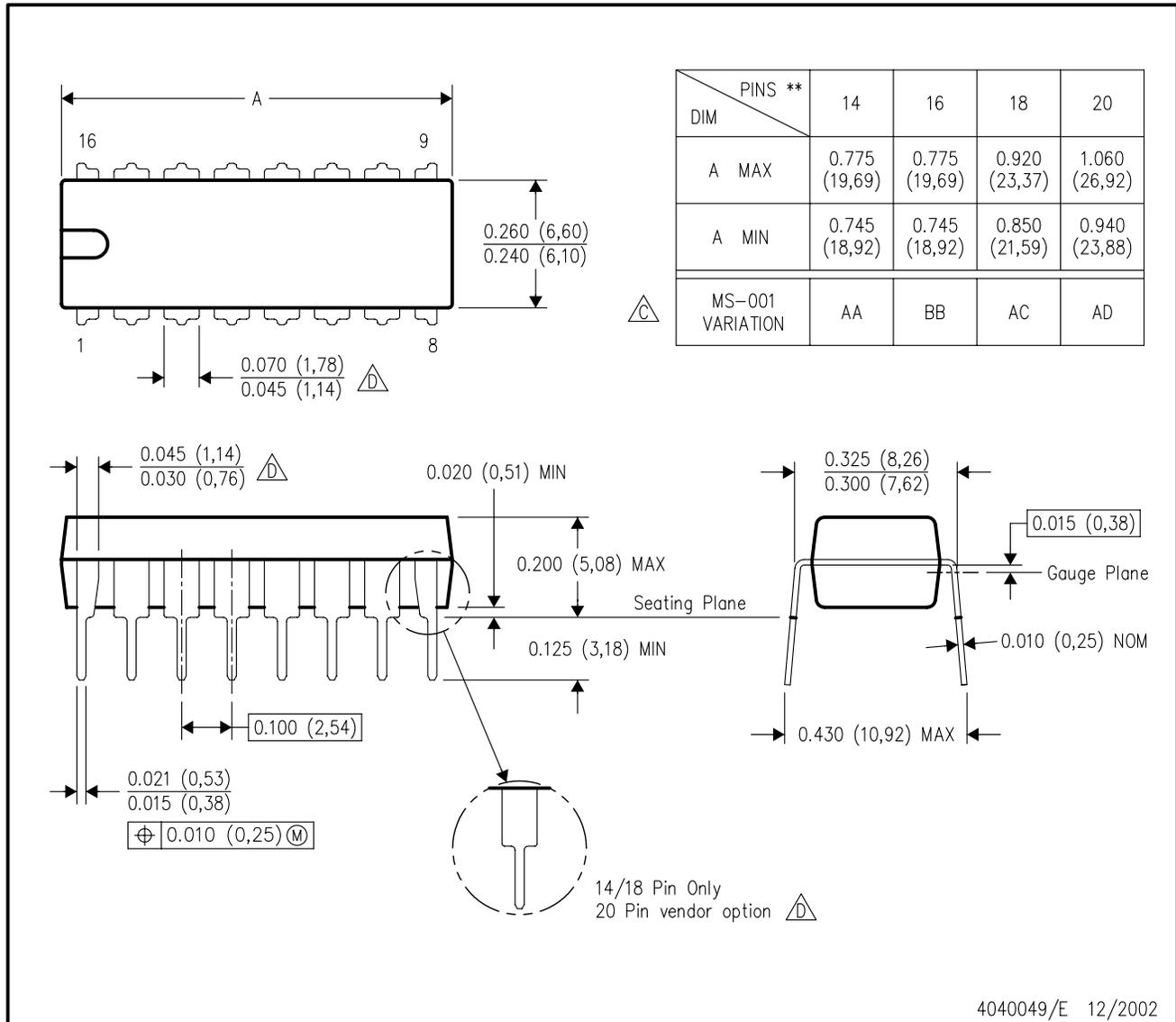


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

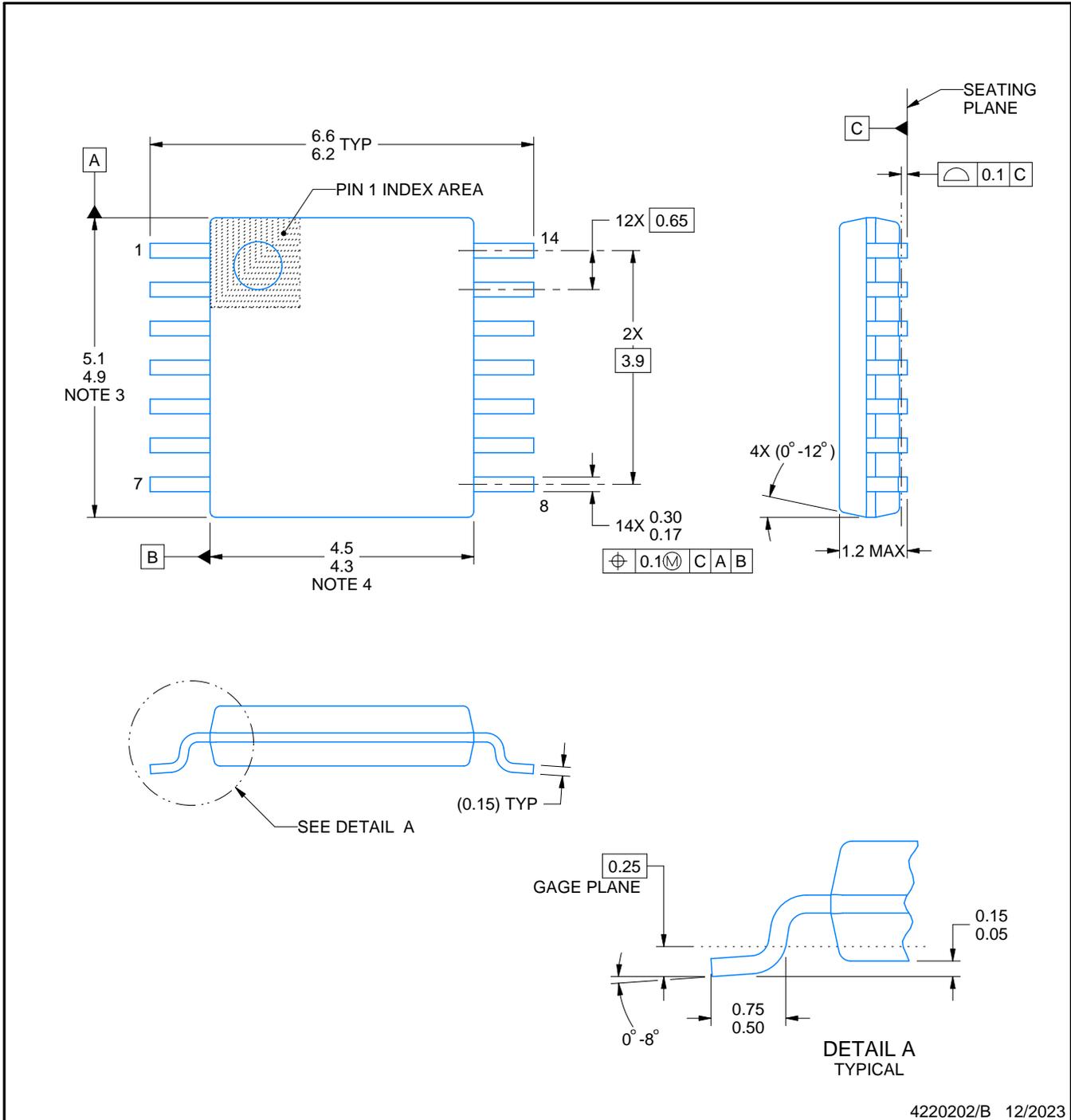
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

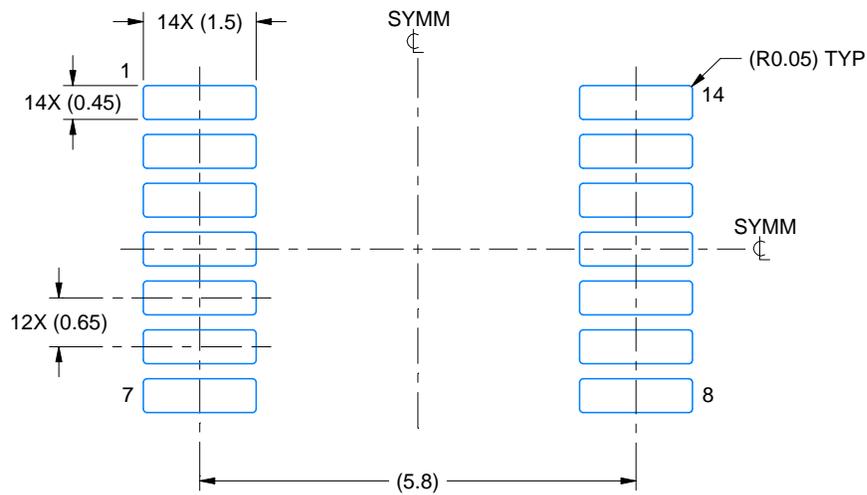
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

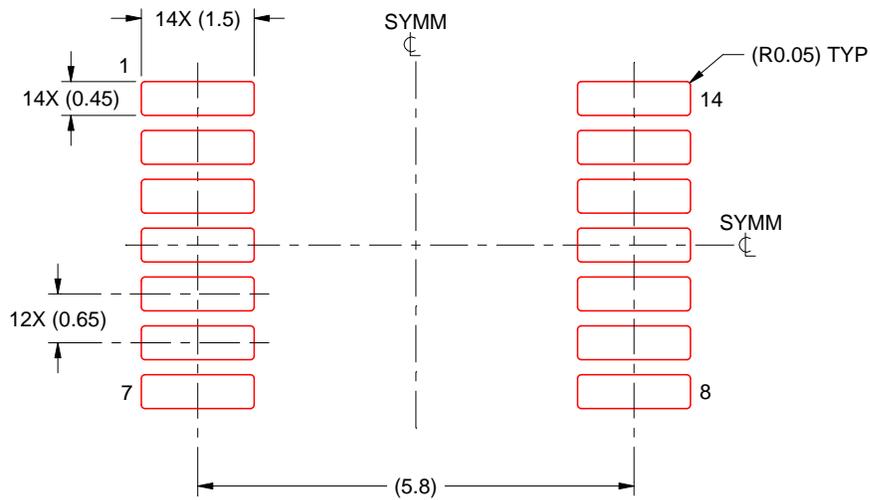
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

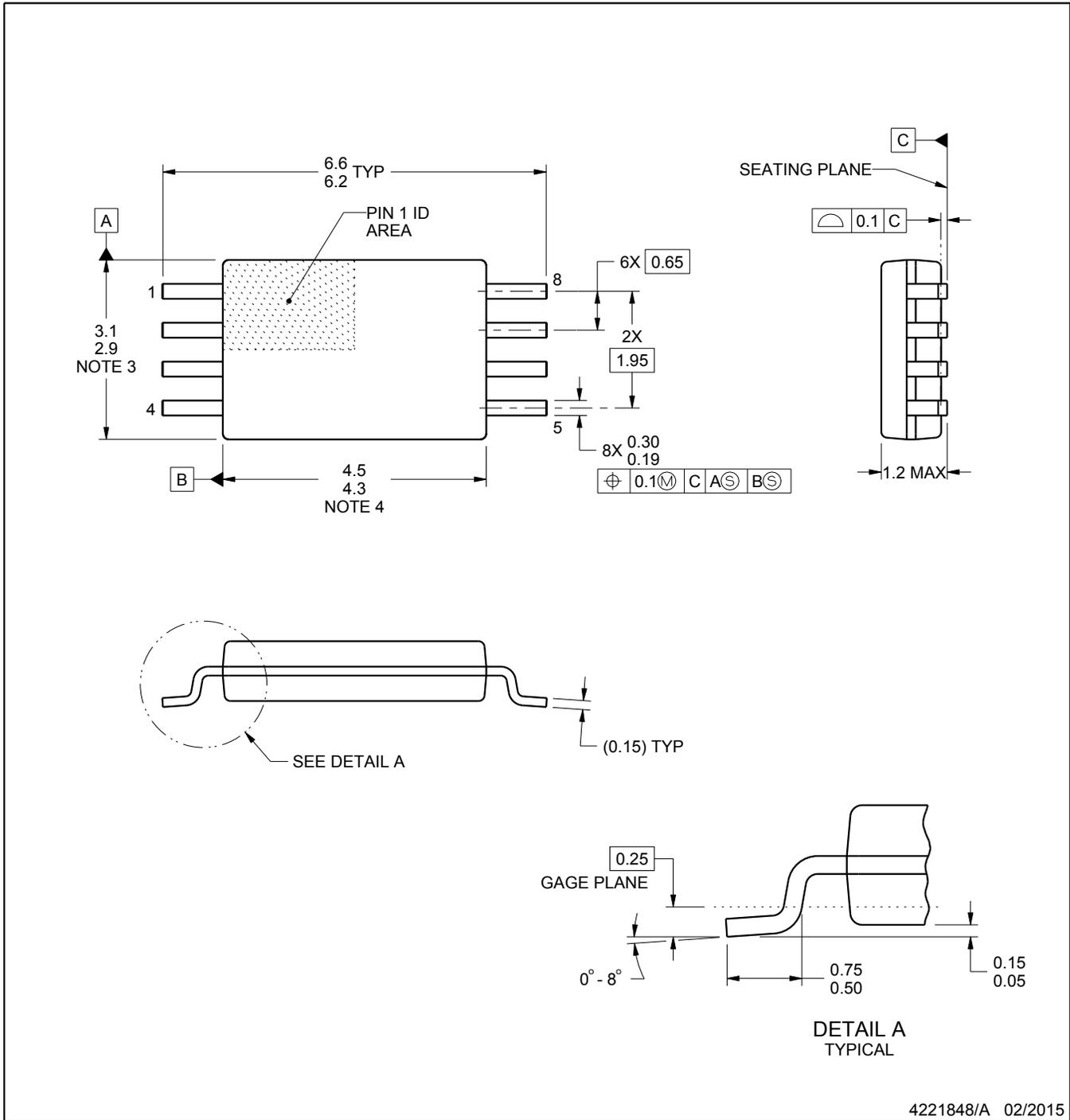
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

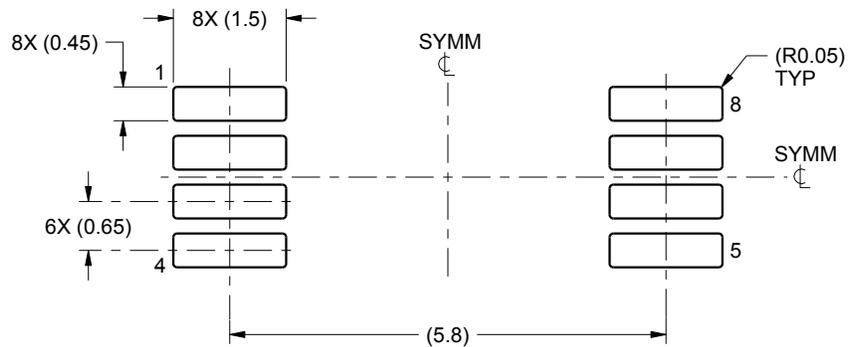
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

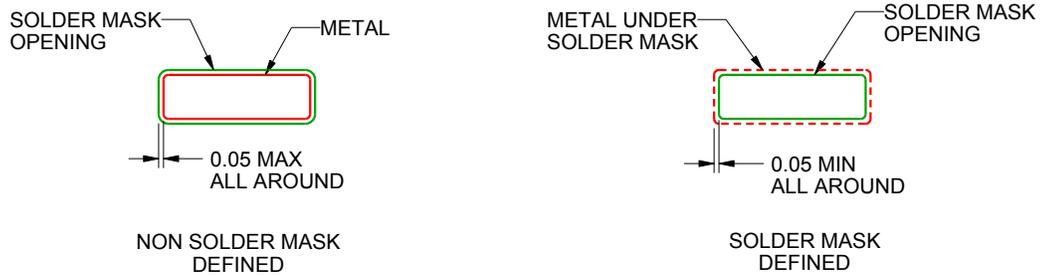
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

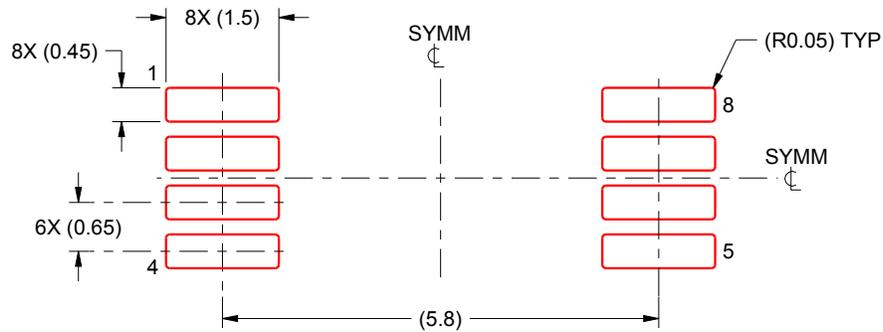
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月