THVD1400V 具有灵活 I/O 电源、压摆率控制和集成 IEC ESD 保护功能的 3V 至 5.5V RS-485 收发器

1 特性

- 符合或超出 TIA/EIA-485A 标准要求
- 3V 至 5.5V RS-485 电源电压
- 差分输出超过 2.1V，在 5V 电源下与 PROFIBUS 兼容
- 用于逻辑信号接口的 1.65V 至 5.5V 电源
- 半双工 RS-422/RS-485
- 最大数据速率可配置
  - SLR = 高：500kbps
  - SLR = 低电平或悬空：20Mbps
- 总线 I/O 保护
  - ±16kV HBM ESD
  - ±12kV IEC 61000-4-2 接触放电
  - ±12kV IEC 61000-4-2 空气间隙放电
  - ±4kV IEC 61000-4-4 快速瞬变脉冲
  - ±16V 总线故障保护（总线引脚上的绝对最大电压）
- 工业级工作温度范围：-40°C 至 125°C
- 低功耗
  - 关断电源电流 < 5μA
  - 运行期间静态电流 < 3mA
- 适用于热插拔功能的无干扰上电/断电
- 开路、短路和空闲总线失效防护
- 1/8 单位负载（多达 256 个总线节点）
- 节省空间的小型高效散热型 10 引脚 VSON 封装 (3mm x 3mm)

2 应用

- 工厂自动化与控制
- 楼宇自动化
- 电机驱动
- 电力输送
- 工业运输
- HVAC 系统
- 智能电表
- 通信基础设施

3 说明

THVD1400 是一款适用于工业应用的半双工 RS-422/ RS-485 收发器。该器件具有 3V 至 5.5V 的总线电源电压、1.65V 至 5.5V 的低电平逻辑接口支持等特性。该器件具有压摆率选择功能，因此可在两种最大速度（根据 SLR 引脚设置）下使用。

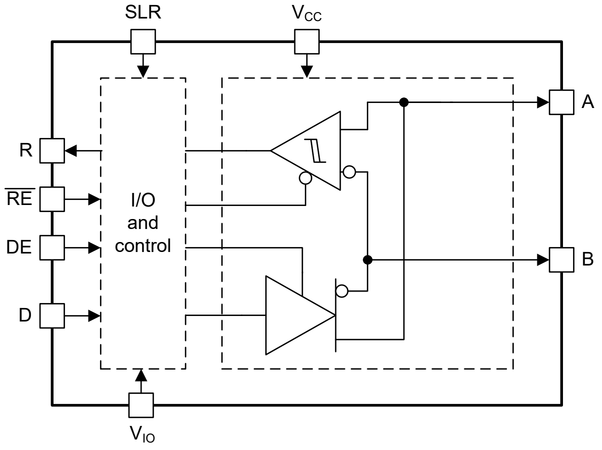
单独的逻辑电源引脚可使 MCU 和 RS-485 收发器在使用不同电源运行时，无需额外的电平转换器。这些总线引脚可耐受高级别的 IEC 接触放电 ESD 事件，因此无需使用其他系统级保护元件。总线引脚具备宽共模电压范围和低输入泄漏，从而使这些器件适用于长线缆上的多点应用。

THVD1400V 采用节省空间的高效散热型 10 引脚 VSON 封装 (3mm x 3mm)。该器件的额定温度范围为 -40°C 至 125°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
THVD1400V	VSON (10)	3mm x 3mm

(1) 有关详细信息，请参阅 节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



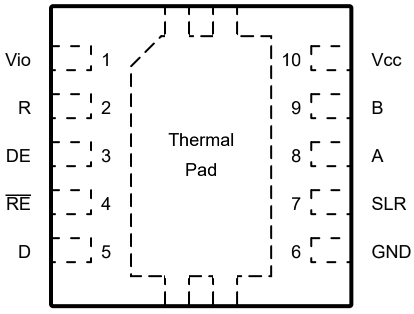
简化版应用

English Data Sheet: SLLSFU3

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 3
5 Specifications 4
  5.1 Absolute Maximum Ratings 4
  5.2 ESD Ratings 4
  5.3 ESD Ratings [IEC] 4
  5.4 Recommended Operating Conditions 5
  5.5 Thermal Information 5
  5.6 Power Dissipation 5
  5.7 Electrical Characteristics 6
  5.8 Switching Characteristics_500 kbps 8
  5.9 Switching Characteristics_20 Mbps 9
  5.10 Typical Characteristics 10
6 Parameter Measurement Information 12
7 Detailed Description 14
  7.1 Overview 14
  7.2 Functional Block Diagrams 14
  7.3 Feature Description 14
  7.4 Device Functional Modes 14
8 Application Information Disclaimer 16
  8.1 Application Information 16
  8.2 Typical Application 16
  8.3 Power Supply Recommendations 22
  8.4 Layout 22
9 Device and Documentation Support 23
  9.1 Device Support 23
  9.2 接收文档更新通知 23
  9.3 支持资源 23
  9.4 Trademarks 23
  9.5 静电放电警告 23
  9.6 术语表 23
10 Revision History 23
11 Mechanical, Packaging, and Orderable Information 23

4 Pin Configuration and Functions



Not to scale

图 4-1. VSON (DRC) Package, 10-Pins (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
V_{IO}	1	Logic Supply	Supply for logic I/O signals (R, $\overline{RE}$, D, DE, and SLR)
R	2	Digital output	Logic output RS-485 data
DE	3	Digital input	Driver enable/disable. Internal pull-down. Driver disabled by default
$\overline{RE}$	4	Digital input	Receiver enable/disable. Internal pull-up. Receiver disabled by default
D	5	Digital input	Logic input RS485 data. Internal pull-up. Drives the bus high by default if driver is enabled
GND	6	GND	Ground
SLR	7	Digital input	Slew rate control. Internal pull-down, default 20 Mbps operation. Logic high SLR enables slow speed (500 kbps)
A	8	Bus input/output	RS-485 bus pin. This pin is non-inverting driver output or non-inverting receiver input
B	9	Bus input/output	RS-485 bus pin. This pin is inverting driver output or inverting receiver input
V_{CC}	10	Power	3 V to 5.5 V supply
Thermal Pad		--	Connect to GND for optimal thermal and electrical performance

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	-0.5	7	V
Supply voltage	V_{CC}	–0.5	7	V
Bus voltage	Voltage at any bus pin (A or B) with respect to GND	–16	16	V
Differntial bus voltage	Max differential voltage between A and B V_{DIFF} = (A - B)	-16	16	V
Input voltage	Range at any logic pin (D, DE, SLR, or $\overline{RE}$)	–0.3	V_{IO} + 0.2,7	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals (A, B) and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)[1]		–7		12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$, SLR inputs)		0.7^*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$, SLR inputs)		0		0.3^*V_{IO}	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8 V or 2.5 V	–4		4	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3 V or 5 V	–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	SLR = V_{IO}			500	kbps
		SLR = GND or floating			20	Mbps
T_A [2]	Operating ambient temperature		-40		125	°C
T_J [2]	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches typical 170°C.

5.5 Thermal Information

THERMAL METRIC[1]		THVD1400V	UNIT
		DRC (VSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.4	°C/W

(1) For more information about traditional and new thermalmetrics, see the see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, D = square wave 50% duty	Unterminated; R_L= 300 Ω, C_L = 50 pF	SLR = H	500 kbps	60	100	mW
			SLR = L	20Mbps	180	220	mW
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, D = square wave 50% duty	RS-422 load; R_L= 100 Ω, C_L = 50 pF	SLR = H	500 kbps	100	150	mW
			SLR = L	20Mbps	200	250	mW
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, D = square wave 50% duty	RS-485 load; R_L= 54 Ω, C_L = 50 pF	SLR = H	500 kbps	175	230	mW
			SLR = L	20Mbps	250	300	mW

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD} \rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, $-7\ V \le V_{test} \le 12\ V$ (See 图 6-1)		1.5	3.3		V
		R_L = 60 Ω, $-7\ V \le V_{test} \le 12\ V$, $4.5\ V \le V_{CC} \le 5.5\ V$ (See 图 6-1)		2.1	3.3		V
		R_L = 100 Ω (See 图 6-2)		2	4		V
		R_L = 54 Ω, $4.5\ V \le V_{CC} \le 5.5\ V$ (See 图 6-2)		2.1	3.3		V
		R_L = 54 Ω (See 图 6-2)		1.5	3.3		V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage	R_L = 54 Ω or 100 Ω (See 图 6-2)		-50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See 图 6-2)			$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See 图 6-2)		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	R_L = 54 Ω , V_{CC} = 3.3 V, DE = H, D = 20 Mbps square wave (See 图 6-2)			375		mV
I_{OS}	Short-circuit output current	DE = V_{IO}, $-7\ V \le (V_A \text{ or } V_B) \le 12\ V$, or A shorted to B		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V		85	100	μA
			$V_I = -7$ V	-100	-70		μA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of - 7 V to 12 V			- 85	- 45	mV
V_{TH-}	Negative-going input threshold voltage(1)			-200	-150		mV
V_{HYS}	Input hysteresis			25	50		mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz			20		pF
V_{OH}	Output high voltage	$I_{OH} = -8$ mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	I_{OL} = 8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V_{OH}	Output high voltage	$I_{OH} = -4$ mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	I_{OL} = 4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	V_O = 0 V or V_{IO}, $\overline{RE} = V_{IO}$		-2		2	μA
Logic							
I_{IN}	Input current (D, $\overline{RE}$, DE , SLR)	$3\ V \le V_{IO} \le 5.5\ V$, $0\ V \le V_{IN} \le V_{IO}$		-5		5	μA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	170		°C
T_{HYS}	Thermal shutdown hysteresis				15		°C
Supply							
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}				2.5	2.7	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}			2	2.1		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				400		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}				1.4	1.6	V
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}			1.2	1.3		V

5.7 Electrical Characteristics （续）

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				100		mV
I_{CC}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		1.5	3	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		1.4	2.5	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		0.8	1.25	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		0.2	4	µA
I_{CC}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		1.4	2.1	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		1	1.6	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		0.7	1.1	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		0.2	4	µA
I_{IO}	Logic supply current (quiescent), V_{IO} = 3 V to 3.6 V	Driver disabled, Receiver enabled, SLR = GND	DE = 0 V, $\overline{RE}$ = 0 V, No load		10	18	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}	DE = 0 V, $\overline{RE}$ = 0 V, No load		13	22	µA
		Driver disabled, Receiver disabled, SLR = GND	DE = 0 V, $\overline{RE}$ = V_{IO}, No load		2	3	µA
		Driver disabled, Receiver disabled, SLR = V_{IO}	DE = 0 V, $\overline{RE}$ = V_{IO}, No load		5	7	µA

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(1) V_{TH+} is specified to be at least V_{HYS} higher than V_{TH-}.

5.8 Switching Characteristics_500 kbps

500-kbps (with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V and V_{IO} = 3.3 V, unless otherwise noted.

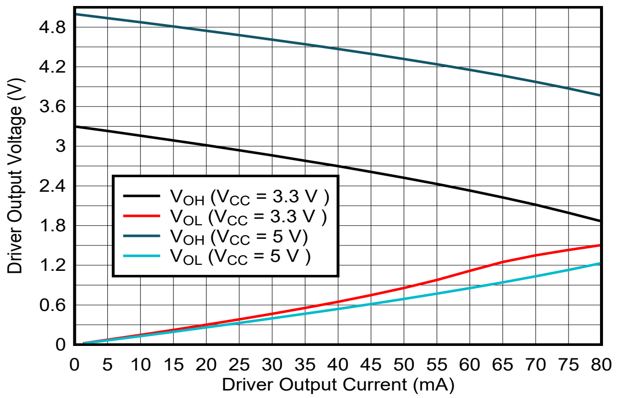
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3V	200	250	600	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	200	270	600	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3V		200	500	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		180	450	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH}\rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3V		2	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 6-4 and 图 6-5		80	200	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			200	650	ns
		$\overline{RE}$ = V_{IO}			6	13	μs
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 6-6		5	20	ns
t_{PHL}, t_{PLH}	Propagation delay				30	90	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH}\rvert$				4	6	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X, V_{IO} < 3 V	See 图 6-7		20	65	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X, $V_{IO} \geqslant$ 3 V				50	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}, V_{IO} < 3 V			80	170	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}, $V_{IO} \geqslant$ 3 V			80	155	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 6-8		7	14	μs

5.9 Switching Characteristics_20 Mbps

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

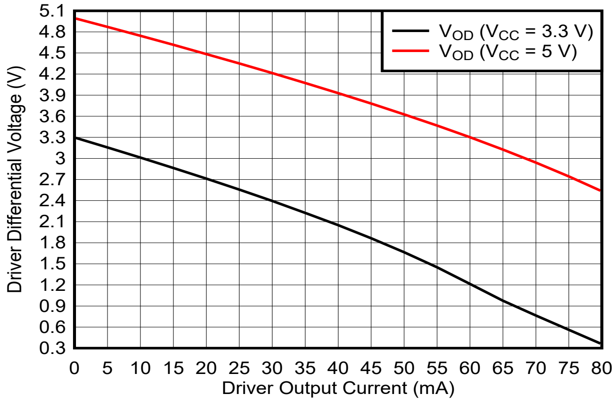
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V		6	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		6	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		25	50	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		20	40	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	6	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	6	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 6-4 and 图 6-5		25	50	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			30	70	ns
		$\overline{RE}$ = V_{IO} , V_{IO} = 1.65 V to 2.75 V			6	13	μs
		$\overline{RE}$ = V_{IO} , V_{IO} = 3 V to 5.5 V			6	13	μs
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 6-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF			30	90	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$	C_L = 15 pF, $V_{IO} < 2.25$ V				6	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$	C_L = 15 pF, $V_{IO} \geqslant 2.25$ V				8	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X, $V_{IO} < 3$ V	See 图 6-7		20	65	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X, $V_{IO} \geqslant 3$ V				50	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}, $V_{IO} < 3$ V			80	170	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}, $V_{IO} \geqslant 3$ V			80	155	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 6-8		6	14	μs

5.10 Typical Characteristics



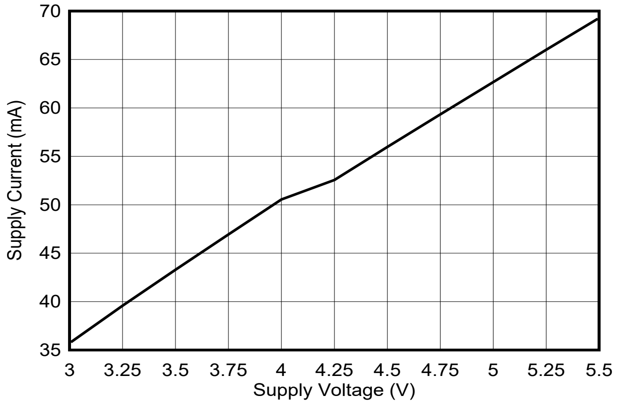
DE = V_{IO} T_A = 25°C

图 5-1. Driver Output voltage vs Driver Output Current



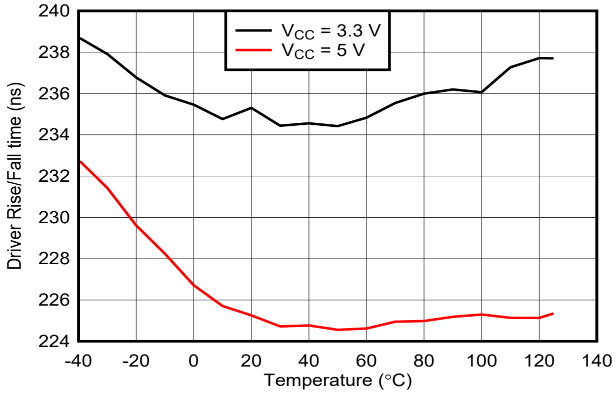
DE = V_{IO} D = 0 V T_A = 25°C

图 5-2. Driver Differential Output voltage vs Driver Output Current



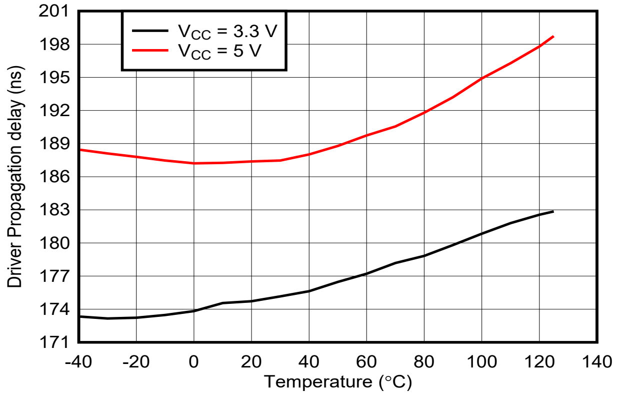
R_L = 54 Ω DE = V_{IO} D = V_{IO}
T_A = 25°C

图 5-3. Supply Current vs Supply Voltage



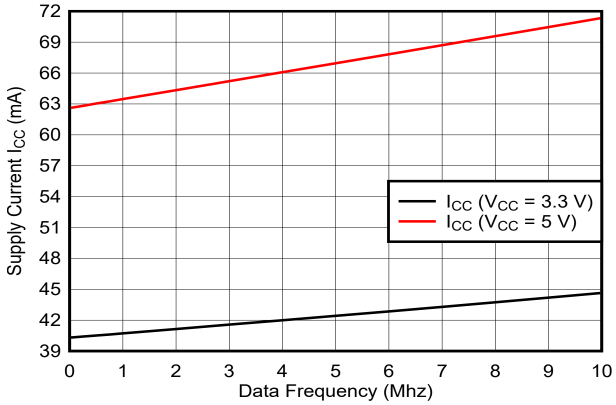
R_L = 54 Ω C_L = 50 pF

图 5-4. Driver Rise or Fall Time vs Temperature (500 kbps)



R_L = 54 Ω C_L = 50 pF

图 5-5. Driver Propagation Delay vs Temperature (500 kbps)



R_L = 54 Ω T_A = 25 °C

图 5-6. Supply Current vs Signal Rate (500 kbps)

5.10 Typical Characteristics (continued)

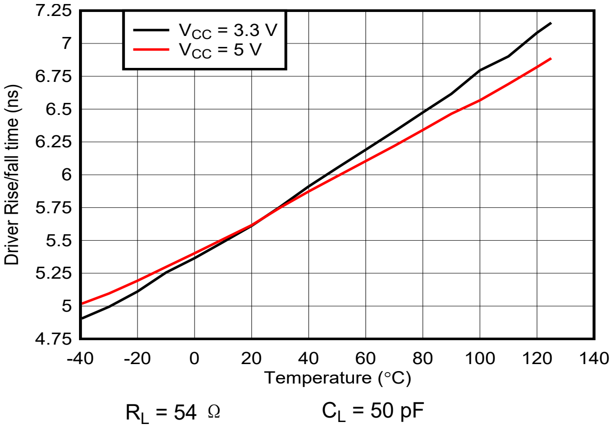


图 5-7. Driver Rise and Fall Time vs Temperature (20 Mbps)

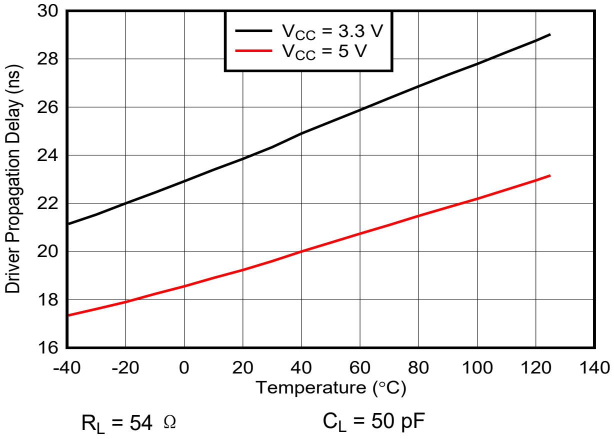


图 5-8. Driver Propagation Delay vs Temperature (20 Mbps)

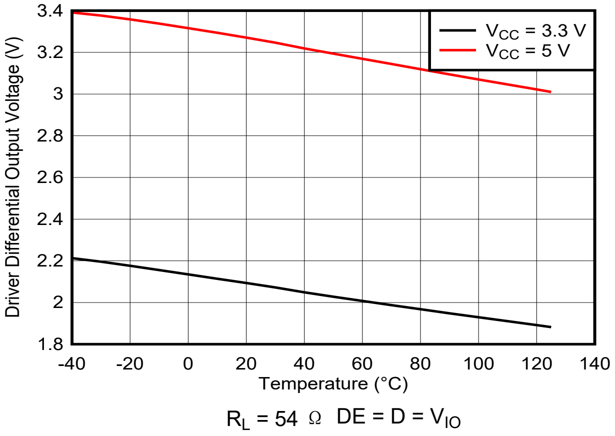


图 5-9. Driver Differential Output voltage vs Temperature

6 Parameter Measurement Information

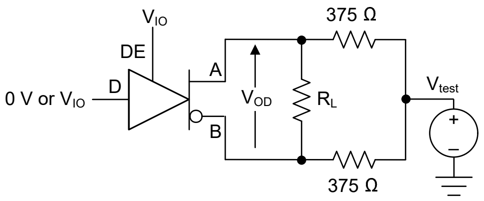


图 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

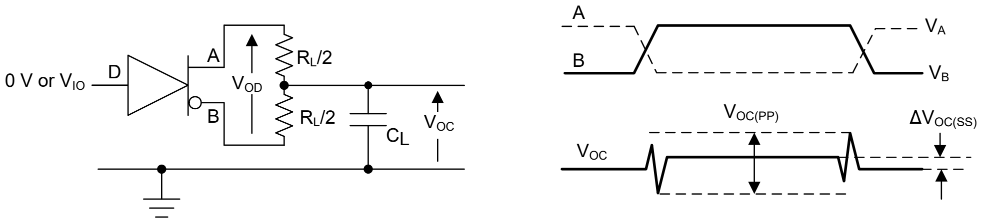


图 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

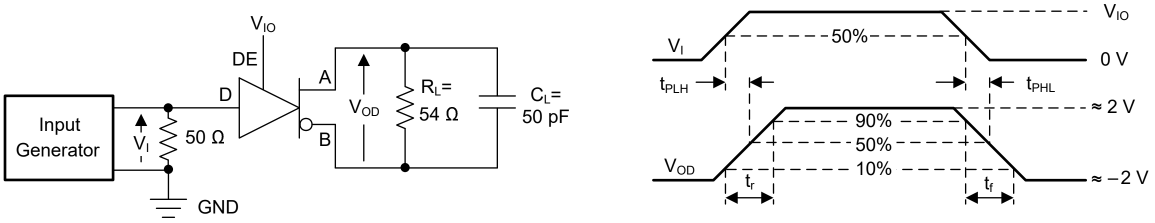


图 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

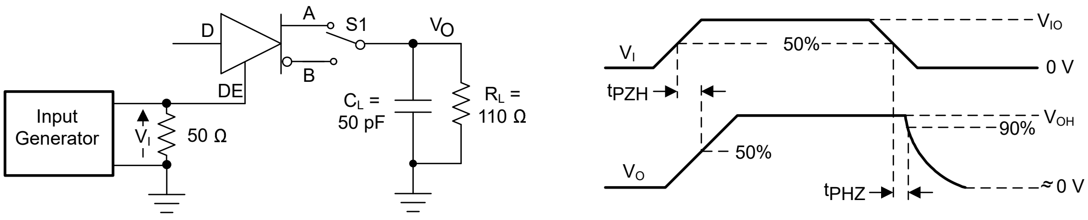


图 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

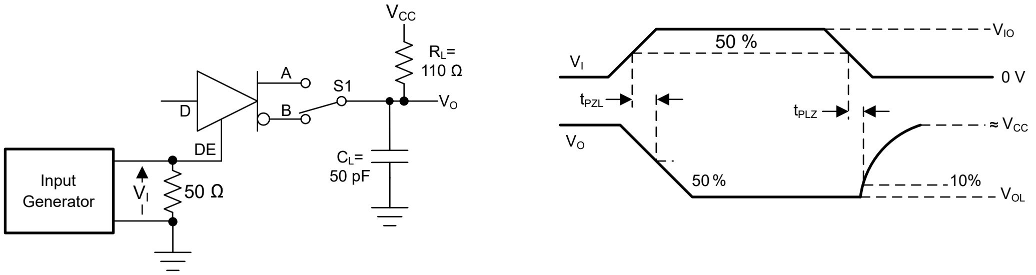


图 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

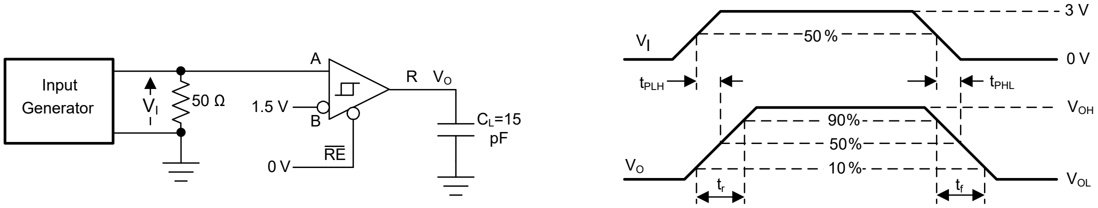


图 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

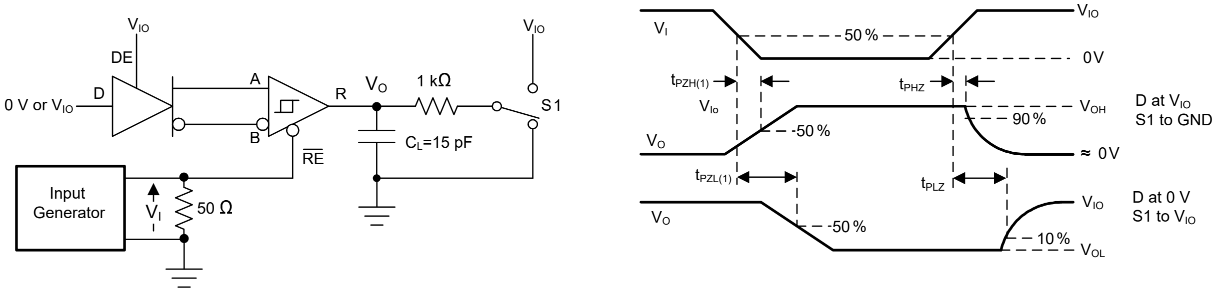


图 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

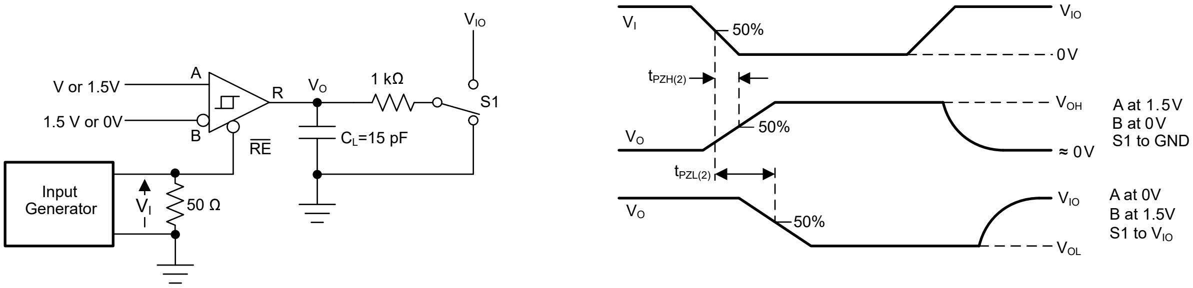


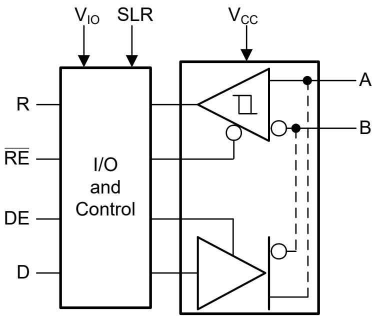
图 6-8. Measurement of Receiver Enable Times With Driver Disabled

7 Detailed Description

7.1 Overview

The THVD1400V is a half duplex RS-485 transceiver. The device has slew rate control pin SLR which can be used to set the device in maximum 20 Mbps mode or slew rate limited 500 kbps mode. THVD1400V also has low level logic interface V_{IO} pin to run RS-485 bus at 3 to 5.5 V supply, while the microcontroller can be at any voltage between 1.65 V to 5.5 V. This feature eliminates any level shifter that may be otherwise needed between the microcontroller and the RS-485 transceiver.

7.2 Functional Block Diagrams



7.3 Feature Description

The THVD1400V operates from 3 V to 5.5 V bus supply and 1.65 to 5.5 V logic supply. For applications wanting to keep same bus supply and logic supply, V_{CC} and V_{IO} can be shorted on PCB. Internal ESD protection circuits on bus pins protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV (Contact Discharge), ±12 kV (Air Gap Discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this condition, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 7-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go fail safe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 7-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

7.4.1 Operational Data rate

THVD1400V can be used in slow speed or fast speed RS-485 networks by configuring Slew rate control (SLR) pin. 表 7-3 describes slew rate control function.

表 7-3. Slew rate control function table

Signal state	Driver	Receiver	Comment
SLR = V_{IO}	Maximum speed of operation = 500kbps	Maximum speed of operation = 500kbps	Active high slew rate limiting applied on driver output and glitch filter in receiver path enabled
SLR = GND or floating	Maximum speed of operation = 20Mbps	Maximum speed of operation = 20Mbps	Slew rate limiting on driver output disabled and glitch filter in receiver path disabled

7.4.2 Protection Features

THVD1400V has in-built protection features such as supply undervoltage, bus short circuit and thermal shutdown.

Supply undervoltage protection is present on both V_{CC} and V_{IO} supply. This maintains the bus output and receiver logic output in known driven state when the supply is above the rising undervoltage threshold. 表 7-4 describes the device behavior in various scenarios of supply levels.

表 7-4. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
$> UV_{VCC(rising)}$	$> UV_{VIO(rising)}$	Determined by DE and D inputs	Determined by $\overline{RE}$ and A-B
$< UV_{VCC(falling)}$	$> UV_{VIO(rising)}$	High impedance	Undetermined
$> UV_{VCC(rising)}$	$< UV_{VIO(falling)}$	High impedance	High impedance
$< UV_{VCC(falling)}$	$< UV_{VIO(falling)}$	High impedance	High impedance

Bus terminals are protected against high voltage short circuit events up to ± 16 V. Additionally, bus short circuit current is limited to 250 mA. In events like bus contention when multiple drivers are driving the bus simultaneously, the current through the bus terminals is internally limited. If the power dissipation makes the junction temperature cross 150°C, thermal shutdown is activated which disables the driver and receiver and reduces the on-chip power dissipation. The device is enabled once the junction temperature falls by the thermal shutdown hysteresis as specified in electrical parameter section of the data sheet.

8 Application Information Disclaimer

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The THVD1400V is a half duplex RS-485 transceiver used for asynchronous data transmissions. The driver and receiver enable pins, slew rate control pins allow the device to be applicable for various point-to-point, multipoint or multidrop network configurations.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length. 图 8-1 shows the two end nodes terminated, while remaining nodes are unterminated.

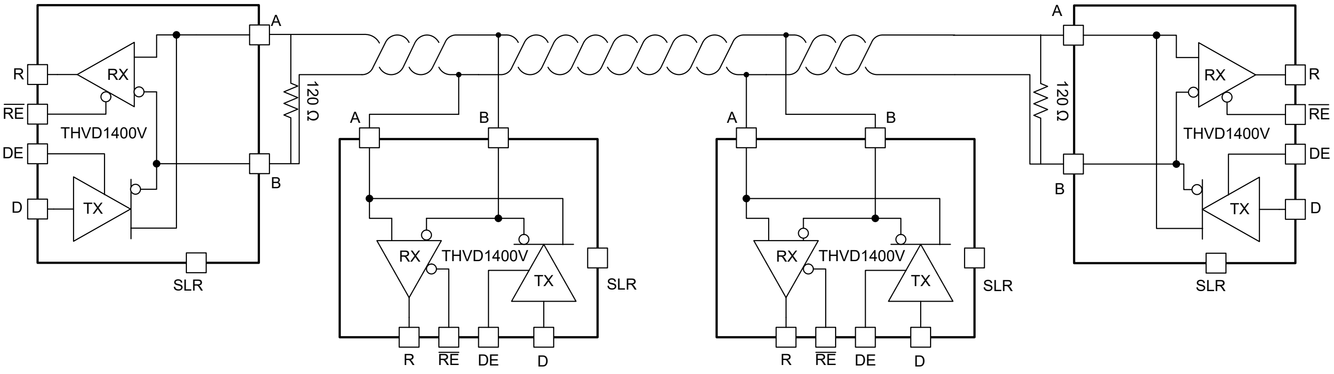


图 8-1. Typical Half Duplex RS-485 Network With all Nodes Using THVD1400V

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5% or 10%.

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{(STUB)} \leqslant 0.1 \times t_r \times v \times c \qquad (1)$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

THVD1400V can be used in both slow speed and high speed networks with SLR pin configurability. Slew rate limiting makes the driver output rise or fall time slower so that stub lengths can be increased.

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1400V consists of 1/8 UL transceivers, connecting up to 256 transceivers to the bus is possible.

8.2.1.4 Receiver Failsafe

The differential receiver of the THVD1400V is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, V_{TH-}, and V_{HYS} (the separation between V_{TH+} and V_{TH-}). As shown in the 表 7-2, differential signals more negative than –200 mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

8.2.1.5 Transient Protection

The bus pins of the THVD1400V transceiver family include on-chip ESD protection against ±16-kV HBM and ±12-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

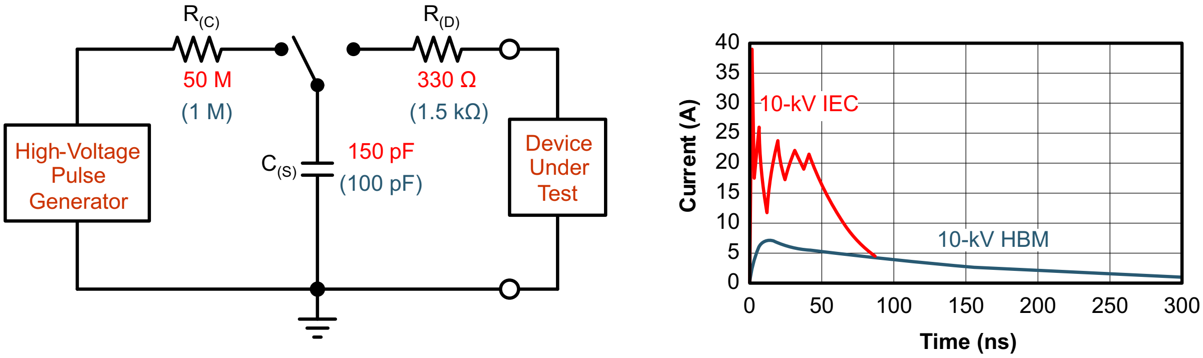


图 8-2. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

图 8-3 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side of the diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which exceed the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side of the diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients may occur in power generation and power-grid systems.

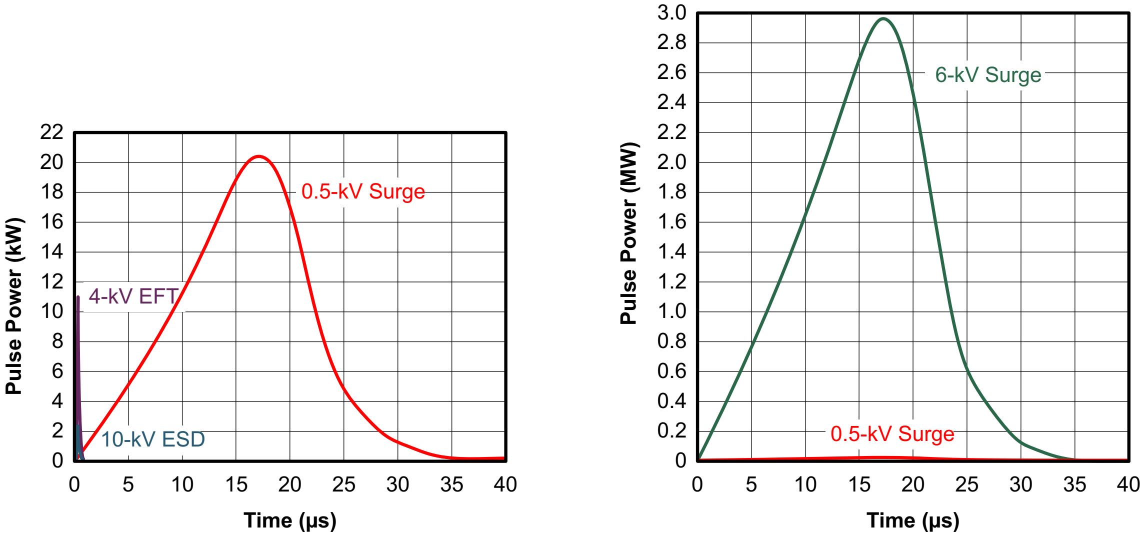


图 8-3. Power Comparison of ESD, EFT, and Surge Transients

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 图 8-4 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

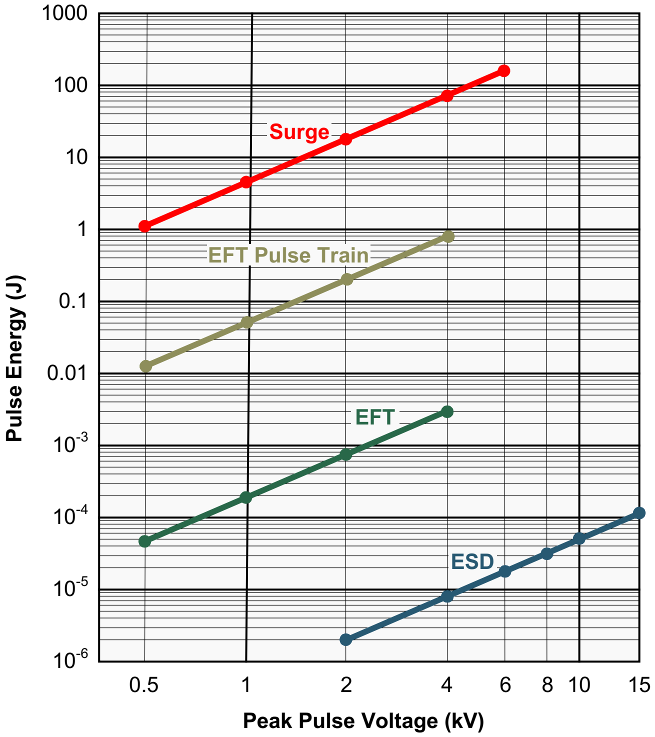


图 8-4. Comparison of Transient Energies

8.2.2 Detailed Design Procedure

To protect bus nodes against high-energy surge transients, the implementation of external transient protection devices is necessary. 图 8-5 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 8-1 shows the associated bill of materials.

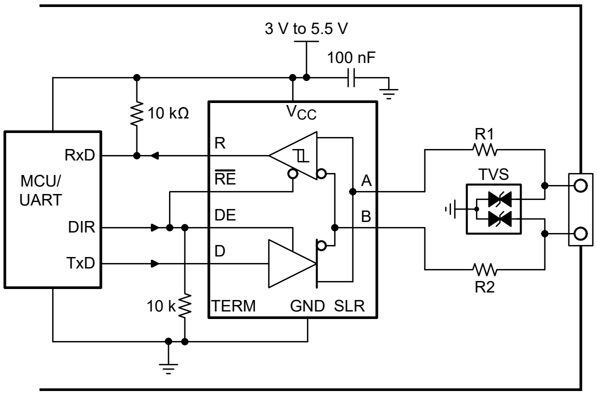


图 8-5. Transient Protection Against Surge Transients for THVD1400V

表 8-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD1400V	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

(1) See the Third Part Disclaimer.

8.2.3 Application Curves

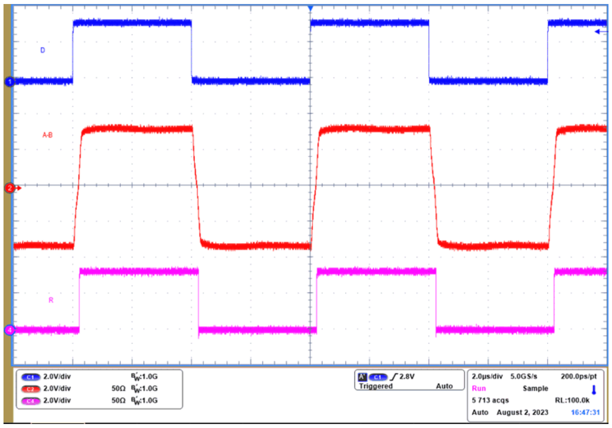


图 8-6. Waveforms at 500 kbps , V_{CC} = 5 V

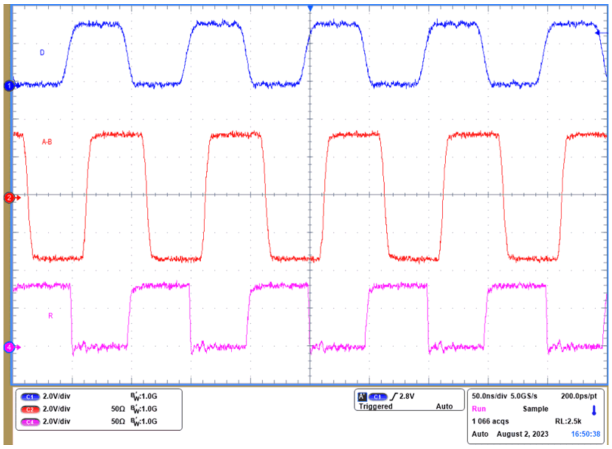


图 8-7. Waveforms at 20 Mbps , V_{CC} = 5 V

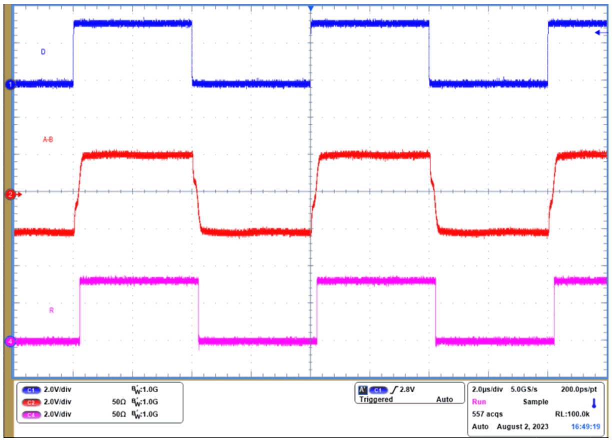


图 8-8. Waveforms at 500 kbps , V_{CC} = 3.3 V

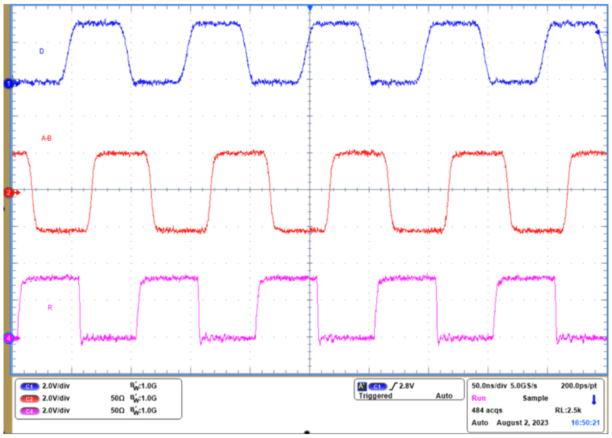


图 8-9. Waveforms at 20 Mbps , V_{CC} = 3.3 V

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pin as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply atleast 100 nF decoupling capacitors as close as possible to the V_{CC} and V_{IO} pin of the transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for logic lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

8.4.2 Layout Example

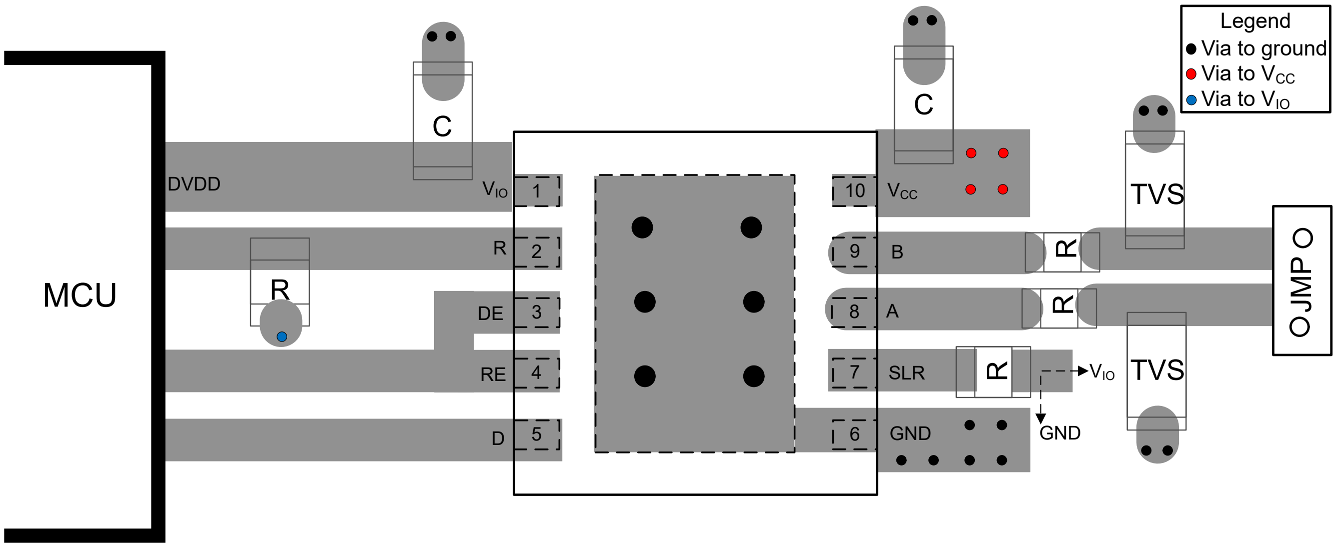


图 8-10. Layout Example for THVD1400V in VSON-10 Package

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1400VDRCR	Active	Production	VSON (DRC) | 10	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1400V
THVD1400VDRCR.A	Active	Production	VSON (DRC) | 10	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1400V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

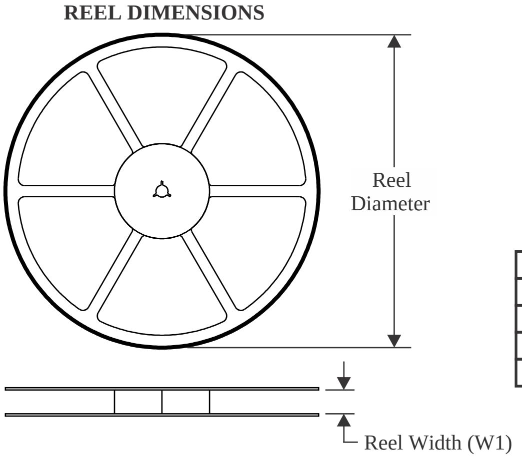
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

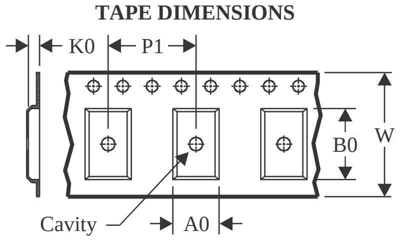
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

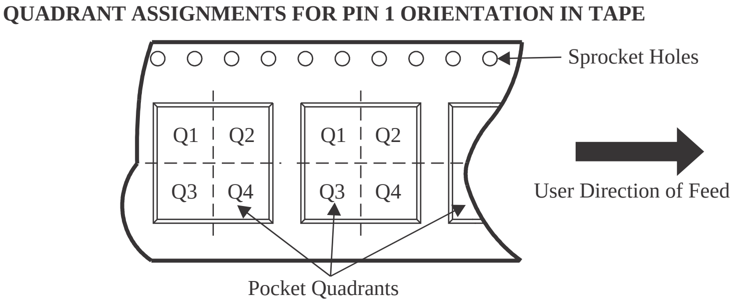
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





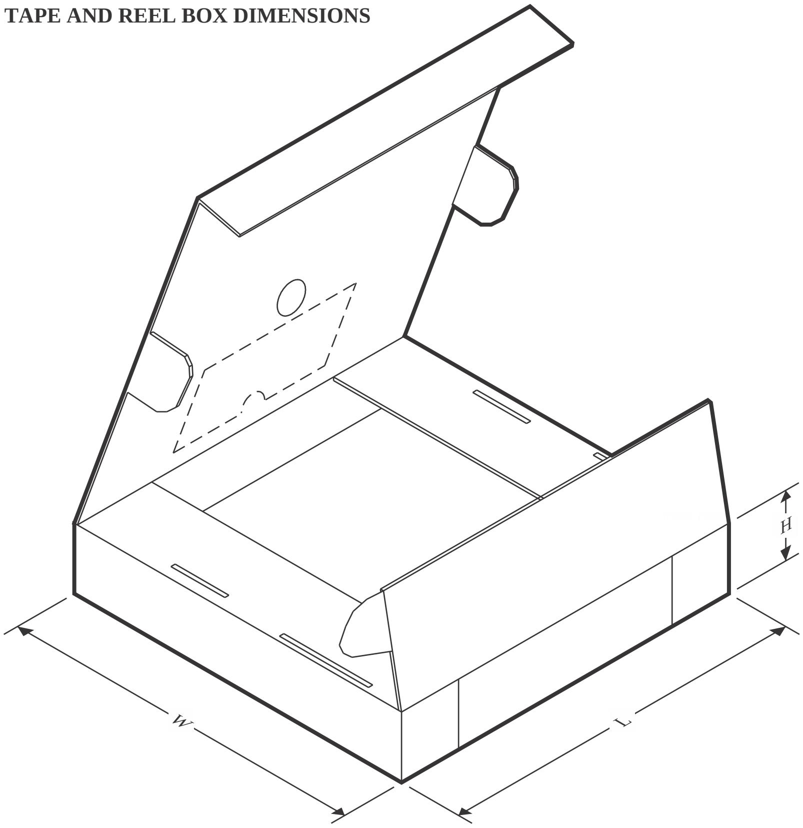
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1400VDRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1400VDRCR	VSON	DRC	10	5000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

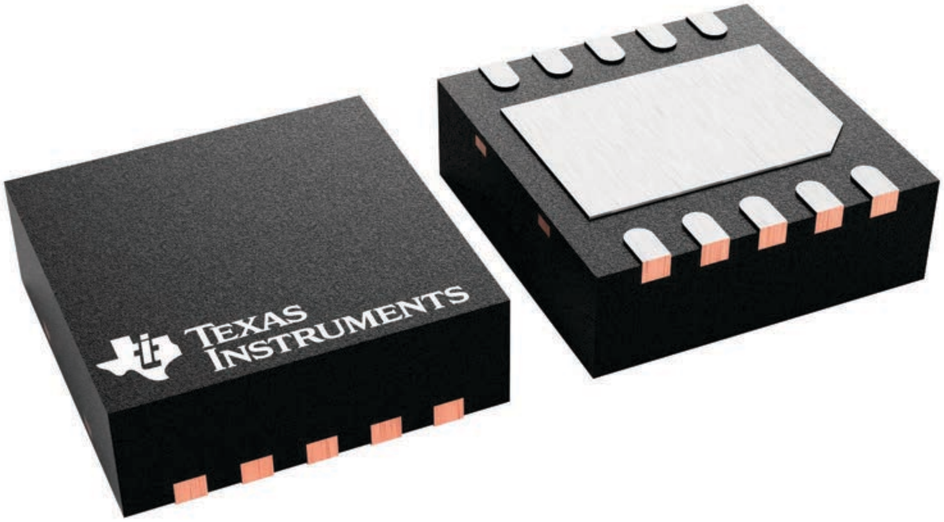
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

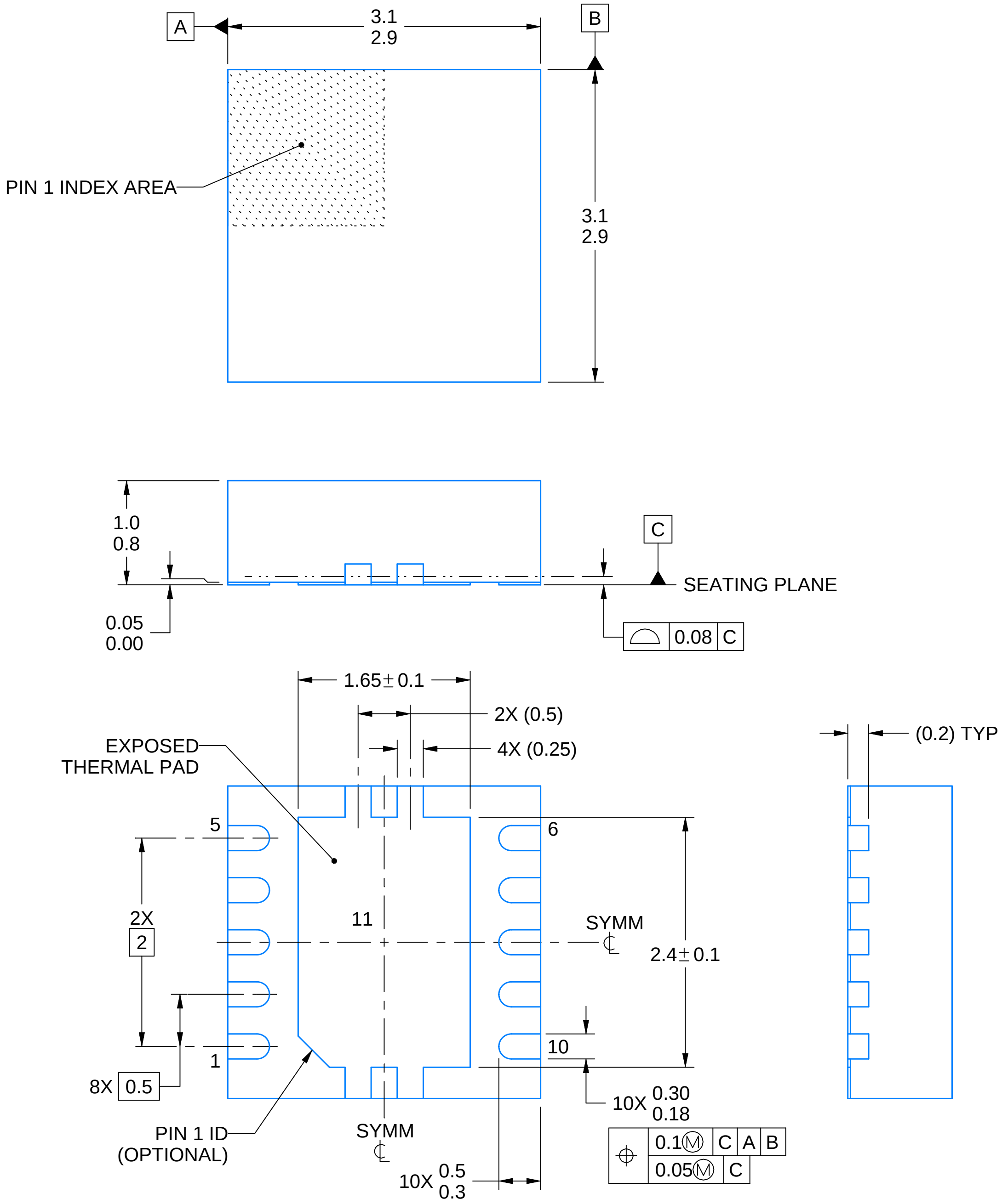


PACKAGE OUTLINE

DRC0010J

VSON - 1 mm max height

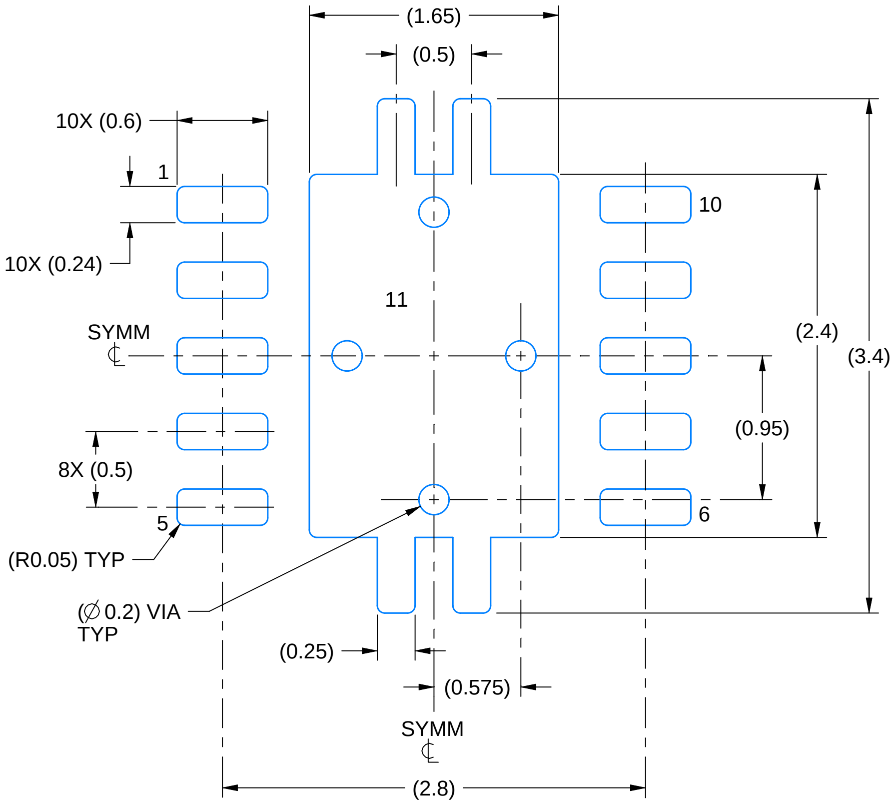
PLASTIC SMALL OUTLINE - NO LEAD



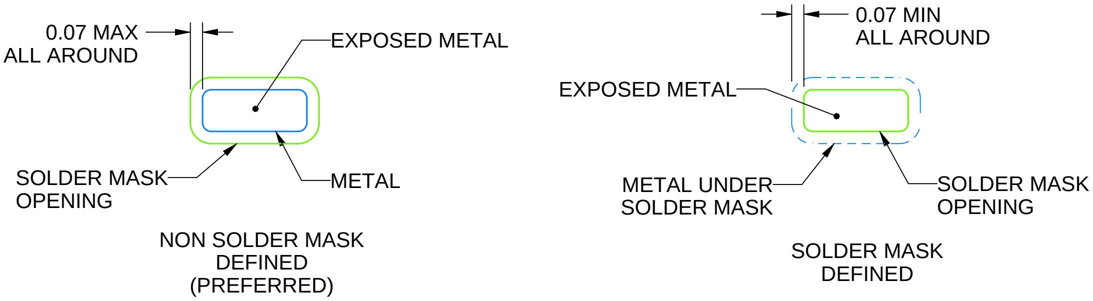
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

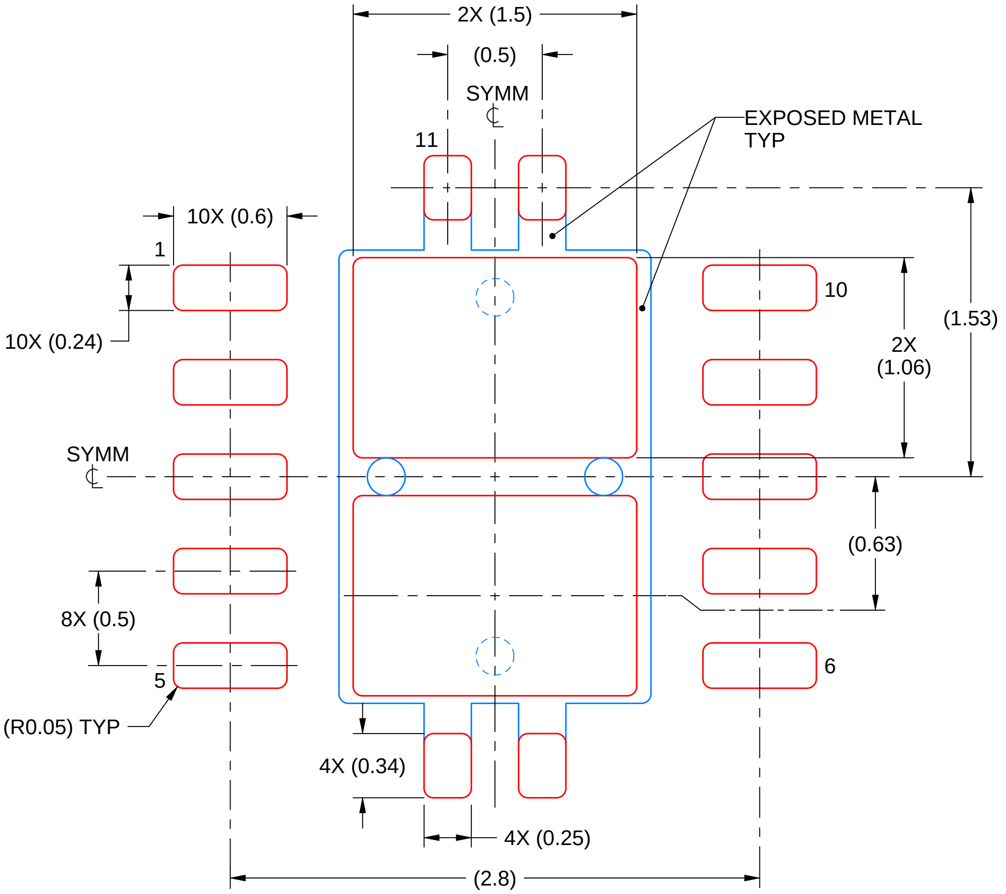


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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