THS6301 G.Fast DSL 线路驱动器放大器（具有带宽和功率调节功能） 特性

1 特性

- 支持 G.Fast 106MHz、212MHz DSL 应用
- 支持传统 VDSL 和 ADSL2+ 应用
- 适合 G.Fast 和传统应用的高 MTPR （线路功率 = 8dBm）：
  - ADSL2+ = 69dB
  - VDSL-17a = 73dB
  - VDSL-30a = 69dB
  - G.Fast 106MHz = 62dB
  - G.Fast 212MHz = 55dB
- 多种电源模式可适应不同外形
- 可通过外部电阻器调节偏置电流
- 低功耗线路端接模式：10.2mA
- 掉电模式
- 12V 技术支持高功率输出

2 应用

- G.Fast 和传统 DSL 线路驱动器
- 通用宽带线路驱动器
- PLC 驱动器
- DAC 输出放大器

3 说明

THS6301 是一款采用单通道电流反馈架构的差分线路驱动器，支持 G.Fast 和不同数字用户线路 (DSL) 家庭网关系统。该器件支持 106MHz 和 212MHz G.Fast 数字用户线路配置文件，使用本地离散多音调制 (DMT) 信号。THS6301 可在 8dBm 线路功率下以 212 MHz 的频率发挥高线性特性。

该器件的独特架构可以最大限度地降低静态电流，同时仍可提供极高的线性特性。对于并不需要该放大器全部性能的线路驱动模式，该器件的内在偏置设置可提供节能效果。为了进一步提高灵活性并节省更多电力，可以通过连接到一个器件引脚的外部偏置电阻器来调节总静态电流。此外，该器件还 具备 两种线路端接模式，以便在非常低的功耗下保持阻抗匹配。

该器件还可用作固定增益差分放大器，可以扩展带宽和功率以适应不同应用的 需求。

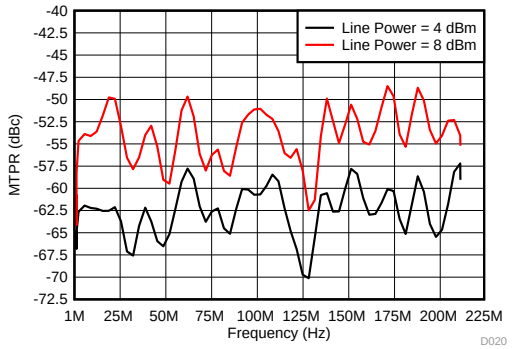
该器件采用 16 引脚 4 x 4mm VQFN 封装。

器件信息(1)

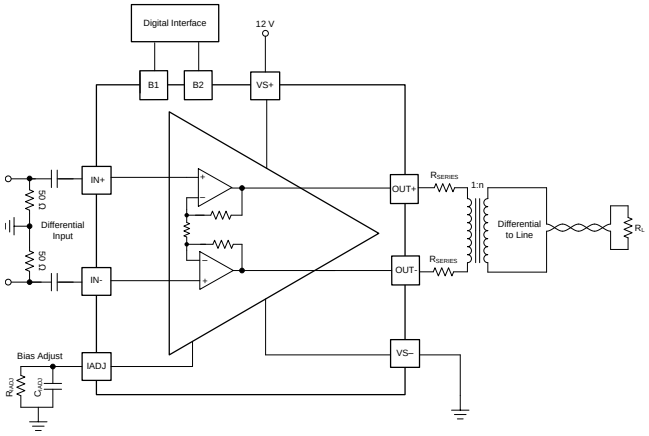
器件型号	封装	封装尺寸（标称值）
THS6301	VQFN (16)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

MTPR G.Fast 212 MHz
（偏置 10，PAR = 15 dB，1/64 丢失音）



多音功率比 **(MTPR)** 图形
（G.Fast，212MHz，8dBm）



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics 5
6.6 Switching Characteristics 9
6.7 Typical Characteristics 10
7 **Detailed Description** 17
7.1 Overview 17
7.2 Functional Block Diagram 17
7.3 Feature Description 18
7.4 Device Functional Modes 19
7.5 Programming 19
8 **Application and Implementation** 20
8.1 Application Information 20
8.2 Typical Application 20
9 **Power Supply Recommendations** 23
10 **Layout** 23
10.1 Layout Guidelines 23
10.2 Layout Example 25
11 器件和文档支持 26
11.1 文档支持 26
11.2 接收文档更新通知 26
11.3 社区资源 26
11.4 商标 26
11.5 静电放电警告 26
11.6 术语表 26
12 机械、封装和可订购信息 26

4 修订历史记录

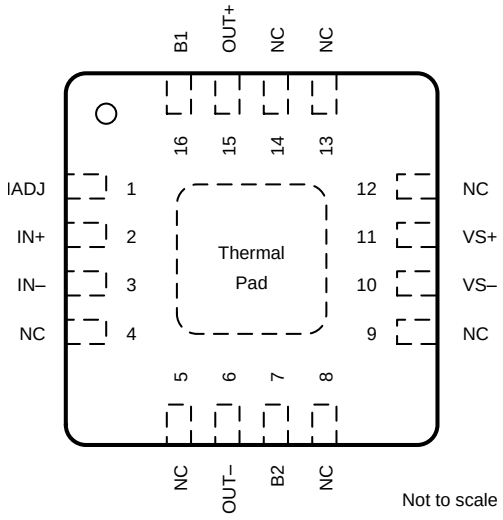
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (April 2018) to Revision A	Page
• 已发布至生产	1

Copyright © 2018, Texas Instruments Incorporated

5 Pin Configuration and Functions

RSA Package
16-Pin VQFN
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
B1	16	I	Most significant bit (MSB), logic level referenced to VS–
B2	7	I	Least significant bit (LSB), logic level referenced to VS–
IADJ	1	—	Bias current reference pin
IN–	3	I	Negative input
IN+	2	I	Positive input
NC	4	—	No internal connection to device (VS– recommended)
NC	5, 8, 9, 12, 13, 14	—	Not connected
OUT–	6	O	Negative output
OUT+	15	O	Positive output
VS–	10	—	Negative supply voltage connection
VS+	11	—	Positive supply voltage connection
Thermal pad		—	The thermal pad is connected to pin 4 via a downbond connection. The pad must be at the same potential as pin 4.

Copyright © 2018, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2)	VS pin to GND (all modes)		13.2	V
Digital inputs to GND	B1, B2	–0.3	5.5	V
Analog inputs to GND	VIN+, VIN–	2	10	V
Differential analog inputs	(VIN+ – VIN–)	–6	6	V
Continuous power dissipation		See Thermal Information		
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Supply bypass capacitor type, value and location relative to the device are critical to prevent damage to the device when the device is turned on. See Power Supply Recommendations.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±3000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Supply voltage	11.4	12	12.6	V
		±5.7	±6	±6.3	
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS6301 RSA (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2018, Texas Instruments Incorporated

6.5 Electrical Characteristics

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, drive mode 5 (B1B2 = 01, G.Fast mid power)(1) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 1 V_{PP}, drive mode 1 (0Z, ADSL2+)		500		MHz	C
		V_{OUT} = 1 V_{PP}, drive mode 2 (Z1, VDSL low power)		565			C
		V_{OUT} = 1 V_{PP}, drive mode 3 (11, G.Fast low power and VDSL mid power)		635			C
		V_{OUT} = 1 V_{PP}, drive mode 4 (1Z, VDSL high power)		540			C
		V_{OUT} = 1 V_{PP}, drive mode 5 (01, G.Fast mid power)		670			C
		V_{OUT} = 1 V_{PP}, drive mode 6 (10, G.Fast high power)		618			C
LSBW	Large-signal bandwidth	V_{OUT} = 15 V_{PP}, drive mode 1 (0Z, ADSL2+)		160		MHz	C
		V_{OUT} = 15 V_{PP}, drive mode 2 (Z1, VDSL low power)		200			C
		V_{OUT} = 15 V_{PP}, drive mode 3 (11, G.Fast low power and VDSL mid power)		260			C
		V_{OUT} = 15 V_{PP}, drive mode 4 (1Z, VDSL high power)		270			C
		V_{OUT} = 15 V_{PP}, drive mode 5 (01, G.Fast mid power)		275			C
		V_{OUT} = 15 V_{PP}, drive mode 6 (10, G.Fast high power)		300			C
SR	Slew rate down	Drive mode 1 (0Z), 10%-90% 15-V_{PP} pulse		3200		V/µs	C
		Drive mode 2 (Z1), 10%-90% 15-V_{PP} pulse		4000			C
		Drive mode 3 (11), 10%-90% 15-V_{PP} pulse		6400			C
		Drive mode 4 (1Z), 10%-90% 15-V_{PP} pulse		7100			C
		Drive mode 5 (01), 10%-90% 15-V_{PP} pulse		8200			C
		Drive mode 6 (10), 10%-90% 15-V_{PP} pulse		10500			C
	Slew rate up	Drive mode 1 (0Z), 10%-90% 15-V_{PP} pulse		2500		V/µs	C
		Drive mode 2 (Z1), 10%-90% 15-V_{PP} pulse		3200			C
		Drive mode 3 (11), 10%-90% 15-V_{PP} pulse		4400			C
		Drive mode 4 (1Z), 10%-90% 15-V_{PP} pulse		5400			C
		Drive mode 5 (01), 10%-90% 15-V_{PP} pulse		6500			C
		Drive mode 6 (10), 10%-90% 15-V_{PP} pulse		8000			C
e_n	Input-referred voltage noise	f > 1 MHz, drive mode 1 (0Z)		4.3		nV/√Hz	C
		f > 1 MHz, drive mode 2 (Z1)		3.9			C
		f > 1 MHz, drive mode 3 (11)		3.9			C
		f > 1 MHz, drive mode 4 (1Z)		3.9			C
		f > 1 MHz, drive mode 5 (01)		3.7			C
		f > 1 MHz, drive mode 6 (10)		3.5			C
	Noise floor, line termination mode	Line-termination modes, referred to R_{SERIES}		–154		dBm/Hz	C
		Power-down mode, referred to R_{SERIES}		–166			C
		Line-termination mode 00, output referred (f > 1 MHz)		5.6		nV/√Hz	C
		Line-termination mode Z0, output referred (f > 1 MHz)		6			C
		Power-down mode, output referred (f > 1 MHz)		1.6			C

(1) See Table 1 for the different Bias Modes of the device
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A ≈ 25°C. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. (D) Simulated value only for information

Copyright © 2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, drive mode 5 (B1B2 = 01, G.Fast mid power)(1) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
	ADSL2+ MTPR(3)	Line power = 8 dBm, f ≤ 552 kHz, PAR = 15 dB		67		dB	C
		Line power = 8 dBm, f ≤ 1.104 MHz, PAR = 15 dB		69			C
		Line power = 8 dBm, f ≤ 2.208 MHz, PAR = 15 dB		67			C
	VDSL2-17a MTPR(3)	Line power = 8 dBm, f ≤ 14 MHz, PAR = 15 dB, bias = 11		73		dB	C
		Line power = 8 dBm, f ≤ 17.6 MHz, PAR = 15 dB, bias = 11		71.5			C
	VDSL2-30a MTPR(3)	Line power = 8 dBm, f ≤ 30 MHz, PAR = 15 dB, bias = 11		69		dB	C
	VDSL2-35b MTPR(3)	Line power = 8 dBm, f ≤ 35 MHz, PAR = 15 dB, bias = 11		66		dB	C
	G.Fast 106-MHz MTPR(3)	Line power = 4 dBm, f ≤ 106 MHz, PAR = 15 dB, bias 01		68		dB	C
		Line power = 8 dBm, f ≤ 106 MHz, PAR = 15 dB, bias 10		62			C
		Line-termination mode, line power = 8 dBm, PAR = 15 dB		60		dB	D
	G.Fast 212-MHz MTPR(3)	Line power = 4 dBm, f ≤ 212 MHz, PAR = 15 dB, bias 10		63		dB	C
		Line power = 8 dBm, f ≤ 212 MHz, PAR = 15 dB, bias 10		55			C
		Line-termination mode, line power = 4 dBm, PAR = 15 dB		50			D
	Differential output impedance	Drive mode 6 (10, G.Fast high power), f = 100 kHz		1.2		Ω	D
		Drive mode 6 (10, G.Fast high power), f = 50 MHz		1.7			D
		Drive mode 6 (10, G.Fast high power), f = 106 MHz		2.8			D
		Drive mode 6 (10, G.Fast high power), f = 212 MHz		5.3			D
		Power-down bias mode		2400			D
		Line-termination modes		1.3			D
DC PERFORMANCE							
A_V	Differential gain	At dc, no load, all modes	8.3	8.6	8.9	V/V	A
	Differential output offset		–100		100	mV	A
	Output swing	Differential, at dc, 200-Ω load at amplifier output	18			V_{PP}	A
$R_{IN-DIFF}$	Differential input resistance		8	10	12	kΩ	A
R_{IN-SE}	Single-ended input resistance		4	5	6	kΩ	A

(3) ADSL2+, VDSL2-17a and VDSL2-30a profiles are specified with 1-in-4 missing tones; VDSL2-35b and G.Fast profiles are specified with 1-in-64 missing tones

Copyright © 2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, drive mode 5 (B1B2 = 01, G.Fast mid power)(1) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
	Linear output current	Drive mode 1 (0Z), sourcing, output offset < 20-mV deviation	40	75		mA	A
		Drive mode 1 (0Z), sinking, output offset < 20-mV deviation	40	70			A
		Drive mode 6 (10), sourcing, output offset < 20-mV deviation	80	160			A
		Drive mode 6 (10), sinking, output offset < 20-mV deviation	80	160			A
		High power termination mode (00), sourcing, output offset <20-mV deviation	50	95			A
		High power termination mode (00), sinking, output offset <20-mV deviation	50	90			A
		Low power termination mode (Z0), sourcing, output offset <20-mV deviation	40	77			A
		Low power termination mode (Z0), sinking, output offset <20-mV deviation	40	74			A
COMMON MODE							
	Input CM bias voltage		5.9	6	6.1	V	A
	Output CM bias voltage		5.9	6	6.1	V	A
POWER SUPPLY							
	Maximum supply voltage range	All modes			12.6	V	A
PSRR	Power-supply rejection ratio	f = dc	61			dB	A
I_Q	Quiescent current	Drive mode 1 (0Z, ADSL2+)	13	15.9	18.9	mA	A
		Drive mode 2 (Z1, VDSL low power)	16.7	20.1	24.3		A
		Drive mode 3 (11, G.Fast low power and VDSL mid power)	22.5	27.2	33.1		A
		Drive mode 4 (1Z, VDSL high power)	24	29.8	36.5		A
		Drive mode 5 (01, G.Fast mid power)	32.1	38.9	47.8		A
		Drive mode 6 (10, G.Fast high power)	36.7	45.3	56		A
		High power line termination mode (00)	13.6	16	18.9		A
		Low power line termination mode (Z0)	8.3	10.2	11.6		A
		Power-down mode		1.9	2.4		A

Copyright © 2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, drive mode 5 (B1B2 = 01, G.Fast mid power)(1) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
	Dynamic power consumption	Drive mode 1 (0Z, ADSL2+), line power = 8 dBm		220		mW	D
		Drive mode 2 (Z1, VDSL low power), line power = 8 dBm		280			D
		Drive mode 3 (11, G.Fast low power and VDSL mid power), line power = 8 dBm		310			D
		Drive mode 4 (1Z, VDSL high power), line power = 8 dBm		340			D
		Drive mode 5 (01, G.Fast mid power), line power = 4 dBm		480			D
		Drive mode 6 (10, G.Fast high power), line power = 8 dBm		590			D
		High power line termination mode (00), line power = 4 dBm		220			D
		Low power line termination mode (Z0), line power = 4 dBm		120			D
		Power-down mode		23			D

Copyright © 2018, Texas Instruments Incorporated

6.6 Switching Characteristics

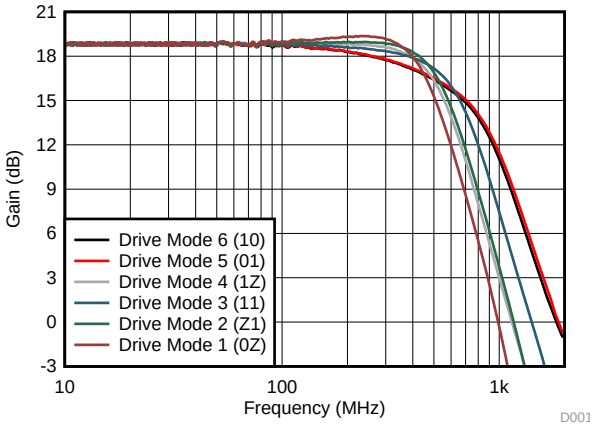
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Minimum logic high level	All digital pins, high	2.3			V
V_{IL}	Maximum logic low level	All digital pins, low			0.6	V
V_{MID}	Logic mid range	All digital pins, driven externally	1.2		1.6	V
V_{Float}	Logic self-bias voltage	All digital pins, floating	1.3	1.4	1.5	V
I_{IH}	Logic high-level leakage current	All digital pins, logic level = 3.6 V		110	135	µA
I_{IL}	Logic low-level leakage current	All digital pins, logic level = ground	–85	–75		µA
	Turn-on switching time	High power line termination mode (00) to drive mode 6 (10, G.Fast high power)		64		ns
		Low power line termination mode (Z0) to drive mode 6 (10, G.Fast high power)		50		
		Power down mode (ZZ) to Drive mode 6 (10, G.Fast high power)		60		
	Turn-off switching time	Drive mode 6 (10, G.Fast high power) to high power line termination mode (00)		76		ns
		Drive mode 6 (10, G.Fast high power) to low power line termination mode (Z0)		400		
		Drive mode 6 (10, G.Fast high power) to power-down mode (ZZ)		380		

版权 © 2018, Texas Instruments Incorporated

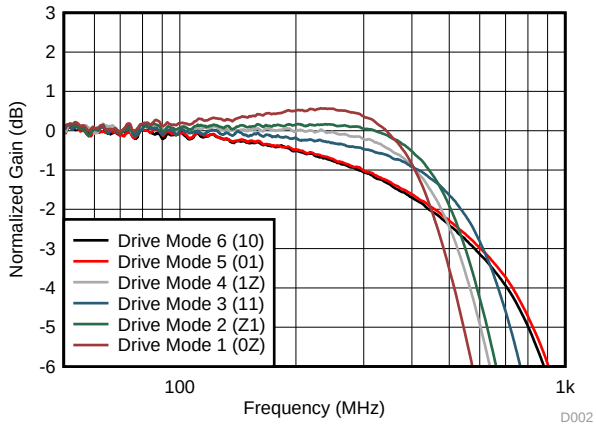
6.7 Typical Characteristics

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



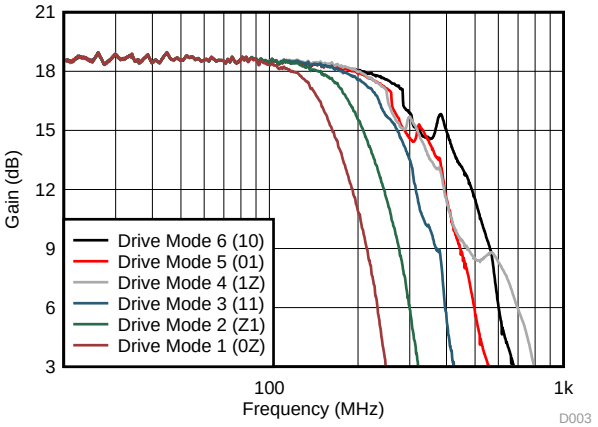
V_{OUT} = 1 V_{PP}

图 1. Small-Signal Bandwidth



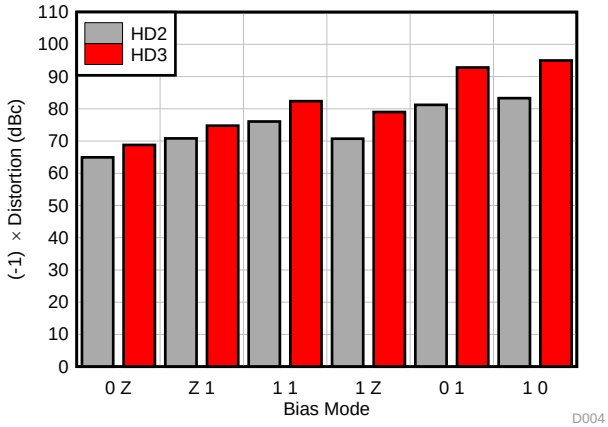
V_{OUT} = 1 V_{PP}

图 2. 3-dB Normalized Gain Small-Signal Bandwidth



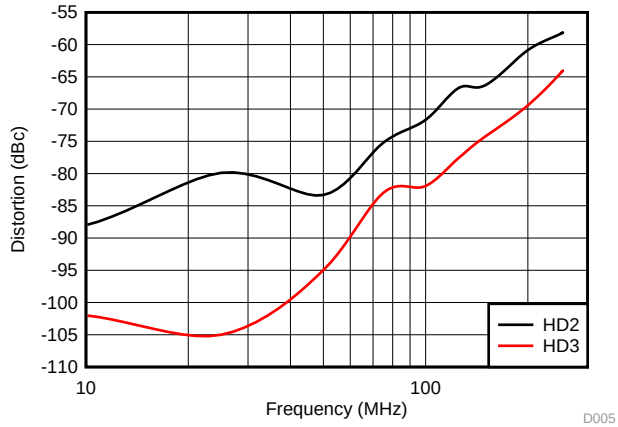
V_{OUT} = 15 V_{PP}

图 3. Large-Signal Bandwidth



Frequency = 50 MHz, V_{OUT} = 1 V_{PP}

图 4. Bias Modes vs Distortion



V_{OUT} = 1 V_{PP}

图 5. Distortion vs Frequency Drive Mode 6 (Bias 10)

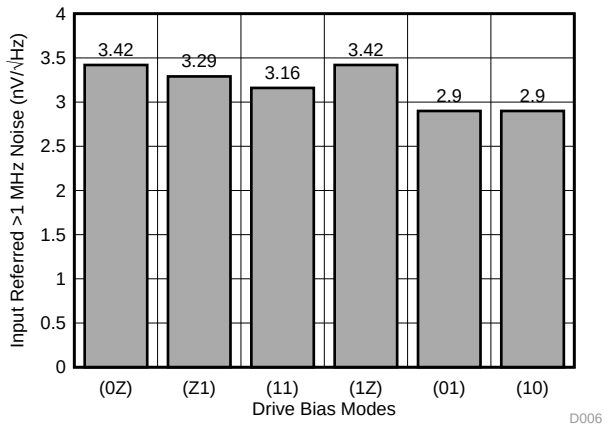


图 6. Input Voltage Noise

版权 © 2018, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

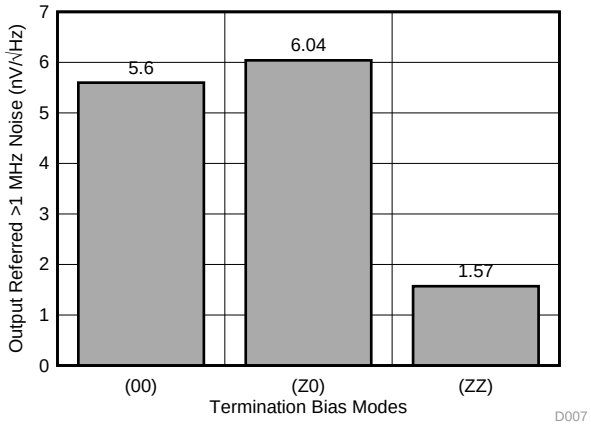
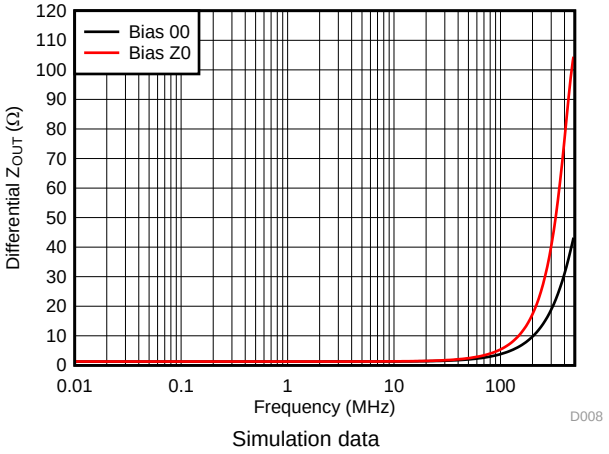
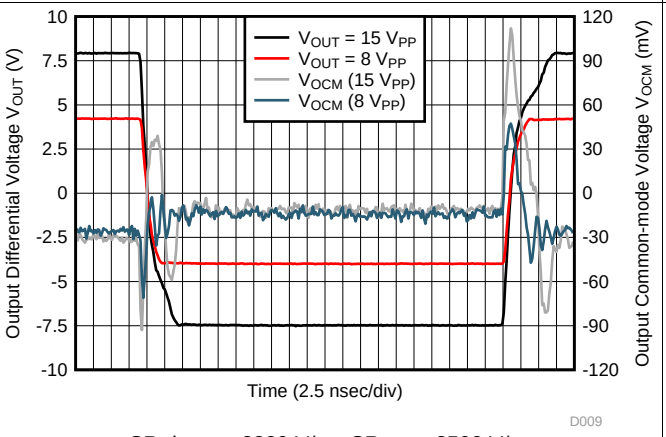


图 7. Termination Mode Noise Floor



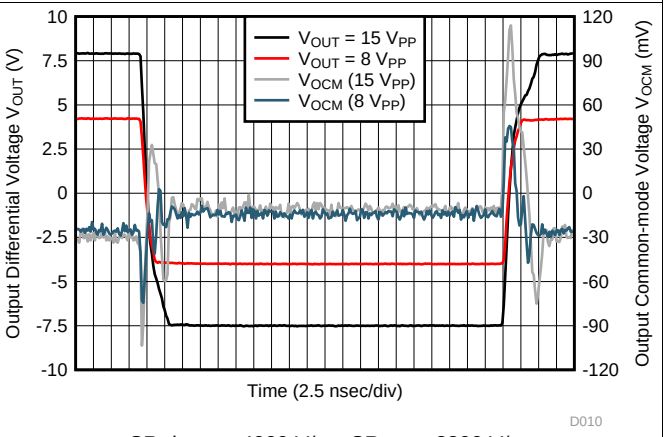
Simulation data

图 8. Termination Mode Differential Output Impedance



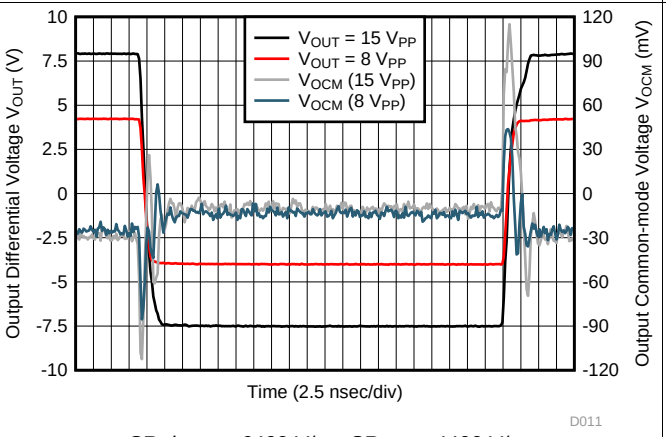
SR down = 3200 V/µs, SR up = 2500 V/µs

图 9. Pulse Response Drive Mode 1 (Bias 0Z)



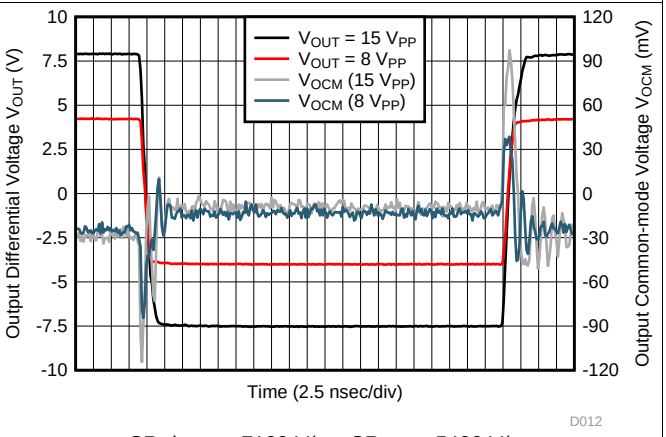
SR down = 4000 V/µs, SR up = 3200 V/µs

图 10. Pulse Response Drive Mode 2 (Bias Z1)



SR down = 6400 V/µs, SR up = 4400 V/µs

图 11. Pulse Response Drive Mode 3 (Bias 11)



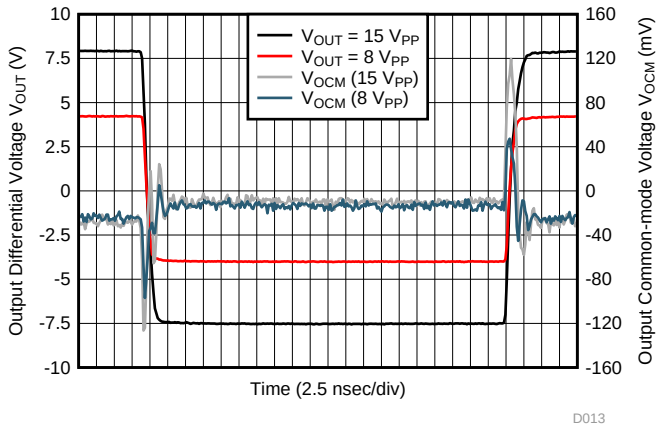
SR down = 7100 V/µs, SR up = 5400 V/µs

图 12. Pulse Response Drive Mode 4 (Bias 1Z)

版权 © 2018, Texas Instruments Incorporated

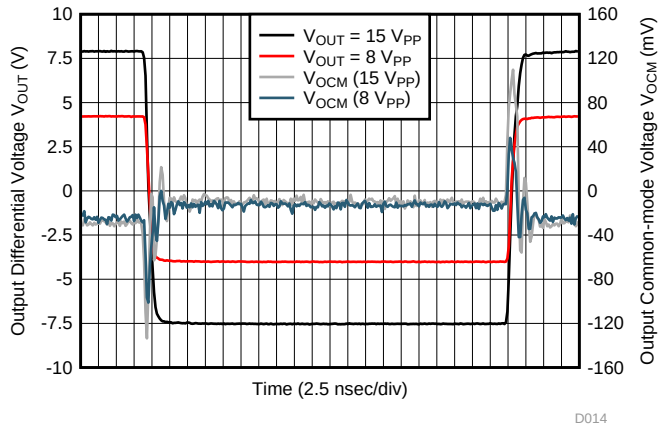
Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



SR down = 8200 V/µs, SR up = 6500 V/µs

图 13. Pulse Response Drive Mode 5 (Bias 01)



SR down = 10500 V/µs, SR up = 8000 V/µs

图 14. Pulse Response Drive Mode 6 (Bias 10)

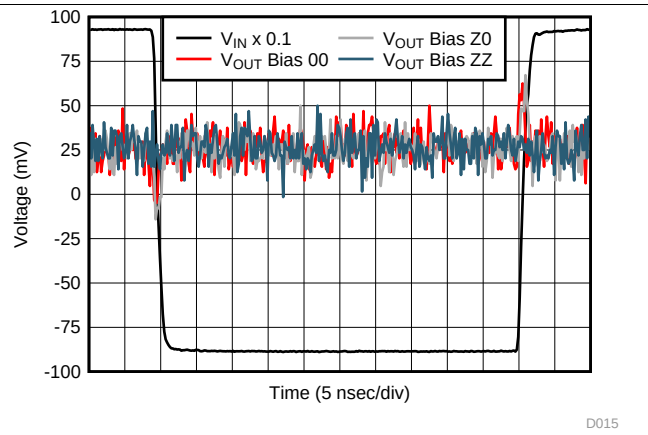
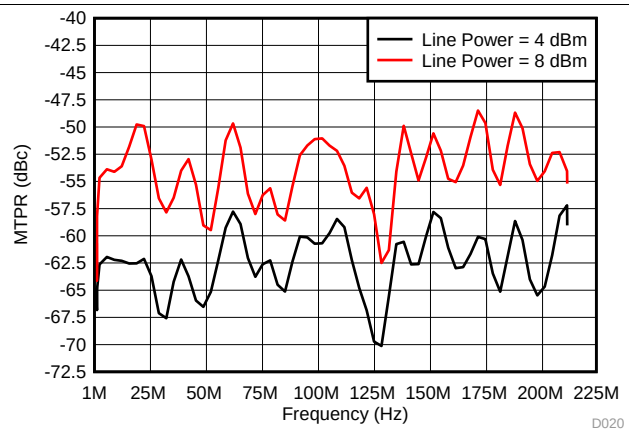
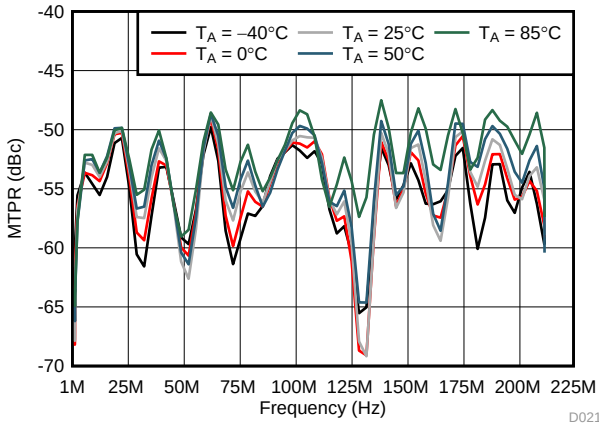


图 15. Pulse Response Termination and Power-Down Modes



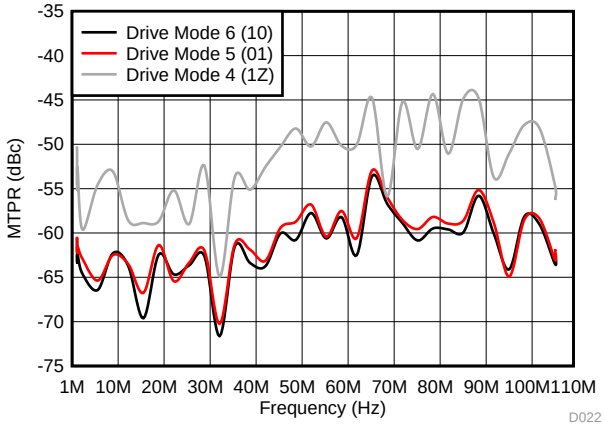
PAR = 15 dB, 1-in-64 missing tones

图 16. MTPR G.Fast 212-MHz Profile (Bias 10)



PAR = 15 dB, 1-in-64 missing tones, Line power = 8 dBm

图 17. MTPR Over Temperature G.Fast 212-MHz Profile (Bias 10)



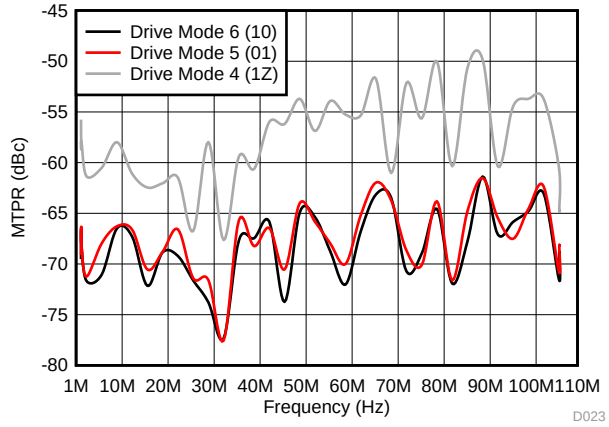
PAR = 15 dB, 1-in-64 missing tones, line power = 8 dBm

图 18. MTPR G.Fast 106-MHz Profile

版权 © 2018, Texas Instruments Incorporated

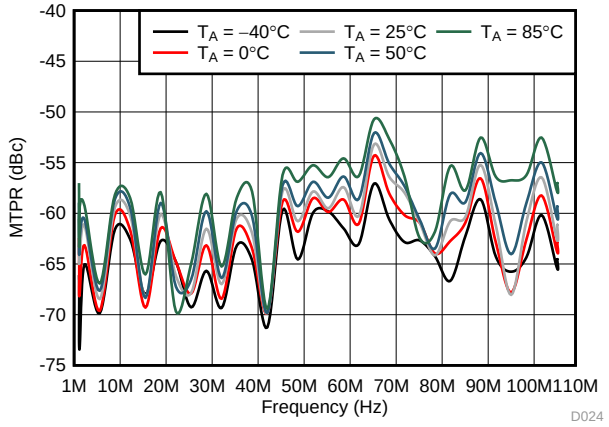
Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



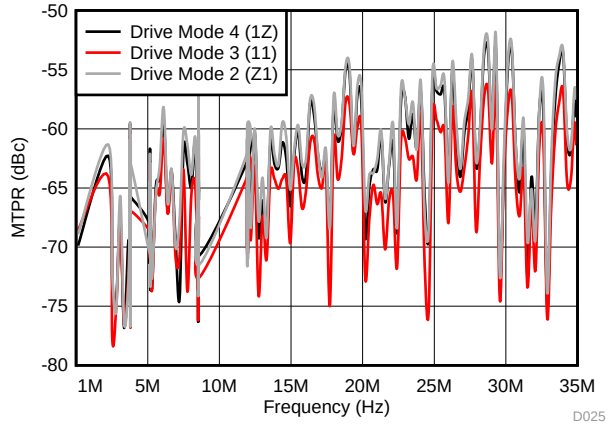
PAR = 15 dB, 1-in-64 missing tones, line power = 4 dBm

图 19. MTPR G.Fast 106-MHz Profile



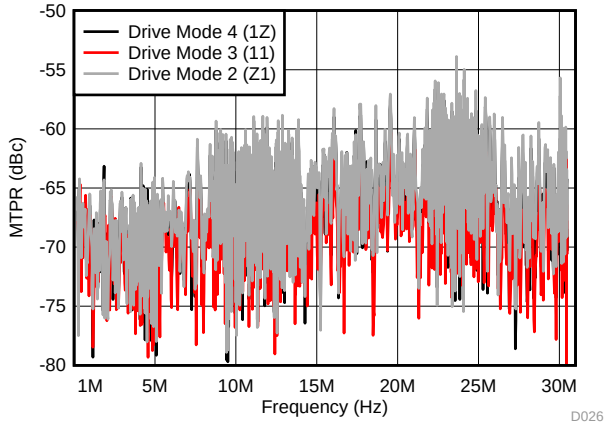
Line power = 8 dBm, PAR = 15 dB, 1-in-64 missing tones

图 20. MTPR Over Temperature G.Fast 106-MHz Profile (Bias 01)



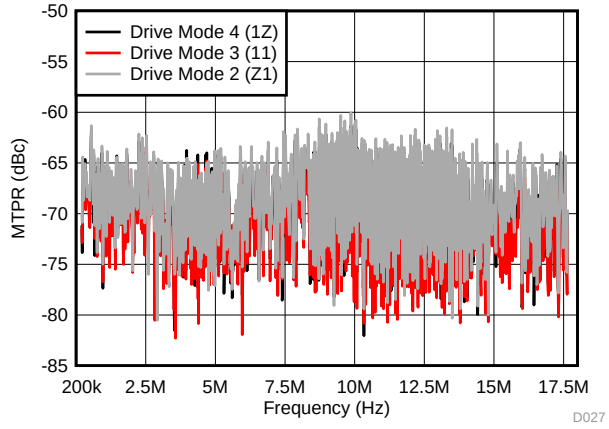
PAR = 15 dB, 1-in-64 missing tones, line power = 8 dBm

图 21. MTPR VDSL2-35b Profile



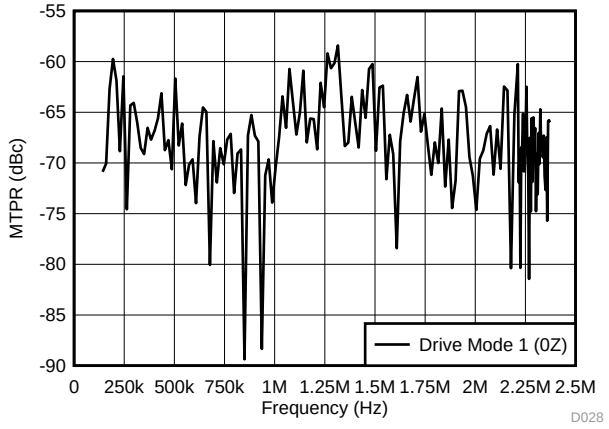
PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

图 22. MTPR VDSL2-30a Profile



PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

图 23. MTPR VDSL2-17a Profile

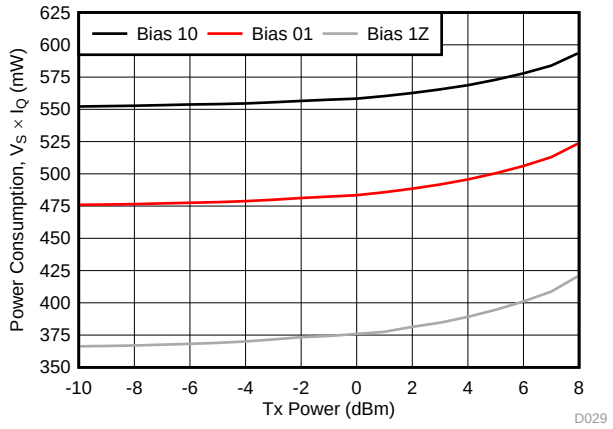


PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

图 24. MTPR ADSL2+ Profile

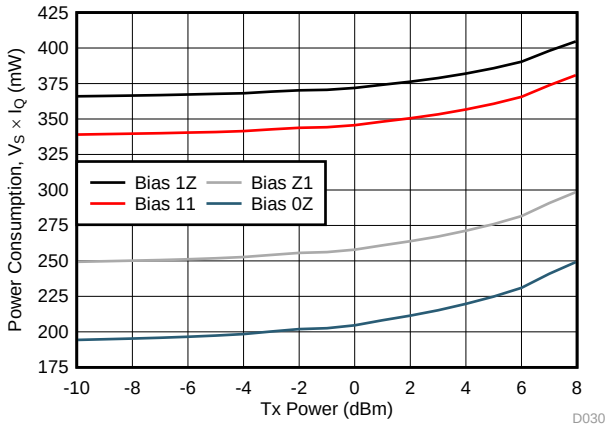
Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



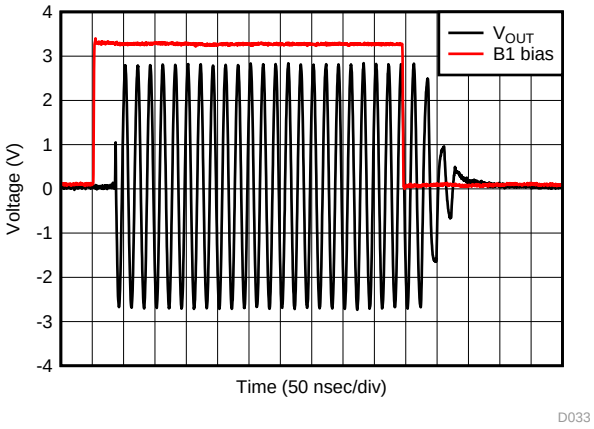
G.Fast 106-MHz profile used

图 25. G.Fast Modes Power Consumption



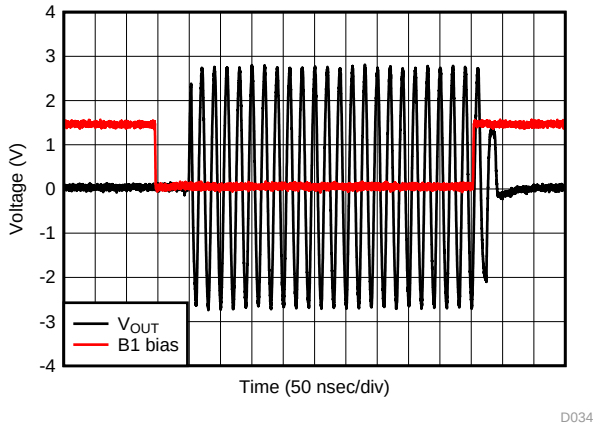
VDSL2-30a profile used

图 26. xDSL Modes Power Consumption



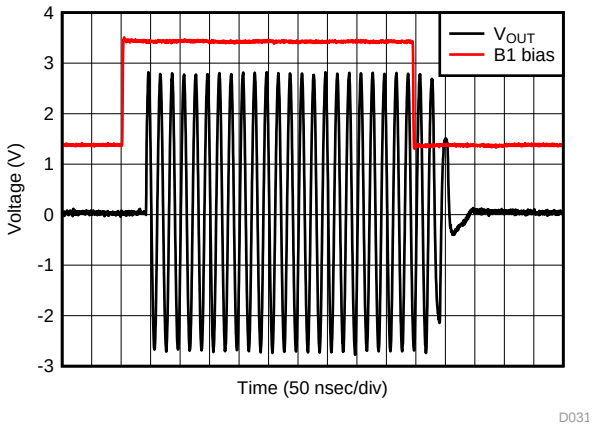
Bias mode 00 to 10 and 10 to 00

图 27. Mode Switch Time 00 to 10



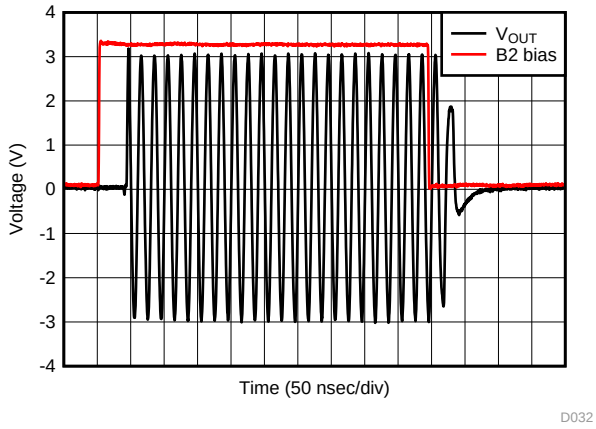
Bias mode ZZ to 0Z and 0Z to ZZ

图 28. Mode Switch Time ZZ to 0Z



Bias mode ZZ to 1Z and 1Z to ZZ

图 29. Mode Switch Time ZZ to 1Z



Bias mode Z0 to Z1and Z1 to Z0

图 30. Mode Switch Time Z0 to Z1

版权 © 2018, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

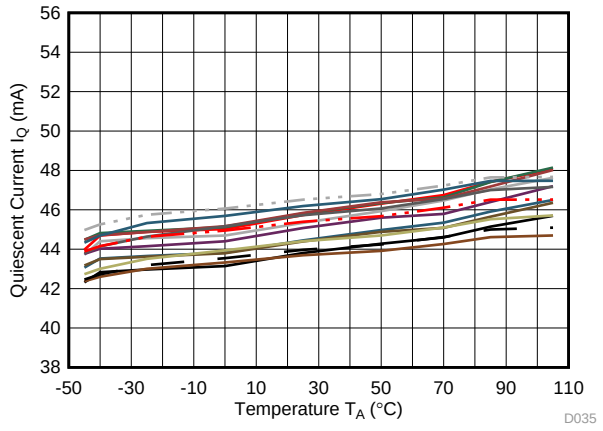


图 31. I_Q vs Temperature Drive Mode 6 (Bias 10)

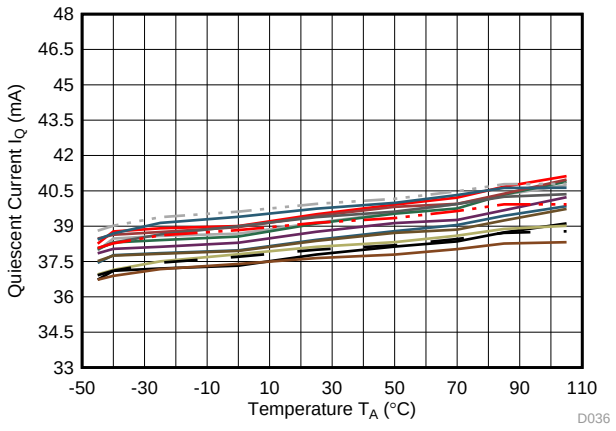


图 32. I_Q vs Temperature Drive Mode 5 (Bias 01)

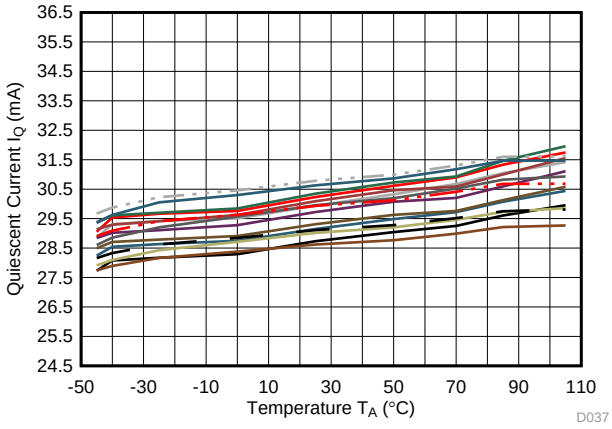


图 33. I_Q vs Temperature Drive Mode 4 (Bias 1Z)

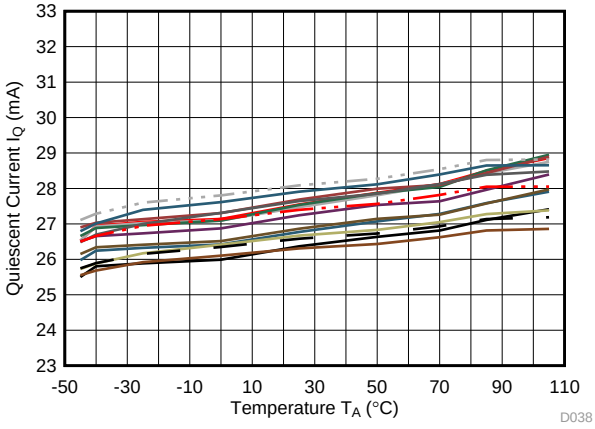


图 34. I_Q vs Temperature Drive Mode 3 (Bias 11)

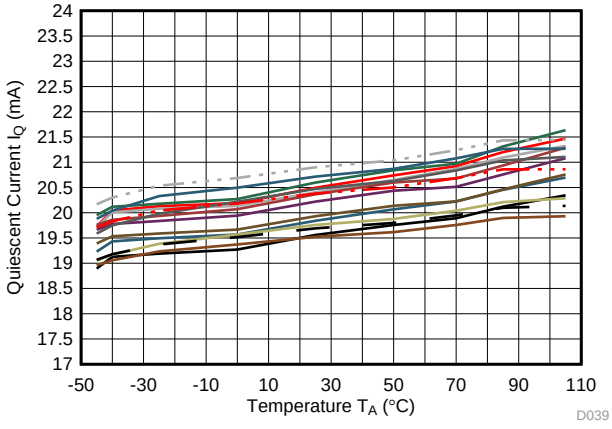


图 35. I_Q vs Temperature Drive Mode 2 (Bias Z1)

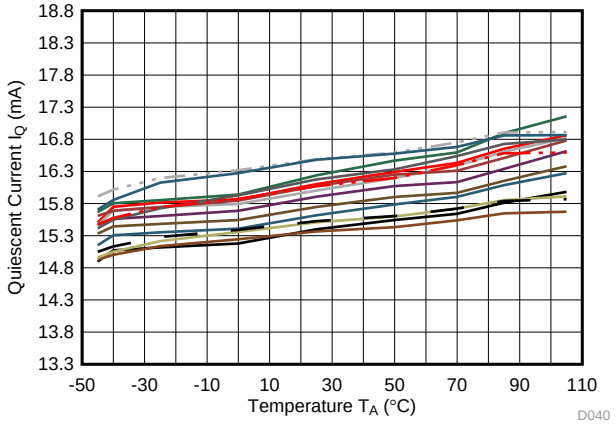


图 36. I_Q vs Temperature Drive Mode 1 (Bias 0Z)

版权 © 2018, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A ≈ 25°C, VS+ = 12 V, VS– = 0 V, voltage gain (A_V) = 8.5 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IADJ} = 75 kΩ, C_{IADJ} = 100 pF, and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

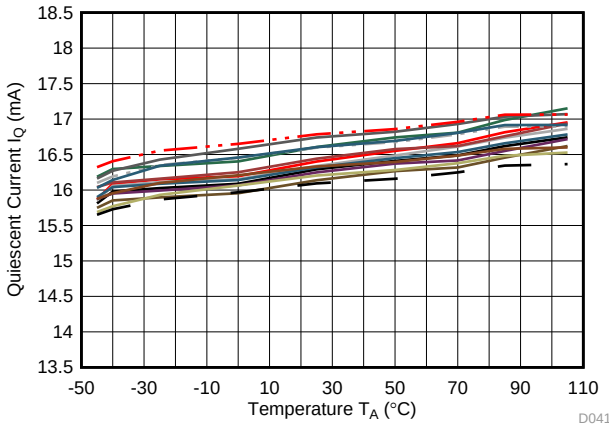


图 37. I_Q vs Temperature High-Power Termination Mode (Bias 00)

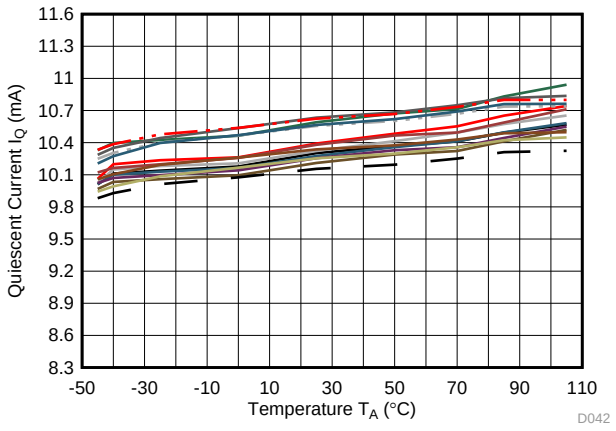


图 38. I_Q vs Temperature Low-Power Termination Mode (Bias Z0)

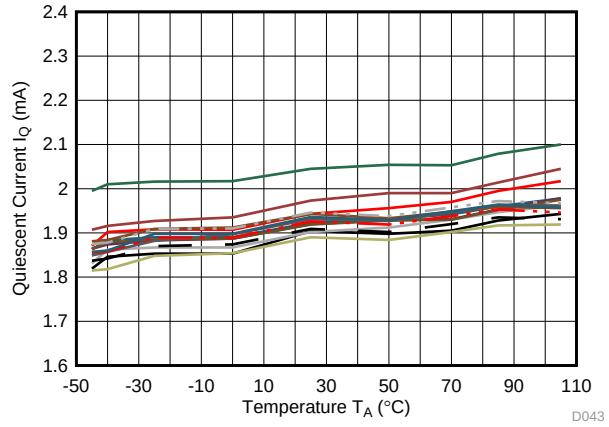


图 39. I_Q vs Temperature Power-Down Mode (Bias ZZ)

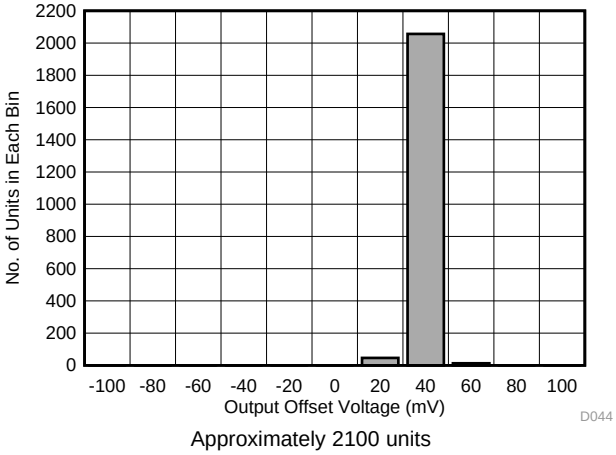


图 40. Output Offset Voltage Histogram

版权 © 2018, Texas Instruments Incorporated

7 Detailed Description

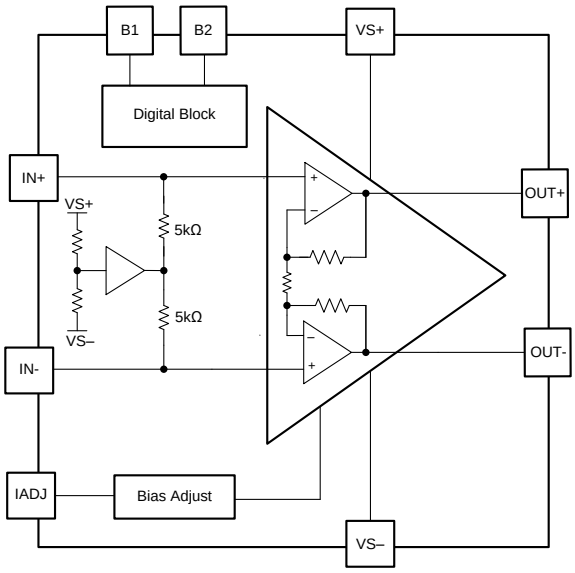
7.1 Overview

The THS6301 is a current-feedback architecture, differential line driver designed for G.Fast and xDSL systems. The device is targeted for use in G.Fast digital subscriber line (DSL) systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The device consists of a unique architecture consisting of an amplifier in a noninverting configuration with an internally-fixed gain of 8.5 V/V. The THS6301 is designed to drive the high-performance G.Fast 212-MHz DSL profile, but is also backwards-compatible to drive lower frequency profiles. The device features selectable bias modes for the G.Fast 106-MHz profile, VDSL profiles, and ADSL profiles. These modes reduce the quiescent current of the device based on the frequency requirements of the various DSL profiles to maximize power efficiency. Along with adjustable bias modes, the device features two line-termination modes that maintain an output impedance match with low power consumption. The line-termination modes allow for the device to be in a low-power state without causing distortion on a shared signal line.

For further flexibility, the THS6301 features an IADJ pin that is used to further adjust the quiescent current of the device. A resistor connected to this pin can be changed to increase or decrease the device current to meet performance requirements and uses the lowest amount of power possible.

7.2 Functional Block Diagram



7.3 Feature Description

The THS6301 is a line driver that has a high current drive and a differential input and output. 图 41 shows an example circuit of the THS6301 configured to drive the G.Fast 212-MHz DSL profile. The bias control pins B1 and B2 are set to 3.3 V and ground, respectively, to put the device in the G.Fast 212-MHz bias mode. This bias mode optimizes the internal power consumption of the device to meet performance specifications of the G.Fast 212-MHz profile and can be changed to meet several different DSL profiles and other modes listed in 表 1. The IADJ pin is biased with a 75-kΩ (R_{IADJ}) resistor that adjusts the device quiescent current to a nominal state. R_{IADJ} can be increased to lower the quiescent current or decreased to raise the quiescent current of the device for fine-tuning. C_{IADJ} provides decoupling for the IADJ pin and is typically 100 pF.

The THS6301 has a 10-kΩ, internally-set differential input impedance and low output impedance. In 图 41 the input impedance is matched to 100 Ω by using a 100-Ω resistor connected differentially across the inputs. This value can easily be changed by using a different resistor to create the desired impedance at the input. Remember that the impedance in the device is actually the parallel combination of 10 kΩ and the external input resistor. For low impedances, this effect is minimal, but must be considered if the matched input impedance is increased. The output impedance of the THS6301 in 图 41 is set by the two R_{SERIES} resistors to match 100 Ω. The internal output resistance is very low (< 2 Ω per output), so the output impedance is primarily set by the R_{SERIES} resistors. These resistors can be adjusted to match various output impedance values.

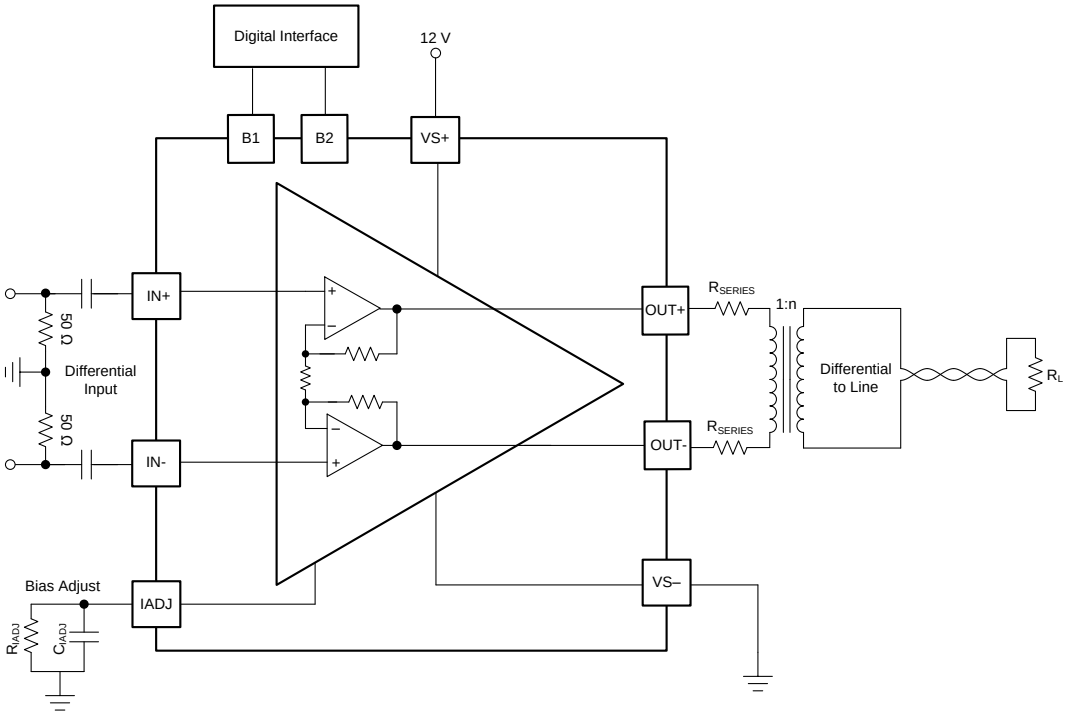


图 41. G.Fast, 212-MHz Driving Mode Example Circuit

版权 © 2018, Texas Instruments Incorporated

7.4 Device Functional Modes

The THS6301 features nine different device operational modes, as listed in 表 1, to accommodate the G.Fast, xDSL, line termination, and power-down scenarios. The device is controlled by a 2-pin parallel interface that uses three-level logic to control the device state. The G.Fast and xDSL modes change the quiescent current of the device to meet signal performance requirements and maintain the lowest power possible, which allows for legacy DSL compatibility with maximum power efficiency. The two line-termination modes maintain a low impedance at the output and place the device in a low-power state. The line-termination modes allow for the muxing of multiple devices to one output line by putting the non-driving devices in a state that does not add distortion to the line. A power-down mode is also included to digitally shut down the device for the highest level of power savings. 表 1 lists the device power modes and the typical quiescent currents for each mode.

表 1. Bias Modes Truth Table

MODE DESCRIPTION	BIAS CONTROL PINS		RECOMMENDED DSL PROFILE	TYPICAL QUIESCENT CURRENT (R_{IADJ} = 75 KΩ	SSBW (V_{OUT} = 1.7 V_{PP})
	B1	B2			
Power down	Z	Z	Power down	1.9 mA	N/A
Low-power termination	Z	0	Line termination (low power)	10.2 mA	N/A
High-power termination	0	0	Line termination (high power)	16 mA	N/A
Drive mode 1	0	Z	ADSL2+	15.9 mA	564 MHz
Drive mode 2	Z	1	VDSL (low power)	20.1 mA	659 MHz
Drive mode 3	1	1	G.Fast (low power) and VDSL (mid power)	27.2 mA	755 MHz
Drive mode 4	1	Z	VDSL (high power)	29.8 mA	605 MHz
Drive mode 5	0	1	G.Fast (mid power)	38.9 mA	864 MHz
Drive mode 6	1	0	G.Fast (high power)	45.3 mA	814 MHz

7.5 Programming

The THS6301 programming is controlled by two parallel pins, B1 and B2. These pins use three-level logic to create nine different combinations for each pair of pins. The pins have a high state (*1*) when the pin voltage is greater than 2.3 V, a low state (*0*) when the pin voltage is less than 0.6 V, and an open state (*Z*) where the pin floats at approximately 1.4 V or can be driven between 1.2 V and 1.6 V. 表 1 lists the logic combinations for the two pins and the corresponding power modes.

版权 © 2018, Texas Instruments Incorporated

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a single-port, very-high-bit-rate linear xDSL, G.Fast differential line driver where the device drives a twisted pair cable. The signal is generated by a high-speed, digital-to-analog converter (DAC) at low signal swings that is amplified by the G.Fast line driver.

The G.Fast system is ac-coupled when transmitting information above the audio band. On the input of the line driver, this ac-coupling translates into the series capacitors to isolate the dc voltage coming from the DAC output common-mode voltage. On the output, a transformer is used to help isolate the 48 V present between the tip and ring of the telephone line.

The transformer can be set to any useful ratio. In practice, the transformer-turn ratio is set between 1:1 and 1:1.4 for the device. The output transformer usually has the active impedance synthesis factor set to 5. This synthesis factor means that the termination resistor (R_T) is 1/5th of the load impedance reflected to the transformer secondary. Thus, the correct termination can be selected based on the transformer-turn ratio.

Note that the resulting load detected by the amplifier may affect the amplifier linearity or output voltage swing capabilities.

8.2 Typical Application

图 42 shows a typical application circuit for this device.

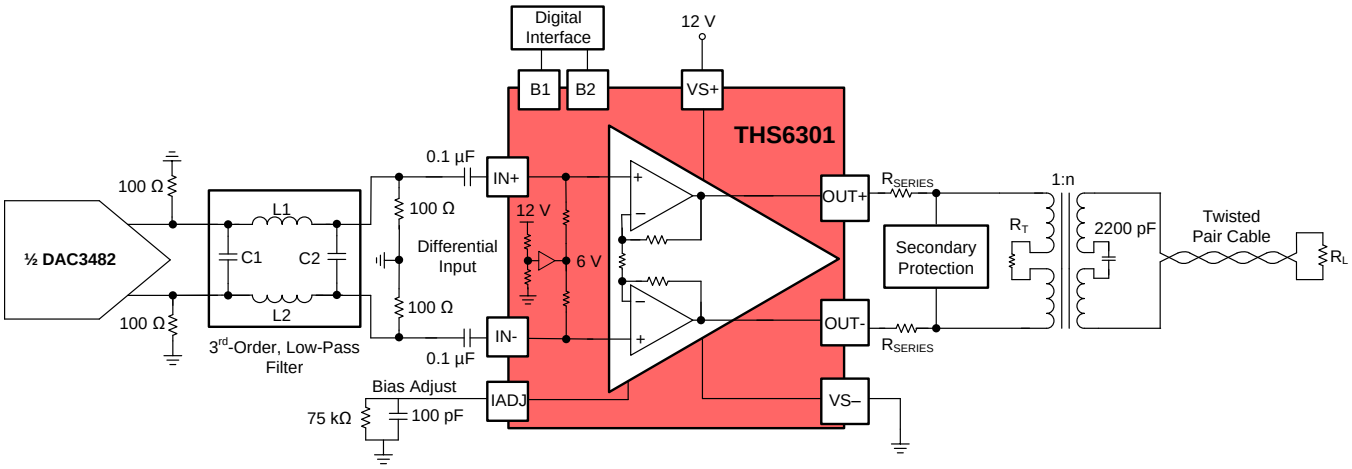


图 42. Typical G.FAST Line Driver Configuration

版权 © 2018, Texas Instruments Incorporated

Typical Application (接下页)

8.2.1 Design Requirements

表 2 provides the design requirements for a G.Fast line driver, which is met by the THS6301 device.

表 2. Design Requirements

DESIGN REQUIREMENT	CONDITION
G.Fast, 106-MHz, 212-MHz transmit profile	Yes, using the bias control pins for line power = 8 dBm and PAR = 15 dBm
Legacy DSL profile support	Yes
Supply voltage	12 V
Output current drive	±80 mA, each output
Power-down functionality	High isolation from input to output
Input interface	AC coupled
Output transformer ratio	1:1.5
Surge protection	External needed

8.2.2 Detailed Design Procedure

The G.Fast signal input to the THS6301 comes from a high-speed DAC whose interleaving spurs are filtered out using either a 3rd- or 5th-order filter. Digital pre-emphasis can be employed in the DAC output such that the differential line driver compensates for the transmission line cable losses at long distance and high frequency. The THS6301 is operated on a 12-V single supply. Resulting from the single-supply operation, the device input is AC-coupled using a capacitor that blocks any DC current flowing out of the inputs to the adjacent circuitry. The AC-coupling capacitor forms a high-pass filter with the device input impedance. This pole must be set at a frequency low enough to not interfere with the desired xDSL or G.Fast signal.

The THS6301 differential outputs usually drive a 1:n output transformer with a transformer turns ratio that can be changed depending upon the application. The output transformer selected must have low insertion loss in the desired frequency band in order to maintain good multi-tone power rejection (MTPR) for a given line power. The load is expected to be a transmission line with 100-Ω characteristic impedance on the primary side of the transformer. Referred to the transformer secondary, the load detected by the amplifier is $1 / n^2$ with 1:n being the transformer turn ratio. Practical limitations force the transformer-turn ratio to be between 1:1 and 1:1.6. At the lighter load detected by the amplifier (1:1), the voltage swing is limited by the class AB output stage and the maximum achievable swing of the amplifier. At the heaviest load (1:1.6), the voltage swing is limited by the current drive capability of the amplifier. To satisfy the synthesis impedance factor and the loading, the termination resistance (R_T) can be set to $R_T = R_L / 5 = 100\ \Omega / (5 \times n^2)$.

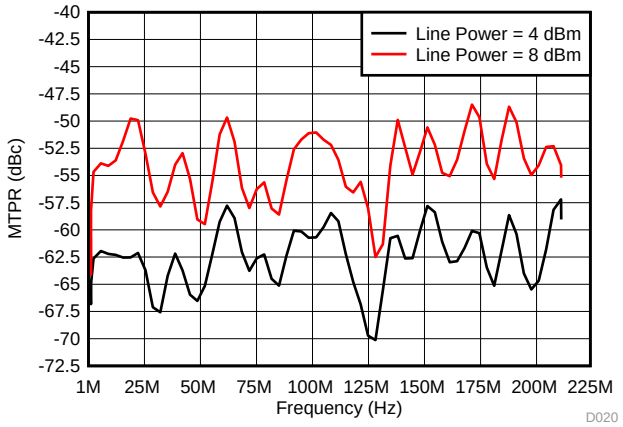
For surge protection, consider adding a gas discharge tube (GDT) on the primary side of the output transformer. The gas discharge tube is required to shunt the large current that could flow through the cables during lightning surge, and protect the device outputs. The secondary protection is also normally added after the series resistance on the secondary transformer side. The secondary protection could be in the form of back to back switching diodes, which also help limit the residual surge current flowing into the device outputs.

For the power-supply bypass, consider using X7R or X5R because of the better stability of these materials over temperature.

版权 © 2018, Texas Instruments Incorporated

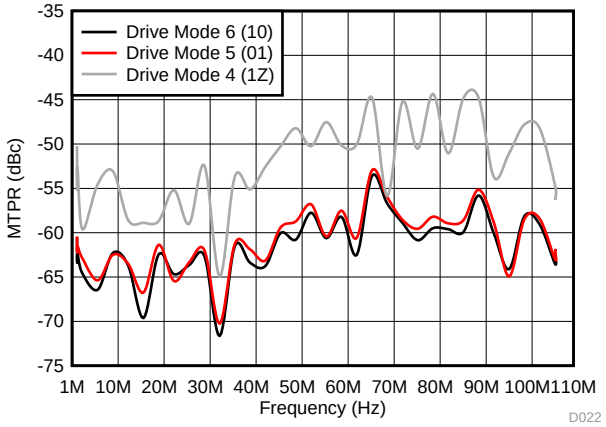
8.2.3 Application Curves

图 43 and 图 44 show the MTPR results for 212-MHz and 160-MHz G.Fast profiles, respectively.



PAR = 15 dB, 1-in-64 missing tones

图 43. MTPR G.Fast 212-MHz Profile



PAR = 15 dB, 1-in-64 missing tones, line power = 8 dBm

图 44. MTPR G.Fast 106-MHz Profile

版权 © 2018, Texas Instruments Incorporated

9 Power Supply Recommendations

The THS6301 is recommended to operate using a total supply voltage of 12 V. If a lower or higher supply voltage is required, select one that is between 11.4 V and 12.6 V for optimal performance. Use supply-decoupling capacitors on the power-supply pins to minimize distortion caused by parasitic signals on the power supply. This usage is especially important in applications where many devices share a single power-supply bus.

The device can be operated on split supplies (such as ±6 V). However, the bias adjust resistor must be tied to the negative supply for proper device operation. When operating the device on split supply, pins 4 and 10 act as the negative supply voltage pin. The thermal pad must be tied to either GND or the negative supply voltage in split-supply operation. The device bias mode pins are now referenced to the negative supply voltage for the different logic levels.

As with all high-speed amplifiers, supply bypass capacitors are required for operation of the THS6301. Multiple capacitors are required to cover the entire frequency range of the device. For low frequency bypassing use a 10 µF or larger tantalum capacitor (see the description of C1 in the *THS6301EVM User's Guide*). Place this capacitor within two or three centimeters of the amplifier. Use 0.1-µF and 1-nF high-frequency bypass capacitors (these capacitors are labeled C2 and C3 on the EVM). Place these capacitors within two to three millimeters of the amplifier and must be directly connected to the power-supply planes with low-impedance vias. Texas Instruments recommends using the capacitors shown in the bill of materials (BOM) that accompanies the *THS6301EVM User's Guide*. The capacitor part numbers are listed in the THS6301EVM user's guide.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6301 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Excessive parasitic capacitance on the input pin can cause instability. In the line driver application, the parasitic capacitance forms a pole with the load detected by the amplifier and can reduce the effective bandwidth of the application circuit, thus leading to degraded performance. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b. Minimize the distance (< 0.25") from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors.

c. Make sure the bias adjust resistor connected to the IADJ pin is not routed close to the device inputs in-order to avoid any high-frequency noise coupling into the IADJ pin and result in unexpected device behavior.

d. Careful selection and placement of external components preserves the high-frequency performance of the device. Use very-low reactance-type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and printed circuit board (PCB) traces as short as possible. Never use wire-wound type resistors in a high-frequency application.

e. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

f. Do not socket a high-speed part such as the THS6301. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the device onto the board.

g. TI recommends soldering the thermal pad to the PCB in order to conduct heat out of the device package. Vias underneath the part help regulate the flow of free air and also help conduct heat out of the package.

版权 © 2018, Texas Instruments Incorporated

Layout Guidelines (接下页)

10.1.1 Power Dissipation and Thermal Considerations

For maximum performance and reliability, the designer must ensure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. 公式 1 calculates maximum power dissipation for a given package:

$$P_{D(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA} \quad (1)$$

where

- $P_{D(MAX)}$ is the maximum power dissipation in the amplifier (W)
- $T_{J(MAX)}$ is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
- $R_{\theta JC}$ is the thermal coefficient from silicon transistors to the case (°C/W)
- $R_{\theta CA}$ is the thermal coefficient from case to ambient temperature (°C/W)

For systems where heat dissipation is more critical, the THS6301 is offered in an 16-pin VQFN package with thermal pad. Because of the thermal pad, the thermal coefficient for the VQFN package is substantially improved over the traditional SOIC. The data for the VQFN packages with thermal pad assume a board layout that follows the thermal pad layout guidelines referenced in this section and detailed in the *Quad Flatpack No-Lead Logic Packages* application note. If the thermal pad is not soldered to the PCB, the thermal impedance increases substantially, which may cause serious heat and performance issues. Be sure to always solder the thermal pad to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

版权 © 2018, Texas Instruments Incorporated

10.2 Layout Example

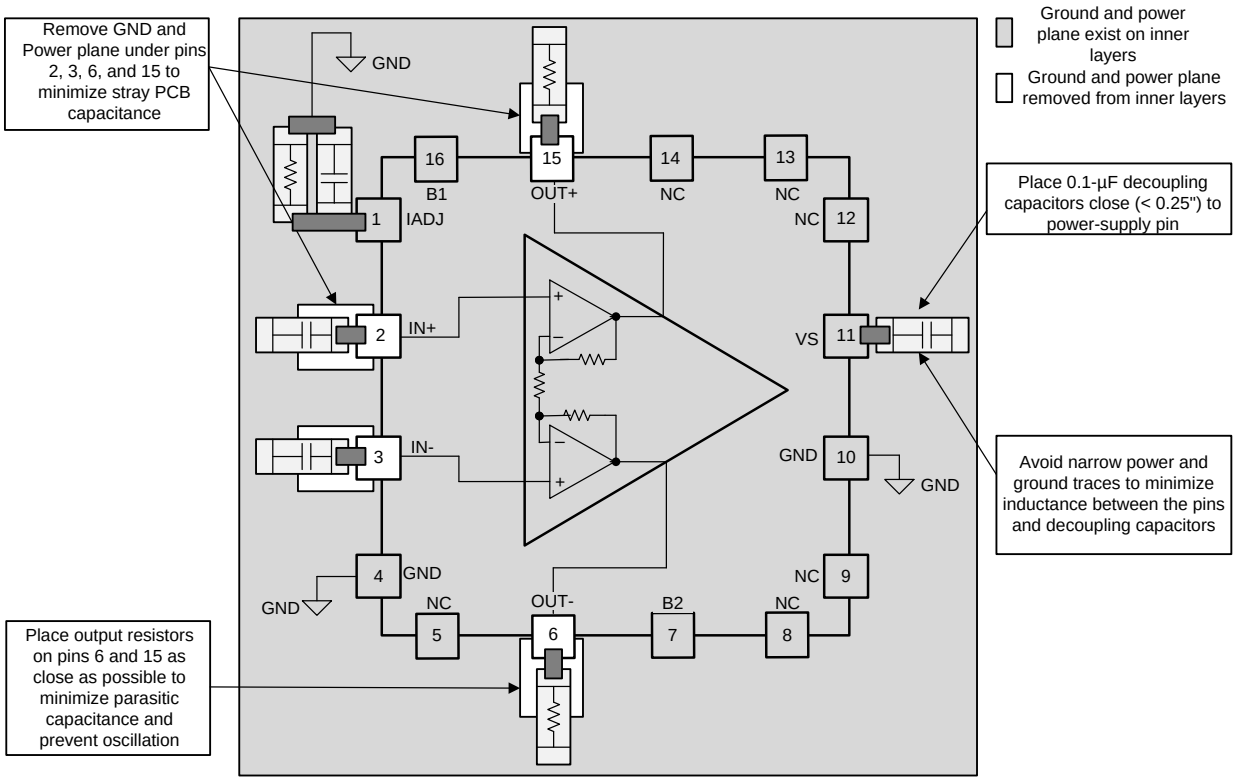


图 45. Example Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《四方扁平封装无引线逻辑封装》应用手册*
- *《ADSL 线路驱动器的有源输出阻抗》应用手册*
- *THS6301EVM 用户指南*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

版权 © 2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6301IRSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	THS 6301
THS6301IRSAR.A	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	THS 6301
THS6301IRSAT	Active	Production	QFN (RSA) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	THS 6301
THS6301IRSAT.A	Active	Production	QFN (RSA) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	THS 6301

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

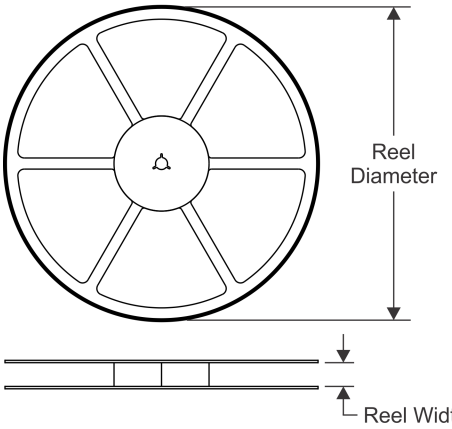
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

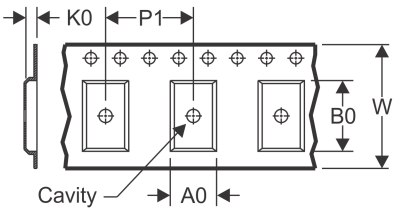
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

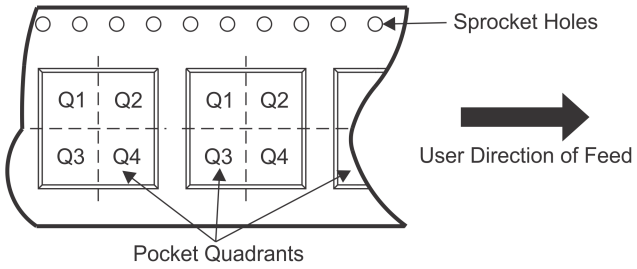


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

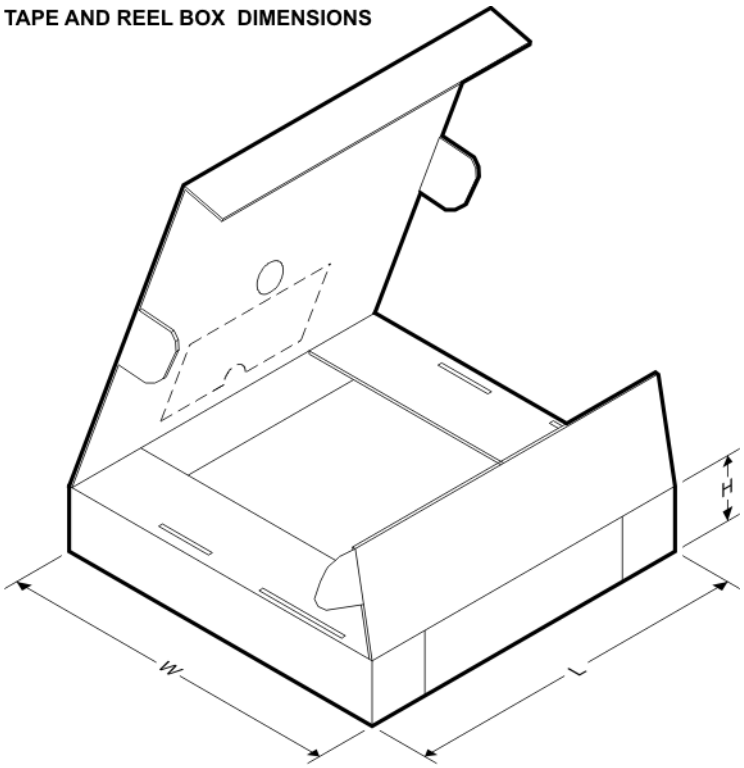
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6301IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS6301IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6301IRSAR	QFN	RSA	16	3000	367.0	367.0	35.0
THS6301IRSAT	QFN	RSA	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

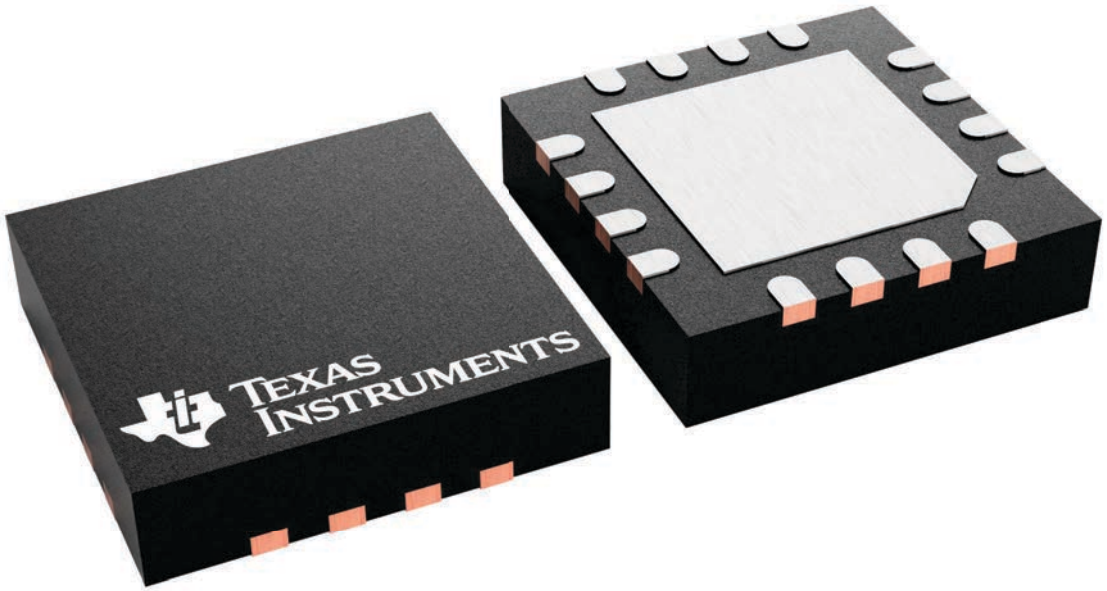
RSA 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

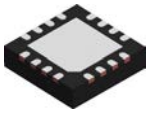
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230969/A

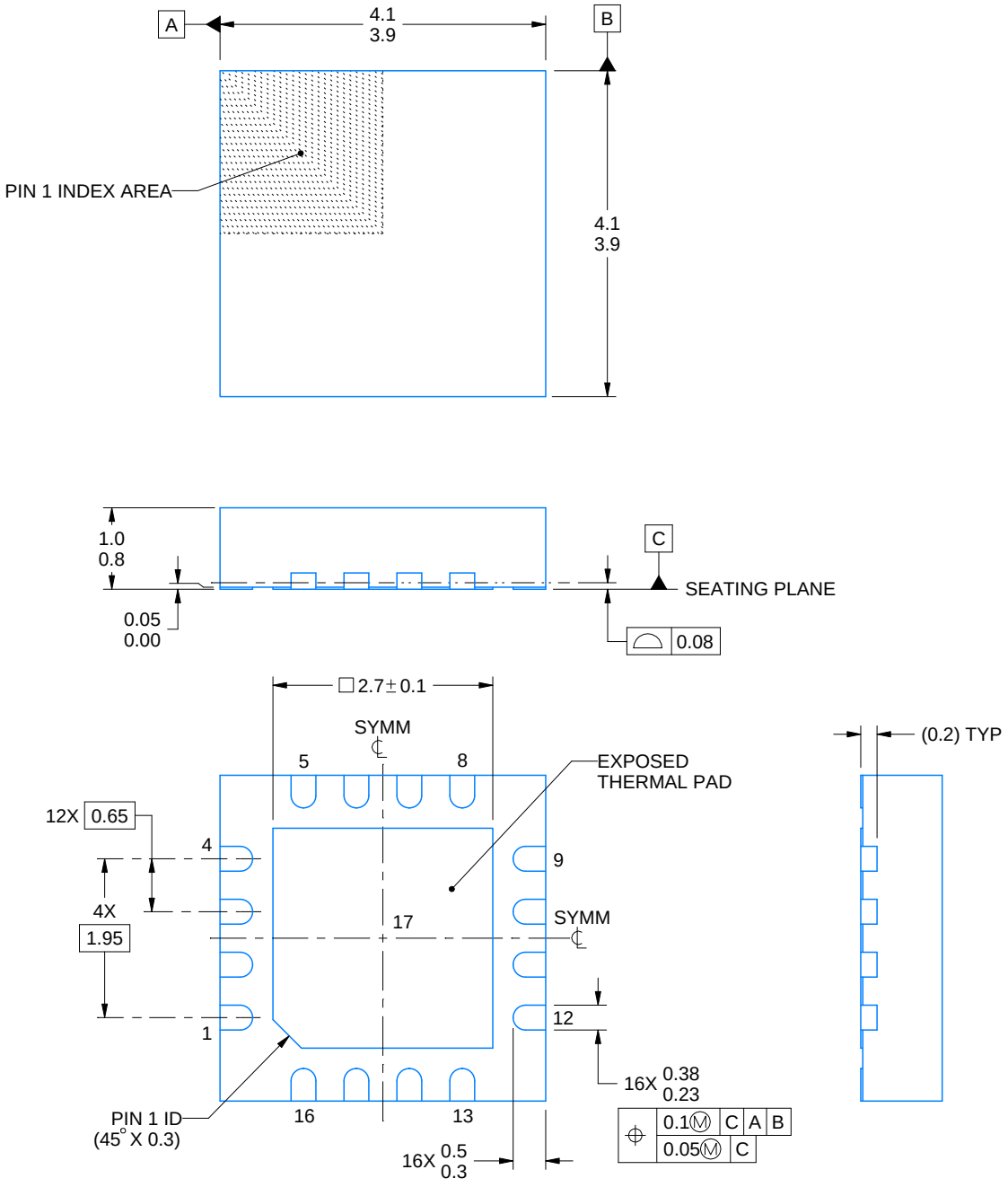
RSA0016B



PACKAGE OUTLINE

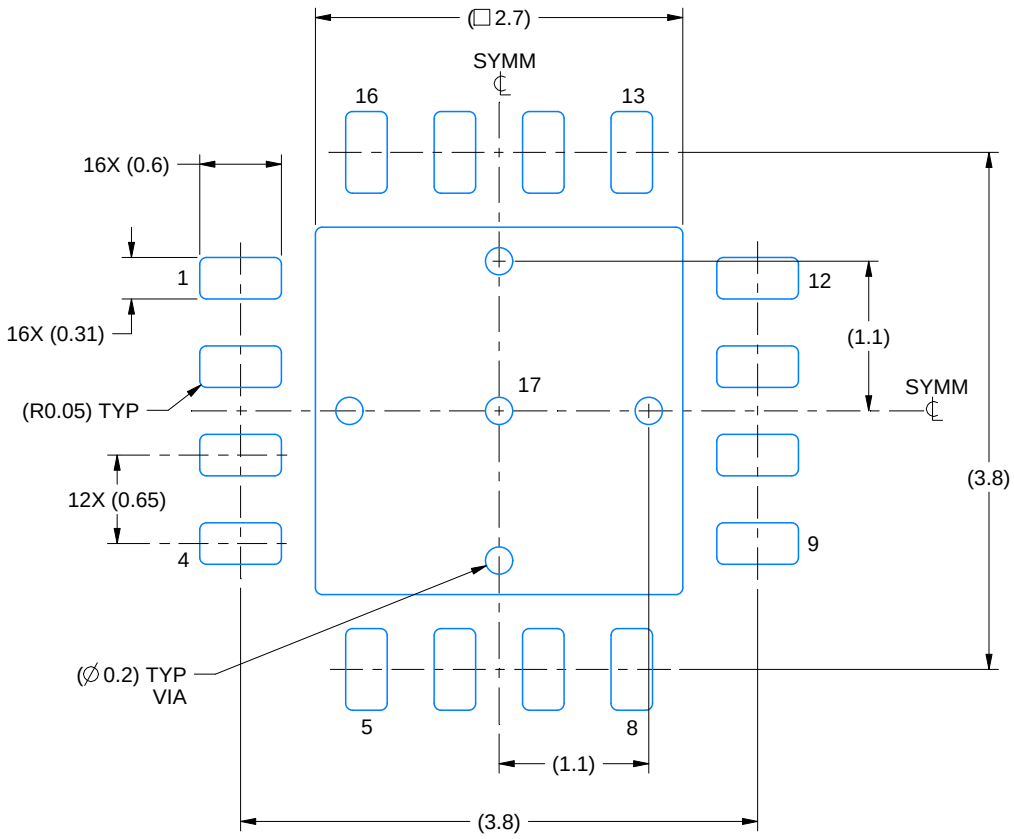
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

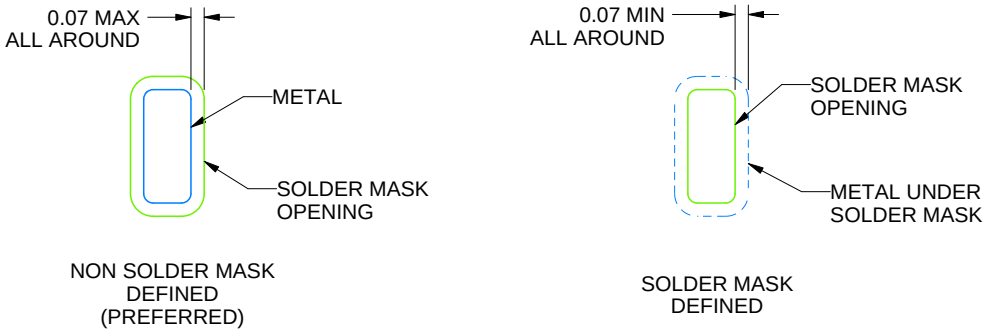


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

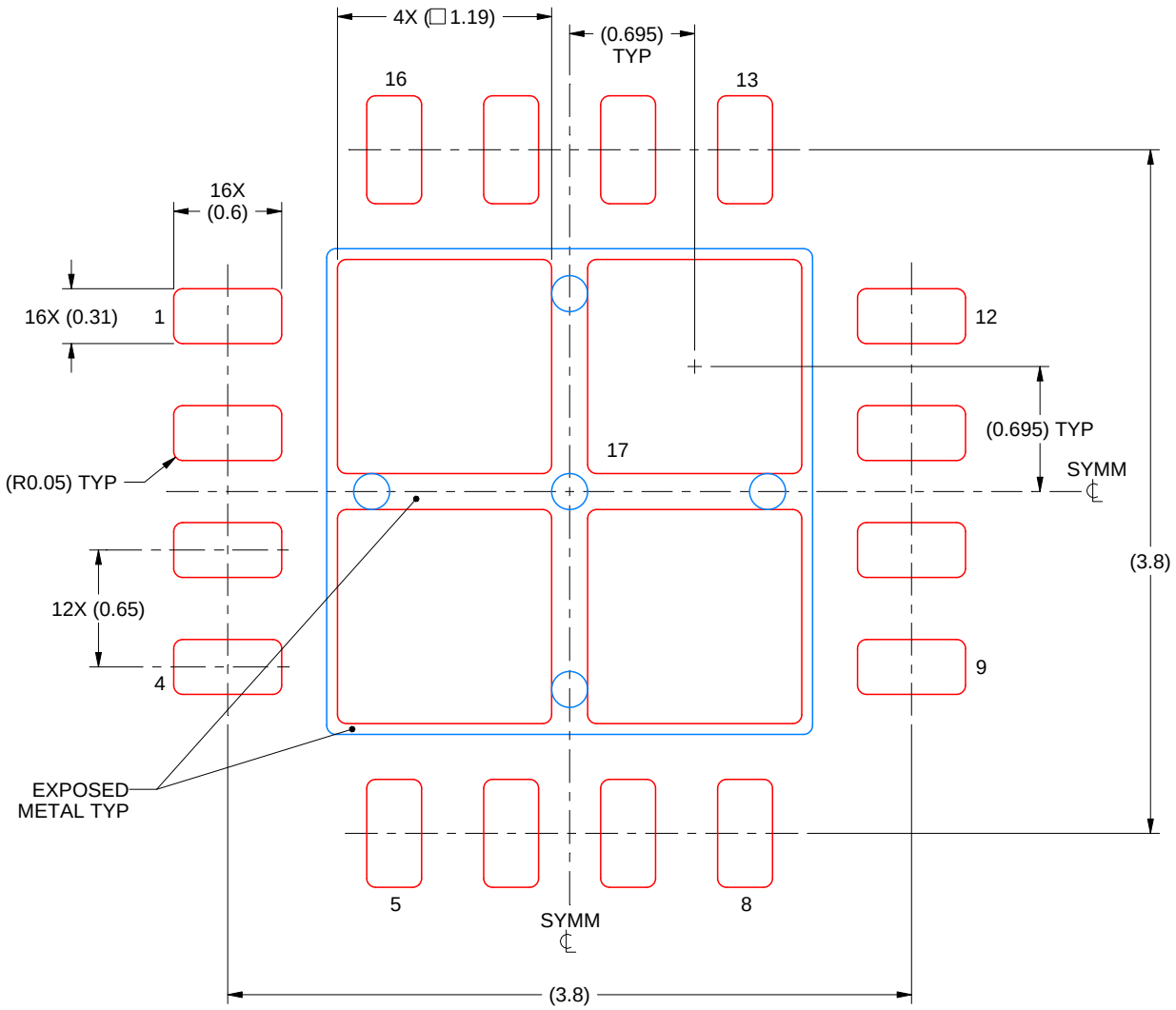


SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月