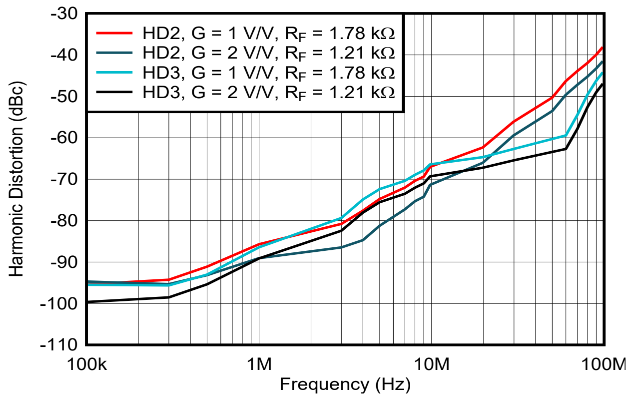
THS309x 高电压、低失真、电流反馈运算放大器

1 特性

- 低失真：
  - 在 10MHz、R_L = 1kΩ 下为 84dBc HD2
  - 在 10MHz、R_L = 1kΩ 下为 99dBc HD3
- 低噪声：
  - 15pA/ $\sqrt{\text{Hz}}$ 同相电流噪声
  - 14pA/ $\sqrt{\text{Hz}}$ 反相电流噪声
  - 1.1nV/ $\sqrt{\text{Hz}}$ 电压噪声
- 高压摆率：6000V/μs（G = 5，V_O = $20V_{PP}$）
- 宽带宽：305MHz（G = 2，R_L = 100Ω）
- 高输出电流驱动：±310mA
- 宽电源电压范围：±5V 至 ±16V
- 断电特性：仅 THS3095

2 应用

- 高电压任意波形发生器
- 引脚驱动器
- 功率 FET 驱动器
- 源测量单元 (SMU)
- 高容性负载压电元件驱动器



HD2 和 HD3 与频率间的关系（R_L = 100Ω 时）

3 描述

THS3091 和 THS3095 (THS309x) 是高电压、低失真、电流反馈、高速放大器，可在 ±5V 至 ±16V 的宽电源电压范围内运行。这几款器件非常适合需要线性输出大信号的应用（如引脚驱动器、功率 FET 驱动器和任意波形发生器）。

THS3095 具有一个断电引脚 ($\overline{\text{PD}}$)，可将放大器置于低功耗待机模式，并将静态电流从 9.5mA 降至 500μA。

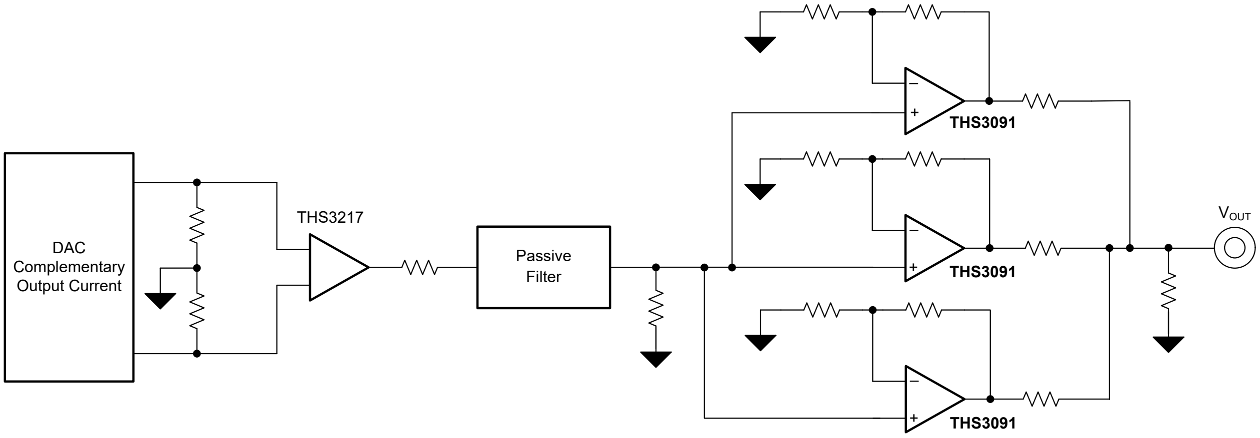
THS309x 具有 32V 的宽电源电压范围、6000V/µs 的压摆率和 310mA 的输出电流驱动能力，非常适合高电压任意波形驱动器应用。此外，这些器件能够处理大电压摆幅，驱动低阻性和高容性负载，同时保持良好的稳定时间性能，因此非常适合引脚驱动器和功率 FET 驱动器应用。

THS309x 采用 8 引脚 SOIC (DDA) PowerPAD™ 集成电路封装。THS3091 还可采用 8 引脚 HVSSOP (DGN) 封装。

器件信息(1)(2)

器件型号	$\overline{\text{PD}}$ PIN	封装
THS3091	否	DDA（SO PowerPAD，8）
		DGN（HVSSOP，8）
THS3095	是	DDA（SO PowerPAD，8）

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。
(2) 有关详细信息，请参阅*器件比较表*。



典型的任意波形发生器输出驱动电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (February 2023) to Revision K (April 2023) **Page**

- 将 THS3091 DGN 封装状态从预发布更改为量产数据（正在供货）并添加了相关内容.......... 1
- Changed voltage step from 10 V to 20 V for slew rate parameter in *Electrical Characteristics*: V_S = ± 15 V table.......... 6
- Added *Functional Block Diagram* section.......... 19

Changes from Revision I (December 2022) to Revision J (February 2023) **Page**

- 更新了 *特性* 部分.......... 1
- 更新了 *说明* 部分.......... 1
- Updated the *Device Comparison Table* section.......... 4
- Removed D package information from the data sheet.......... 4
- Removed continuous power dissipation specification from *Absolute Maximum Ratings* table.......... 5
- Updated *ESD Ratings* table.......... 5
- Updated *Thermal Information* table.......... 5
- Changed *Electrical Characteristics THS3091 table* to *Electrical Characteristics: V_S = ±15 V*.......... 6
- Updated small signal bandwidth, -3 dB specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Added small signal bandwidth, -3 dB specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables at G=1 for DGN package.......... 6
- Removed slew rate (25% to 75% level) specifications from *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Added slew rate (10% to 90% level) specifications to *Electrical Characteristics:V_S = ±15 V and Electrical Characteristics:V_S = ±5 V tables*.......... 6
- Updated rise and fall time specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated settling time specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated distortion specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6

- Updated input voltage noise specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated input current noise specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Removed differential gain and differential phase specifications from *Electrical Characteristics: V_S = ±15 V and Electrical Characteristics: VS = ±5 V* tables.......... 6
- Updated transimpendance specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Removed specifications with T_A = 0℃ to 70℃ test conditions in Electrical Characteristics: V_S = ±15 V and Electrical Characteristics: V_S = ±5 V tables.......... 6
- Updated max input voltage specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated max inverting input bias current specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated max input offset current drift specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated average offset voltage drift specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated average bias current drift specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated average offset current drift specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated common-mode rejection ratio specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated noninverting input resistance and capacitance specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated output current specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Removed specified operating voltage specifications from *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Updated power supply rejection specifications in *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±5 V* tables.......... 6
- Changed Electrical Characteristics THS3095 to *Electrical Characteristics: V_S = ±5V* 9
- Removed *Dissipation Ratings* table.......... 11
- Updated *Typical Characteristics (±15 V)* section.......... 11
- Updated *Typical Characteristics: (±5 V)* section.......... 17
- Updated *Feature Description* section.......... 19
- Updated *Device Functional Modes* section.......... 21
- Updated *Application and Implementation* section.......... 22
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- Updated *Layout* section.......... 25

Changes from Revision H (October 2015) to Revision I (December 2022) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.......... 1
- 向数据表添加了 *DGN* 封装信息.......... 1
- Added the *Device Comparison Table* section.......... 4
- Updated *Thermal Information* table.......... 5

5 Device Comparison Table

DEVICE	MAX SUPPLY, V_S (V)	SSBW, A_V = 5 (MHz)	MAXIMUM ICC AT 25°C (mA)	INPUT NOISE V_n (nV/√Hz)	SLEW RATE (V/μs)	LINEAR OUTPUT CURRENT (mA)
THS3491	±16	900	17.3	1.7	8000	±420
THS3095	±16	205	10.5	1.1	6000	±310
OPA695	±6	700 (A_V = 4)	13.3	1.8	4300	±90
THS3001	±16	350	7.5	1.6	6300	±120
THS3115	±15	100 (A_V = 4)	5.5	2.2	1550	±270

6 Pin Configuration and Functions

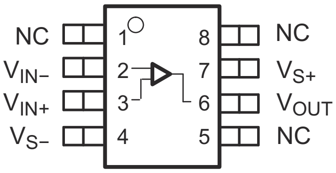


图 6-1. DGN or DDA Package, 8-Pin SOIC, HVSSOP or SO-PowerPAD THS3091 (Top View)

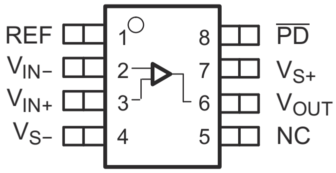


图 6-2. DDA Package, SO-PowerPAD THS3095 (Top View)

表 6-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	THS3091	THS3095		
NC	1, 5, 8	5	—	No connection
$\overline{PD}$	—	8	I	Amplifier power down Low = amplifier disabled High (default) = amplifier enabled
REF	—	1	I	Voltage reference input to set $\overline{PD}$ threshold level
V_{IN-}	2	2	I	Inverting input
V_{IN+}	3	3	I	Noninverting input
V_{OUT}	6	6	O	Output of amplifier
V_{S-}	4	4	P	Negative power supply
V_{S+}	7	7	P	Positive power supply

[1] I= input, O = output, POW= power, and NC = no internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			33	V
V_I	Input voltage			$\pm V_S$	V
V_{ID}	Differential input voltage			±4	V
I_O	Output current			350	mA
T_J (2)	Junction temperature	Maximum		150	°C
		Continuous operation, long-term reliability		125	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature can result in reduced reliability, reduced lifetime of the device, or both.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Dual supply	±5	±15	±16	V
		Single supply	10	30	32	
T_A	Operating free-air temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS309x	THS3091	UNIT
		DDA (SO PowerPAD)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.4	60.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.0	87.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.2	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.5	32.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.1	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: V_S = ±15 V

at T_A ≅ 25°C, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth, –3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}	DDA package		715		MHz
		DGN package		600		
	G = 2, R_F = 1.21 kΩ, V_O = 200 mV_{PP}			305		
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}			205		
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}			190		
0.1-dB bandwidth flatness	V_O = 200 mV_{PP}			95		MHz
Large-signal bandwidth	G = 5, R_F = 1 kΩ, V_O = 4 V_{PP}			135		MHz
Slew rate (10% to 90% level)	G = 2, V_O = 10-V step, R_F = 1.21 kΩ			3600		V/μs
	G = 5, V_O = 20-V step, R_F = 1 kΩ			6000		
Rise and fall time	V_O = 5 V_{PP}			2		ns
Settling time	G = –2, V_O = 2-V_{PP} step	to 0.1%		12.5		ns
		to 0.01%		18.5		
HARMONIC DISTORTION						
2nd harmonic distortion	V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω		72		dBc
		R_L = 1 kΩ		84		
3rd harmonic distortion	V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω		70		dBc
		R_L = 1 kΩ		99		
Input voltage noise	f > 10 kHz			1.1		nV/√Hz
Noninverting input current noise	f > 10 kHz			15		pA/√Hz
Inverting input current noise	f > 10 kHz			14		pA/√Hz
DC PERFORMANCE						
Open-loop transimpedance	V_O = ±7.5 V, G = 1	T_A = 25°C	350	1800		kΩ
		T_A = –40°C to +85°C	300			
Input offset voltage	V_{CM} = 0 V	T_A = 25°C		0.9	3	mV
		T_A = –40°C to +85°C			5	
Noninverting input bias current	V_{CM} = 0 V	T_A = 25°C		4	15	μA
		T_A = –40°C to +85°C			20	
Inverting input bias current	V_{CM} = 0 V	T_A = 25°C		3.5	15	μA
		T_A = –40°C to +85°C			25	
Input offset current	V_{CM} = 0 V	T_A = 25°C		1.7	20	μA
		T_A = –40°C to +85°C			30	
Average offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±19		μV/°C
Average noninverting bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±20		nA/°C
Average inverting bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±80		nA/°C
Average offset current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±80		nA/°C

7.5 Electrical Characteristics: V_S = ±15 V (continued)

at T_A ≅ 25°C, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Common-mode input range	T_A = 25°C		±13.3	±13.6		V
	T_A = –40°C to +85°C		±13			
Common-mode rejection ratio	V_{CM} = ±10 V	T_A = 25°C	62	78		dB
		T_A = –40°C to +85°C	59			
Noninverting input resistance				0.7		MΩ
Noninverting input capacitance				2.4		pF
Inverting input resistance				30		Ω
Inverting input capacitance				1.4		pF
OUTPUT CHARACTERISTICS						
Output voltage swing	R_L = 1 kΩ	T_A = 25°C	±12.8	±13.2		V
		T_A = –40°C to +85°C	±12.5			
	R_L = 100 Ω	T_A = 25°C	±12.1	±12.5		
		T_A = –40°C to +85°C	±11.8			
Output current	Sourcing, R_L = 40 Ω	T_A= 25°C	225	310		mA
		T_A = –40°C to +85°C	200			
	Sinking, R_L = 40 Ω	T_A = 25°C	200	310		
		T_A = –40°C to +85°C	175			
Output impedance	f = 1 MHz, closed loop			0.06		Ω
POWER SUPPLY						
Quiescent current	T_A = 25°C		8.5	9.5	10.5	mA
	T_A = –40°C to +85°C		8		11	
Power supply rejection	+PSRR	T_A = 25°C	70	85		dB
		T_A = –40°C to +85°C	65			
	–PSRR	T_A = 25°C	68	82		
		T_A = –40°C to +85°C	65			
POWER-DOWN CHARACTERISTICS (THS3095 ONLY)						
REF voltage range((1))			V_{S-}		V_{S+} – 4	V
Power-down voltage level(1)	Enable			$\overline{PD}$ ⩾ REF +2		V
	Disable			$\overline{PD}$ ⩽ REF +0.8		
Power-down quiescent current	$\overline{PD}$ = 0 V	T_A = 25°C		500	700	μA
		T_A = –40°C to +85°C			800	

7.5 Electrical Characteristics: V_S = ±15 V (continued)

at $T_A \cong 25°C$, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\overline{PD}$ bias current	$\overline{PD}$ = 0 V, REF = 0 V,	T_A = 25°C		11	15	µA
		T_A = –40°C to +85°C			20	
	$\overline{PD}$ = 3.3 V, REF = 0 V	T_A = 25°C		11	15	
		T_A = –40°C to +85°C			20	
Turn-on time delay	90% of final value			60		µs
Turn-off time delay	10% of final value			150		

(1) For detailed information on the behavior of the power-down circuit, see 节 8.3.1.

7.6 Electrical Characteristics: V_S = ±5 V

at T_A ≅ 25°C, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth, –3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}	DDA package		485		MHz
		DGN package		435		
	G = 2, R_F = 1.15 kΩ, V_O = 200 mV_{PP}			215		
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}			160		
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}			160		
0.1-dB bandwidth flatness	V_O = 200 mV_{PP}			50		MHz
Large-signal bandwidth	V_O = 4 V_{PP}			205		MHz
Slew rate (10% to 90% level)	G = 2, V_O= 5-V step, R_F = 1.21 kΩ			1800		V/μs
	G = 5, V_O= 5-V step, R_F = 1.21 kΩ			1700		
Rise and fall time	G = 2, V_O = 5-V step, R_F = 1.21 kΩ			2		ns
Settling time	G = –2, V_O = 2-V_{PP} step	to 0.1%		12.5		ns
		to 0.01%		26		
HARMONIC DISTORTION						
2nd harmonic distortion	V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω		74		dBc
		R_L = 1 kΩ		76		
3rd harmonic distortion	V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω		70		dBc
		R_L = 1 kΩ		75		
Input voltage noise	f > 10 kHz			1.1		nV/√Hz
Noninverting input current noise	f > 10 kHz			15		pA/√Hz
Inverting input current noise	f > 10 kHz			14		pA/√Hz
DC PERFORMANCE						
Open-loop transimpedance	V_O = ±2.5 V, G = 1	T_A = 25°C	250	1500		kΩ
		T_A= –40°C to +85°C	200			
Input offset voltage	V_{CM} = 0 V	T_A = 25°C		0.6	2	mV
		T_A= –40°C to +85°C			3.5	
Noninverting input bias current	V_{CM} = 0 V	T_A = 25°C		2	15	μA
		T_A= –40°C to +85°C			20	
Inverting input bias current	V_{CM} = 0 V	T_A = 25°C		5	15	μA
		T_A= –40°C to +85°C			25	μA
Input offset current	V_{CM} = 0 V	T_A = 25°C		1.5	10	μA
		T_A= –40°C to +85°C			20	
Average offset voltage drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±20		μV/°C
Average noninverting bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±20		nA/°C
Average inverting bias current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±95		nA/°C
Average offset current drift	V_{CM} = 0 V, T_A = –40°C to +85°C			±90		nA/°C

7.6 Electrical Characteristics: V_S = ±5 V (continued)

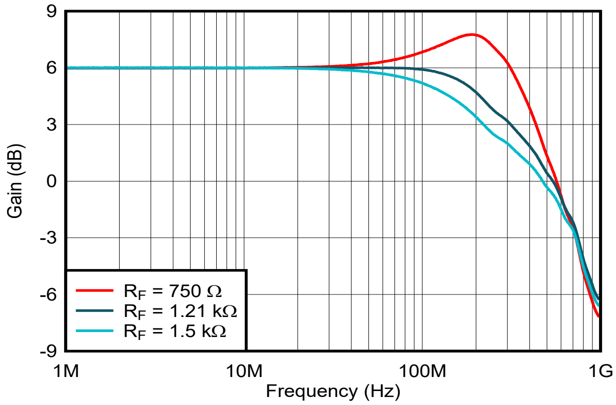
at T_A ≅ 25°C, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Common-mode input range	T_A = 25°C		±3.3	±3.6		V
	T_A= –40°C to +85°C		±3			
Common-mode rejection ratio	V_{CM} = ±2.0 V, V_O = 0 V	T_A = 25°C	60	66		dB
		T_A= –40°C to +85°C	57			
Noninverting input resistance				0.45		MΩ
Noninverting input capacitance				2.6		pF
Inverting input resistance				32		Ω
Inverting input capacitance				1.5		pF
OUTPUT CHARACTERISTICS						
Output voltage swing	R_L = 1 kΩ	T_A = 25°C	±3.1	±3.4		V
		T_A= –40°C to +85°C	±2.8			
Output voltage swing	R_L = 100 Ω	T_A = 25°C	±2.7	±3.1		
		T_A= –40°C to +85°C	±2.5			
Output current	Sourcing, R_L = 10 Ω	T_A = 25°C	140	250		mA
		T_A= –40°C to +85°C	120			
	Sinking, R_L = 10 Ω	T_A = 25°C	–140	–250		
		T_A= –40°C to +85°C	–120			
Output impedance	f = 1 MHz, closed loop			0.09		Ω
POWER SUPPLY						
Quiescent current	T_A = 25°C		7	8.2	9	mA
	T_A= –40°C to +85°C		6.5		9.5	
Power supply rejection	+PSRR	T_A = 25°C	68	81		dB
		T_A= –40°C to +85°C	63			
	–PSRR	T_A = 25°C	65	79		
		T_A= –40°C to +85°C	60			
POWER-DOWN CHARACTERISTICS (THS3095 ONLY)						
REF voltage range((1))			V_{S-}		V_{S+} – 4	V
Power-down voltage level(1)	Enable			$\overline{PD}$ ≥ REF+2		V
	Disable			$\overline{PD}$ ≤ REF+0.8		
Power-down quiescent current	$\overline{PD}$ = 0 V	T_A = 25°C		300	500	µA
		T_A= –40°C to +85°C			600	
$\overline{PD}$ bias current	$\overline{PD}$ = 0 V, REF = 0 V,	T_A = 25°C		11	15	µA
		T_A –40°C to +85°C			20	
	$\overline{PD}$ = 3.3 V, REF = 0 V	T_A = 25°C		11	15	
		T_A= –40°C to +85°C			20	
Turn-on time delay	90% of final value			60		µs
Turn-off time delay	10% of final value			150		µs

(1) For detailed information on the behavior of the power-down circuit, see 节 8.3.1.

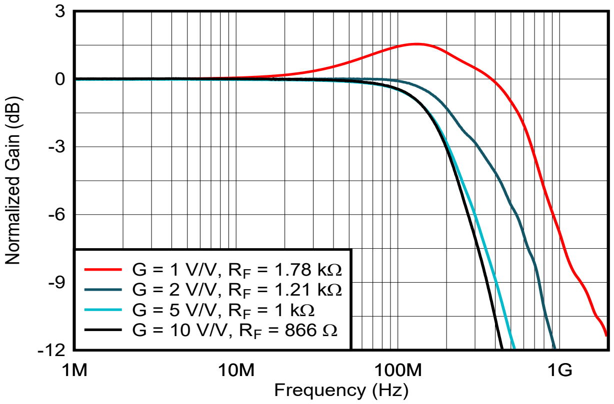
7.7 Typical Characteristics: ±15 V

at T_A ≅ 25°C, V_S = ±15 V, R_F = 1.21 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)



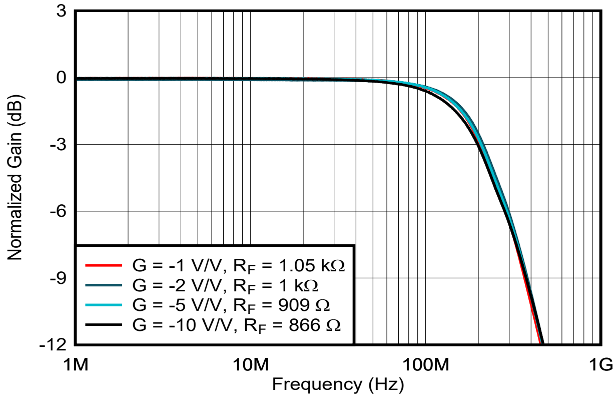
V_{OUT} = 200 mV_{PP}

图 7-1. Noninverting Small-Signal Frequency Response



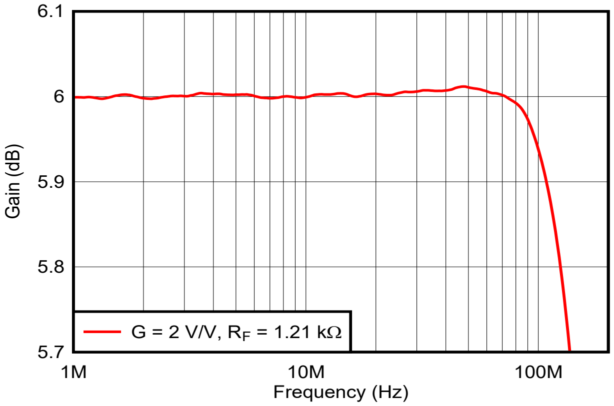
V_{OUT} = 200 mV_{PP}

图 7-2. Noninverting Small-Signal Frequency Response



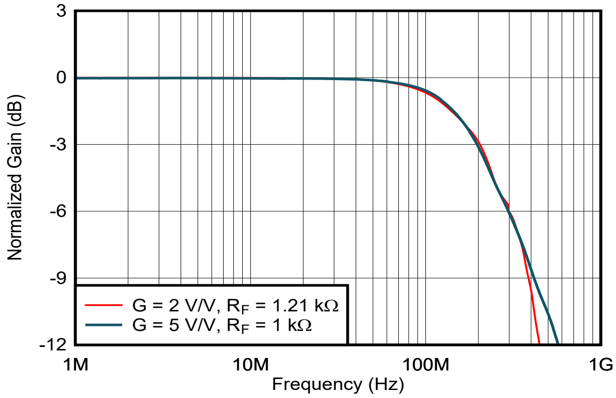
V_{OUT} = 200 mV_{PP}

图 7-3. Inverting Small-Signal Frequency Response



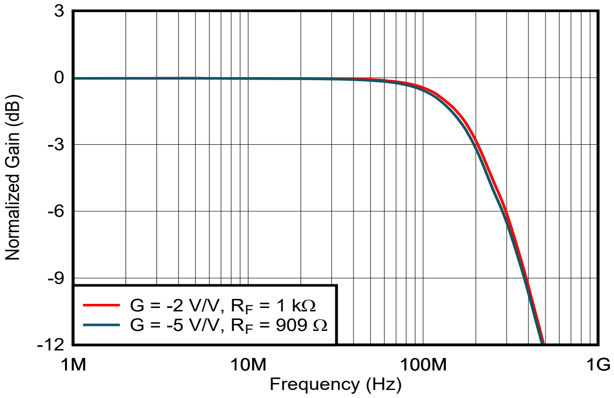
V_{OUT} = 200 mV_{PP}

图 7-4. 0.1-db Gain Flatness Frequency Response



V_{OUT} = 4 V_{PP}

图 7-5. Noninverting Large-Signal Frequency Response

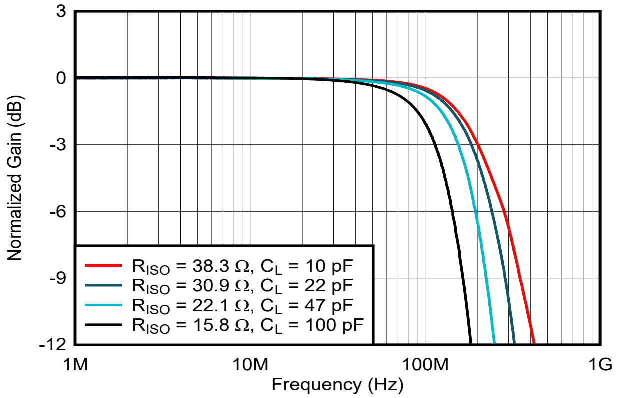


V_{OUT} = 4 V_{PP}

图 7-6. Inverting Large-Signal Frequency Response

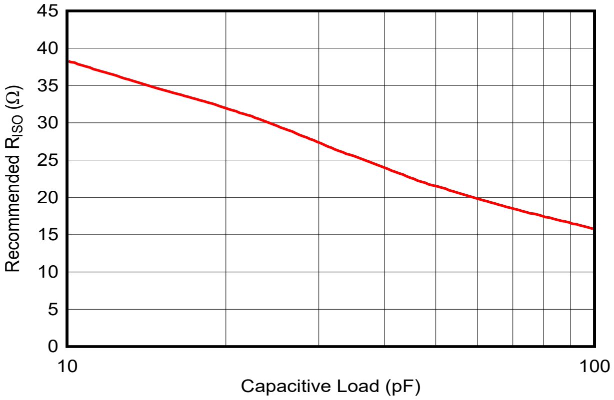
7.7 Typical Characteristics: ±15 V (continued)

at T_A ≅ 25°C, V_S = ±15 V, R_F = 1.21 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)



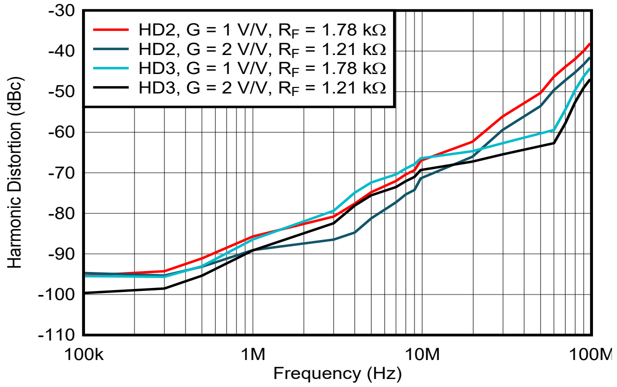
V_{OUT} = 200 mV$_{PP}$, Gain = 5 V/V, R_F = 1 kΩ

图 7-7. Capacitive Load Frequency Response



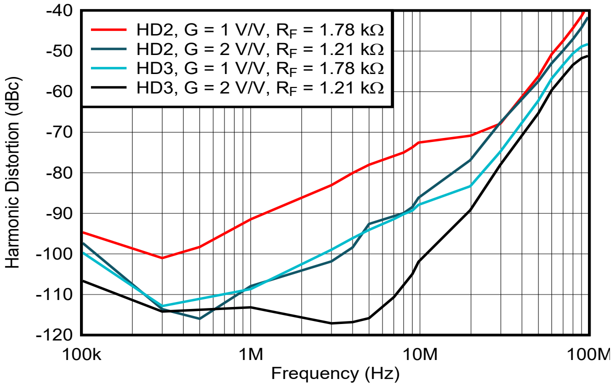
Gain = 5 V/V, R_F = 1 kΩ

图 7-8. Recommended R_{ISO} vs Capacitive Load



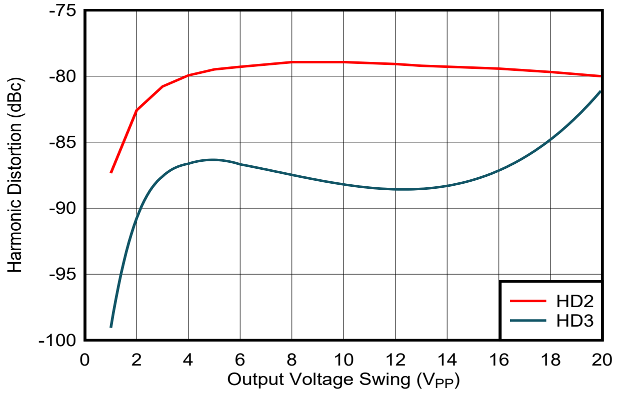
V_{OUT} = 4 V_{PP}

图 7-9. Harmonic Distortion vs Frequency



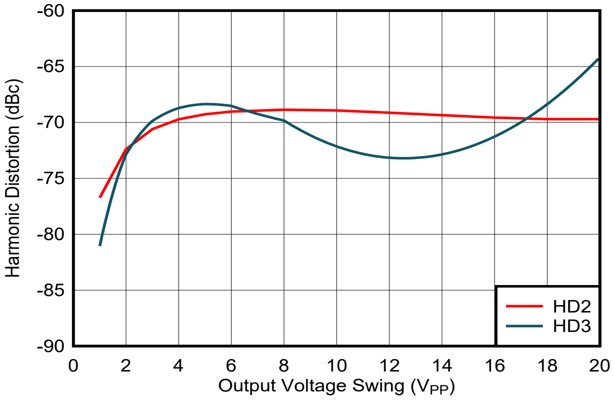
V_{OUT} = 4 V_{PP}, R_L = 1 kΩ

图 7-10. Harmonic Distortion vs Frequency



Gain = 5 V/V, R_F = 1 kΩ, f = 1 MHz

图 7-11. Harmonic Distortion vs Output Voltage Swing

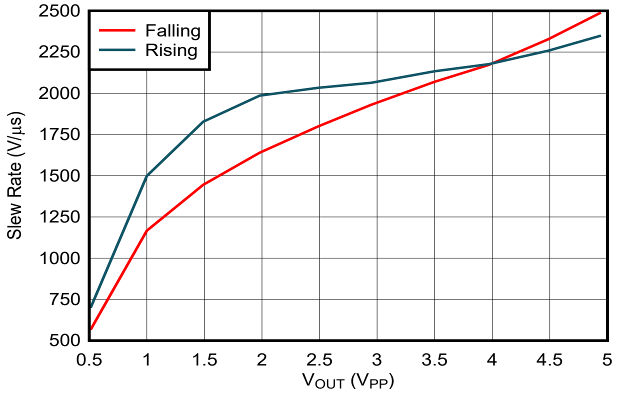


Gain = 5 V/V, R_F = 1 kΩ, f = 8 MHz

图 7-12. Harmonic Distortion vs Output Voltage Swing

7.7 Typical Characteristics: ±15 V (continued)

at T_A ≅ 25°C, V_S = ±15 V, R_F = 1.21 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)



Gain = 1 V/V, R_F = 1.78 kΩ

图 7-13. Slew Rate vs Output Voltage Step

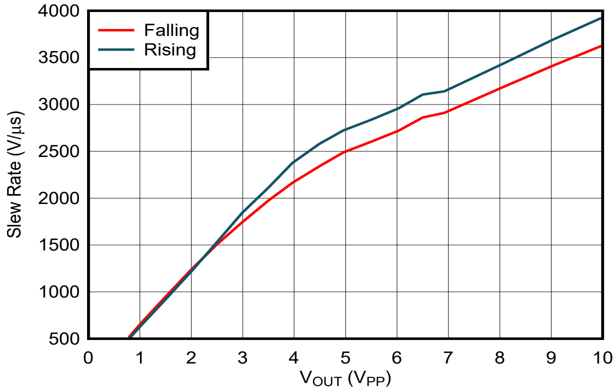
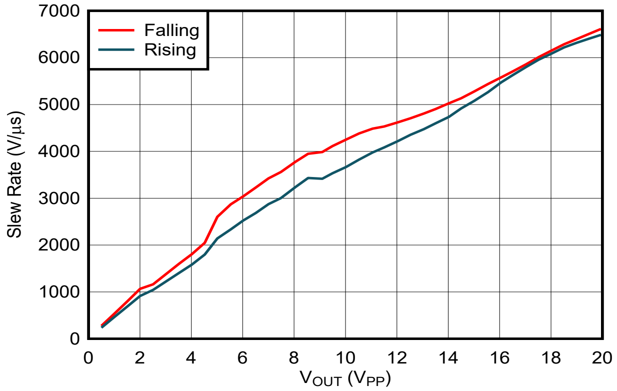


图 7-14. Slew Rate vs Output Voltage Step



Gain = 5 V/V, R_F = 1 kΩ

图 7-15. Slew Rate vs Output Voltage Step

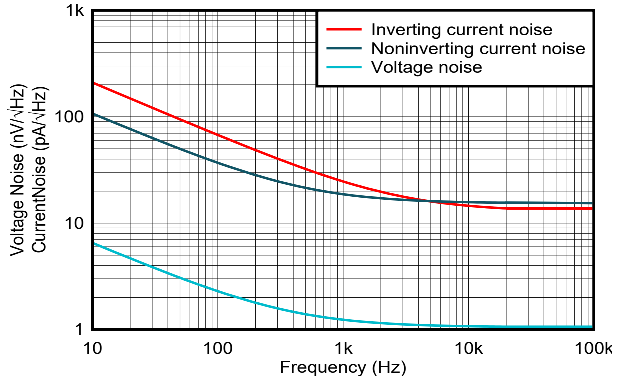
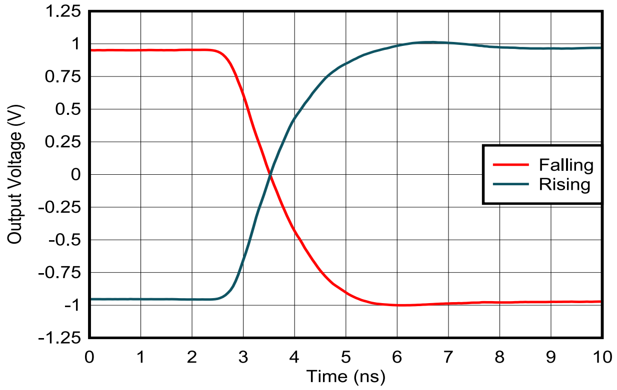
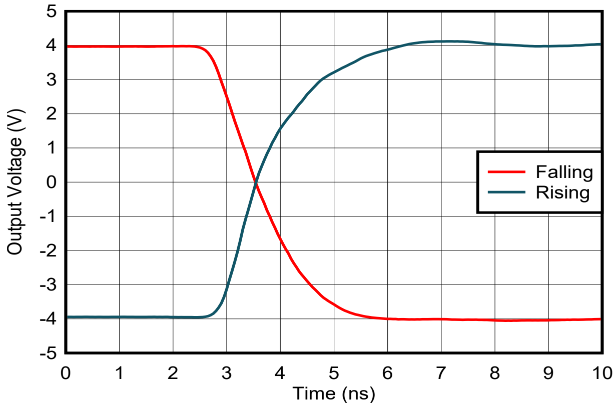


图 7-16. Noise vs Frequency



Gain = –2 V/V, R_F = 1 kΩ

图 7-17. Settling Time



Gain = 5 V/V, R_F = 1 kΩ

图 7-18. Settling Time

7.7 Typical Characteristics: ±15 V (continued)

at $T_A \cong 25°C$, $V_S = ±15$ V, $R_F = 1.21$ kΩ, G = +2 V/V, and $R_L = 100$ Ω (unless otherwise noted)

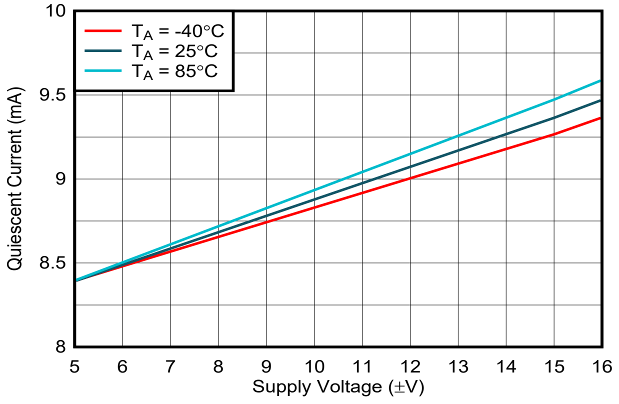


图 7-19. Quiescent Current vs Supply Voltage

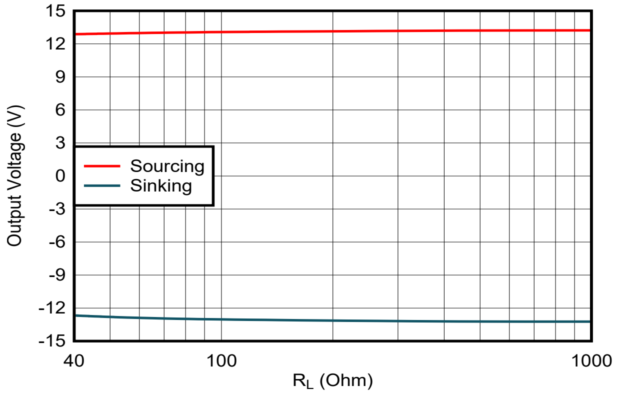


图 7-20. Output Voltage vs Load Resistance

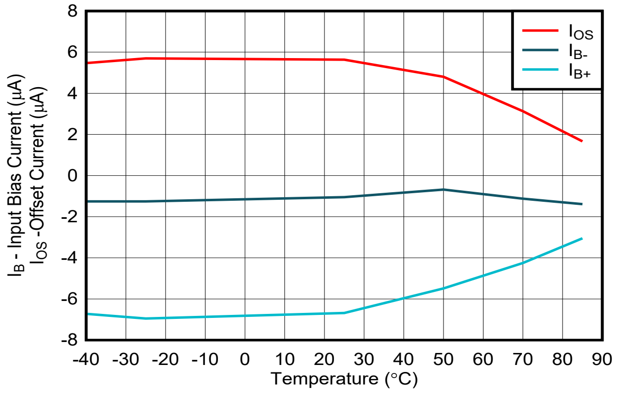


图 7-21. Input Bias and Offset Current vs Case Temperature

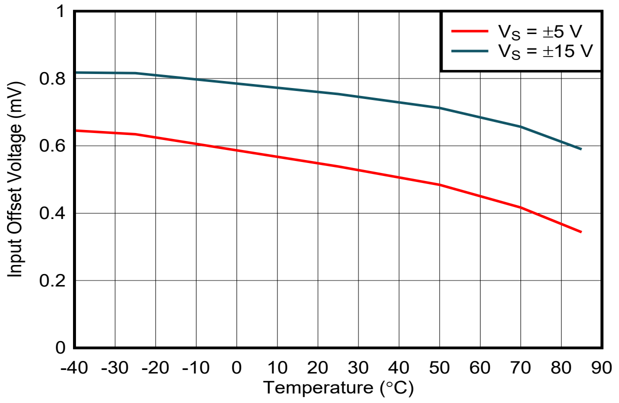


图 7-22. Input Offset Voltage vs Case Temperature

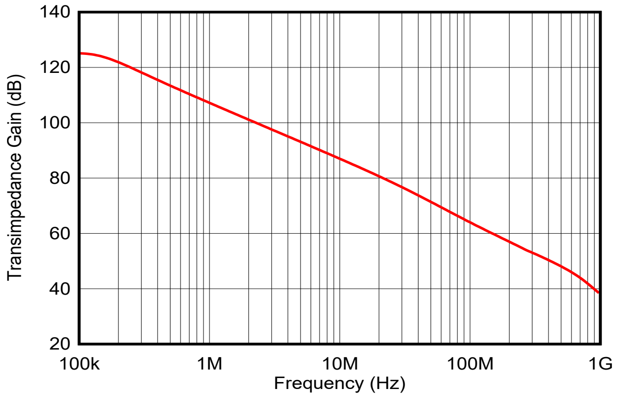


图 7-23. Transimpedance vs Frequency

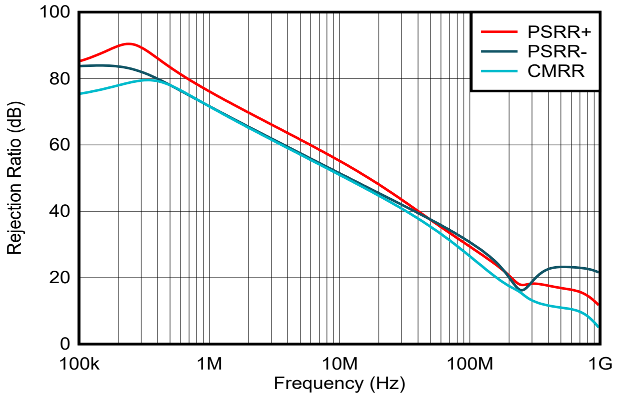
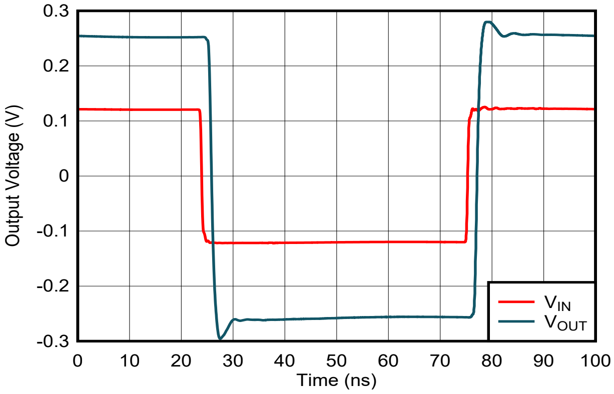


图 7-24. Rejection Ratio vs Frequency

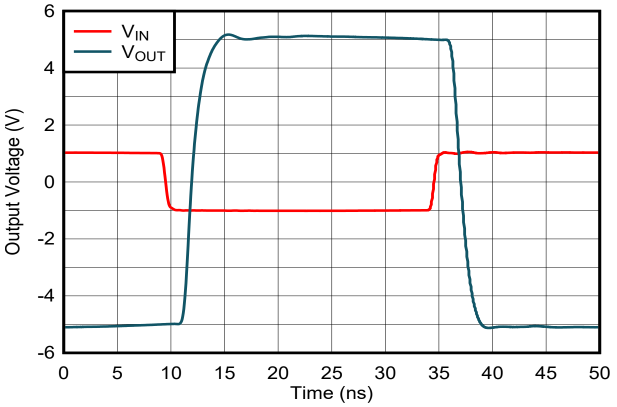
7.7 Typical Characteristics: ±15 V (continued)

at T_A ≅ 25°C, V_S = ±15 V, R_F = 1.21 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)



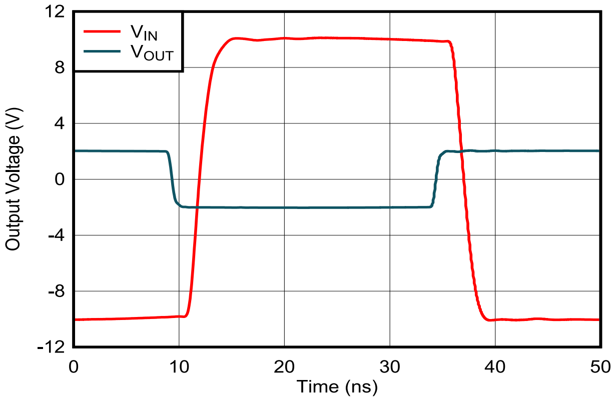
Gain = 2 V/V, R_F = 1 kΩ

图 7-25. Noninverting Small-Signal Transient Response



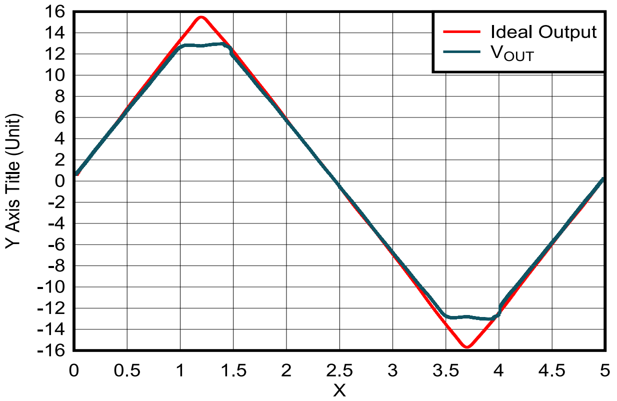
Gain = -5 V/V, R_F = 909 Ω

图 7-26. Inverting Large-Signal Transient Response



Gain = -5 V/V, R_F = 909 Ω

图 7-27. Inverting Large-Signal Transient Response



Gain = 5 V/V, R_F = 1 kΩ

图 7-28. Output Overdrive Recovery Time

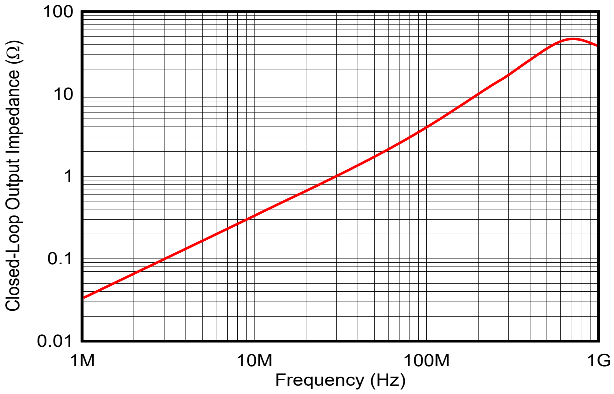


图 7-29. Closed-Loop Output Impedance vs Frequency

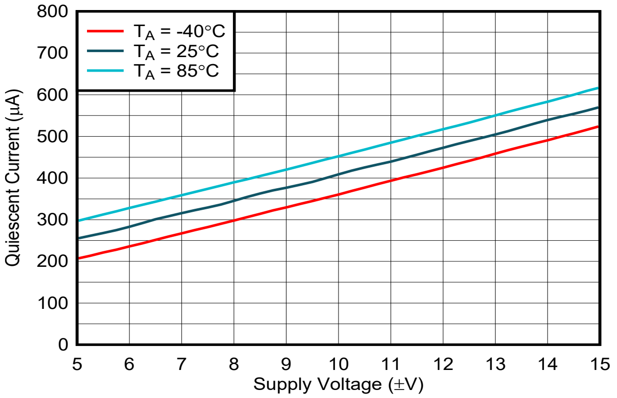
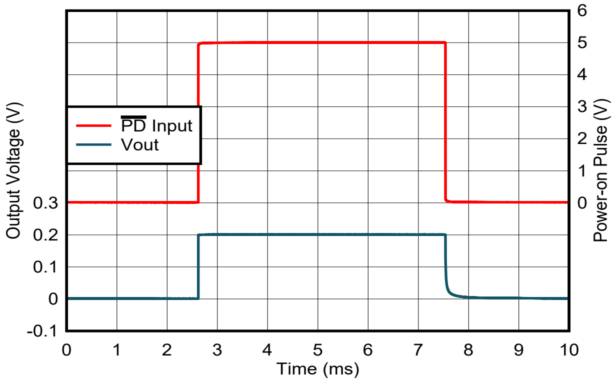


图 7-30. Power-Down Quiescent Current vs Supply Voltage

7.7 Typical Characteristics: ±15 V (continued)

at T_A ≅ 25°C, V_S = ±15 V, R_F = 1.21 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)

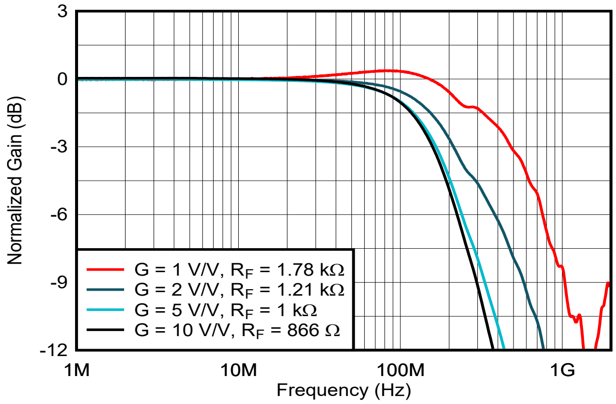


V_{IN} = 0.1 V

图 7-31. Turnon and Turnoff Time Delay

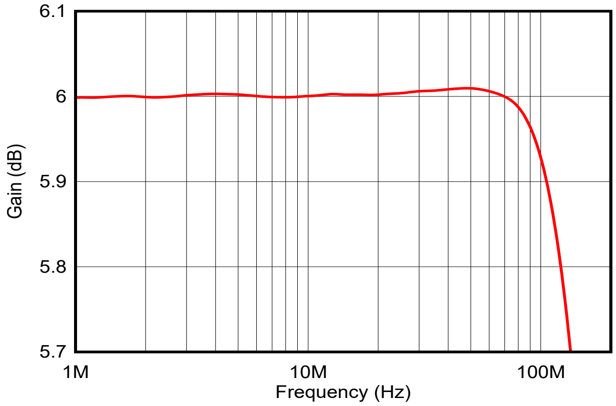
7.8 Typical Characteristics: ±5 V

at T_A ≅ 25°C, V_S = ±5 V, R_F = 1.15 kΩ, G = +2 V/V, and R_L = 100 Ω (unless otherwise noted)



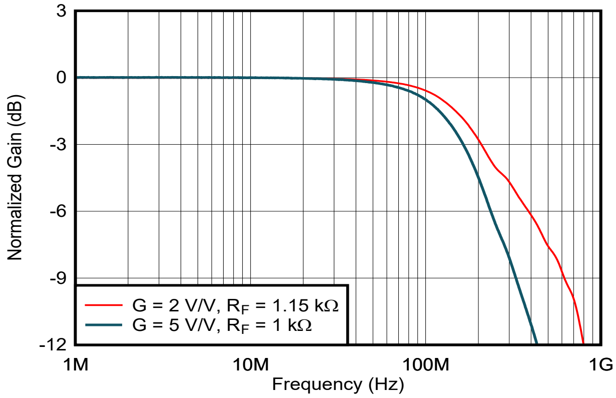
V_{OUT} = 200 mV_{PP}

图 7-32. Noninverting Small-Signal Frequency Response



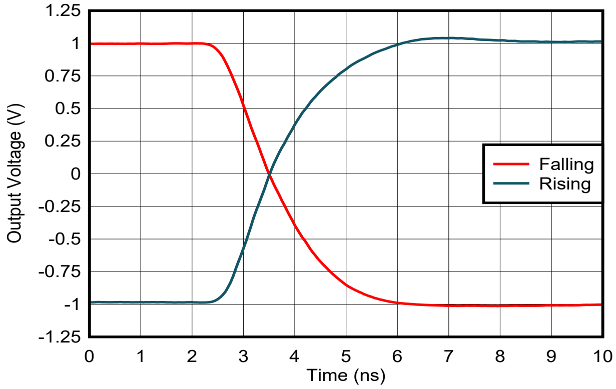
V_{OUT} = 200 mV_{PP}, R_F = 1.21 kΩ

图 7-33. 0.1-db Gain Flatness Frequency Response



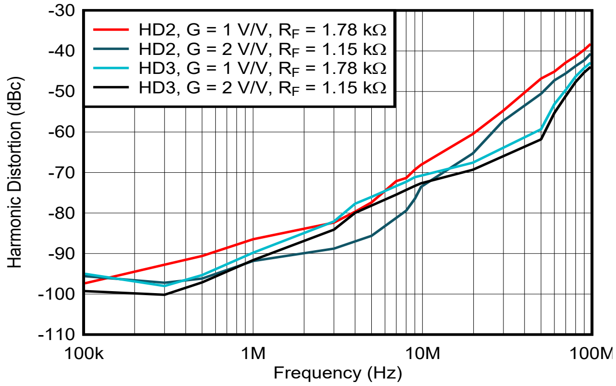
V_{OUT} = 4 V_{PP}

图 7-34. Noninverting Large-Signal Frequency Response



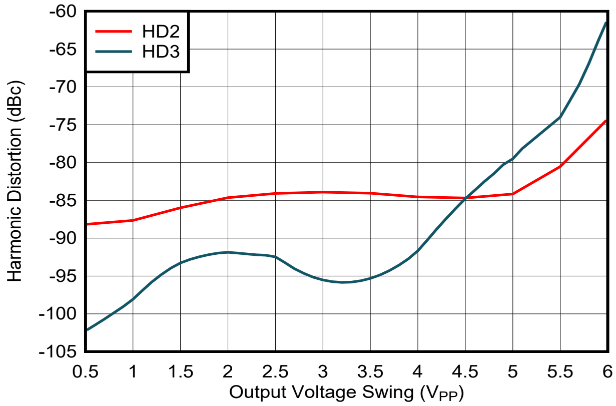
G = -2 V/V, R_F = 1 kΩ

图 7-35. Settling Time



V_{OUT} = 2 V_{PP}

图 7-36. Harmonic Distortion vs Frequency

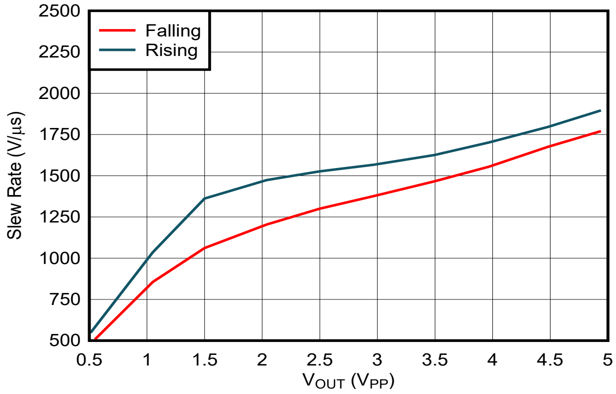


G = 5 V/V, R_F = 1 kΩ, f = 1 MHz

图 7-37. Harmonic Distortion vs Output Voltage Swing

7.8 Typical Characteristics: ±5 V (continued)

at $T_A \cong 25°C$, $V_S = ±5$ V, $R_F = 1.15$ kΩ, G = +2 V/V, and $R_L = 100$ Ω (unless otherwise noted)



G = 1 V/V, R_F = 1.78 kΩ

图 7-38. Slew Rate vs Output Voltage Step

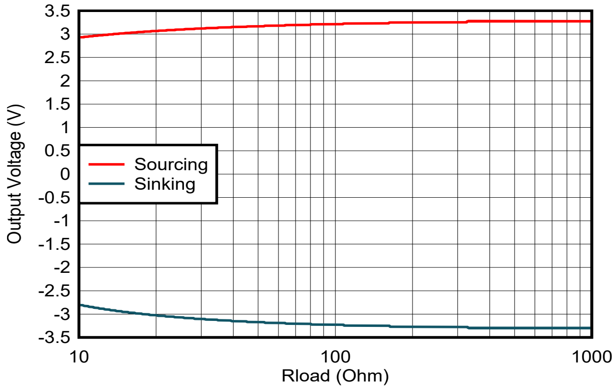


图 7-39. Output Voltage vs Load Resistance

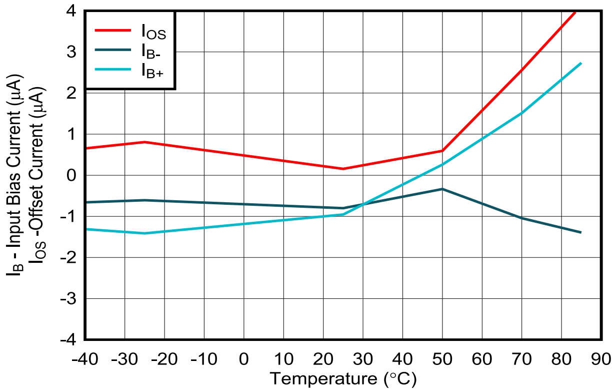


图 7-40. Input Bias and Offset Current vs Case Temperature

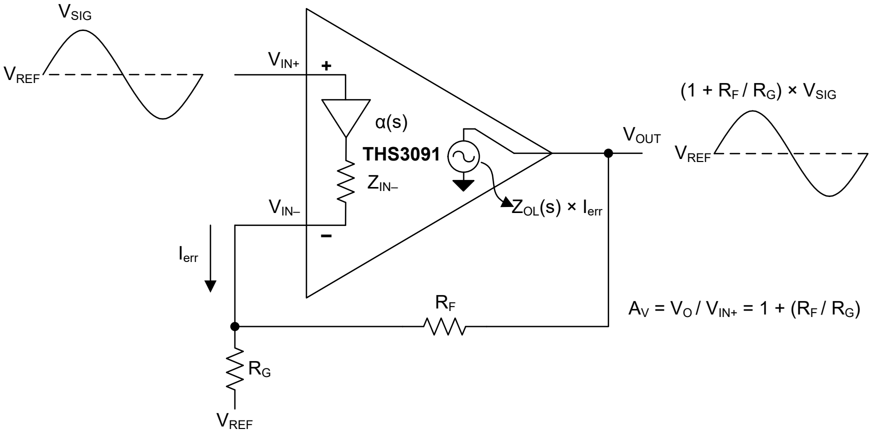
8 Detailed Description

8.1 Overview

The THS3091 and THS3095 (THS309x) are high-voltage, low-distortion, high-speed, current feedback amplifiers. The THS309x are designed to operate over a wide supply range of ±5 V to ±16 V for applications requiring large, linear output swings, such as arbitrary waveform generators.

The THS3095 also features a power-down pin that puts the amplifier into a low-power standby mode, and lowers the quiescent current from 9.5 mA to 500 µA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Down and Reference Pins Functionality

The THS3095 features a power-down pin ($\overline{PD}$) designed to reduce system power that lowers the quiescent current from 9.5 mA down to 500 µA. The THS3095 also features a reference pin (REF) that allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin.

The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. Driving the power-down pin towards the negative rail will turn off the amplifier and conserve power The following equations show the relationship between the reference voltage and the power-down thresholds:

$$\overline{PD} \leq REF + 0.8\,V\,for\ disable \tag{1}$$

$$\overline{PD} \leq REF + 2.0\,V\,for\ enable \tag{2}$$

where the usable range at the REF pin is:

$$V_{S-} \leq V_{REF} \leq (V_{S+} - 4\,V) \tag{3}$$

The recommended mode of operation is to tie the REF pin to midrail, thus setting the disable or enable thresholds to the following equations:

$$V_{midrail} + 0.8\,V \tag{4}$$

$$V_{midrail} + 2\,V \tag{5}$$

Power-Down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a tri-state bus driver. When in Power-Down mode, the impedance at the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device varies depending on the voltage applied to the outputs.

图 8-1 shows the total system output impedance, which includes the amplifier output impedance in parallel with the feedback plus gain resistors, and cumulates to 2416 Ω. 图 8-2 shows this circuit configuration for reference.

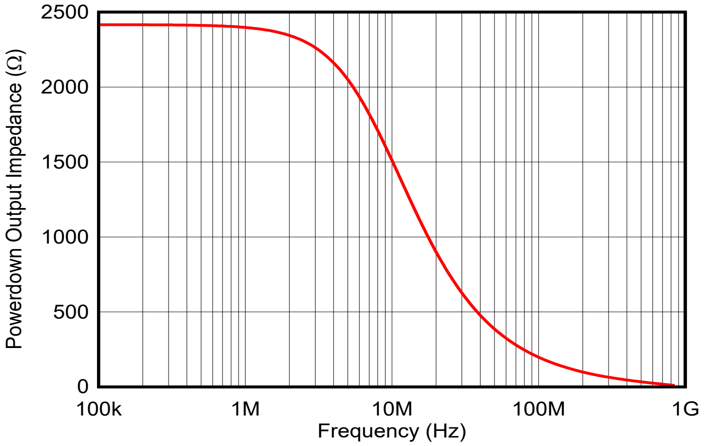


图 8-1. Power-Down Output Impedance vs Frequency

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in Power-Down mode. Most notably is the fact that the amplifier actually turns on if there is a ±0.7 V or greater difference between the two input nodes (V_{IN+} and V_{IN-}) of the amplifier. If this difference exceeds ±0.7 V, then the output of the amplifier creates an output voltage equal to approximately $[(V_{IN+} - V_{IN-}) - 0.7\ V] \times \text{Gain}$. This also implies that if a voltage is applied to the output while in Power-Down mode, the $V-$ node voltage is equal to $V_{O(applied)} \times R_G / (R_F + R_G)$. For low-gain configurations and a large applied voltage at the output, the amplifier can actually turn on due to the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time required for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

8.4 Device Functional Modes

8.4.1 Wideband, Noninverting Operation

The THS309x are unity gain stable 715-MHz current-feedback operational amplifiers designed to operate from a ±5-V to ±15-V power supply. 图 8-2 shows the THS3091 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with a 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

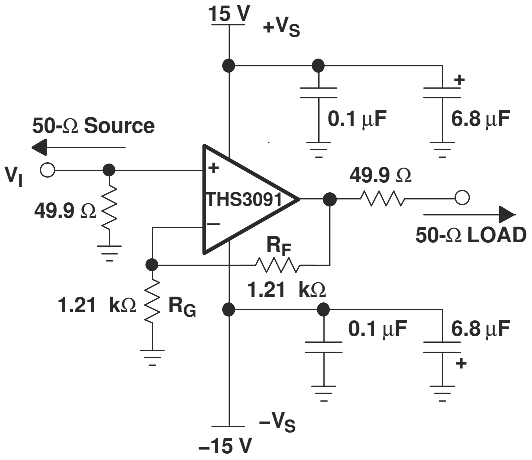


图 8-2. Wideband, Noninverting Gain Configuration

Current-feedback amplifiers are highly dependent on feedback resistor R_F for maximum performance and stability. 表 8-1 shows the optimal gain-setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved (at the expense of added peaking in the frequency response) by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but improves stability.

表 8-1. Recommended Resistor Values for Optimum Frequency Response

THS3091 AND THS3095 R_F AND R_G VALUES FOR MINIMAL PEAKING WITH R_L = 100 Ω			
GAIN (V/V)	SUPPLY VOLTAGE (V)	R_G (Ω)	R_F (Ω)
1	±5 and ±15	—	1.78 k
2	±5	1.15 k	1.15 k
	±15	1.21 k	1.21 k
5	±5 and ±15	249	1 k
10	±5 and ±15	95.3	866
–1	±5 and ±15	1.05 k	1.05 k
–2	±5 and ±15	499	1 k
–5	±5 and ±15	182	909
–10	±5 and ±15	86.6	866

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.2 Typical Application

The fundamental concept of load sharing is to drive a load using two or more of the same operational amplifiers. Each amplifier is driven by the same source. 图 9-1 illustrates the schematic for this design. This concept effectively reduces the current load of each amplifier by 1/N, where N is the number of amplifiers. For further details on the design and performance of this circuit, see the *Reference Design for Implementation of the Load Sharing Concept for Large-Signal Applications*.

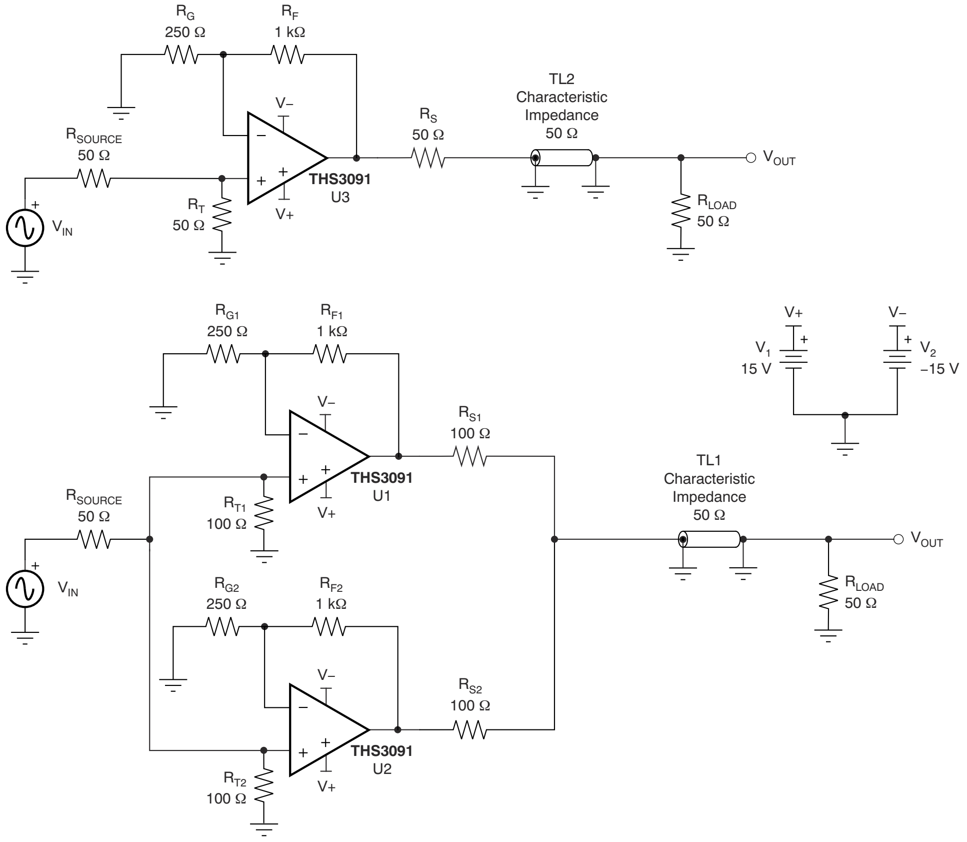


图 9-1. Reference THS3091 and THS3091 Load Sharing Test Configurations

9.2.1 Design Requirements

Use two THS3091 amplifiers in a parallel load-sharing circuit to improve distortion performance.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
V_{OPP}	20 V
R_{LOAD}	100 Ω

9.2.2 Detailed Design Procedure

In addition to providing higher output current drive to the load, the load sharing configuration can also provide improved distortion performance. In many cases, an operational amplifier shows better distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor starts to dominate the current load. In a load sharing configuration of N amplifiers in parallel, the equivalent current load that each amplifier drives is 1/N times the total load current.

As shown in 图 9-1 for example, in a two-amplifier load sharing configuration with matching resistance driving a resistive load (RL), each series resistance is 2×RL and each amplifier drives 2×RL. A convenient indicator of whether an op amp will function well in a load sharing configuration is the characteristic performance graph of harmonic distortion versus load resistance. 图 7-9 and 图 7-10 show more information. Such graphs can be found in most of TI’s high-speed amplifier data sheets. These graphs can be used to obtain a general sense of whether or not an amplifier will show improved distortion performance in load sharing configurations.

图 9-1 shows two test circuits: one for a single THS3091 amplifier driving a double-terminated (50-Ω cable), and one with two THS3091 amplifiers in a load sharing configuration. In the load sharing configuration, the two 100-Ω series output resistors act in parallel to provide 50-Ω back-matching to the 50-Ω cable.

图 9-2 and 图 9-3 show the 32-MHz, 18-VPP sine wave output amplitudes for the single THS3091 configuration and the load sharing configuration, respectively, measured using an oscilloscope. An ideal sine wave is also included as a visual reference (the dashed red line). 图 9-2 shows visible distortion in the single THS3091 output. In the load sharing configuration of 图 9-3, however, no obvious degradation is visible.

图 9-4 and 图 9-5 show the 64-MHz sine wave outputs of the two configurations from 图 9-1. While the single THS3091 output is clearly distorted in 图 9-4, the output of the load sharing configuration in 图 9-5 shows only minor deviations from the ideal sine wave.

9.2.3 Application Curves

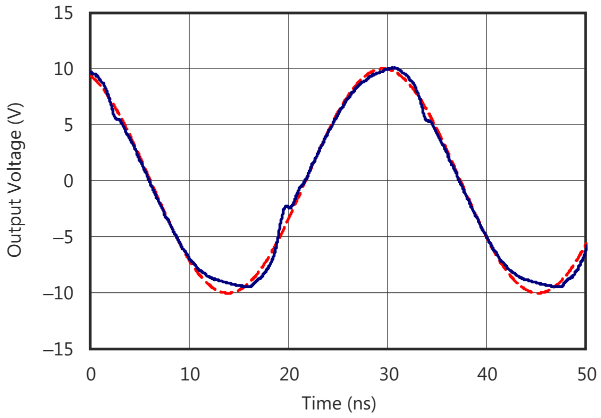


图 9-2. 32-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Single THS3091 Circuit Configuration

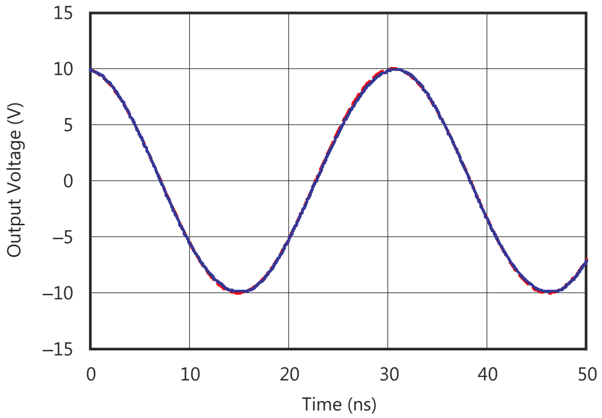


图 9-3. 32-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Two THS3091 Amplifiers in Load Sharing Configuration

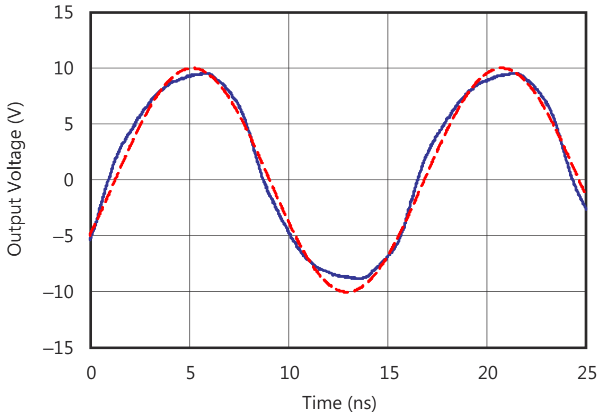


图 9-4. 64-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Single THS3091 Circuit Configuration

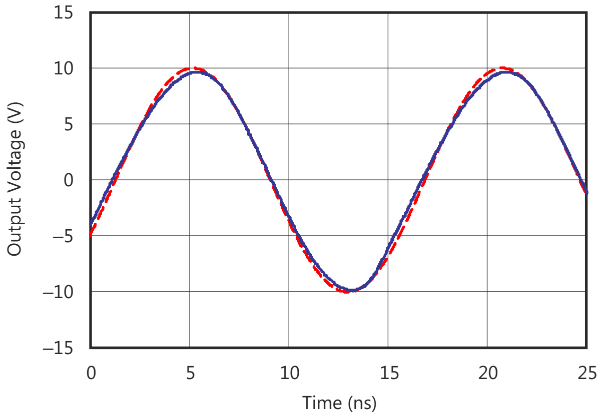


图 9-5. 64-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Two THS3091 Amplifiers in Load Sharing Configuration

9.3 Power Supply Recommendations

The THS3091 operates using a single or dual supply as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Operating from a single supply has numerous advantages. With the negative supply at ground, the dc errors due to the –PSRR term are minimized. Decouple the supplies with low-inductance, ceramic capacitors to ground less than 0.5 inches from the device pins. The use of a ground plane is recommended; as in most high-speed devices, remove the ground plane near device sensitive pins such as the inputs. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

9.4 Layout

9.4.1 Layout Guidelines

To optimize performance with a high-frequency amplifier, such as the THS309x, pay careful attention to board layout parasitic and external component types.

Recommendations to optimize performance include the following:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, keep ground and power planes unbroken elsewhere on the board.
- Minimize the distance [< 0.25 inch (6.35 mm)] from the power supply pins to the high-frequency 0.1- μ F and 100-pF decoupling capacitors. At the device pins, keep the ground and power plane layout away from the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. Use larger (6.8 μ F or more) tantalum decoupling capacitors, effective at lower frequency, on the main supply pins. The decoupling capacitors can be placed somewhat farther from the device, and can be shared among several devices in the same area of the printed circuit board (PCB).
- Connections to other wideband devices on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces [0.05 inch (1.3 mm) to 0.1 inch (2.54 mm)], preferably with ground and power planes opened up around the traces. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low-parasitic capacitive loads (< 4 pF) may not need an R_{ISO} because the THS309x are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_{ISO} are allowed as the signal gain increases (increasing the unloaded phase margin).

9.4.1.1 PowerPAD Design Considerations

The THS309x are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted [see 图 9-6(a) and 图 9-6(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see 图 9-6(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS309x have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the awkward mechanical methods of heatsinking.

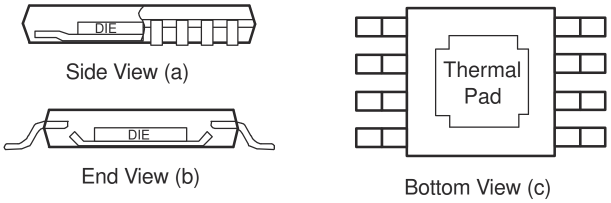


图 9-6. Views of Thermal Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following section lists the recommended steps.

9.4.1.1.1 PowerPAD Layout Considerations

1. 图 9-7 shows a PCB with a top-side etch pattern. Place an etch for the leads as well as etch for the thermal pad.
2. Place 13 holes in the area of the thermal pad. The recommended holes size is 0.01 inch (0.254 mm) in diameter. Keep the holes small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These additional vias help dissipate the heat generated by the THS309x device. The additional vias can be larger than the 0.01-inch (0.254 mm) diameter vias directly under the thermal pad. The additional vias can be larger because these vias are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. The PowerPAD is electrically isolated from the silicon and all leads. Therefore, connecting the PowerPAD to any potential voltage, such as V_{S-}, is acceptable because there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance that is useful for slowing the heat transfer during soldering operations. This high thermal resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, connect the holes under the THS309x PowerPAD package connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. On the top-side solder mask, leave the terminals of the package and the thermal pad area with the 13 holes exposed. On the bottom-side solder mask, cover the 13 holes of the thermal pad area. This guideline prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the device pins.
8. With these preparatory steps in place, the device is simply placed in position and run through the solder reflow operation as with any standard surface-mount component. This process results in a device that is properly installed.

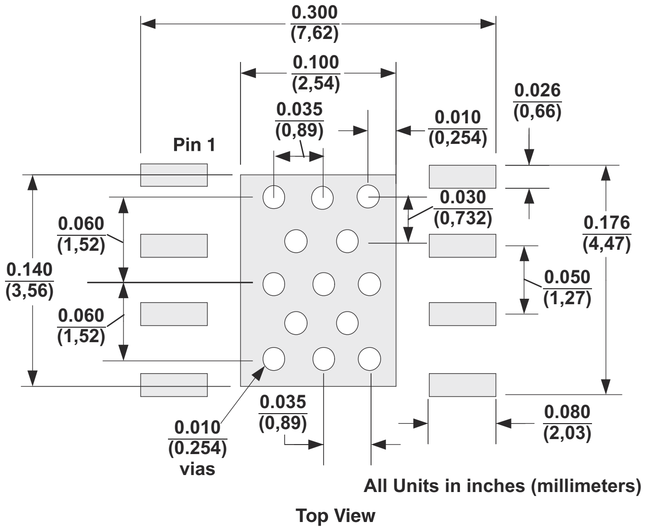


图 9-7. DDA PowerPAD PCB Etch and Via Pattern

9.4.1.2 Power Dissipation and Thermal Considerations

The THS309x incorporates automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature reduces to approximately 140°C, the amplifier turns on again. But, for maximum performance and reliability, the designer must ensure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package is calculated using the following equation:

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \tag{6}$$

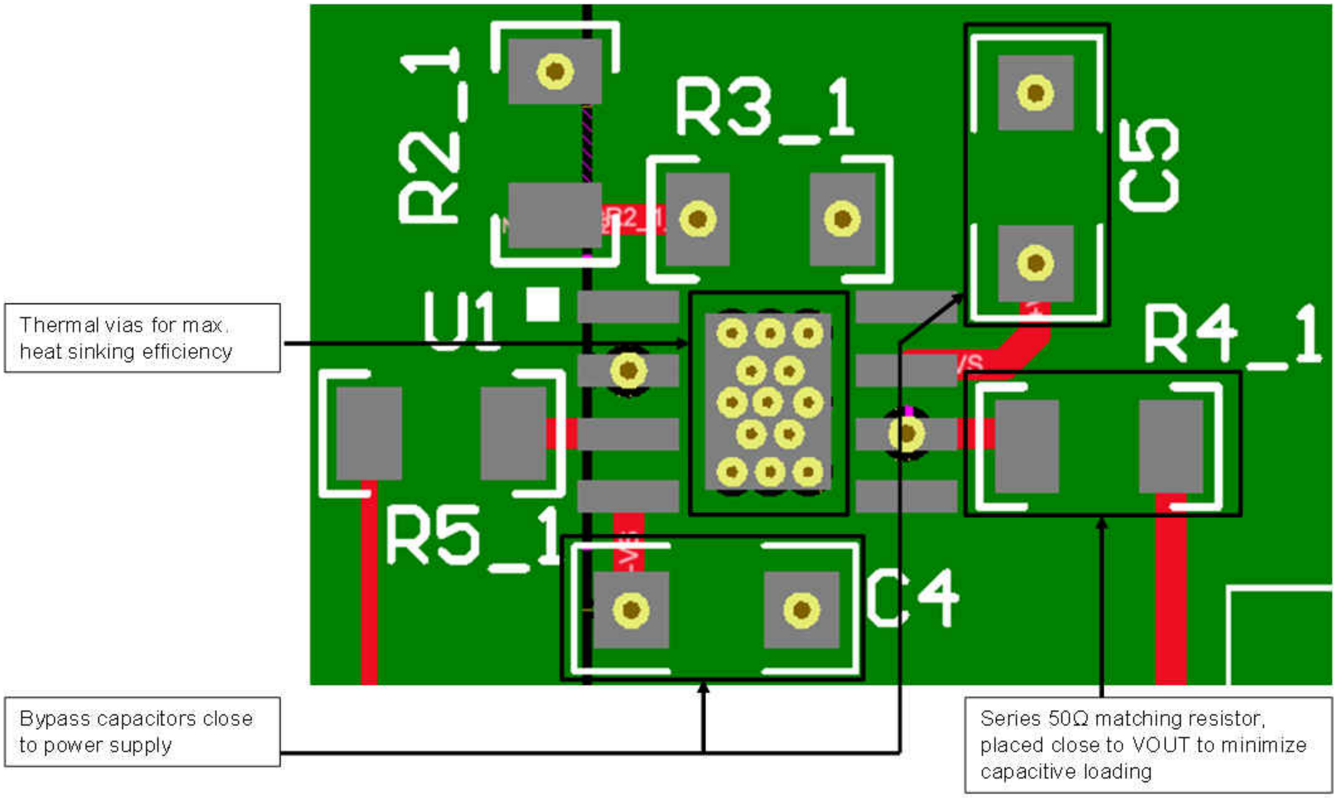
Where:

- P_{Dmax} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the THS3091 and THS3095 are offered in an 8-pin SOIC (DDA) with PowerPAD package. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the *PowerPAD™ Thermally Enhanced Package* application note. If the PowerPAD is not soldered to the PCB, then the thermal impedance increases substantially, which can cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB to optimize performance.

When determining whether or not the device satisfies the maximum power-dissipation requirement, consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, ynamic power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

9.4.2 Layout Example



Thermal vias for max. heat sinking efficiency

Bypass capacitors close to power supply

Series 50Ω matching resistor, placed close to VOUT to minimize capacitive loading

图 9-8. Layout Recommendation

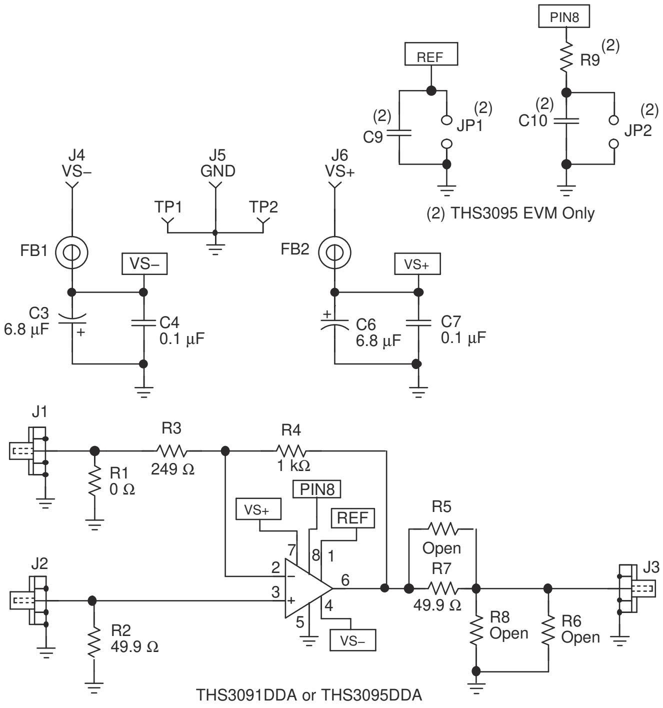


图 9-9. THS3091 EVM Circuit Configuration

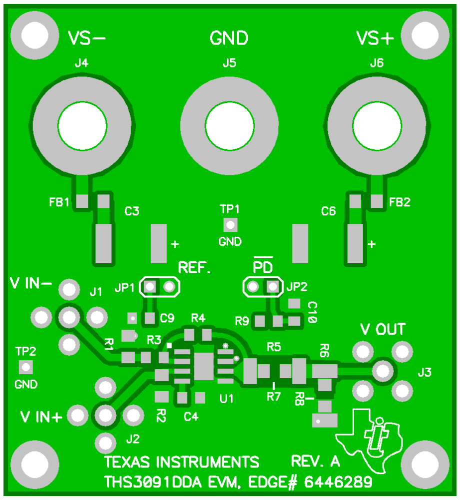


图 9-10. THS3091 EVM Board Layout (Top Layer)

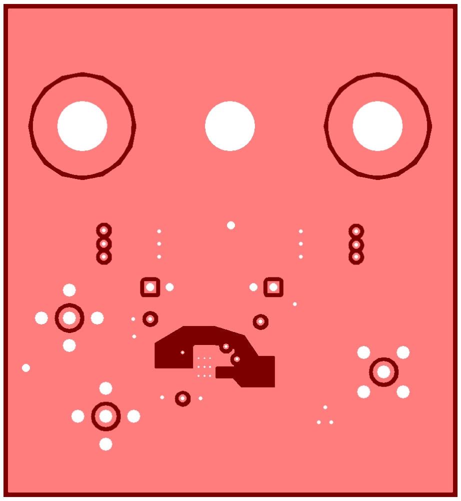


图 9-11. THS3091 EVM Board Layout (Second and Third Layers)

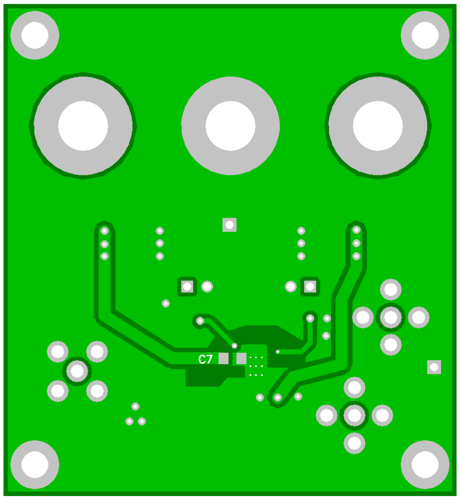


图 9-12. THS3091 EVM Board Layout (Bottom Layer)

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- TIDA-00684: High-Bandwidth Arbitrary Waveform Generator Reference Design: DC or AC coupled, High-Voltage output
- TIDA-00075: Wide-Bandwidth and High-Voltage Arbitrary Waveform Generator Front End
- TIDA-00023: Reference Design for Implementation of the Load Sharing Concept for Large-Signal Applications

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD™ Made Easy* application brief
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* technical brief
- Texas Instruments, *Voltage Feedback vs Current Feedback Amplifiers* application note
- Texas Instruments, *Current Feedback Analysis and Compensation* application note
- Texas Instruments, *Current Feedback Amplifiers: Review, Stability, and Application* application note
- Texas Instruments, *Effect of Parasitic Capacitance in Op Amp Circuits* application note
- Texas Instruments, *Expanding the Usability of Current-Feedback Amplifiers* analog journal

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3091D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091
THS3091D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091
THS3091DDA	Obsolete	Production	SO PowerPAD (DDA) | 8	-	-	Call TI	Call TI	-40 to 85	3091
THS3091DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3091DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3091DDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3091DDARG4.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3091DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091
THS3091DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091
THS3091IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3091IDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3091
THS3095D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3095
THS3095D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3095
THS3095DDA	Obsolete	Production	SO PowerPAD (DDA) | 8	-	-	Call TI	Call TI	-40 to 85	3095
THS3095DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3095
THS3095DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3095

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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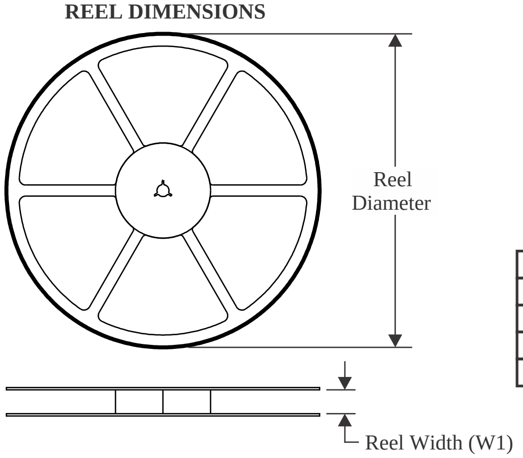
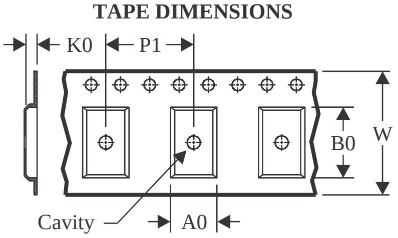
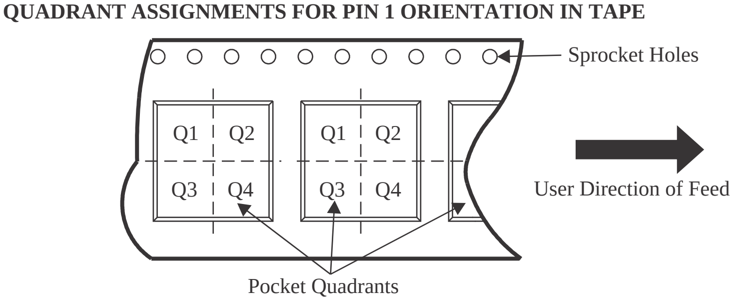
TAPE AND REEL INFORMATION





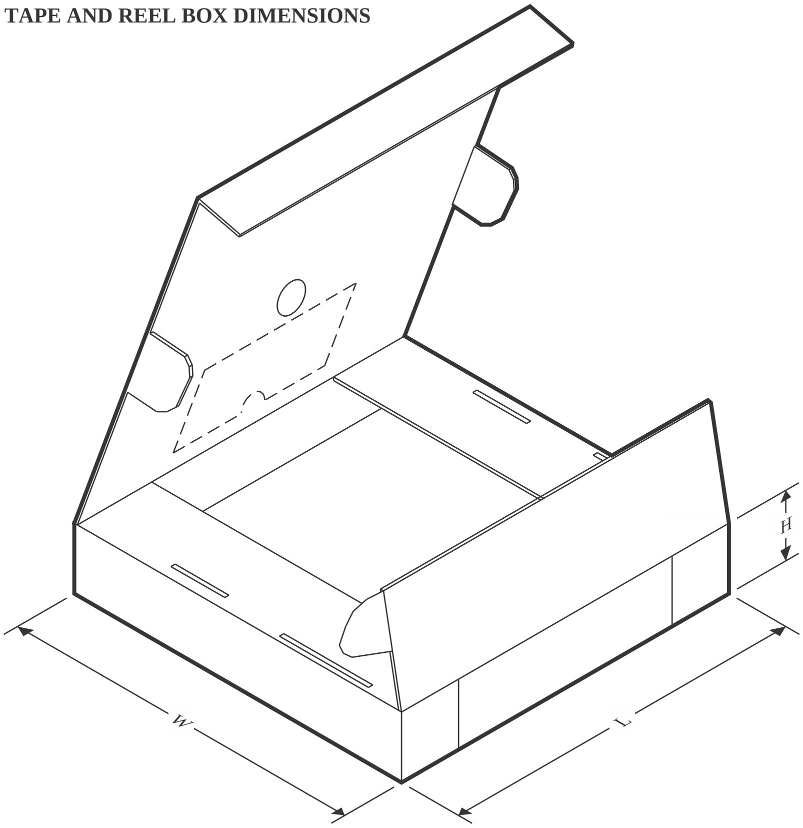
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3091DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3091IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

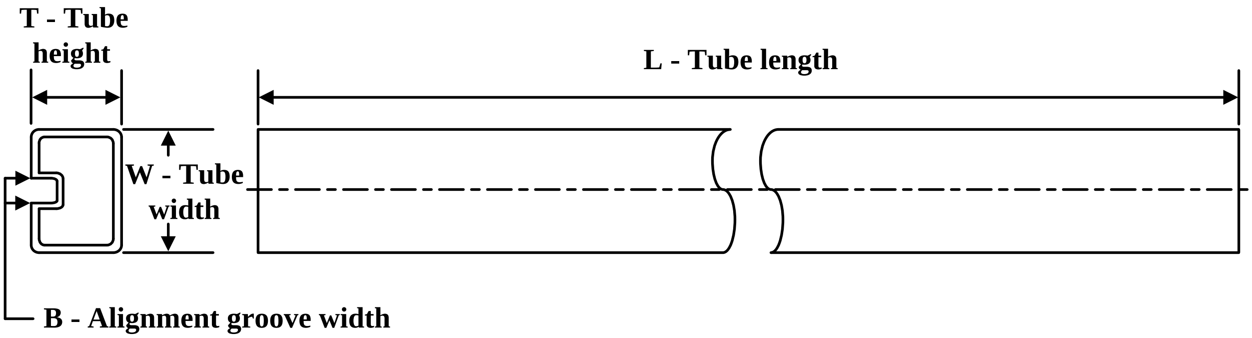
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3091DR	SOIC	D	8	2500	350.0	350.0	43.0
THS3091IDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0

TUBE

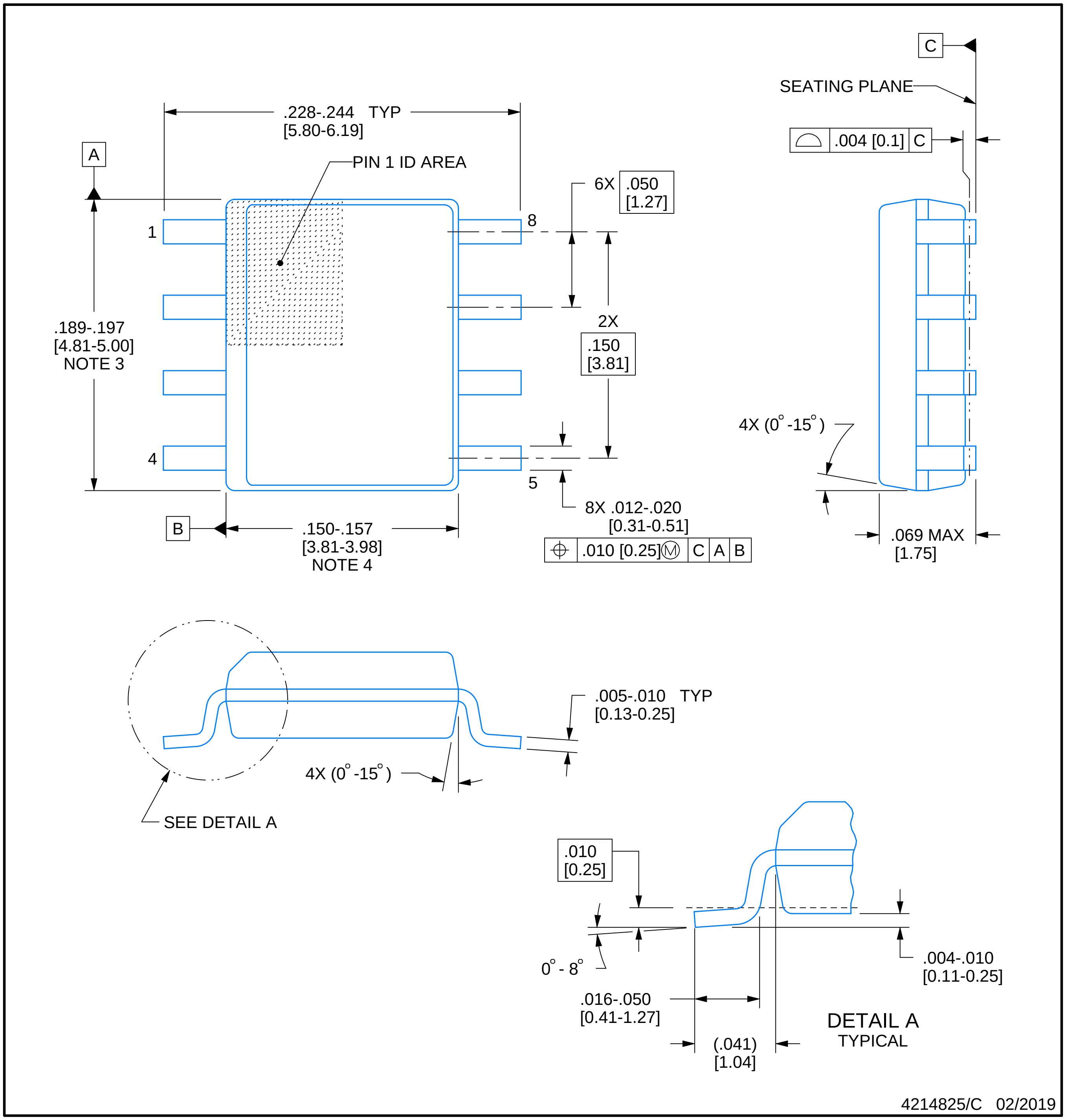


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS3091D	D	SOIC	8	75	505.46	6.76	3810	4
THS3091D.A	D	SOIC	8	75	505.46	6.76	3810	4
THS3095D	D	SOIC	8	75	505.46	6.76	3810	4
THS3095D.A	D	SOIC	8	75	505.46	6.76	3810	4

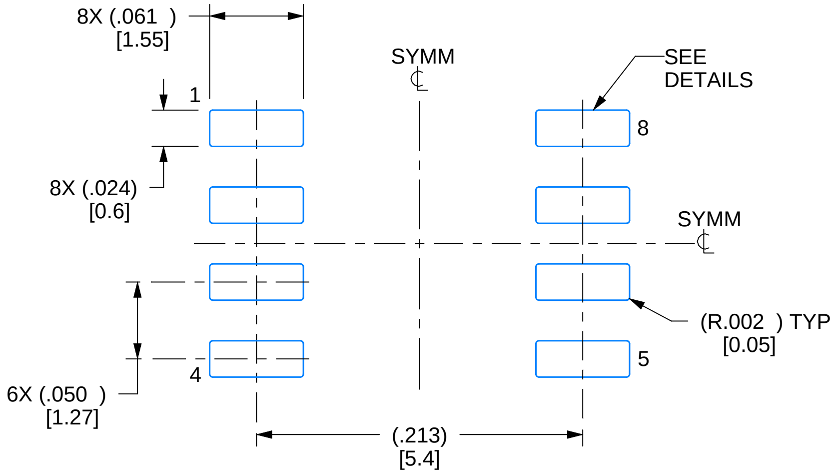
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

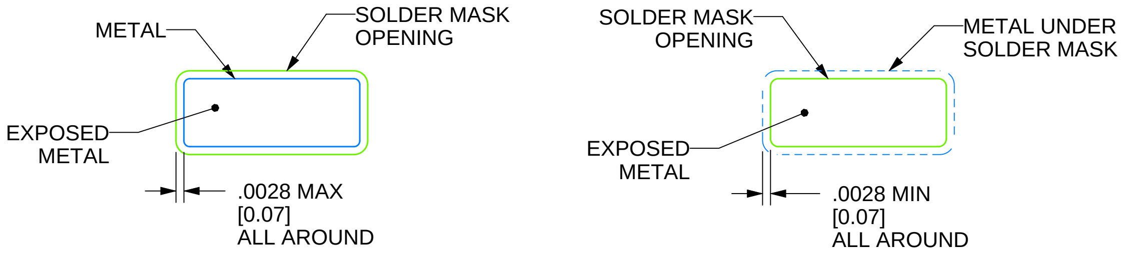


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



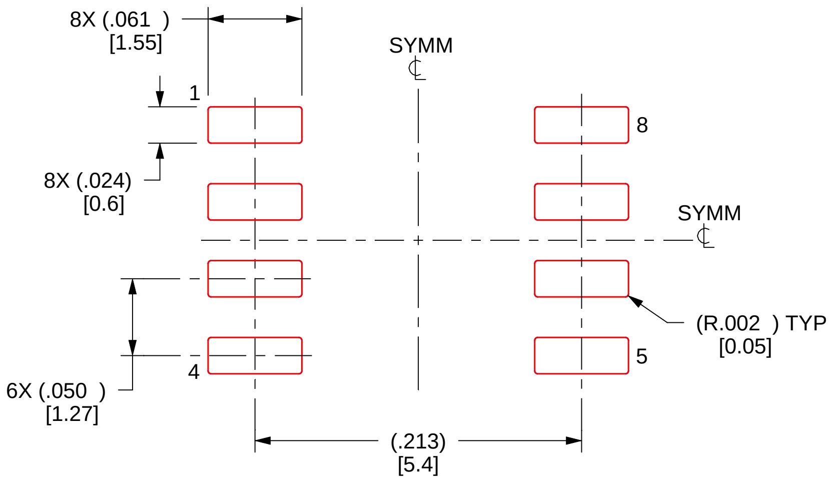
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

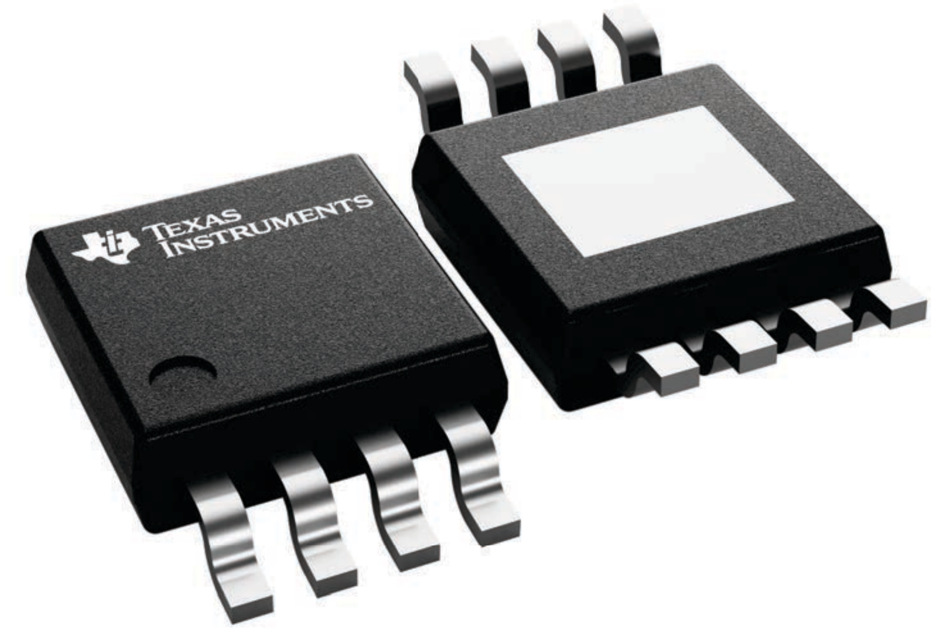
DGN 8

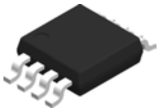
PowerPAD™ HVSSOP - 1.1 mm max height

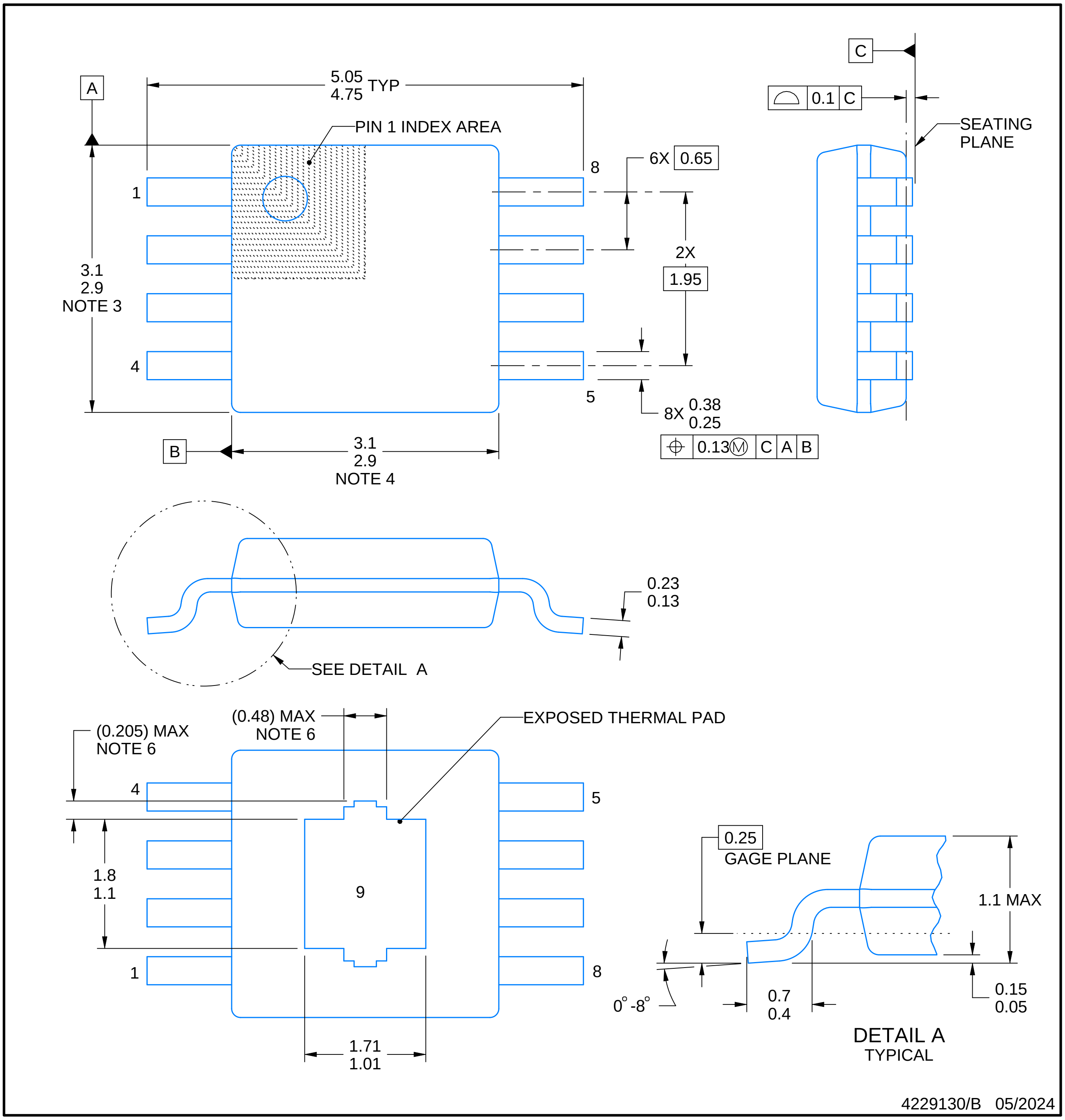
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

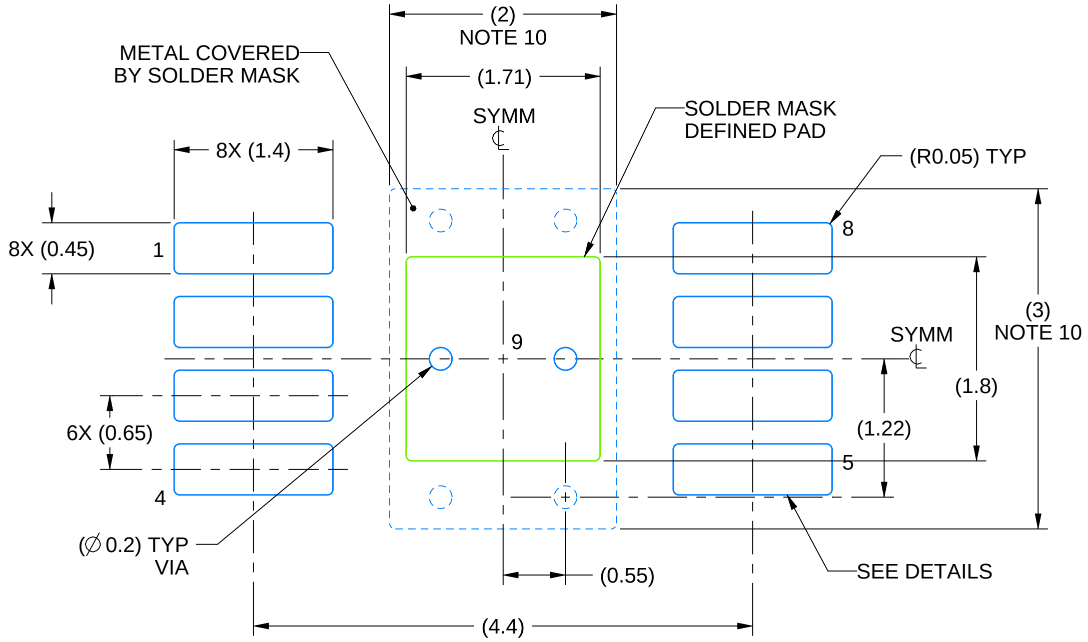






NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

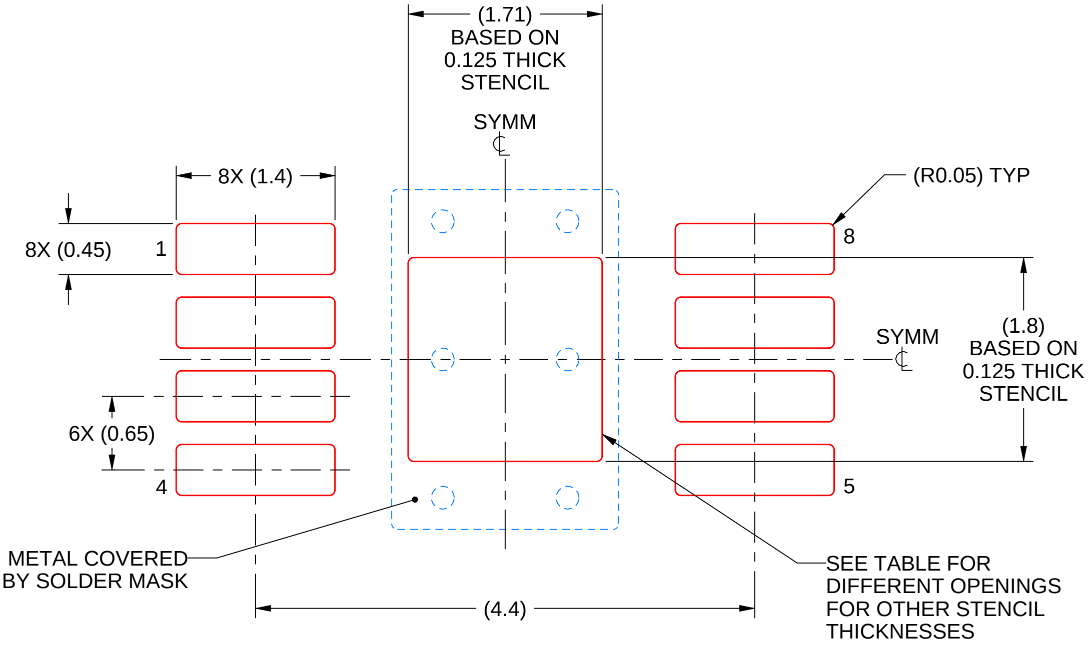
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

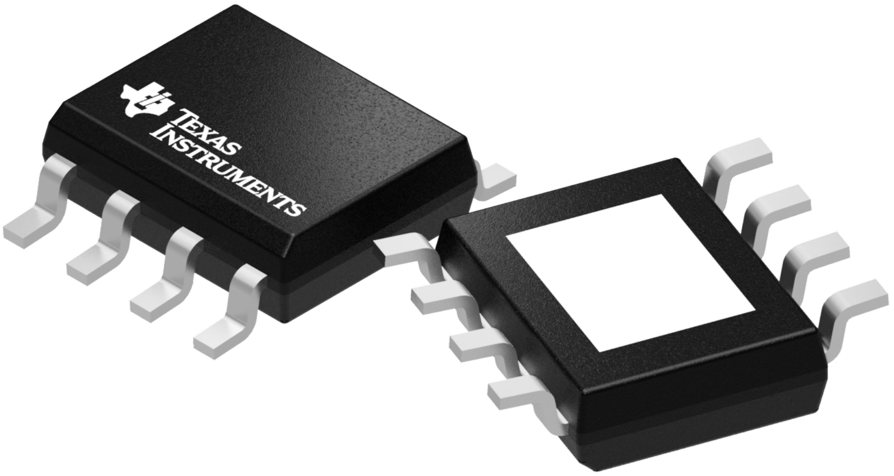
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA 8

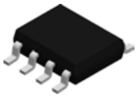
PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

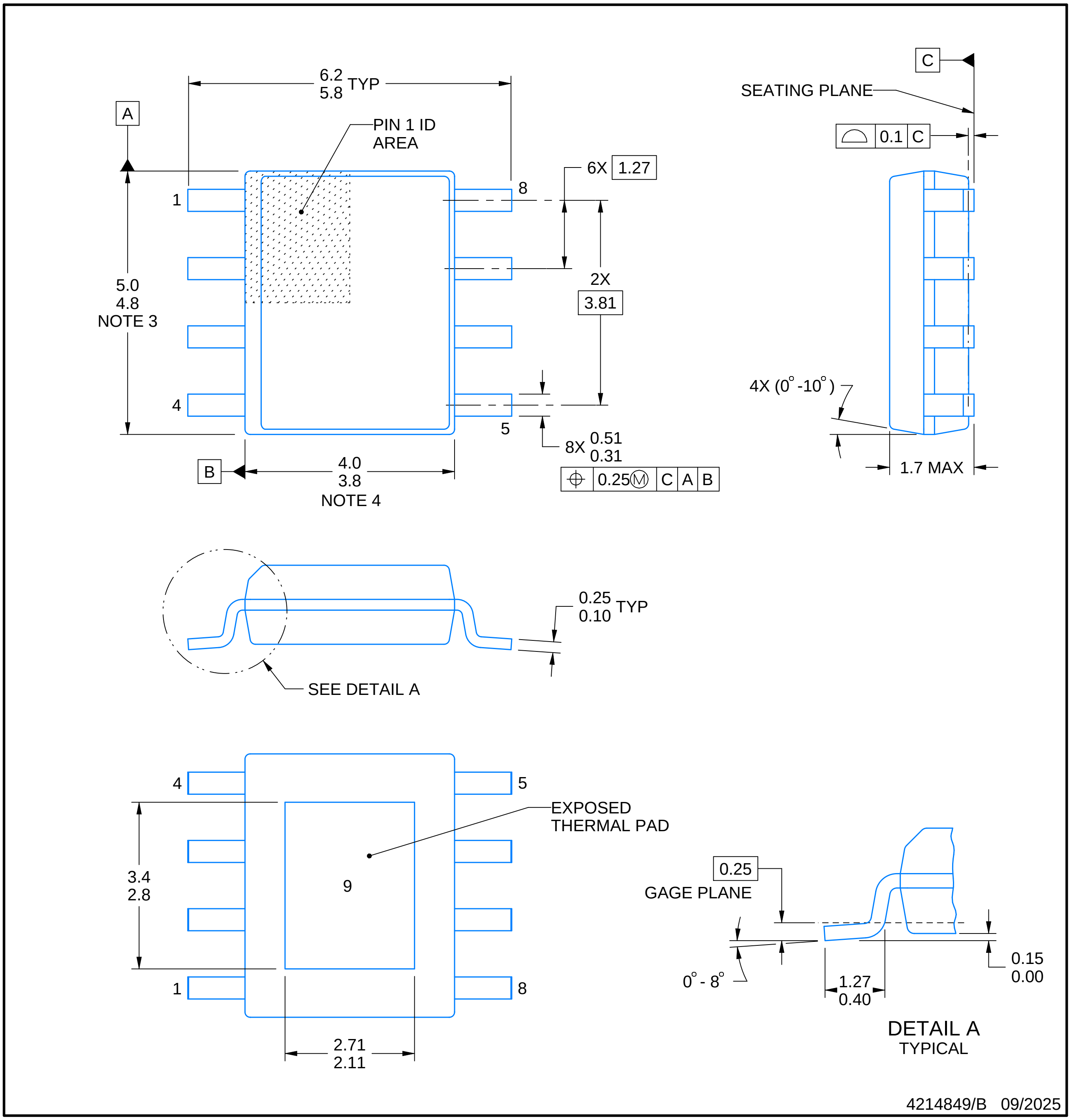
DDA0008B



PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

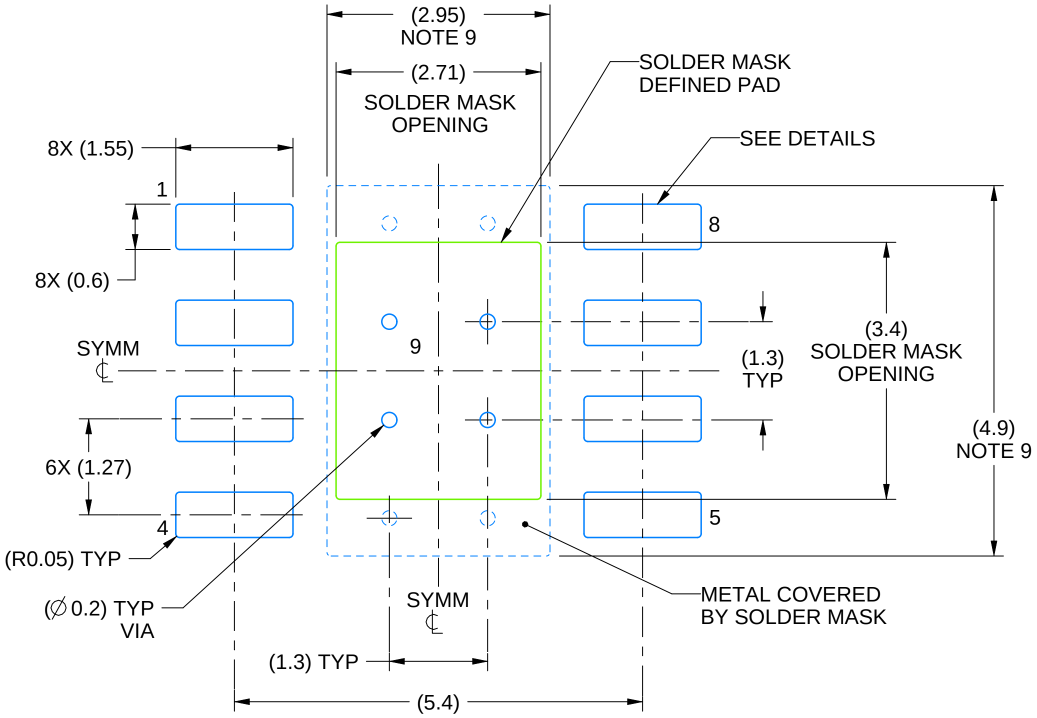
PLASTIC SMALL OUTLINE



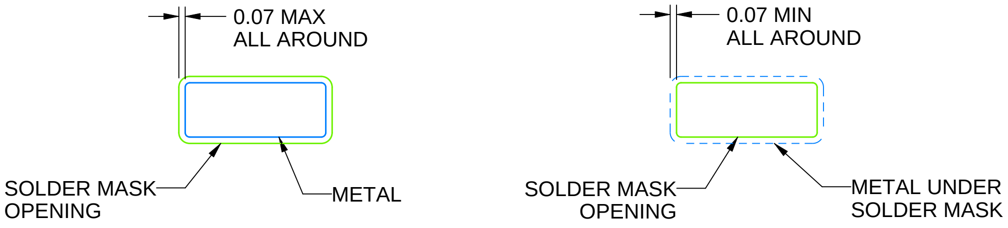
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



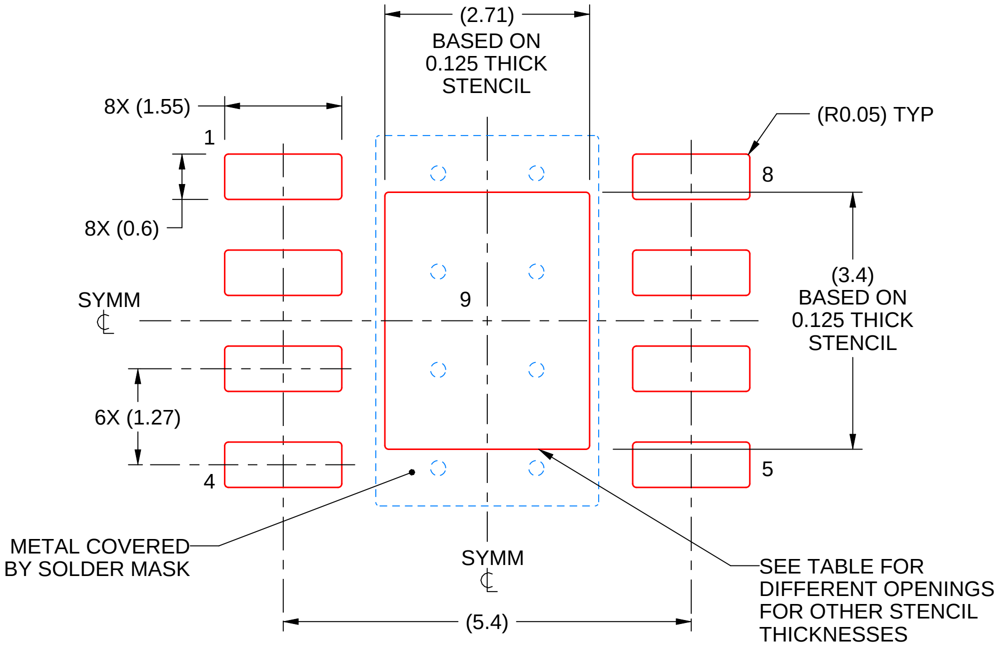
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
PADS 1-8

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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