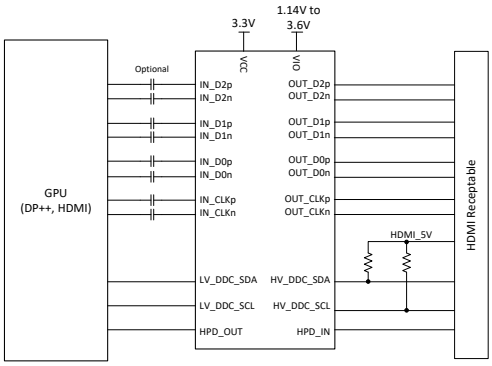
TDP1204 12Gbps、直流/交流耦合转 HDMI™ 2.1 电平转换器混合转接驱动器

1 特性

- 支持高达 12Gbps HDMI 2.1 数据速率的交流耦合或直流耦合输入和输出
  - 向后兼容 HDMI 1.4b 和 HDMI 2.0b
  - HDMI 2.1 固定速率链路 (FRL) 为 3、6、8、10 和 12Gbps
  - 支持 HDMI 2.1 三通道和四通道 FRL
- 已针对 HDMI 源应用进行优化
- 6GHz 时高达 12dB 的可编程接收器均衡器
- I^2C 或引脚搭接可编程
- 集成的 HPD 电平转换器同时支持 1.8V 和 3.3V LVCMOS 电平
- 集成的 DDC 缓冲器支持最低 1.2V 电平
- 主通道上全通道交换
- 用于链路配置的数字显示控制 (DDC) 监控功能
- 低功耗：
  - 12G FRL 四通道有源限制：575mW
  - 12G FRL 四通道有源线性：220mW
  - 断电：0.6mW
- 可用于商业级和工业级温度范围
- 3.3V 单电源
- 40 引脚 0.4mm 间距 4mm × 6mm WQFN 封装

2 应用

- 笔记本电脑和台式机
- 电视
- 家庭影院和娱乐系统
- 游戏系统
- 扩展坞
- 专业音频、视频和标牌



简化版原理图

3 说明

TDP1204 是一款 HDMI 2.1 转接驱动器，支持高达 12Gbps 的数据速率，向后兼容 HDMI 1.4b 和 HDMI 2.0b。高速差分输入和输出可以是交流耦合或直流耦合，支持将 TDP1204 用作 DP++ 转 HDMI 电平转换器或 HDMI 转接驱动器。TDP1204 可支持 3、6、8、10 和 12Gbps 的三通道和四通道 HDMI 2.1 FRL。

TDP1204 是一款混合转接驱动器，同时支持源端和接收端应用。混合转接驱动器可用作线性转接驱动器，也可用作限幅转接驱动器。配置为限幅转接驱动器时，TDP1204 的差分输出电压电平独立于图形处理单元 (GPU) 的输出电平，从而确保插座的 HDMI 电平符合要求。限幅转接驱动器模式推荐用于 HDMI 源端应用。配置为线性转接驱动器时，TDP1204 的差分输出电平是 GPU 输出电平的线性函数，从而支持将 TDP1204 用于透明呈现链路训练或用作通道缩短器。建议将线性转接驱动器模式用于 HDMI 接收端应用。

TDP1204 有一个集成的 HPD 电平转换器，该转换器可将 5V HPD 信号转换为 1.8V 或 3.3V。电平转换器输出还可配置为推挽式或开漏式。另外，TDP1204 还集成了一个数字显示控制 (DDC) 缓冲器。DDC 缓冲器可提供电容隔离，电平转换器可将 5V DDC 电平转换为 3.3V、1.8V 或 1.2V 电平。集成电平转换器后，无需分立式解决方案，因此节省了系统成本。

TDP1204 支持 3.3V V_{CC} 单电源轨，可用于商业级温度范围 (TDP1204) 和工业级温度范围 (TDP1204I)。

器件信息

器件型号(1)	温度	封装
TDP1204	Ta = 0°C 至 70°C	RNQ（WQFN，40）
TDP1204I	Ta = -40°C 至 85°C	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2022) to Revision A (July 2023)	Page
• 更新了 *器件信息* 表以包含环境温度	1
• Corrected swap of R and F in EQ1 pin column in *Receiver EQ Settings When GLOBAL_DCG = 0x2* table	27
• Added *DisplayPort* section	38

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5 Pin Configuration and Functions

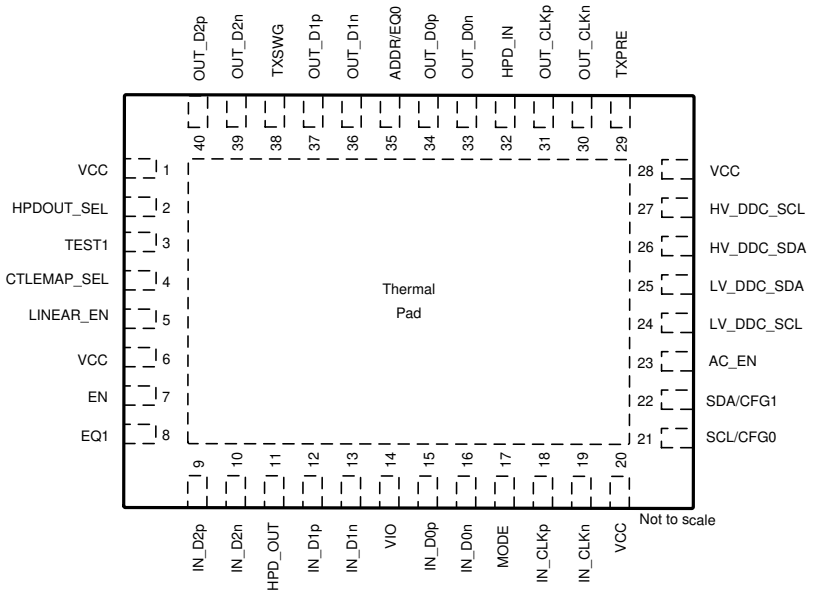


图 5-1. RNQ Package 40-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VCC	1	P	3.3-V power supply
HPDOUT_SEL	2	I 2-level (PD)	HPDOUT_SEL. Selects whether HPD_OUT pin is push, pull, or open-drain. Open-drain is not supported in pin-strap mode. Therefore this pin should be left floating or pull-down to GND.
TEST1	3	O	Test1. For TI internal use only. This pin can be left unconnected.
CTLEMAP_SEL	4	I 4-level (PU/PD)	CTLE Map select. When TDP1204 is configured in pin-strap mode, this pin selects the CTLE Map used. 表 8-8 lists more details. Also in pin-strap this pin will control whether or not AEQ is enabled. 表 8-9 lists more details. In I^2C mode, CTLE map and AEQ enable is determined by registers.
LINEAR_EN	5	I 4-level (PU/PD)	In pin-strap mode, selects whether TDP1204 operates in linear or limited redriver mode. 表 8-5 lists more details.
VCC	6	P	3.3-V power supply
EN	7	I 2-level (PU)	When low, TDP1204 will be held in reset. The IN_D[2:0], IN_CLK, OUT_D[2:0] and OUT_CLK pins will be held in high impedance while EN is low. On rising edge of EN, the device will sample four-level inputs and function based on the sampled state of the pins. This pin has an internal 250-k pull-up to VIO.
EQ1	8	I 4-level (PU/PD)	EQ1 pin setting when TDP1204 is configured for pin strap mode; works in conjunction with EQ0; 表 8-6 lists the settings. In I^2C mode, EQ settings are controlled through the registers.
IN_D2p	9	I	Channel 2 differential positive input
IN_D2n	10	I	Channel 2 differential negative input
HPD_OUT	11	O	Hot plug detect output to source side. If not used, then this pin can be left floating. If used, then it is recommended to have an external 220k resistor to GND on this pin.
IN_D1p	12	I	Channel 1 differential positive input.
IN_D1n	13	I	Channel 1 differential negative input.

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表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIO	14	P	Voltage supply for I/Os. 表 8-2 lists more details.
IN_D0p	15	I	Channel 0 differential positive input
IN_D0n	16	I	Channel 0 differential negative input
MODE	17	I 4-level (PU/PD)	Mode control pin. Selects between pin-strap and I2C mode. For more details, refer to 节 8.3.1.
IN_CLKp	18	I	Clock differential positive input
IN_CLKn	19	I	Clock differential negative input
VCC	20	P	3.3-V power supply
SCL/CFG0	21	I	I^2C Clock/CFG0: when TDP1204 is configured for I^2C mode, this pin will function as the I^2C clock. 表 8-18 lists how this pin otherwise functions as CFG0.
SDA/CFG1	22	I/O	I^2C Data / CFG1: when TDP1204 is configured for I^2C mode, this pin will function as the I^2C clock. 表 8-19 lists how this pin will otherwise function as CFG1.
AC_EN	23	I 2-level (PD)	In pin-strap mode, the AC_EN pin selects whether high speed transmitters are externally AC or DC-coupled. 0: DC-coupled 1: AC-coupled
LV_DDC_SCL	24	I/O	Low voltage side bidirectional DDC clock line. Internally pulled-up to VIO.
LV_DDC_SDA	25	I/O	Low voltage side bidirectional DDC data line. Internally pulled-up to VIO.
HV_DDC_SDA	26	I/O	High voltage side bidirectional DDC data line. Pull-up externally to HDMI 5-V.
HV_DDC_SCL	27	I/O	High voltage side bidirectional DDC clock line. Pull-up externally to HDMI 5-V.
VCC	28	P	3.3-V power supply
TXPRE	29	I 4-level (PU/PD)	TX pre-emphasis control: in pin-strap mode with limited enabled, this pin controls TX EQ. In pin-strap with linear and AEQ enabled, this pin will adjust the adapted value. 表 8-15 lists the available settings for the TXPRE when operating in pin strap mode. In I^2C mode, Tx pre-emphasis is controlled through the registers.
OUT_CLKn	30	O	TMDS data clock differential negative output
OUT_CLKp	31	O	TMDS data clock differential positive output
HPD_IN	32	I 2-level (PD)	Hot plug detect input from sink side. This pin has an internal pull-down resistor and is fail-safe.
OUT_D0n	33	O	TMDS data 0 differential negative output
OUT_D0p	34	O	TMDS data 0 differential positive output
ADDR/EQ0	35	I 4-level (PU/PD)	Address bit for I2C programming when TDP1204 is configured for I^2C mode. 表 8-22 lists more details. EQ0 pin setting when TDP1204 is configured for pin strap mode; works in conjunction with EQ1; 表 8-6 lists the EQ pin settings. In I^2C mode, EQ settings are controlled through the registers.
OUT_D1n	36	O	TMDS data 1 differential negative output
OUT_D1p	37	O	TMDS data 1 differential positive output
TXSWG	38	I 4-level (PU/PD)	TX output swing control: 4 settings. This pin is only used in pin strap mode. 表 8-17 lists the available TX swing settings. In I^2C mode, Tx output swing is controlled through the registers.
OUT_D2n	39	O	TMDS data 2 differential negative output
OUT_D2p	40	O	TMDS data 2 differential positive output
Thermal Pad		—	Thermal pad. Connect to a solid ground plane.

(1) I = input, O = output, G = ground, and P = power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	V_{CC} and V_{IO}	-0.5	4	V
Input Voltage	Differential Inputs (IN_D[2:0], IN_CLK)	-0.3	4	V
Output voltage	HPD_OUT output	– 0.3	4	V
Output voltage	Differential outputs (OUT_D[2:0], OUT_CLK)	– 0.3	4	V
Control pins	LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, SDA/CFG1, MODE, CLTEMAP_SEL, HPDOUT_SEL, TXSWG, TXPRE, EQ1, ADDR/EQ0, EN, AC_EN, LINEAR_EN	– 0.5	4	V
	HPD_IN, HV_DDC_SCL, HV_DDC_SDA	– 0.5	6	V
T_J	TDP1204 Junction temperature		105	°C
T_J	TDP1204I Junction temperature		125	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the *Recommended Operating Condition*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage when high-speed RX pins (IN_D[2:0] and IN_CLK) is AC-coupled to a DP++ TX	3.0	3.3	3.6	V
V_{CC}	Supply voltage when high-speed RX pins (IN_D[2:0] and IN_CLK) is DC-coupled to a HDMI TX	3.135	3.3	3.465	V
V_{IO}	VIO supply when 1.2-V LVCMOS level used.	1.14	1.2	1.26	V
V_{IO}	VIO supply when 1.8-V LVCMOS level used.	1.7	1.8	1.9	V
V_{IO}	VIO supply when 3.3-V LVCMOS level used.	3	3.3	3.6	V
V_{PSN}	Peak to peak Power supply noise on V_{CC} pins (less than 4 MHz).			100	mV
V_{CTL3}	DC input voltage for SCL/CFG0, SDA/CFG1, MODE, AC_EN, LINEAR_EN, EN, CTLEMAP_SEL, TXSWG, TXPRE, EQ1, ADDR1/EQ0, LV_DDC_SCL, LV_DDC_SDA, HPDOUT_SEL	– 0.3		3.6	V
V_{CTL5}	DC input voltage for HV_DDC_SCL, HV_DDC_SDA, HPD_IN pins	– 0.3		5.5	V
C_{ACRX}	Optional external AC-coupling capacitor on IN_Dx and IN_CLK.	85		253	nF
C_{ACTX}	External AC-coupling capacitor on OUT_Dx and OUT_CLK when AC_EN = H.	85		253	nF
T_A	TDP1204 Ambient temperature	0		70	°C

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6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	TDP1204I Ambient temperature	– 40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TDP1204 RNQ (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
$P_{ACTIVE-H14-LT-ARX-DTX}$	Power dissipation in HDMI 1.4 3.4 Gbps active operation	Pin Strap mode; DR = 3.4 Gbps; HPD_IN = H; No de-emphasis/pre-emphasis; Limited redriver mode; DC-coupled TX; AC-coupled RX; 3 Gbps CTLE;		190	265	mW
$P_{ACTIVE-H20-LT-ARX-DTX}$	Power dissipation in HDMI 2.0 6 Gbps active operation	Pin Strap mode; DR = 6 Gbps; HPD_IN = H; No de-emphasis/pre-emphasis; Limited redriver mode; DC-coupled TX; AC-coupled RX; 6 Gbps CTLE;		215	305	mW
$P_{ACTIVE-FRL-LT-ARX-ATX}$	Power dissipation in FRL 12 Gbps active operation when TX is AC-coupled (AC_EN = H)	Pin Strap mode; DR = 12 Gbps; HPD_IN = H; TXFFE0; Limited redriver mode; AC-coupled TX; AC-coupled RX;12 Gbps CTLE;		840	1220	mW
$P_{ACTIVE-FRL-LT-ARX-DTX}$	Power dissipation in FRL 12 Gbps active operation when TX is DC-coupled (AC_EN = L)	Pin Strap mode; DR = 12 Gbps; HPD_IN = H; TXFFE0; Limited redriver mode; DC-coupled TX; AC-coupled RX; 12 Gbps CTLE;		575	785	mW
$P_{ACTIVE-FRL-LR-ARX-DTX}$	Power dissipation in FRL 12 Gbps active operation when TX is DC-coupled (AC_EN = L)	Pin Strap mode; DR = 12 Gbps; HPD_IN = H; Highest linearity setting; Linear redriver mode; DC-coupled TX; AC-coupled RX; 12 Gbps CTLE;		220	310	mW
$P_{ACTIVE-FRL-LR-ARX-ATX}$	Power dissipation in FRL 12 Gbps active operation when TX is AC-coupled (AC_EN = H)	Pin Strap mode; DR = 12 Gbps; HPD_IN = H; Highest linearity setting; Linear redriver mode; AC-coupled TX; AC-coupled RX; 12 Gbps CTLE		660	990	mW
P_{PD}	Power in power-down (HPD_IN = L)	Pin Strap mode; HPD_IN = L; EN = L or H; High-speed outputs are disconnected;		0.6	2	mW
P_{SD}	Power in standby (HPD_IN = H) but no incoming signal with DDC Buffer disabled	Pin Strap mode; HPD_IN = H; No incoming signal; EN = H; DC-coupled TX; AC-coupled RX; Limited redriver mode; High-speed outputs are connected;		1.0	1.85	mW

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{SD}	Power in standby (HPD_IN = H) but no incoming signal with DDC buffer enabled.	Pin Strap mode; HPD_IN = H; No incoming signal; EN = H; DC-coupled TX; AC-coupled RX; Limited redriver mode; High-speed outputs are connected;		1.2	2.05	mW
I_{VIOQ}	VIO quiescent current	HPD_IN = H;VCC = VIO = 3.6 V; LV_DDC_SDA/SCL = H; HV_DDC_SDA/SCL = H;			16	µA
I_{VIOA}	VIO active instantaneous current	VCC = VIO = 3.6 V; HPD_IN = H;			1	mA
2-LEVEL CONTROL PINS (EN, SCL/CFG0, SDA/CFG1, AC_EN, HPDOUT_SEL)						
V_{IO_TRSHD}	Threshold for selecting between 1.2-V LVCMOS / 1.8-V LVCMOS			1.5		V
V_{IO_TRSHD}	Threshold for selecting between 1.8-V LVCMOS / 3.3-V LVCMOS			2.5		V
V_{IL_1p2V}	Low-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 1.26 V; VCC = 3.0 V;	-0.3		0.378	V
V_{IH_1p2V}	High-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 1.14 V; VCC = 3.6 V;	0.8		3.6	V
V_{IL_1p8V}	Low-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 1.9 V; VCC = 3.0 V;	-0.3		0.57	V
V_{IH_1p8V}	High-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 1.7 V; VCC = 3.6 V;	1.19		3.6	V
V_{IL_3p3V}	Low-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 3.6 V; VCC = 3.0 V;	-0.3		0.8	V
V_{IL_3p3V}	Low-level input voltage for AC_EN, HPDOUT_SEL	VIO = 3.6 V; VCC = 3.0 V;	-0.3		0.8	V
V_{IH_3p3V}	High-level input voltage for SCL/CFG0, SDA/CFG1	VIO = 3.0 V; VCC = 3.6 V;	2.2		3.6	V
V_{IH_3p3V}	High-level input voltage for AC_EN, HPDOUT_SEL	VIO = 3.0 V; VCC = 3.6 V;	2.2		3.6	V
V_{OL_1p2V}	Low-level output voltage SDA/CFG1	V_{CC} = 3.0 V; VIO = 1.2 V;	-0.3		0.3	V
I_{OL_1p2V}	Low-level output current SDA/CFG1	V_{CC} = 3.0 V; VIO = 1.2 V;	2			mA
V_{OL}	Low-level output voltage SDA/CFG1	V_{CC} = 3.0 V; VIO = 1.8 V or 3.3 V;	-0.3		0.4	V
I_{OL}	Low-level output current SDA/CFG1	V_{CC} = 3.0 V; VIO = 1.8 V or 3.3 V;	4			mA
I_{IL_I2C}	Low-level input current SCL/CFG0, SDA/CFG1	V_{IN} = 0 V; VIO = 1.8 V or 3.3 V;	– 1		1	µA
I_{LEAK}	Fail-safe input current for SCL/CFG0, SDA/CFG1	V_{IN} = 3.6 V; VCC = 0 V;	– 25		25	µA
V_{IL_EN}	Low-level input voltage for EN pin.	VIO = 1.14 V; VCC = 3.3 V;	-0.3		0.4	V
V_{IH_EN}	High-level input voltage for EN pin.	VIO = 3.6 V; VCC = 3.3 V;	0.8		3.6	V
I_{IL}	Low-level input current EN	V_{IN} = 0 V; VIO = 1.8 V or 3.3 V; VCC = 3.6 V	– 20		20	µA
I_{IL}	Low-level input current AC_EN, HPDOUT_SEL	V_{IN} = 0 V; VIO = 1.8 V or 3.3 V;	– 1		1	µA
I_{IH_EN}	High-level input current for EN	V_{IN} = 3.6 V; VIO = 1.8 V or 3.3 V;	– 1		1	µA
I_{IH_ACEN}	High-level input current for AC_EN	V_{IN} = 3.6 V; VIO = 1.8 V or 3.3 V;	– 24		24	µA
$I_{IH_HPDOUTSEL}$	High-level input current for HPDOUT_SEL	V_{IN} = 3.6 V; VIO = 1.8 V or 3.3 V;	– 24		30	µA
R_{PU_EN}	Internal Pull-up resistance on EN.		125	250	350	kΩ
R_{PD_ACEN}	Internal Pull-down resistance on AC_EN		125	250	350	kΩ

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PD_HPD\ OUTSEL}$	Internal Pull-down resistance on HPDOUT_SEL		125	250	350	kΩ
$C_{I2C-PINS}$	Capacitance for SCL/CFG0 and SDA/CFG1	f = 100 kHz;			5	pF
$C_{(I2C_FM+_BUS)}$	I2C bus capacitance for FM+ (1 MHz)				150	pF
$C_{(I2C_FM_BUS)}$	I2C bus capacitance for FM (400 kHz)				150	pF
$R_{(EXT_I2C_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1 MHz)	$C_{(I2C_FM+_BUS)}$ = 150 pF	620	820	910	Ω
$R_{(EXT_I2C_FM)}$	External resistors on both SDA and SCL when operating at FM (400 kHz)	$C_{(I2C_FM_BUS)}$ = 150 pF	620	1500	2200	Ω
LV_DDC_SDA and LV_DDC_SCL (DDC Buffer Disabled)						
V_{IL_1p2V}	Low-level input voltage	VCC = 3.0 V;	-0.3		0.378	V
V_{IH_1p2V}	High-level input voltage	VCC = 3.6 V;	0.8		3.6	V
V_{IL_1p8V}	Low-level input voltage	VCC = 3.0 V;	-0.3		0.57	V
V_{IH_1p8V}	High-level input voltage	VCC = 3.6 V;	1.19		3.6	V
V_{IL_3p3V}	Low-level input voltage	VCC = 3.0 V;	-0.3		0.8	V
V_{IH_3p3V}	High-level input voltage	VCC = 3.6 V;	2.2		3.6	V
DDC Buffer (LV_DDC_SCL, LV_DDC_SDA, HV_DDC_SCL, HV_DDC_SDA)						
V_{HV_IH}	High-level input voltage for HV_DDC_SCL and HV_DDC_SDA	VIO = 3.3 V; VCC = 3.0 V	3.3		5.3	V
V_{HV_IL}	Low-level input voltage for HV_DDC_SCL and HV_DDC_SDA	VIO = 3.3 V; VCC = 3.0 V	-0.3		1.6	V
V_{LV_IH}	High-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 1.2-V LVCMOS	VIO = 1.14 V; VCC = 3.3 V	0.8		3.6	V
V_{LV_IH}	High-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 1.8-V LVCMOS	VIO = 1.7 V; VCC = 3.3 V	1.15		3.6	V
V_{LV_IH}	High-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 3.3-V LVCMOS	VIO = 3.0 V; VCC = 3.3 V	2.1		3.6	V
V_{LV_IL}	Low-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 1.2-V LVCMOS	VIO = 1.26 V; VCC = 3.3 V	-0.3		0.082 * VIO	V
V_{LV_IL}	Low-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 1.8-V LVCMOS	VIO = 1.9 V; VCC = 3.3 V	-0.3		0.10 * VIO	V
V_{LV_IL}	Low-level input voltage for LV_DDC_SCL and LV_DDC_SDA for 3.3-V LVCMOS	VIO = 3.6 V; VCC = 3.3 V	-0.3		0.10 * VIO	V
$I_{HV_IL_FS}$	Failsafe Input leakage for HV_DDC_SCL and HV_DDC_SDA	V_{IN} = 5.3 V through 1.5 kΩ; VCC = 0 V; VIO = 0 V;	-5		5	µA
I_{HV_IL}	Input leakage for HV_DDC_SCL and HV_DDC_SDA	HV V_{IN} = 5.3 V; LV V_{IN} = VIO;	-5		5	µA
I_{LV_IL}	Input leakage for LV_DDC_SCL and LV_DDC_SDA	HV V_{IN} = 5.3 V; LV V_{IN} = VIO;	-5.5		5.5	µA
I_{HV_OL}	Low-level output current	V_{HV_OL} = 0.4 V; HDMI5V= 5.3 V; Pullup with 1.4 kΩ; VCC = 3.0 V;	3.5			mA
V_{HV_OL}	Low-level output voltage for HV_DDC_SCL and HV_DDC_SDA	HDMI5V= 5.3 V; Pullup with 1.4 kΩ; VCC = 3.0 V;			0.4	V
V_{LV_OL}	Low-level output voltage for LV_DDC_SCL and LV_DDC_SDA for 1.2-V LVCMOS	VCC = 3.0 V; VIO = 1.26 V	0.2		0.3	V

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LV_OL}	Low-level output voltage for LV_DDC_SCL and LV_DDC_SDA for 1.8-V LVCMOS	VCC = 3.0 V; VIO = 1.9 V	0.3		0.4	V
V_{LV_OL}	Low-level output voltage for LV_DDC_SCL and LV_DDC_SDA for 3.3-V LVCMOS	VCC = 3.0 V; VIO = 3.6 V	0.6		0.75	V
$\Delta V_{LV_HYST_3p3V}$	Hysteresis on LV side for 3.3 V LVCMOS	VIO = 3.3 V; VCC = 3.3 V		50		mV
R_{PULV}	Internal pull-up resistor to VIO		7450	10000	13000	Ω
R_{PUHV}	External pull-up resistor to HDMI 5 V		1500	1800	2000	Ω
C_{IOHV}	Capacitance for HV_DDC_SCL and HV_DDC_SDA				12	pF
C_{IOLV}	Capacitance for LV_DDC_SCL and LV_DDC_SDA				7	pF
V_{HDMI5V}	HDMI 5V		4.8		5.3	V
C_{HV_BUS}	Bus capacitance for HV_DDC_SCL and HV_DDC_SDA				750	pF
C_{LV_BUS}	Bus capacitance for LV_DDC_SCL and LV_DDC_SDA				50	pF
HPD_IN						
$V_{IL\text{-}HPDIN}$	Low-level input voltage for HPD_IN	V_{CC} = 3.6 V;	-0.3		0.8	V
$V_{IH\text{-}HPDIN}$	High-level input voltage for HPD_IN	V_{CC} = 3.6 V	2.0		5.5	V
$I_{H\text{-}HPDIN}$	High-level input current for HPD_IN	Device powered; V_{IH} = 5.5 V; Includes internal pull-down resistor	-50		50	µA
$I_{L\text{-}HPDIN}$	Low-level input current for HPD_IN	Device powered; V_{IL} = 0 V; Includes internal pull-down resistor	-1		1	µA
$R_{PD\text{-}HPDIN}$	Internal Pull-down resistance on HPD_IN	V_{CC} = 3.3 V; HPD_IN = 5.5 V	110	150	210	kΩ
$I_{LEAK\text{-}HPDIN}$	Fail-safe condition leakage current for HPD_IN	V_{CC} = 0 V; HPD_IN = 5.5 V	-50		50	µA
HPD_OUT						
V_{OH_3p3V}	High level output voltage when configured for 3.3 V LVCMOS push/pull.	V_{CC} = 3.0 V;	2.4		3.465	V
V_{OH_1p8V}	High level output voltage when configured for 1.8 V LVCMOS push/pull.	V_{CC} = 3.0 V;	1.3		1.95	V
V_{OL_PP}	Low level output voltage when configured for push/pull.	V_{CC} = 3.0 V;	-0.3		0.4	V
V_{OL_OD}	Low level output voltage when configured for open drain.	V_{CC} = 3.0 V; 0.5 kΩ to 3.6 V load;	-0.3		0.4	V
I_{OH_3p3V}	High level output current for 3.3-V LVCMOS	HPD_IN = $V_{IH\text{-}HPDIN}$;			-4	mA
I_{OL_3p3V}	Low level output current for 3.3-V LVCMOS	HPD_IN = $V_{IL\text{-}HPDIN}$; I^2C mode;	4			mA
I_{OH_1p8V}	High level output current for 1.8-V LVCMOS	HPD_IN = $V_{IH\text{-}HPDIN}$;			-1.1	mA
I_{OL_1p8V}	Low level output current for 1.8-V LVCMOS	HPD_IN = $V_{IL\text{-}HPDIN}$; I^2C mode;	1.2			mA
4-LEVEL CONTROL (MODE, LINEAR_EN, EQ1, ADDR/EQ0, TXSLEW, TXPRE, TXSWG)						
V_{TH}	Threshold "0" / "R"	V_{CC} = 3.3 V		0.55		V
V_{TH}	Threshold "R" / "F"	V_{CC} = 3.3 V		1.65		V

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH}	Threshold "F" / "1"	V_{CC} = 3.3 V		2.7		V
I_{IH}	High-level input current	V_{IH} = 3.6 V; V_{CC} = 3.6 V;	20		60	μA
I_{IL}	Low-level input current	V_{IL} = 0 V; V_{CC} = 3.6 V;	–100		-40	μA
R_{4PU}	Internal pullup resistance			48		kΩ
R_{4PD}	Internal pull-down resistance			98		kΩ
HDMI HIGH SPEED INPUTS						
$D_{R_RX_DATA}$	Data lanes data rate		0.25		12	Gbps
$D_{R_RX_CLK}$	Clock lane data rate		0.25		12	Gbps
$V_{ID(DC)}$	DC differential input swing	At pins; LINEAR_EN = L;	400		1200	mVpp
$V_{ID(EYE)}$	Differential input swing eye opening	At pins;	75			mVpp
V_{RX_ASSERT}	Signal detect assert level.	PRBS7 pattern; 12 Gbps;		180		mVpp
$V_{RX_DEASSERT}$	Signal detect deassert level.	PRBS7 pattern; 12 Gbps;		110		mVpp
V_{ICM-DC}	Input DC common mode voltage bias	At pins;	2.5	3.3	VCC	V
$E_{EQ_12Gbs_MAX_LT}$	Maximum Fixed EQ gain (AC - DC)	At 6 GHz; 12 Gbps CTLE; EQ15; DC Gain = 0 dB; Limited Mode; At output of RX;		12		dB
$E_{EQ_12Gbps_MIN_LT}$	Minimum Fixed EQ gain (AC - DC)	At 6 GHz; 12 Gbps CTLE; EQ0; DC Gain = 0 dB; Limited Mode; At output of RX;		1.0		dB
$E_{EQ_12Gbps_BYPASS_LT}$	Maximum Fixed EQ Gain when EQ is bypassed. (AC - DC)	At 6 GHz; 12 Gbps CTLE; DC Gain = 0 dB; Limited Mode; At output of RX;		-1.5		dB
$E_{EQ_6Gbs_MAX_LT}$	Maximum Fixed EQ gain (AC - DC)	At 3 GHz; 6 Gbps CTLE; EQ15; DC Gain = 0 dB; Limited Mode; At output of RX;		12.0		dB
$E_{EQ_6Gbps_MIN_LT}$	Minimum Fixed EQ gain (AC - DC)	At 3 GHz; 6 Gbps CTLE; EQ0; DC Gain = 0 dB; Limited Mode; At output of RX;		0.6		dB
$E_{EQ_3Gbs_MAX_LT}$	Maximum Fixed EQ gain (AC - DC)	At 1.5 GHz; 3 Gbps CTLE; EQ15; DC Gain = 0 dB; Limited Mode; At output of RX;		12		dB
$E_{EQ_3Gbps_MIN_LT}$	Minimum Fixed EQ gain (AC - DC)	At 1.5 GHz; 3 Gbps CTLE; EQ0; DC Gain = 0 dB; Limited Mode; At output of RX;		0.8		dB
R_{INT}	Input differential impedance when termination is enabled	At TTP2; HPD_IN = H; 0℃ ⩽ T_A ⩽ 70℃	90	100	110	Ω
R_{INT}	Input differential impedance when termination is enabled	At TTP2; HPD_IN = H; –20℃ ⩽ T_A ⩽ 85℃	85	100	115	Ω
HDMI HIGH SPEED OUTPUTS (Limited Mode)						
V_{OL_open}	Single-ended low-level output voltage for DR ⩽ 1.65 Gbps data rate	DR = 270 Mbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0dB); TX termination open; VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	2.7		2.9	V
V_{OL_300}	Single-ended low-level output voltage 1.65 Gbps < DR ⩽ 3.4 Gbps.	DR = 3.4 Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); TX termination 300-ohms; VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	2.6		2.9	V

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL_DAT20}	Data lane single-ended low-level output voltage 3.4 Gbps < DR ⩽ 6 Gbps.	DR = 5.94 Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	2.3		2.9	V
$V_{SWING_DA_14}$	Single-ended output voltage swing on data lanes with TX term set to open.	DR = 1.5 Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	400	500	600	mV
$V_{SWING_DA_14}$	Single-ended output voltage swing on data lanes with TX term set to 300-ohms.	DR = 3.4 Gbps;HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	400	500	600	mV
$V_{SWING_DA_20}$	Single-ended output voltage swing on data lanes for HDMI2.0 operation.	DR = 5.94 Gbps;HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	400	500	600	mV
$V_{SWING_CLK_14_OPEN}$	Single-ended output voltage swing on clock lane for DR ⩽ 3.4 Gbps datarate	HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃; TERM set to open;	400	500	600	mV
$V_{SWING_CLK_20}$	Single-ended output voltage swing on clock lane for HDMI 2.0	HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); VCC_EXT = 3.3 V; 25℃ ⩽ T_A ⩽ 85℃;	300	400	600	mV
$V_{OCM-DC-ON}$	FRL DC common mode voltage when actively transmitting	At TTP4; AC_EN = L or H; LTP5, 6, 7 or 8; TXFFE0; 25℃ ⩽ T_A ⩽ 85℃;	2.335		3.495	V
$V_{OCM-DC-OFF}$	FRL DC common mode voltage when lane 3 is disabled	At TTP4; FRL 3 lane mode; AC_EN = L or H; 25℃ ⩽ T_A ⩽ 85℃;	2.335		3.495	V
V_{OD_3G}	Data lanes Differential output swing	At TTP4; 2.97 Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); 25℃ ⩽ T_A ⩽ 85℃;	400		1560	mV
V_{OD_6G}	Data lanes Differential output swing	At TTP4_EQ; 5.94 Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000 mV); TXPRE = "F" (0 dB); 25℃ ⩽ T_A ⩽ 85℃;	150		1560	mV
$V_{OD_12G_FRL}$	Data lanes Differential output swing at 12 G FRL.	At TTP4_EQ; 12 Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000 mV); TXFFE0; 25℃ ⩽ T_A ⩽ 85℃;	100		1560	mV
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0 V; DC-coupled; TMDS output pulled to 3.465 V with 50 Ω resistors			35	µA
I_{OS}	Short circuit current limit	OUT_CLK, OUT_D[2:0] outputs P or N shorted to GND			70	mA
R_{TERM14}	Internal termination for DR ⩽ 3.4 Gbps when DC-coupled	TERM = 1h; AC_EN = L (DC-coupled);HPD_IN=H; Active state; –20℃ ⩽ T_A ⩽ 85℃;	235	295	375	Ω
R_{TERM14}	Internal termination for DR ⩽ 3.4 Gbps when AC-coupled	TERM = 1h; AC_EN = H (AC-coupled); HPD_IN=H; Active state; –20℃ ⩽ T_A ⩽ 85℃;	235	295	375	Ω
R_{TERM2+}	Internal termination for DR > 3.4 Gbps when DC-coupled.	TERM = 3h; AC_EN = L (DC-coupled); HPD_IN=H; Active state; –20℃ ⩽ T_A ⩽ 85℃;	85	100	115	Ω

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TERM2+}	Internal termination for DR > 3.4 Gbps when AC-coupled.	TERM = 3h; AC_EN = H (AC-coupled); HPD_IN=H; Active state; –20℃ ⩽ T_A ⩽ 85℃;	85	100	115	Ω
$V_{TXPRE0-RATIO}$	Transmitter FFE pre-emphasis ratio for 0 dB.	TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 0h; D0_VOD = 3h; D1_TXFFE = 0h; D1_VOD = 3h; D2_TXFFE = 0h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		0		dB
$V_{TXPRE1-RATIO}$	Transmitter FFE pre-emphasis ratio for 3.5 dB for data lanes	At 5.94 Gbps HDMI 2.0; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 1h; D0_VOD = 3h; D1_TXFFE = 1h; D1_VOD = 3h; D2_TXFFE = 1h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		4.0		dB
$V_{TXPRE2-RATIO}$	Transmitter FFE pre-emphasis ratio for 6 dB for data lanes	At 5.94 Gbps HDMI 2.0; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 2h; D0_VOD = 3h; D1_TXFFE = 2h; D1_VOD = 3h; D2_TXFFE = 2h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		6.5		dB
$V_{TXFFE0-RATIO}$	Transmitter FRL TXFFE0 de-emphasis ratio	At 12 Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 4h; CLK_VOD = 3h; D0_TXFFE = 4h; D0_VOD = 3h; D1_TXFFE = 4h; D1_VOD = 3h; D2_TXFFE = 4h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		-2.5		dB
$V_{TXFFE1-RATIO}$	Transmitter FRL TXFFE1 de-emphasis ratio	At 12 Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 5h; CLK_VOD = 3h; D0_TXFFE = 5h; D0_VOD = 3h; D1_TXFFE = 5h; D1_VOD = 3h; D2_TXFFE = 5h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		-3.2		dB
$V_{TXFFE2-RATIO}$	Transmitter FRL TXFFE2 de-emphasis ratio.	At 12 Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 6h; CLK_VOD = 3h; D0_TXFFE = 6h; D0_VOD = 3h; D1_TXFFE = 6h; D1_VOD = 3h; D2_TXFFE = 6h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		-3.5		dB
$V_{TXFFE3-RATIO}$	Transmitter FRL TXFFE3 de-emphasis ratio	At 12 Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 7h; CLK_VOD = 3h; D0_TXFFE = 7h; D0_VOD = 3h; D1_TXFFE = 7h; D1_VOD = 3h; D2_TXFFE = 7h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones;		-4.5		dB
HDMI HIGH SPEED OUTPUTS (Linear Mode)						
$CP_{LF-TXSWG-0}$	Low-frequency 1-dB compression point Dx_VOD = 0.	At 10 MHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100 MHz clock starting at 200 mV to 1200 mV in 50 mV steps;TX DC coupled to VCC_EXT;		900		mVpp

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6.5 Electrical Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$CP_{HF-TXSWG-0}$	High-frequency 1-dB compression point Dx_VOD = 0.	At 6 GHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT;		750		mVpp
$CP_{LF-TXSWG-R}$	Low-frequency 1-dB compression point Dx_VOD = 1.	At 10 MHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100 MHz clock starting at 200 mV to 1200 mV in 50 mV steps; TX DC coupled to VCC_EXT;		1000		mVpp
$CP_{HF-TXSWG-R}$	High-frequency 1-dB compression point Dx_VOD = 1.	At 6 GHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12Gbps CTLE; CTLEBYP_EN = 0;TX DC coupled to VCC_EXT;		800		mVpp
$CP_{LF-TXSWG-F}$	Low-frequency 1-dB compression point Dx_VOD = 2.	At 10 MHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100 MHz clock starting at 200 mV to 1200 mV in 50 mV steps; TX DC coupled to VCC_EXT;		1100		mVpp
$CP_{HF-TXSWG-F}$	High-frequency 1-dB compression point Dx_VOD = 2.	At 6 GHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT;		875		mVpp
$CP_{LF-TXSWG-1}$	Low-frequency 1-dB compression point Dx_VOD = 3.	At 10 MHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100 MHz clock starting at 200 mV to 1200 mV in 50 mV steps; TX DC coupled to VCC_EXT;		1200		mVpp
$CP_{HF-TXSWG-1}$	High-frequency 1-dB compression point Dx_VOD = 3.	At 6 GHz; 200 mVpp < V_{ID} < 1200 mVpp; EQ0; DCGAIN = 0 dB; 12 Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT;		950		mVpp

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Local I2C (SCL/CFG0, SDA/CFG1). Refer to 图 7-9.					
f_{SCL}	I^2C clock frequency			1	MHz
t_{BUF}	Bus free time between START and STOP conditions	0.5			µs
t_{HD_STA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.26			µs
t_{LOW}	Low period of the I^2C clock	0.5			µs
t_{HIGH}	High period of the I^2C clock	0.26			µs
t_{SU_STA}	Setup time for a repeated START condition	0.26			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data setup time	50			ns
t_R	Rise time of both SDA and SCL signals			120	ns
t_F	Fall time of both SDA and SCL signals	4		120	ns
t_{SU_STO}	Setup time for STOP condition	0.26			µs
DDC Snoop I2C Timings. Refer to 图 7-9.					
f_{SCL}	I^2C DDC clock frequency			100	kHz

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6.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
t_{BUF}	Bus free time between START and STOP conditions	4.7			µs
t_{HD_STA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	4			µs
t_{LOW}	Low period of the I^2C clock	4.7			µs
t_{HIGH}	High period of the I^2C clock	4			µs
t_{SU_STA}	Setup time for a repeated START condition	4.7			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SUDAT}	Data setup time	250			ns
t_R	Rise time of both SDA and SCL signals. Measured from 30% to 70%.			1000	ns
t_F	Fall time of both SDA and SCL signals Measured from 70% to 30%.			300	ns
t_{SU_STO}	Setup time for STOP condition	4			µs
C_{b_LV}	Capacitive load for each bus line on LV side			50	pF
Power-On. Refer to 图 7-1.					
t_{VCC_RAMP}	V_{CC} supply ramp. Measured from 10% to 90%.	0.10		50	ms
t_{D_PG}	Internal POR de-assertion delay			5	ms
t_{VIO_SU}	V_{IO} supply stable before reset(2) high.	100			µs
t_{CFG_SU}	Configuration pins(1) setup before reset(2) high.	0			µs
t_{CFG_HD}	Configuration pins(1) hold after reset(2)high.	500			µs

(1) Follow comprise the configuration pins: MODE, ADDR/EQ0, EQ1, TXSWG, TXSLEW, TXPRE, AC_EN, HPDOUT_SEL, DCGAIN
(2) Reset is the logical AND of internal POR and EN pin.

6.7 Switching Characteristics

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Redriver						
f_{HDMI14_open}	Maximum HDMI 1.4 clock frequency at which TX termination is assured to be open	HDMI1.4; 25 MHz ⩽ IN_CLK ⩽ 340 MHz; TXTERM_AUTO_HDMI14 = 0h; TERM = 2h; TX is DC-coupled;	165			MHz
f_{HDMI14_300}	Minimum HDMI 1.4 clock frequency at which TX termination is assured to be 300-ohms	HDMI1.4; 25 MHz ⩽ IN_CLK ⩽ 340 MHz; TXTERM_AUTO_HDMI14 = 0h; TERM = 2h; TX is DC-coupled;			250	MHz
t_{AEQ_DONE}	Time from start of FRL link training to AEQ complete for 3 Gbps.				0.7	ms
t_{AEQ_DONE}	Time from start of FRL link training to AEQ complete for 6 Gbps, 8 Gbps, 10 Gbps, and 12 Gbps				0.5	ms
t_{PD}	Propagation delay time	At TTP4;	90		220	ps
$t_{SK1(T)}$	Data lane Intra-pair output skew with worse case skew at inputs	At TTP4; With 0.15 UI skew at input; At 12 Gbps; LTP5, 6, 7, or 8; TXFFE0; TX termination 100-Ω; Linear mode;			0.15	UI
$t_{SK1(T)}$	Clock lane Intra-pair output skew with zero intra-pair skew at inputs	At TTP4; No intra-pair skew at input; 6 Gbps with 150 MHz clock; TX termination 100-Ω; Limited mode;		0.10	0.15	UI
$t_{SK1(T)}$	Data lane Intra-pair output skew with zero intra-pair skew at inputs	At TTP4; No intra-pair skew at input; At 12 Gbps; LTP5, 6, 7, or 8; TXFFE0; TX termination 100-Ω; Limited mode;		0.053	0.11	UI
$t_{SK2(T)}$	Inter-pair output skew	At TTP4; At 12 Gbps; LTP5, 6, 7, or 8; TXFFE0;			30	ps

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6.7 Switching Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{RF\text{-}CLK\text{-}14}$	Transition time (rise and fall time) for clock lane when operating at HDMI1.4	At TTP4; 20% to 80%; Clock Frequency = 300 MHz;	75		600	ps
$t_{RF\text{-}CLK\text{-}20}$	Transition time (rise and fall time) for clock lane when operating at HDMI 2.0	At TTP4; 20% to 80%; Clock Frequency = 150 MHz;	75		600	ps
t_{RF_14}	Transition time (rise and fall time) for data lanes when operating at HDMI 1.4	At TTP4; 20% to 80%; DR = 3 Gbps; SLEW_HDMI14 = default; PRBS7 pattern; Clock Frequency = 300 MHz;	75		195	ps
t_{RFDAT_20}	Transition time (rise and fall time) for data lanes when operating at HDMI 2.0	At TTP4; 20% to 80%; DR = 6 Gbps; SLEW_HDMI20 = default; PRBS7 pattern; Clock Frequency = 150 MHz;	42.5		115	ps
t_{SLEW_FRL}	Single-ended TX slew rate for data lanes when operating at HDMI 2.1 FRL	At TTP4; Slope at 50% level; All FRL DR up to 12 Gbps; SLEW_HDMI21 = Default; clock pattern of 128 zeros and 128 ones;			16	mV/ps
t_{TRANS_3G}	Transition bit duration when de-emphasis/ pre-emphasis is enabled	At TTP4; DR = 3 Gbps; Clock pattern of 128 zeros followed by 128 ones;	0.4		1	UI
t_{TRANS_6G}	Transition bit duration when de-emphasis/ pre-emphasis is enabled	At TTP4; DR = 6 Gbps; Clock pattern of 128 zeros followed by 128 ones;	0.4		1	UI
t_{TRANS_8G}	Transition bit duration when de-emphasis/ pre-emphasis is enabled	At TTP4; DR = 8 Gbps; Clock pattern of 128 zeros followed by 128 ones;	0.4		1	UI
t_{TRANS_10G}	Transition bit duration when de-emphasis/ pre-emphasis is enabled	At TTP4; DR = 10 Gbps; Clock pattern of 128 zeros followed by 128 ones;	0.5		1.1	UI
t_{TRANS_12G}	Transition bit duration when de-emphasis/ pre-emphasis is enabled	At TTP4; DR = 12 Gbps; Clock pattern of 128 zeros followed by 128 ones;	0.6		1.3	UI
HPD						
t_{HPD_PD}	HPD_IN to HPD_OUT propagation delay	Refer to 图 7-7			100	µs
$t_{HPD_PWR DOWN}$	HPD_IN debounce time before declaring Powerdown. Enter Powerdown if HPD_IN is low after debounce time.	Refer to 图 7-7	2		4	ms
$t_{HPD_STANDBY}$	HPD_IN debounce time required for exiting Powerdown to Standby. Exit Powerdown if HPD_IN is high after debounce time.	Refer to 图 7-8	2		4	ms
Standby						
$t_{STANDBY_ENTRY}$	Detection of electrical idle to entry into Standby.	HPD_IN = H;			300	µs
t_{SIGDET_DB}	Maximum differential signal glitch time rejected during debounce before transitioning from standby to active	HPD_IN = H;			25	µs
t_{SIGDET_DB}	Maximum differential signal glitch time rejected during debounce before transitioning from active to standby	HPD_IN = H;			50	ns
$t_{STANDBY_EXIT}$	Detection of differential signal to exit from Standby to Active state	HPD_IN = H; Does not include AEQ time if AEQ_TX_DELAY_EN = 1;			200	µs
DDC Buffer						
f_{SCL}	DDC buffer frequency				100	kHz
t_{PLH1}	Propagation delay time. Low-to-high-level output. VIO set to 1.2 V LVCMOS levels.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1400	ns
	Propagation delay time. Low-to-high-level output. VIO set to 1.8 V LVCMOS levels.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1400	ns
	Propagation delay time. Low-to-high-level output. VIO set to 3.3 V LVCMOS levels.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1400	ns

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6.7 Switching Characteristics (continued)

over recommended voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH2}	Propagation delay time. Low-to-high-level output. VIO set to 1.2 V LVCMOS levels.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			410	ns
	Propagation delay time. Low-to-high-level output. VIO set to 1.8 V LVCMOS levels.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			410	ns
	Propagation delay time. Low-to-high-level output. VIO set to 3.3 V LVCMOS levels.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			410	ns
t_{PHL1}	Propagation delay time. High to low-level output. VIO set to 1.2 V LVCMOS.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1200	ns
	Propagation delay time. High to low-level output. VIO set to 1.8 V LVCMOS.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1200	ns
	Propagation delay time. High to low-level output. VIO set to 3.3 V LVCMOS.	LV to HV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			1200	ns
t_{PHL2}	Propagation delay time. High to low-level output. VIO set to 1.2 V LVCMOS.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			535	ns
	Propagation delay time. High to low-level output. VIO set to 1.8 V LVCMOS.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			535	ns
	Propagation delay time. High to low-level output. VIO set to 3.3 V LVCMOS.	HV to LV; C_{LV_BUS} = C_{HV_BUS} = 50 pF; DDC_LV_DCC_EN = 1'b1;			535	ns
t_{LV_FALL}	LV side fall time for 1.2-V LVCMOS	70% to 30%; C_{LV_BUS} = C_{HV_BUS} = 50 pF;	75		260	ns
	LV side fall time for 1.8-V LVCMOS	70% to 30%; C_{LV_BUS} = C_{HV_BUS} = 50 pF;	75		260	ns
	LV side fall time for 3.3-V LVCMOS	70% to 30%; C_{LV_BUS} = C_{HV_BUS} = 50 pF;	75		260	ns
t_{HV_FALL}	HV side fall time	70% to 30%; C_{LV_BUS} = C_{HV_BUS} = 50 pF;	75		260	ns
t_{LV_RISE}	LV side rise time for 1.2-V LVCMOS	30% to 70%; C_{LV_BUS} = C_{HV_BUS} = 50 pF; Pulled up to VIO using R_{PULV};	300		670	ns
	LV side rise time for 1.8-V LVCMOS	30% to 70%; C_{LV_BUS} = C_{HV_BUS} = 50 pF; Pulled up to VIO using R_{PULV};	300		670	ns
	LV side rise time for 3.3-V LVCMOS	30% to 70%; C_{LV_BUS} = C_{HV_BUS} = 50 pF; Pulled up to VIO using R_{PULV};	300		670	ns
$t_{HV_RISE_50pF}$	HV side rise time (50 pF load)	30% to 70%; C_{LV_BUS} = C_{HV_BUS} = 50 pF; VCC = 3.0 V; HDMI5V = 5.3 V; Pulled up to HDMI5V using R_{PUHV};			225	ns
$t_{HV_RISE_750pF}$	HV side rise time (750 pF load)	30% to 70%; C_{LV_BUS} = 50 pF; C_{HV_BUS} = 750 pF; VCC = 3.0 V; HDMI5V = 5.3 V; Pulled up to HDMI5V using R_{PUHV};			1250	ns

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6.8 Typical Characteristics

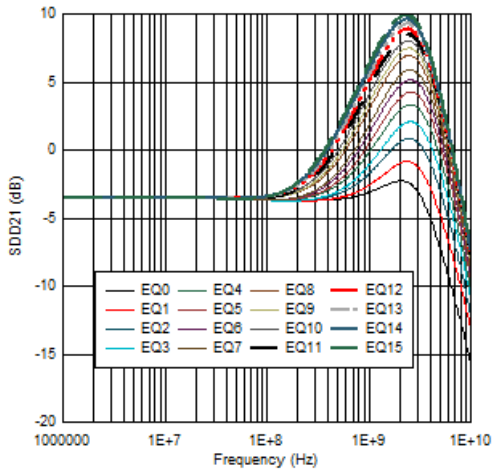


图 6-1. 3 Gbps CTLE EQ Curves with GLOBAL_DCG = 0x2 in Limited Mode

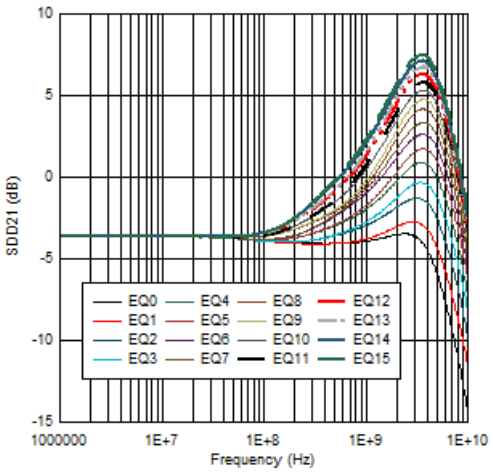


图 6-2. 6 Gbps CTLE EQ Curves with GLOBAL_DCG = 0x2 in Limited Mode

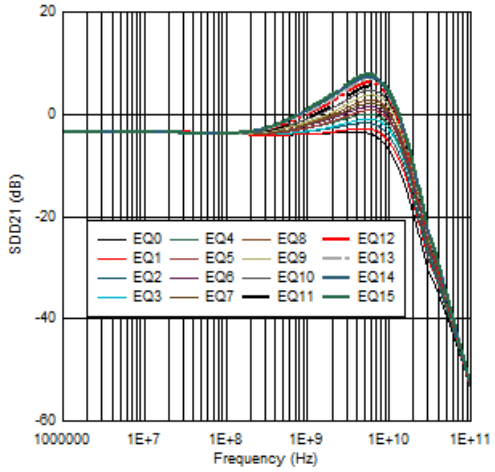


图 6-3. 12 Gbps CTLE EQ Curves with GLOBAL_DCG =0x2 in Limited Mode

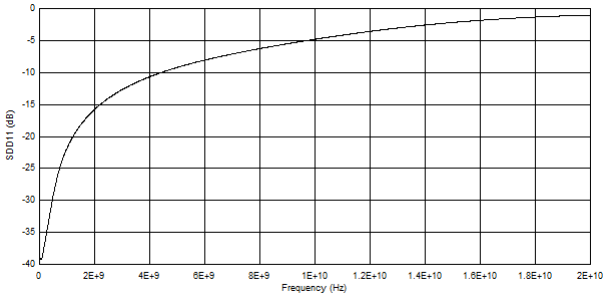


图 6-4. Input Differential Return Loss (SDD11)

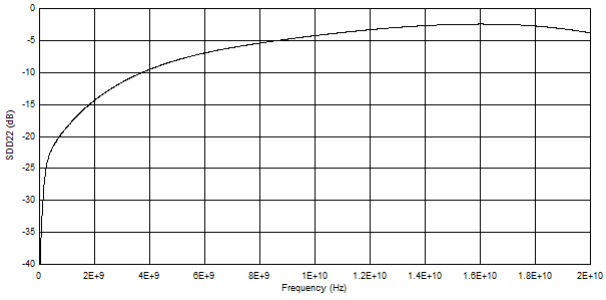


图 6-5. Output Differential Return Loss (SDD22)

7 Parameter Measurement Information

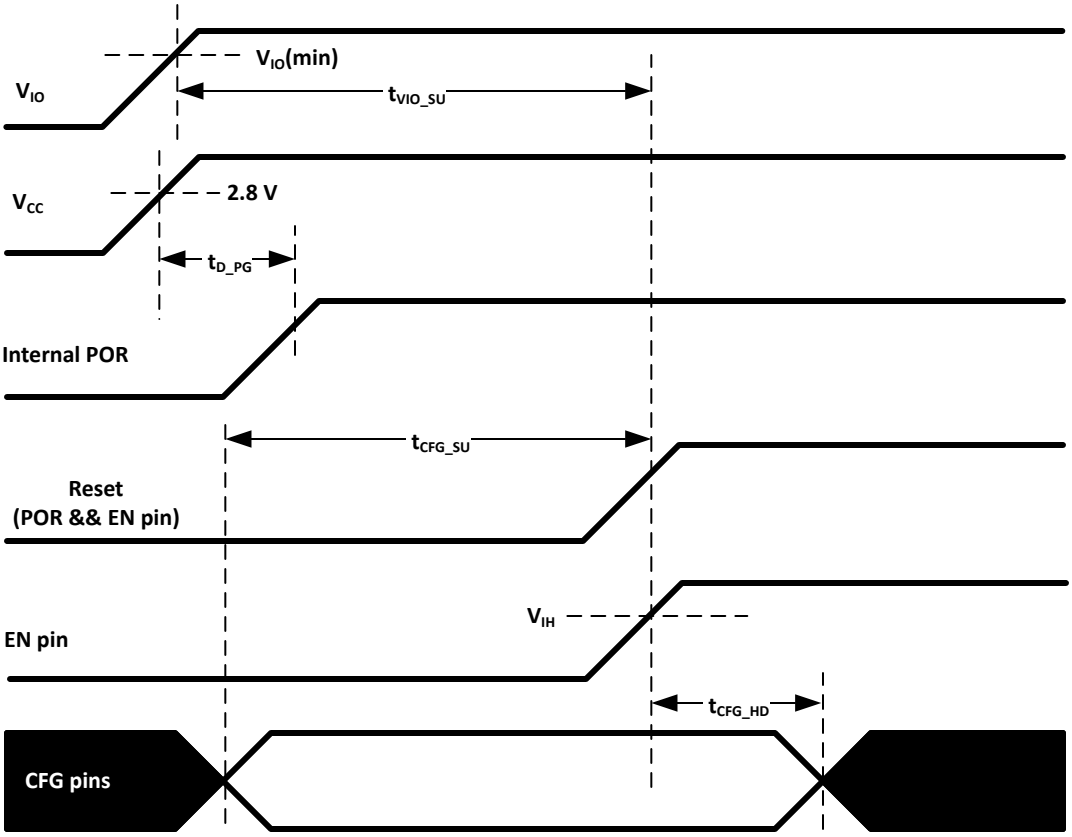


图 7-1. Power-On Timing Requirements

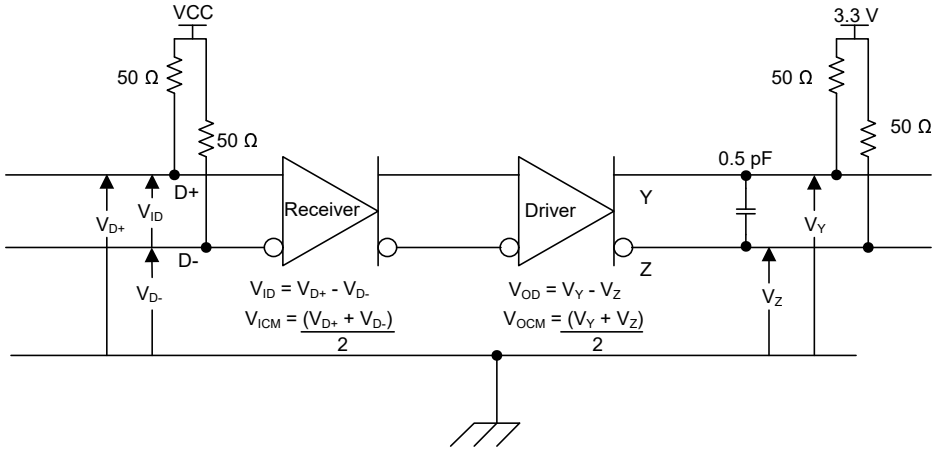


图 7-2. TMDS Main Link Test Circuit

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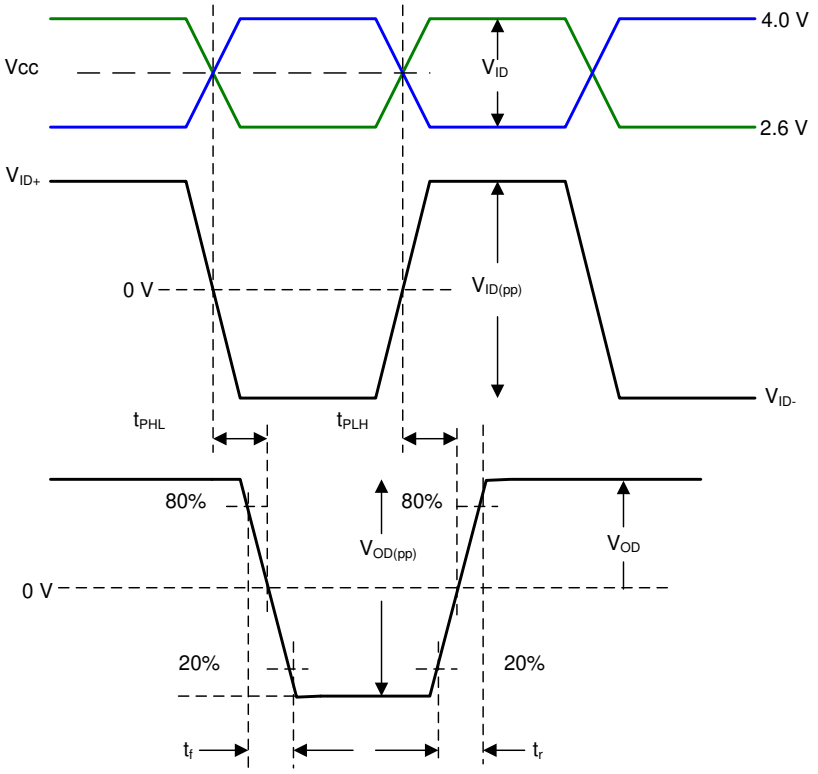


图 7-3. Input or Output Timing Measurements

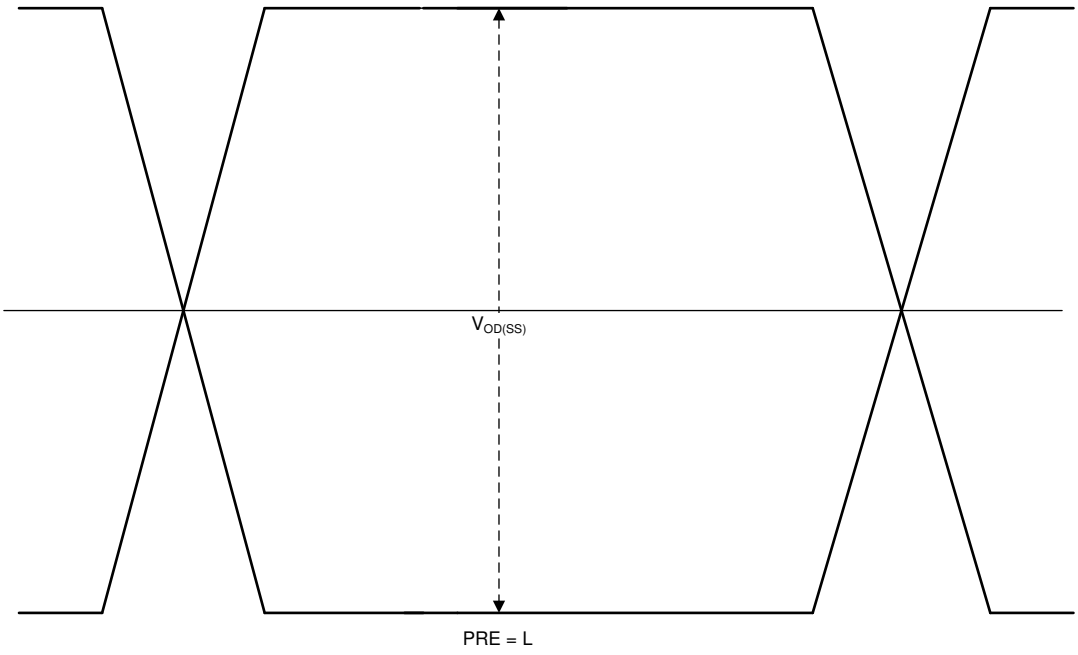


图 7-4. Output Differential Waveform

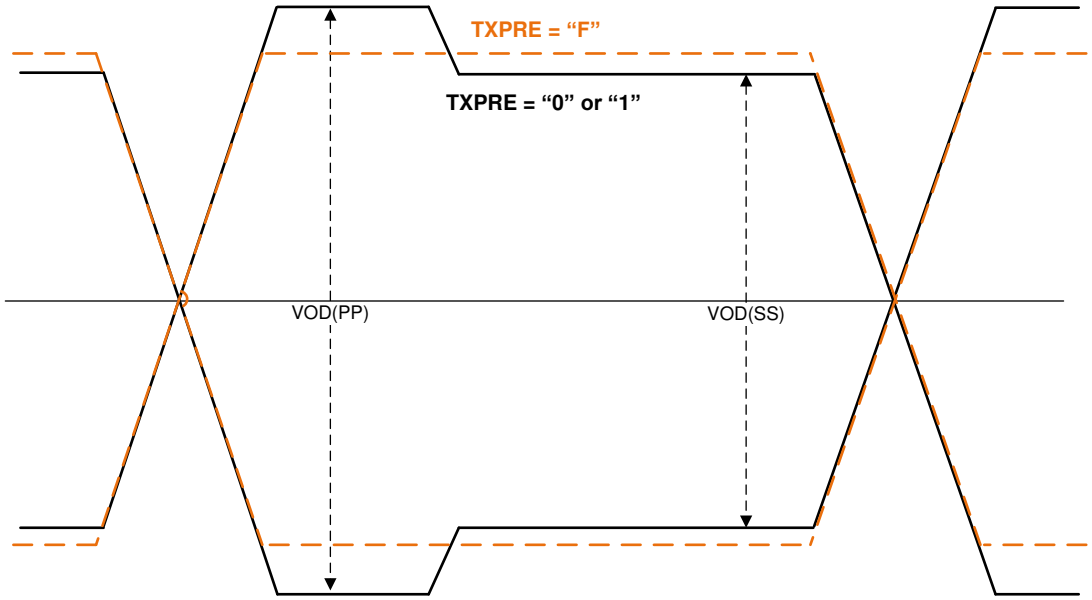
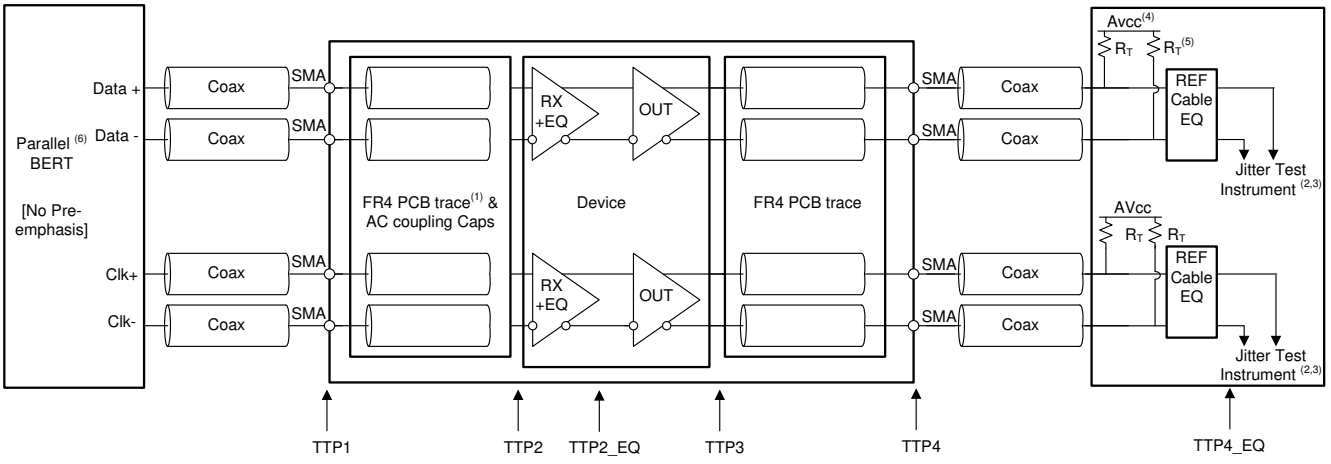


图 7-5. Output Differential Waveform with De-Emphasis



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(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-12" of FR4, AC-coupling capacitor, connector and another 2" of FR4. Trace width – 4 mils. 100 Ω differential impedance.

(2) All Jitter is measured at a BER of 10^{9}. HDMI 2.1 jitter measured at BER 10^{-10}.

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP

(4) AVCC = 3.3 V.

(5) R_T = 50 Ω.

(6) For HDMI 1.4 or 2.0, the input signal from parallel Bert does not have any pre-emphasis or de-emphasis. For HDMI 2.1 FRL, the input signal from BERT will have 2.18 dB pre-shoot and −3.1 dB de-emphasis. Refer to *Recommended Operating Conditions*.

图 7-6. HDMI Output Jitter Measurement

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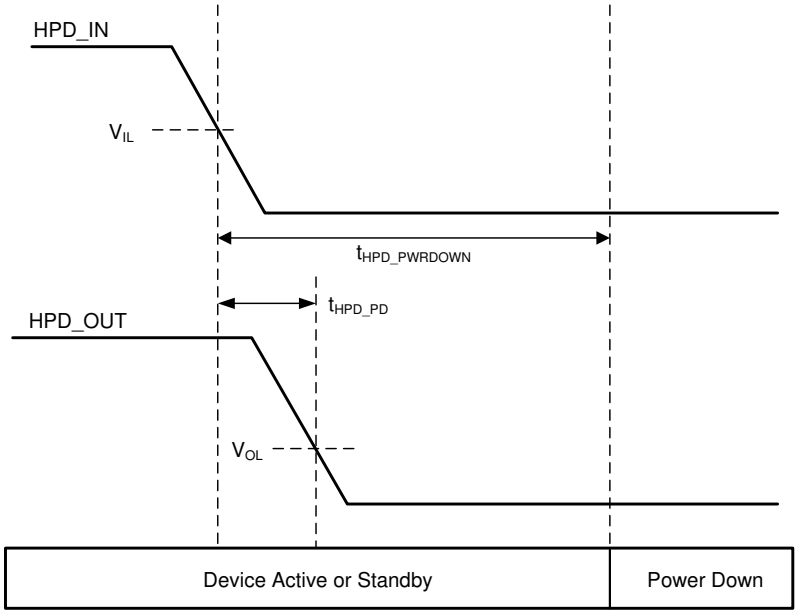


图 7-7. HPD Logic Shutdown and Propagation Timing

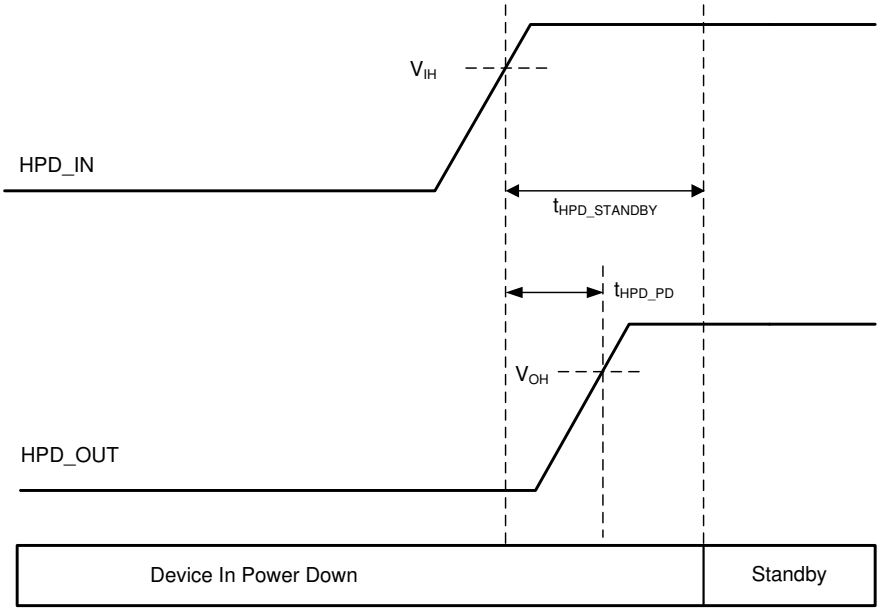


图 7-8. HPD Logic Standby and Propagation Timing

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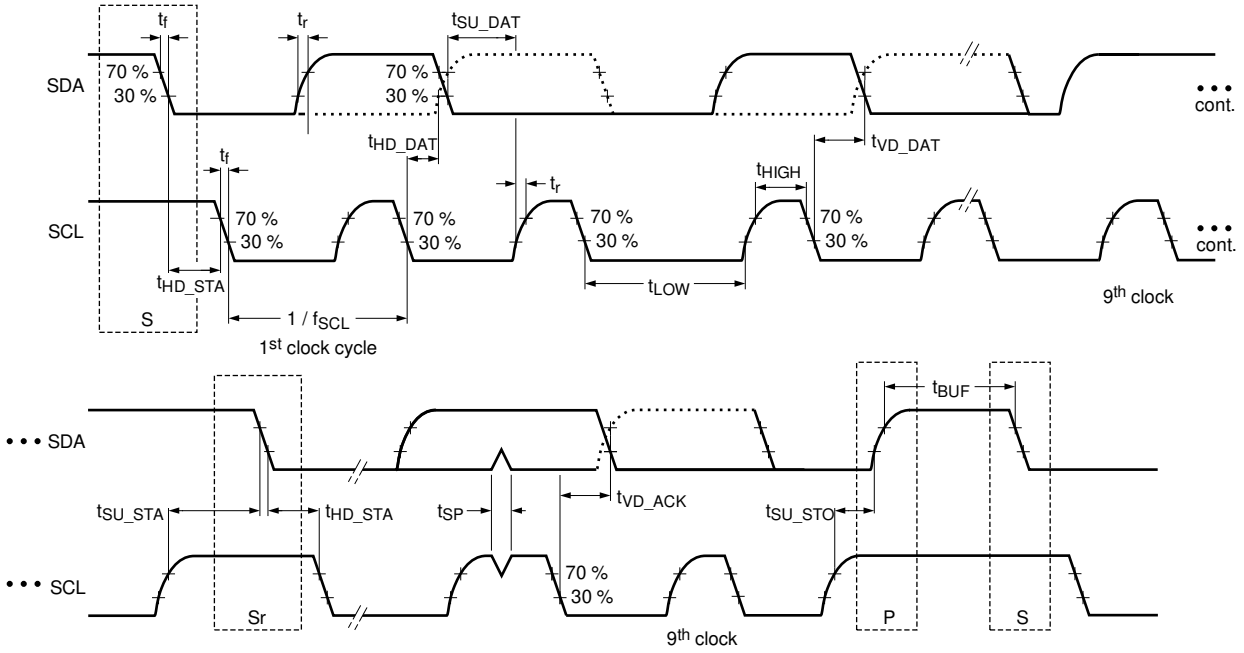


图 7-9. I²C SCL and SDA Timing

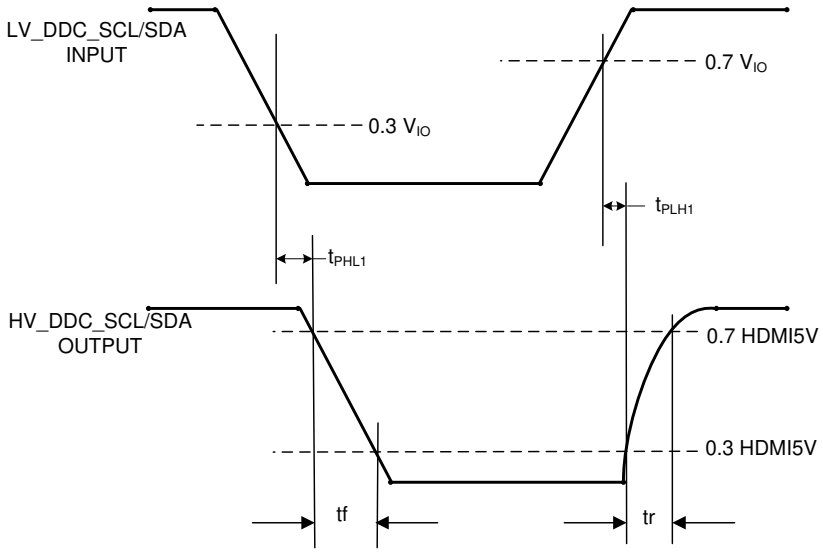


图 7-10. DDC Propagation Delay – Source to Sink

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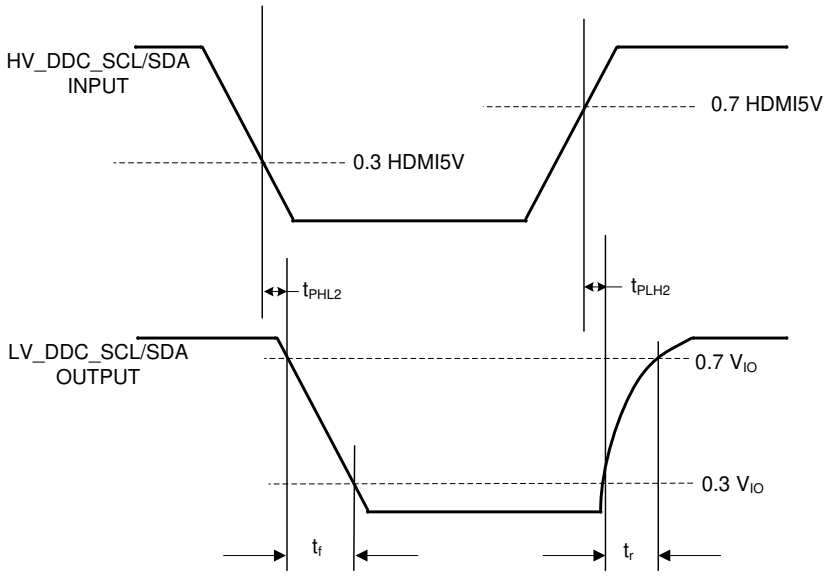


图 7-11. DDC Propagation Delay – Sink to Source

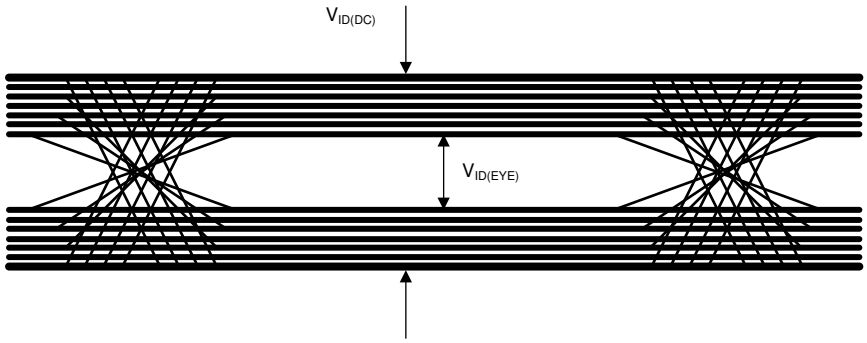
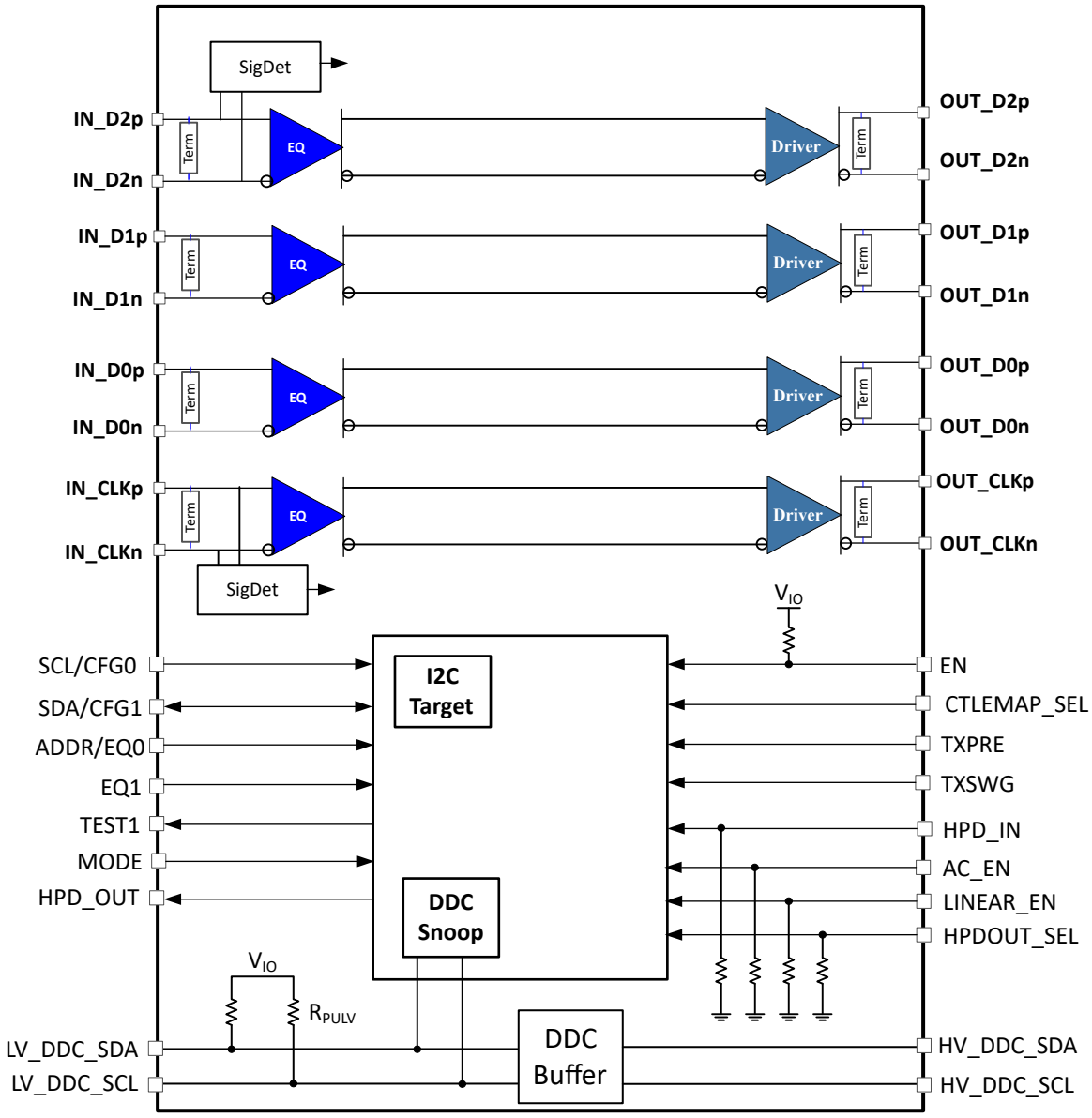


图 7-12. $V_{ID(DC)}$ and $V_{ID(EYE)}$

8 Detailed Description

8.1 Functional Block Diagram



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8.2 Feature Description

8.2.1 4-Level Inputs

The TDP1204 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP1204 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

表 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1-kΩ 5% to GND.
R	Tie 20-kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1-kΩ 5% to V_{CC}.

备注

图 7-1 shows how all 4-level inputs are latched after the rising edge of the EN pin. After these pins are sampled, the internal pull-up and pull-down resistors will be isolated to save power.

8.2.2 I/O Voltage Level Selection

The TDP1204 supports 1.2-V, 1.8-V, and 3.3-V LVCMOS levels. The VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1.

The AC_EN pin threshold is fixed at 3.3-V LVCMOS levels. EN pin threshold is fixed at 1.2-V LVCMOS threshold.

表 8-2. Selection of LVCMOS Signaling Level

VIO pin	LVCMOS Signaling Level
VALUE < 1.5-V	1.2-V
1.5-V < VALUE < 2.5-V	1.8-V
VALUE > 2.5-V	3.3-V

8.2.3 HPD_OUT

The TDP1204 will level shift the 5-V signaling level present on the HPD_IN pin to a lower voltage such as 1.8-V or 3.3-V levels on the HPD_OUT pin. The HPD_OUT supports both push-pull and open drain. The default operation is push-pull. Selection between push-pull and open drain is done through the HPDOUT_SEL register.

表 8-2 lists how the VIO determines the output level of HPD_OUT when HPD_OUT is configured for push-pull operation. Please note push-pull operation is not supported for VIO less than 1.7-V.

备注

Open-drain operation is only supported when TDP1204 is configured for I2C mode.

When EN pin is low, the HPD_OUT pin will be in a high impedance state. It is recommended to have a weak pull-down resistor (such as 220k) on HPD_OUT.

8.2.4 Lane Control

The TDP1204 has various lane control features. Pin strapping globally controls features like receiver equalization, V_{OD} swing, slew rate, and pre-emphasis or de-emphasis. Through I^2C receiver equalization, transmitter swing, and pre-emphasis for each lane can be independently controlled.

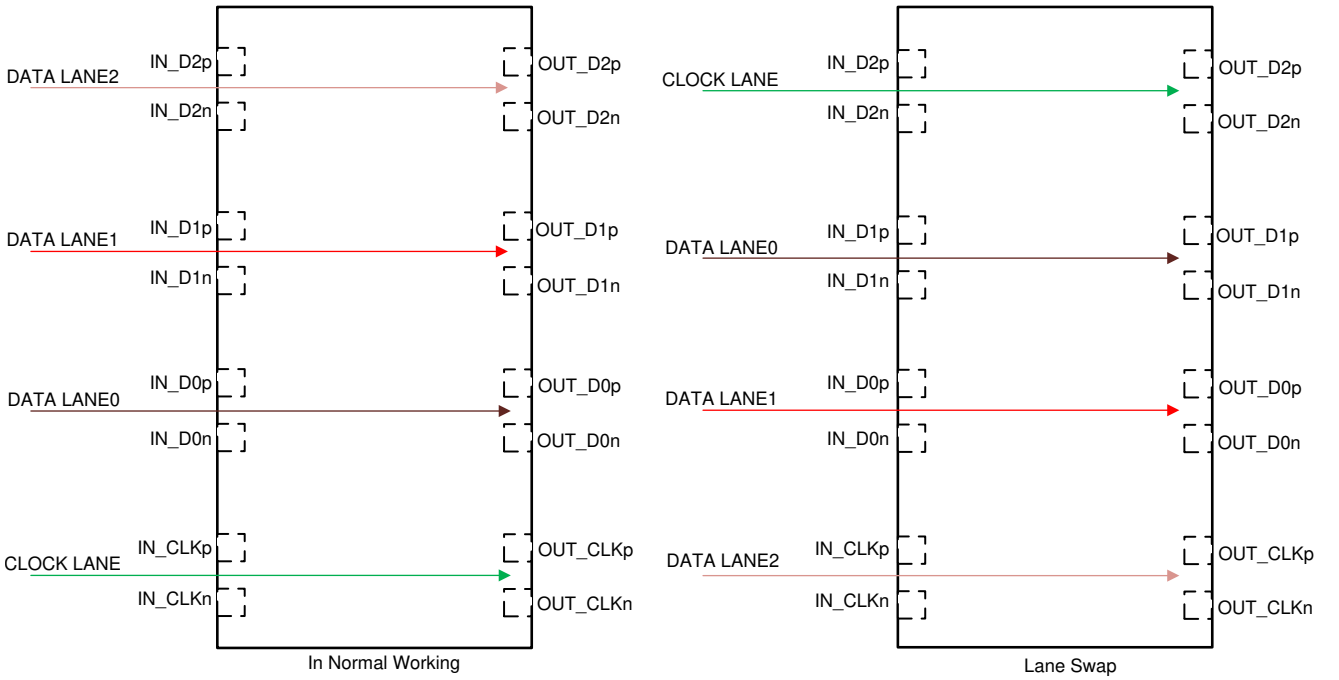
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8.2.5 Swap

图 8-1 shows how TDP1204 incorporates a swap function which can swap the lanes. The RX EQ, pre-emphasis, termination, and slew configurations will follow the new mapping. This function is supported in pin strap mode as well as when TDP1204 is configured for I²C mode. A register controls the swap function in I²C mode.

表 8-3. Swap Functions

Normal Operation CFG1 pin = L or LANE_SWAP Register is 0h	CFG1 = H or LANE_SWAP Register is 1h
IN_D2 → OUT_D2	IN_CLK → OUT_CLK
IN_D1 → OUT_D1	IN_D0 → OUT_D0
IN_D0 → OUT_D0	IN_D1 → OUT_D1
IN_CLK → OUT_CLK	IN_D2 → OUT_D2



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图 8-1. TDP1204 Swap Function

8.2.6 Linear and Limited Redriver

The TDP1204 supports both linear and limited redriver. Selection between linear and limited can be done from the LINEAR_EN pin in pin-strap mode or through GLOBAL_LINR_EN register in I²C mode.

The limited redriver mode will decouple TDP1204 transmitter's voltage swing, pre-emphasis or de-emphasis, and slew rate from the GPUs transmitter. This allows the GPU to use a lower power TX setting and depends on the TDP1204 transmitter to meet TX compliance requirements. For source applications, it is recommended to configure TDP1204 as a limited redriver. It is not recommended to use limited redriver mode in sink applications.

Unlike limited redriver mode, in linear redriver mode the TDP1204 transmitter's output is not decoupled from the GPU's transmitter. In linear redriver mode, the TDP1204 transmitter's output is a linear function of its input. The linear redriver mode offers transparency to link training which makes it perfect for HDMI 2.1 applications. For HDMI sink applications, it is recommended to configure TDP1204 as a linear redriver.

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表 8-4 lists the requirements that the GPU transmitter must meet if linear redriver mode is used in an HDMI 2.1 source application. Linear redriver mode should only be used for HDMI 2.1 data rates. For HDMI 1.4 and 2.0, the TDP1204 should be configured for limited mode (LINEAR_EN = "0" or "1").

表 8-4. Linear Redriver Mode: GPU TX Requirements for HDMI Source Applications

GPU TX Parameter	Min	Max	Units
Single-ended TX swing for HDMI 2.1	400	500	mV
TX rise/fall time for 3, 6, 8, 10, and 12-Gbps FRL		16	mV/ps

The TDP1204 in pin-strap mode provides the option to dynamically switch between limited and linear based on the HDMI mode of operation. The feature is enabled by setting LINEAR_EN pin = "1".

表 8-5. Pin-Strap Mode LINEAR_EN Pin Function

LINEAR_EN Pin Level	HDMI 1.4, 2.0, or DP	HDMI 2.1 FRL
1	Limited Enabled	Linear Enabled
F	Linear Enabled Recommended for DP and HDMI sink application.	Linear Enabled Recommended for DP and HDMI sink application.
R	Reserved	Reserved
0	Limited Enabled. Recommended for HDMI source application	Limited Enabled Recommended for HDMI source application

8.2.7 Main Link Inputs

Each main link input (IN_D[2:0] and IN_CLK) is internally biased to 3.3-V through approximately 100-Ω (50-Ω single-ended). When using TDP1204 in DisplayPort++ applications, external AC-coupling capacitance should be used. When using TDP1204 in an HDMI application such as in an HDMI monitor, the main link inputs can be DC-coupled to a compliant HDMI transmitter. Each input data channel contains an equalizer to compensate for cable or board losses.

8.2.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TDP1204 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through the I^2C register. 表 8-6 lists the pin strap settings and EQ values.

The TDP1204 has three sets of CTLE curves (3-Gbps CTLE, 6-Gbps CTLE, and 12-Gbps CTLE) with each curve having 16 AC gain settings and 3 DC gain settings. 表 8-6 provides details about the 16 AC gain settings with GLOBAL_DCG = 0x2.

The TDP1204 in pin-strap mode has three CTLE HDMI Datarate Maps: Map A, Map B, and Map C. 表 8-7 provides details about these maps. The expectation is Map A and C should be used if TDP1204 is used in a source application and Map B for a sink application.

表 8-8 lists how the sampled state of the CTLEMAP_SEL pin determines the default CTLE HDMI Datarate map when the TDP1204 is configured for pin-strap mode.

In I^2C mode, the default CTLE (3-Gbps, 6-Gbps, or 12-Gbps) used for each HDMI mode can be controlled from a register.

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表 8-6. Receiver EQ Settings When GLOBAL_DCG = 0x2

EQ Setting(1)	RX EQ Level for 3-Gbps CTLE (Gain at 1.5-GHz – Gain at 10-MHz)	RX EQ Level for 6-Gbps CTLE (Gain at 3-GHz – Gain at 10-MHz)	RX EQ Level for 12-Gbps CTLE (Gain at 6-GHz – Gain at 10-MHz)	EQ1 PIN	EQ0 PIN
0(2)	1.0	0.5	0	0	0
1	2.0	1.0	0.8	0	R
2	3.2	2.4	1.8	0	F
3	4.2	3.3	2.7	0	1
4	5.3	4.4	3.7	R	0
5	6.0	5.2	4.4	R	R
6	7.0	6.0	5.0	R	F
7	7.7	6.8	5.8	R	1
8	9.0	7.5	6.5	F	0
9	9.5	8.2	7.5	F	R
10	10.0	8.8	8.3	F	F
11	10.5	9.3	9.1	F	1
12	11.0	10.0	9.8	1	0
13	11.5	10.5	10.3	1	R
14	12.0	11.0	11.0	1	F
15	12.3	11.8	11.6	1	1

(1) CLK_EQ, D0_EQ, D1_EQ, and D2_EQ registers determine the receiver EQ setting in I2C mode.
(2) When CTLEBYP_EN = 1 and DCGAIN = 0-dB, EQ settings 0 will be 0-dB due to the CTLE is bypassed.

表 8-7. CTLE HDMI Datarate Map A, B, and C

HDMI Mode	Map A	Map B	Map C
1.4	12 Gbps CTLE	3 Gbps CTLE	6 Gbps CTLE
2.0	12 Gbps CTLE	6 Gbps CTLE	6 Gbps CTLE
3 Gbps FRL	12 Gbps CTLE	3 Gbps CTLE	6 Gbps CTLE
6 Gbps FRL	12 Gbps CTLE	6 Gbps CTLE	6 Gbps CTLE
8 Gbps FRL	12 Gbps CTLE	12 Gbps CTLE	12 Gbps CTLE
10 Gbps FRL	12 Gbps CTLE	12 Gbps CTLE	12 Gbps CTLE
12 Gbps FRL	12 Gbps CTLE	12 Gbps CTLE	12 Gbps CTLE

表 8-8. Pin-strap Mode CTLE HDMI Datarate Mapping

	Sampled State of CTLEMAP_SEL pin			
	"0"	"R"	"F"	"1"
CTLE HDMI Datarate Map	Map A	Map C	Map A	Map B

备注

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

8.2.9 CTLE Bypass

The TDP1204 will operate as a buffer when CTLE bypass is enabled. In pin-strap mode, this feature is disabled. In I^2C mode, this feature is enabled when CTLEBYP_EN = 1h and GLOBAL_DCG = 2h. Any lane that has EQ setting of 0h will operate in CTLE bypass.

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8.2.10 Adaptive Equalization in HDMI 2.1 FRL

The TDP1204 supports adaptive equalization (AEQ) for HDMI 2.1 FRL. It does not support AEQ for HDMI 1.4 or 2.0. In HDMI 1.4 and HDMI 2.0 modes, TDP1204 will use the sampled state of the EQ[1:0] pins or value programmed into the register. The AEQ is supported in some pin-strap modes as well as in I^2C mode. In I^2C mode, AEQ can be enabled by setting the AEQ_EN register. The TDP1204 adaptation algorithm scans through available equalization settings searching for a setting for which the incoming high-speed signal is not over equalized.

The TDP1204 will perform adaptive equalization when FRL link training begins. It will also re-adapt each time the data rate changes. The adaption will only occur during the TXFFE0 portion of FRL link training when LTP5, LTP6, LTP7, or LTP8 is being received. The TDP1204 adaption will complete within t_{AEQ_DONE} from the time FRL link training begins. If the sink requests additional TXFFE levels (TXFFE1, 2, or 3), then the TDP1204 will keep its equalizer settings fixed at the value adapted during TXFFE0. If for some reason the FRL link training fails and transitions to legacy mode (HDMI 1.4 or HDMI 2.0), then the EQ [1:0] pins sample the EQ settings that the TDP1204 switches to if in pin-strap mode or programmed into the register (if in I2C mode).

The TDP1204 will keep OUT_D[2:0] and OUT_CLK disabled until after adaptation completes. After adaptation completes, the appropriate lanes will be enabled. In I^2C mode, this behavior can be overridden by clearing the AEQ_TX_DELAY_EN field.

表 8-9. Adaptive Equalization Enable and Disable

	CTLEMAP_SEL pin level			
MODE pin level	**0**	**R**	**F**	**1**
0	AEQ disabled	AEQ disable	AEQ disabled	AEQ disabled
R	AEQ disabled	AEQ disabled	AEQ enabled	AEQ enabled
F	I^2C register	I^2C register	I^2C register	I^2C register
1	AEQ disabled	AEQ disabled	AEQ enabled	AEQ enabled

备注

The AEQ operates only on IN_D1 pins (pins 12 and 13). The EQ value determined by AEQ will be applied to the other FRL data lanes.

8.2.10.1 HDMI 2.1 TX Compliance Testing with AEQ Enabled

Care must be taken when performing HDMI 2.1 TX compliance testing with AEQ enabled. Because the TDP1204 will only adapt to LTP5 through 8 during the TXFFE0 part of link training, it is important the test equipment initiate a FRL link training before performing any TX measurements, especially TX eye and jitter measurement. After completion of FRL link training, the test equipment can then switch the current pattern (LTP5, LTP6, LTP7, or LTP8) to the desired test pattern (LTP1, LTP2, LTP3, or LTP4). If the test equipment request LTP1, LTP2, LTP3, or LTP4 before initiating link training, the TDP1204 will use the sampled state of EQ[1:0] pins.

The following HDMI 2.1 TX tests use LTP5, LTP6, LTP7, and LTP8 as the required pattern for the measurement: HFR1-1, HFR1-2, HFR1-4, HFR1-7, and HFR1-8. If the TDP1204 AEQ adaption has not completed and instead uses sampled state of EQ[1:0] pins, then it is possible these tests may fail or inaccurately represent system performance.

8.2.11 HDMI 2.1 Link Training Compatible Rx EQ

This mode is recommended in source applications in which the GPU is unaware of the TDP1204 presence and will adjust its transmitter levels (VOD, de-emphasis, and pre-shoot) during HDMI 2.1 FRL link training. This mode is only supported if the TDP1204 is enabled for limited redriver. 表 8-10 lists the TXFFE levels that this mode assumes the GPU is using.

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This feature is supported in I²C mode and all pin-strap modes with the exception of MODE = "0".

In HDMI 2.1 with AEQ disabled, the TDP1204 will initially set the RX EQ based on the EQ0 and EQ1 pins. The pins determine what value will be used when the TXFFE0 is snooped during FRL link training. 表 8-11 lists how TDP1204 uses the EQ setting for each increase in TXFFE level (TXFFE1, 2, or 3) from the sampled state of the EQ [1:0] pins.

When HDMI 2.1 with AEQ is enabled, the TDP1204 will adapt during the TXFFE0 portion of FRL link training. 表 8-11 lists how TDP1204 uses the EQ setting for each increase in TXFFE level (TXFFE1, 2, or 3) from the adapted EQ value.

表 8-10. Recommended GPU FRL TXFFE Levels

GPU FRL TXFFE Levels	Pre-Shoot (dB)	De-Emphasis (dB)
TXFFE0	2.18	−3.10
TXFFE1	2.50	−4.43
TXFFE2	2.92	−6.02
TXFFE3	3.52	−7.96

表 8-11. Link Training Compatible RX EQ Adjustments

Initial EQ Setting from sampled state of EQ[1:0] pins or adapted EQ value	EQ Setting Used for TXFFE1	EQ Setting Used for TXFFE2	EQ Setting Used for TXFFE3
0	0	0	0
1	0	0	0
2	1	0	0
3	1	0	0
4	2	1	0
5	2	1	0
6	3	1	0
7	3	1	0
8	4	2	1
9	5	3	1
10	6	4	1
11	7	5	1
12	8	6	2
13	9	7	3
14	10	8	4
15	11	9	5

8.2.12 Input Signal Detect

When standby is enabled and swap is disabled, the TDP1204 waits for a signal on either IN_CLK (if HDMI 1.4 or 2.0) or IN_D2 (if HDMI 2.1). When standby is enabled and swap is enabled, the TDP1204 looks for a signal on either IN_CLK (if HDMI 2.1) or IN_D2 (if HDMI 1.4 or 2.0). The TDP1204 is fully functional when a signal is detected. If no signal is detected, then the device reenters standby state waiting for a signal again. In the standby state, all of the TMDS outputs are in high-Z status. In both pin-strap mode and I²C mode, standby is enabled by default. In I²C mode, standby can be disabled by setting the STANDBY_DISABLE register mode.

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8.2.13 Main Link Outputs

8.2.13.1 Transmitter Bias

The TDP1204 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I^2C mode. The AC_EN pin informs the TDP1204 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TDP1204 transmitters are internally biased to approximately V_{CC}. For DisplayPort, HDMI 2.1 FRL AC-coupled, or any other AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TDP1204 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

备注

图 8-3 shows that if using AC-coupled TX mode (AC_EN = high) in an HDMI source application, then an external 499 Ω pull-down to GND must be placed on each OUT pin (OUT_D2:0p/n and OUT_CLKp/n) between the AC-coupling capacitor and the HDMI receptacle. The purpose of the 499 Ω resistor is to set the common mode voltage to HDMI compliant levels.

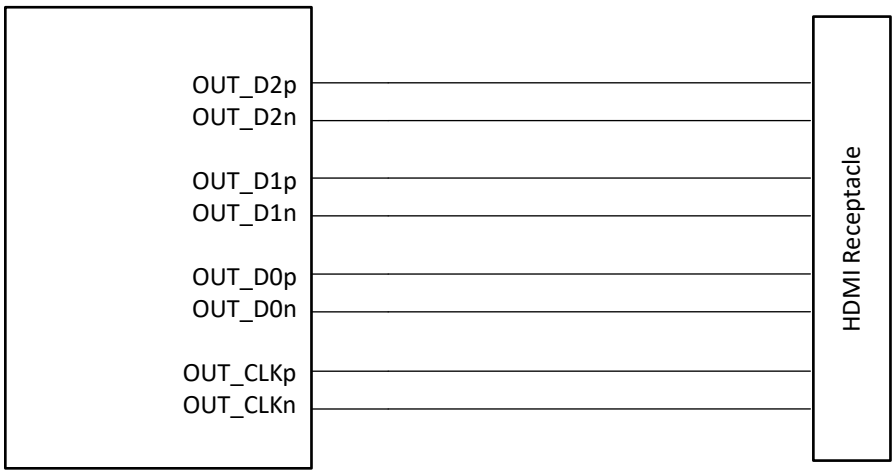


图 8-2. DC-Coupled TX in HDMI Source Application (AC_EN = Low). External ESD is Not Shown.

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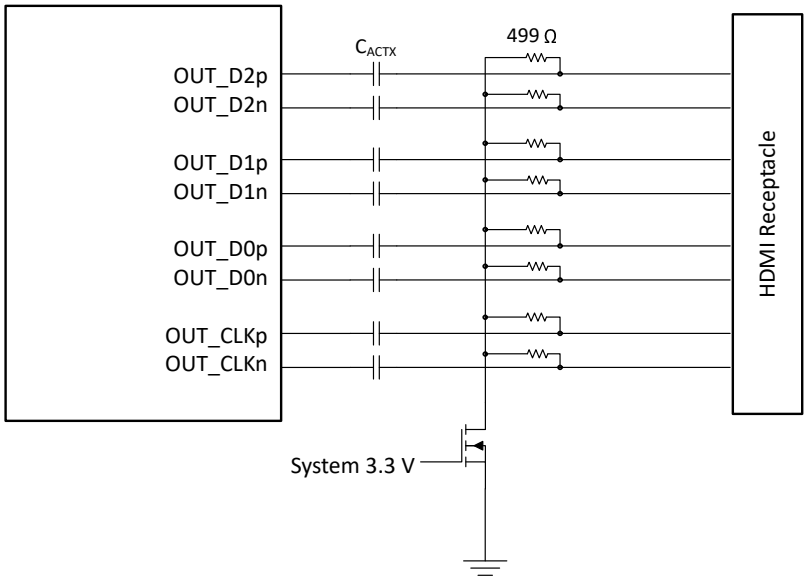


图 8-3. AC-Coupled TX in HDMI Source Application (AC_EN = High). External ESD is Not Shown.

8.2.13.2 Transmitter Impedance Control

HDMI 2.0 standards require a source termination impedance approximately 100-Ω for data rates > 3.4-Gbps. HDMI 1.4b requires no source termination but has a provision for termination for higher data rates greater than 1.65-Gbps. Enabling this termination is optional. 表 8-13 lists how the TDP1204 terminations are controlled automatically when in pin strap mode. Depending on the MODE pin, the CFG0 pin can be used to select the HDMI 1.4 termination between open and 300-Ω.

The TDP1204 supports automatic selection between open and 300-Ω termination when operating in HDMI 1.4. In pin-strap mode with CTL0 low, the TDP1204 will enable open termination when HDMI clock frequency is less than f_{HDMI14_open} and will enable 300-Ω termination when HDMI clock frequency is greater than f_{HDMI14_300}. TXTERM_AUTO_HDMI14 register controls this feature in I2C mode.

In I^2C mode, termination is controlled through the registers as provided in 表 8-12.

表 8-12. Source Termination Control in I2C mode

TX_AC_EN Register	TERM Register	TXTERM_AUTO_HDMI14 Register	Source Termination
0	00	X	None
0	01	X	Parallel ≅ 300-Ω across P and N
0	10	X	Automatic. HDMI 2.0 or HDM 2.1. parallel ≅ 100-Ω across P and N
0	10	1	Automatic. HDMI 1.4. parallel ≅ 300-Ω across P and N
0	10	0	Automatic. HDMI 1.4. No termination if HDMI clock frequency is ≤ f_{HDMI14_open}.
0	10	0	Automatic. HDMI 1.4. Parallel ≅ 300-Ω across P and N termination if HDMI clock frequency is ≥ f_{HDMI14_300}.
0	11	X	Parallel ≈ 100-Ω across P and N
1	00	X	≅ 150-Ω to supply (V_{CC}) on both P and N
1	01	X	≅ 150-Ω to supply (V_{CC}) on both P and N
1	10	X	Automatic. ≅ 150-Ω to supply (V_{CC}) on both P and N for HDMI 1.4. Otherwise ≅ 50-Ω to supply (V_{CC}) on both P and N.

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表 8-12. Source Termination Control in I2C mode (continued)

TX_AC_EN Register	TERM Register	TXTERM_AUTO_HDMI14 Register	Source Termination
1	11	X	≅ 50-Ω to supply (V_{CC}) on both P and N

表 8-13. Automatic Source Termination Control in Pin-Strap Mode

HDMI Mode	AC_EN pin	Source Termination
HDMI 1.4	0	None or parallel ≅ 300-Ω across P and N depending on state of SCL/CFG0 pin
HDMI 2.0	0	Parallel ≅ 100-Ω across P and N
HDMI 1.4	1	≅ 150-Ω to supply (V_{CC}) on both P and N
HDMI 2.0	1	≅ 50-Ω to supply (V_{CC}) on both P and N

8.2.13.3 TX Slew Rate Control

The TDP1204 has the ability to slow down the TMDS output edge rates. In pin-strap mode, the TX slew rate can not be controlled. In I^2C mode, both clock and data lanes slew rate can be controlled from a register. 表 8-14 lists the supported settings for each slew rate register based on HDMI data rate. The TDP1204 must be configured in limited redriver mode to control the TX slew rate.

表 8-14. I^2C Mode TX Slew Register Supported Settings

HDMI Datarate	SLEW_CLK Register	SLEW_3G Register	SLEW_6G Register	SLEW_8G10G12G Register
HDMI 1.4	3'b000 through 3'b011	3'b010 through 3'b101	N/A	N/A
HDMI 2.0	3'b000 through 3'b011	N/A	3'b011 through 3'b110	N/A
HDMI 2.1 3 Gbps FRL	N/A	3'b010 through 3'b101	N/A	N/A
HDMI 2.1 6 Gbps FRL	N/A	N/A	3'b011 through 3'b110	N/A
HDMI 2.1 8Gbps FRL	N/A	N/A	N/A	3'b100 through 3'b111
HDMI 2.1 10 Gbps FRL	N/A	N/A	N/A	3'b110 through 3'b111
HDMI 2.1 12 Gbps FRL	N/A	N/A	N/A	3'b111

8.2.13.4 TX Pre-Emphasis and De-Emphasis Control

The TDP1204 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP1204 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane unless the TDP1204 is in HDMI 2.1 FRL mode and at which time the clock lane becomes a data lane. There are two methods to implement pre-emphasis, pin strapping or through I^2C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP1204 is operating in HDMI 1.4 or HDMI 2.0. 表 8-15 lists these pre-emphasis and de-emphasis values. In HDMI 2.1 FRL mode, the de-emphasis value used is based on the DDC TXFFE snooped value. 表 8-16 lists how the TDP1204 uses the de-emphasis level for each TX FFE level.

表 8-15. Pin-Strap TXPRE Pin Function

	LINEAR_EN pin = "0"			LINEAR_EN pin = "F" or "1"	LINEAR_EN pin = "R"
TXPRE pin	HDMI 1.4 or HDMI 2.0	HDMI 2.1 FRL TXFF0 Level	AEQ ADJUSTMENT	AEQ ADJUSTMENT	AEQ ADJUSTMENT
0	3.5 dB pre-emphasis	Refer to 表 8-16.	0	+1	0
R	-2.5 dB de-emphasis	Refer to 表 8-16.	0	+4	0
F	0 dB	Refer to 表 8-16.	0	0	0

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表 8-15. Pin-Strap TXPRE Pin Function (continued)

	LINEAR_EN pin = "0"			LINEAR_EN pin = "F" or "1"	LINEAR_EN pin = "R"
TXPRE pin	HDMI 1.4 or HDMI 2.0	HDMI 2.1 FRL TXFF0 Level	AEQ ADJUSTMENT	AEQ ADJUSTMENT	AEQ ADJUSTMENT
1	6.0 dB pre-emphasis	Refer to 表 8-16	0	+2	0

表 8-16. HDMI 2.1 FRL TX FFE Levels

FRL TX FFE Snooped Level	De-Emphasis (dB)
TXFFE0	-2.5
TXFFE1	-3.5
TXFFE2	-3.7
TXFFE3	-4.6

8.2.13.5 TX Swing Control

The TDP1204 transmitter swing level can be adjusted in both pin strap and I^2C mode. In I^2C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

表 8-17 lists how the TXSWG pin adjusts the default 1000 mV swing in pin strap mode with limited redeliver mode enabled. In HDMI 1.4 the TXSWG controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the data lanes while the clock lane will remain at the default value. In HDMI 2.1, the TXSWG pin controls data and clock lanes.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mVpp) and therefore TXSWG pin is not used. In I^2C mode, the linearity range can be adjusted from a register.

表 8-17. Pin Strap TXSWG Control

TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Limited Mode for HDMI 2.1	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	Default + 10%	1200 mVpp
R	Default − 5%	Default − 5%	Default − 5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	Default + 5%	1200 mVpp

8.2.14 DDC Buffer

The TDP1204 has a DDC buffer for capacitance isolation and for shifting 5-V levels present on the HDMI connector to as low as 1.2-V levels on the GPU source side. The HV_DDC_SDA and HV_DDC_SCL pins support 5-V levels while the LV_DDC_SDA and LV_DDC_SCL pins support 1.2-V, 1.8-V, and 3.3-V levels. When the DDC buffer is used in source application, the HV side must be pulled up using 1.5-kΩ to 2-kΩ resistors. It is recommended to use 1.8-kΩ ±5% resistor. HV_DDC_SDA and HV_DDC_SCL pins will typically be pulled up to HDMI 5-V. The LV_DDC_SDA and LV_DDC_SCL are internally pulled up to VIO.

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The TDP1204 enables DDC translation from low voltage (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TDP1204 contains 2 bidirectional, open-drain buffers specifically designed to support up and down-translation between the low voltage (LV) side DDC-bus and the high voltage (HV) 5-V DDC-bus. The HV I/Os (HV_DDC_SCL and HV_DDC_SDA) are overvoltage tolerant to 5.5-V. After HPD_IN high, a LOW level on LV side (below VILC = 0.08 × VIO) turns the corresponding HV driver (either SDA or SCL) on and drives HV side down to V_{HVOL}. When LV side rises above approximately 0.10 × VIO, the HV pulldown driver is turned off and the internal pullup resistor pulls the pin HIGH. When HV side falls first and goes below 1.6-V, a CMOS hysteresis input buffer detects the falling edge, turns on the LV driver, and pulls LV down to approximately V_{LVOL} = 0.16 × VIO. The LV side pulldown is not enabled unless the LV voltage goes below VILC. If the LV side low voltage goes below VILC, the HV side pulldown driver is enabled until LV side rises above (VILC + ΔVT-HYST), then HV side, if not externally driven LOW, continues to rise being pulled up by the external pullup resistor.

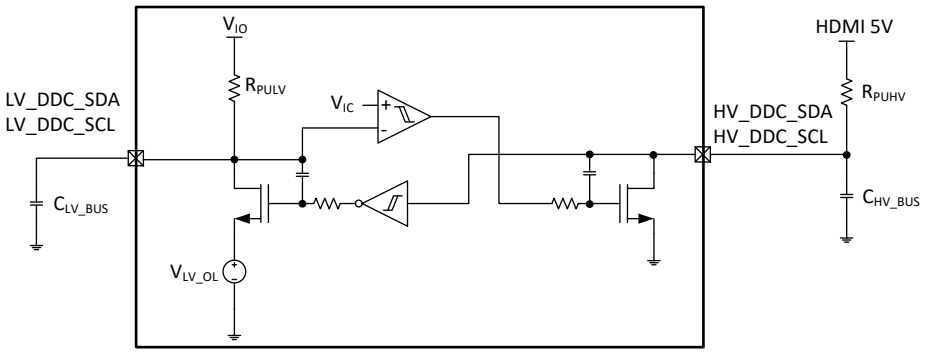


图 8-4. DDC Buffer Block Diagram

图 8-5 shows the connection of the LV and HV DDC pins when using the DDC buffer. This connection is supported in pin-strap mode when MODE pin is "0" or "1". In I2C mode, the DDCBUF_EN register must be set to enable the DDC Buffer.

备注

The TDP1204 has integrated pullups to VIO on the DDC LV pins. Therefore, no external pull-ups shall be present between the TDP1204's DDC LV pins and DDC host when using TDP1204's DDC buffer.

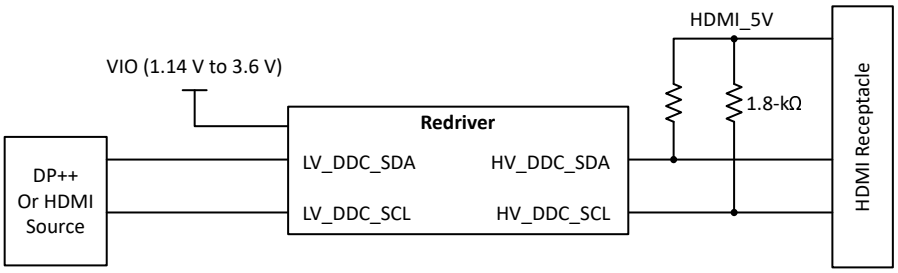


图 8-5. Source Application: DDC Buffer Enabled

图 8-6 shows an example source application of snooping from the HV DDC pins. In this example, the DDC buffer must be enabled and the LV DDC pins must be floating. This connection is supported in pin-strap mode when MODE pin is "0" or "1". In I2C mode, the DDCBUF_EN register must be set to enable the DDC Buffer.

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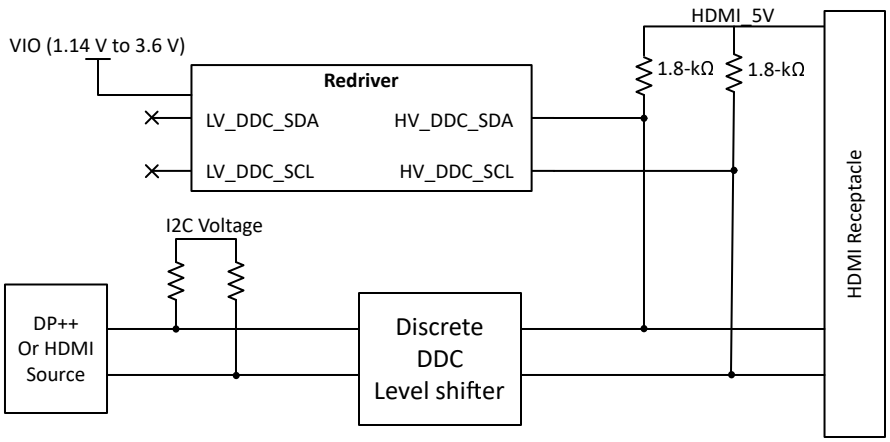


图 8-6. Source Application: DDC Buffer Enabled and Snoop from HV DDC pins

图 8-7 shows an example source application of snooping from the LV DDC pins. In this example, the DDC buffer must be disabled and the HV DDC pins must be floating. This connection is supported in pin-strap mode when MODE pin is "R". In I2C mode, the DDCBUF_EN register must be cleared to disable the DDC Buffer.

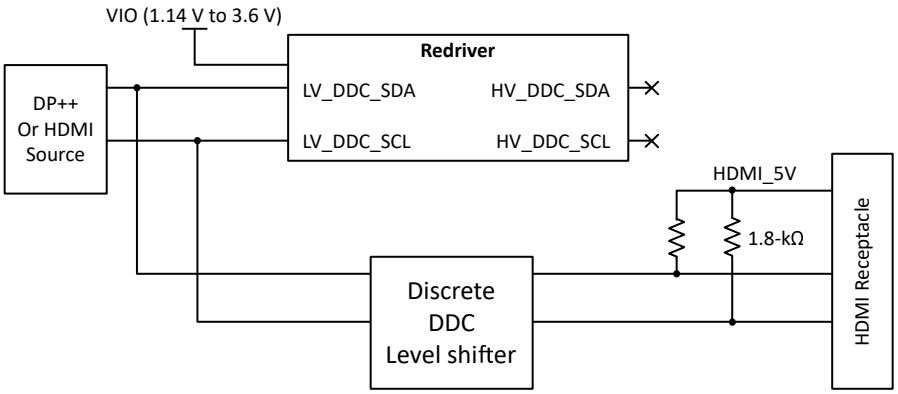


图 8-7. Source Application: DDC Buffer Disabled and Snoop from LV DDC pins

图 8-8 shows the connection of the LV and HV DDC pins when using the DDC buffer in a sink application. This connection is supported in pin-strap mode when MODE pin is "0" or "1". In I2C mode, the DDCBUF_EN register must be set to enable the DDC Buffer.

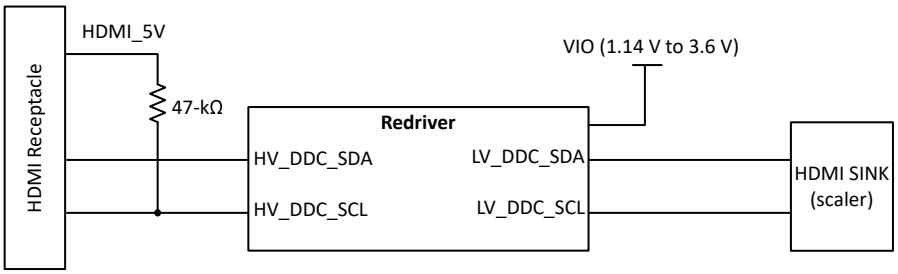


图 8-8. Sink Application: DDC Buffer Enabled

图 8-9 shows an example sink application of snooping from the LV DDC pins. In this example, the DDC buffer must be disabled and the HV DDC pins must be floating. This connection is supported in pin-strap mode when MODE pin is "R". In I2C mode, the DDCBUF_EN register must be cleared to disable the DDC Buffer.

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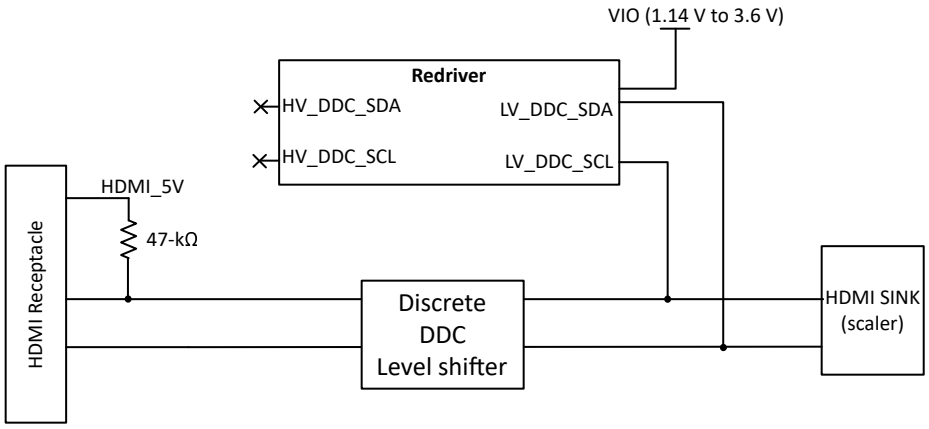


图 8-9. Sink Application: DDC Buffer Disabled and Snoop from LV DDC pins

图 8-10 shows an example sink application of snooping from the HV DDC pins. In this example, the DDC buffer must be enabled and the LV DDC pins must be floating. This connection is supported in pin-strap mode when MODE pin is "0" or "1". In I2C mode, the DDCBUF_EN register must be set to enable the DDC Buffer.

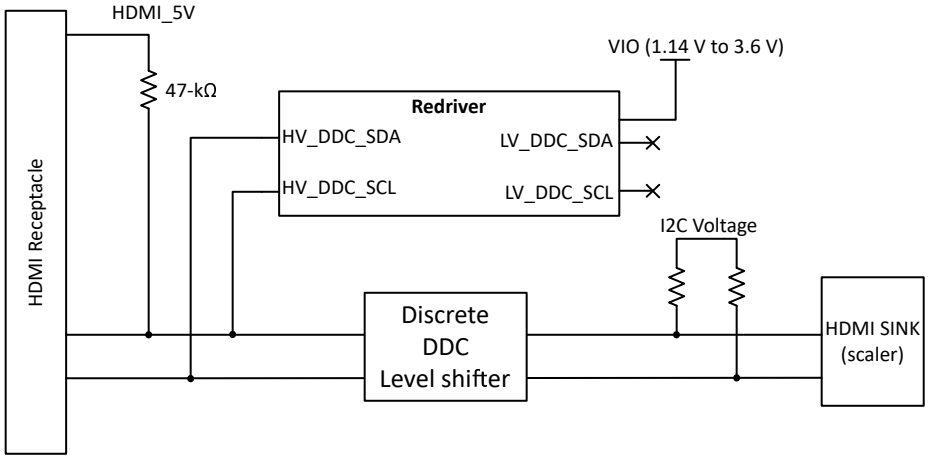


图 8-10. Sink Application: DDC Buffer Enable and Snoop from HV DDC pins

8.2.15 HDMI DDC Capacitance

The HDMI specification limits the DDC bus capacitance to ≤ 50-pF for both an HDMI source and sink. Therefore, care must be taken to make sure the total capacitance of all components (TDP1204, FR4 trace, ESD, source, and sink) is less than 50-pF.

The TDP1204s DDC Buffer offers capacitance isolation between the LV DDC pins and the HV DDC pin. The total capacitance of components, including the FR4 trace, between the TDP1204 HV_DDC_SDA/SCL pins and the HDMI receptacle must be ≤ (50-pF – C_{IOHV}).

If implementing a DDC level shifter using pass gates, then the total capacitance will include all components between source or sink and the HDMI receptacle. These components include and are not limited to Source or Sink, the FR4 trace, ESD components, and TDP1204.

备注

Trace capacitance can be in the range of 2 to 5-pF per inch. A general rule is a 50-Ω FR4 trace will be around 3.3-pF per inch.

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8.2.16 DisplayPort

The TDP1204 supports DisplayPort at datarates up to 8.1 Gbps (HBR3) when configured for either pin-strap and I²C mode. In pin-strap mode, DisplayPort mode is enabled as provided in 表 8-18. In I²C mode, DisplayPort mode is enabled when FRL_RATE field (offset 0x31) is programmed to 0x6, RATE_SNOOP_CTRL (offset 0xA bit 2) is disabled, and TXFFE_SNOOP_CTLE (offset 0xA bits 1:0) is disabled.

备注

The TDP1204 must be configured as a linear redriver when enabled for DisplayPort mode. The linear range should be programmed to highest level (Dx_VOD = 0x3 and CLK_VOD = 0x3). The TDP1204 TX termination must be set to 100-ohms (TERM = 0x3) and TX bias must be set to ac-coupled (TX_AC_EN = 0x1).

8.3 Device Functional Modes

8.3.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one I²C mode. In all three pin strap modes, DDC snooping feature is enabled. In I²C mode, DDC snoop feature is enabled by default but can be disabled by a register.

8.3.1.1 I²C Mode (MODE = "F")

In I²C mode, all settings of the TDP1204 can be controlled through the registers. The TDP1204 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in I²C mode since the functions exist in a register. The SCL/CFG0 pin will function as the I²C clock and the SDA/CFG1 pin will function as the I²C data.

The TDP1204 defaults to power down in I²C mode. Upon completion of initialization of the TDP1204, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TDP1204 supports 1.2-V, 1.8-V, and 3.3-V I²C signaling levels. Selection of 1.2-V, 1.8-V, or 3.3-V is determined by the VIO pin as provided in 表 8-2.

8.3.1.2 Pin Strap Modes

表 8-18 and 表 8-19 lists how the SCL/CFG0 and the SDA/CFG1 pins will be used to control the HDMI 1.4 termination, lane SWAP function, and the DisplayPort mode in pin-strap mode.

表 8-18. SCL/CFG0 Pin in Pin-Strap Mode

SCL/CFG0 Pin	AC_EN Pin	TDP1204 Function
0	0	HDMI 1.4 termination is open if HDMI clock frequency ⩽ f_{HDMI14_open}
0	0	HDMI 1.4 termination is ≅300-Ω if HDMI clock frequency ⩾ f_{HDMI14_300}
1	0	HDMI 1.4 termination is ≅300-Ω
0	1	Normal HDMI. Function determined by MODE pin.
1	1	DisplayPort mode. DDC snoop disabled. All four lanes enabled when HPD_IN is high. 12 Gbps CTLE used.

表 8-19. SDA/CFG1 Pin in Pin-Strap Mode

SDA/CFG1 Pin	TDP1204 Function
0	Normal Lane ordering
1	Lane Swap enabled

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备注

The SCL/CFG0 is the only two-level pin that is continuously sampled in pin-strap mode. AC_EN, HPDOUT_SEL, and SDA/CFG1 will not be continuously sampled in pin-strap mode unless indicated otherwise.

The TDP1204 must be configured as a linear redriver when operating in DisplayPort mode.

8.3.1.2.1 Pin-Strap: HDMI 1.4 and HDMI 2.0 Functional Description

The TDP1204 will always use the sampled state of EQ[1:0] pins when operating in either HDMI 1.4 and HDMI 2.0. The amount of EQ applied is determined by the CTLE Map used (for more information, refer to 节 8.2.8).

If TDP1204 is configured for limited redriver mode, then the OUT_D[2:0] and OUT_CLKP/N levels will be fixed based on the sampled state of TXSWG pin (表 8-17 provides more information) and TXPRE pin (表 8-15 provides more information).

If TDP1204 is configured for linear redriver mode, then OUT_D[2:0] and OUT_CLK will be a linear function of the input signals.

备注

In source application, it is recommended to use limited redriver mode for both HDMI 1.4 and HDMI 2.0.

8.3.1.2.2 Pin-Strap HDMI 2.1 Function (MODE = "0"): Fixed Rx EQ and DDC Buffer Enabled

This mode is recommended in a source applications in which the GPU is aware of the TDP1204 presence and keeps its transmitter levels (VOD, de-emphasis and pre-shoot) fixed during HDMI 2.1 FRL link training. In this mode, the TDP1204 will provide an HDMI compliant signal at the HDMI receptacle.

In this mode, the TDP1204 will operate with a fixed RX EQ based on the value set by EQ0 and EQ1 pins.

In HDMI 2.1 FRL with limited redriver enabled, OUT_D[2:0] and OUT_CLK outputs will change based on the snooped value of TXFFE levels. 表 8-16 lists the TXFFE level used for each snooped value.

In HDMI 2.1 FRL with linear redriver enabled, OUT_D[2:0] and OUT_CLK outputs will function as described in 节 8.2.6.

备注

Adaptive EQ is not supported in this mode. Link Training Compatible Rx EQ is not supported in this mode.

8.3.1.2.3 Pin-Strap HDMI 2.1 Function (MODE = "1"): Flexible RX EQ and DDC Buffer Enabled

This mode is recommended in a source applications in which the GPU is unaware of the TDP1204 presence and will adjust its transmitter levels (VOD, de-emphasis, and pre-shoot) during HDMI 2.1 FRL link training.

In this mode, the TDP1204 supports both 节 8.2.10 and 节 8.2.11.

If TDP1204 is configured for limited redriver mode, then the OUT_D[2:0] and OUT_CLKP/N VOD level will be fixed based on the sampled state of TXSWG (refer to 表 8-17). In HDMI 2.1 FRL, these outputs will change based on the snooped value of TXFFE levels. 表 8-11 lists the TXFFE level used for each snooped value.

In this mode with limited redriver enabled, it is highly that the recommended GPU use TXFFE levels listed in 表 8-10.

8.3.1.2.4 Pin-Strap HDMI 2.1 Function (MODE = "R"): Flexible Rx EQ and DDC Buffer Disabled

This pin strap mode is the same as MODE ="1" with the exception the DDC buffer is disabled.

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备注

This mode is intended to be used when external discrete DDC buffer or level shifter is used. HV_DDC_SDA and HV_DDC_SCL pins can be left floating in this mode.

8.3.2 DDC Snoop Feature

As part of discovery the source reads the sink E-EDID information to understand the sink’s capabilities. Part of this read is HDMI Forum Vendor Specific Data Block (HF-VSDB) located at target address 0xA8. From the LV_DDC_SDA and LV_DDC_SCL pins, the TDP1204 DDC snoop function will monitor both reads and writes to specific offsets of the Status and Control Data Channel Structure (SCDCS) located within the HF-VSDB. The following SCDCS offsets are monitored: Update Flags at offset 10h, TMDS Configuration at offset 20h, Sink Configuration at offset 31h, Source Test Configuration at offset 35h, and Status Flags located at offsets 41h and 42h. The DDC snoop function resides on the LV_DDC_SDA and LV_DDC_SCL pins.

The TDP1204 has similar SCDCS registers within its register space. Through TDP1204 local I^2C interface, external microprocessor can control TDP1204 to perform all the necessary functions required for each HDMI type.

8.3.2.1 HDMI Type

表 8-20 lists the TDP1204 monitors offsets 20h and 31h to determine HDMI type as either HDMI 1.4, HDMI 2.0, or HDMI 2.1 FRL.

表 8-20. HDMI Type Selection

HDMI Type	TMDS_CLK_RATIO SCDCS Offset 20h[1]	FRL_RATE SCDCS Offset 31h[3:0]
HDMI 1.4 (TMDS x10)	0	0h
HDMI 2.0 (TMDS x40)	1	0h
HDMI 2.1 FRL	X	Not 0h

备注

TDP1204 will default to HDMI 1.4 following a power-on reset or whenever it enters the power down state. Upon exiting standby, the TDP1204 will hold data rate value (HDMI 1.4, 2.0, or 2.1) prior to entering the standby.

8.3.2.2 HDMI 2.1 FRL Snoop

In HDMI 2.1 FRL mode, the TDP1204 monitors offset 31h, 35h, 41h, and 42h. Each offset contains information that the TDP1204 uses during FRL link training or during TX compliance testing.

Offset 31h contains FRL lane count (3 or 4 lanes), data rate (3, 6, 8, 10, or 12 Gbps), and maximum TXFFE levels supported. TDP1204 enables the appropriate number of lanes based on the lane count. The TDP1204 uses the data rate information to determine the duration of the TXFFE de-emphasis. The maximum number of supported TXFFE levels sets the number of TXFFE levels TDP1204 uses during FRL link training. 表 8-16 lists the TDP1204 does support all four possible TXFFE levels (TXFFE0 through TXFFE3).

Values snooped from offset 35h is used by TDP1204 during TX FFE compliance testing.

8.3.3 Low Power States

The TDP1204 has two low power states: Power Down and Standby. 表 8-21 lists both lower power states. Power down is entered when HPD_IN is low for $t_{HPD_PWRDOWN}$ or in I^2C if PD_EN bit is set. Power down is also entered when the EN pin is low. The TDP1204 will exit power down to the standby state when HPD_IN is high for $t_{HPD_STANDBY}$.

The TDP1204 implements a two stage standby power process when HPD_IN is high.

Stage 1: if there is no signal (electrical idle) on the IN_CLK lane, and if HDMI 1.4/2.0 or IN_D2 if HDMI 2.1, then the TDP1204 will enter Standby State within $t_{STANDBY_ENTRY}$.

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Stage 2: if a signal is detected which last longer than t_{SIGDET_DB}, then TDP1204 will declare a valid signal and exit standby within t_{STANDY_EXIT}.

- If a signal is detected, then the TDP1204 will go into normal active operation and signals present at IN_CLK and IN_D[2:0] inputs will be passed through to the OUT_CLK and OUT_D[2:0] outputs.
- If it is determined that no signal is present, then the TDP1204 will reenter stage 1.

The TDP1204 will exit standby state and immediately enter active state if LTP1, LTP2, LTP3, or LTP4 is snooped while monitoring status flags at SCDCS offset 41h or 42h.

The TDP1204 will exit normal operation and return to the standby state within $t_{STANDBY_ENTRY}$ anytime electrical idle is detected.

表 8-21. Power States

	INPUTS					STATUS					
EN pin	HPD_IN pin	STANDBY_DISABLE register	HPD_PWRDWN_DISABLE register	PD_EN register	HDMI 1.4/2.0: IN_CLK pin HDMI 2.1: IN_D2 pins	HPD_OUT pin	IN_Dx pins	SDA/SCL	OUT_Dx OUT_CLK	DDC	State
L	X	X	X	X	X	High-Z	High-Z	Disabled	High-Z	Disabled	Power Down State
H	L	X	0	0	X	L	High-Z	Active	High-Z	Disabled	Power Down State
H	X	X	X	1	X	L	High-Z	Active	High-Z	Disabled	Power Down State
H	H	1	X	0	X	HPD_IN	All RX Active	Active	TX Active	Active	Normal operation
H	X	1	1	0	X	H	All RX Active	Active	TX Active	Active	Normal operation
H	H	0	X	0	No signal	HPD_IN	HDMI 1.4/2.0: IN_CLK Active HDMI 2.1: IN_D2 Active	Active	High-Z	Active	Standby State (Squelch waiting)
H	H	0	X	0	Valid signal detected	HPD_IN	All RX Active	Active	TX Active	Active	Normal operation
H	X	0	1	0	No signal	H	HDMI 1.4/2.0: IN_CLK Active HDMI 2.1: IN_D2 Active	Active	High-Z	Active	Standby State (Squelch waiting)
H	X	0	1	0	Valid signal detected	H	All RX Active	Active	TX Active	Active	Normal operation

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8.4 Programming

8.4.1 Pseudocode Examples

These are examples of configuring TDP1204 when it is configured for I2C mode.

8.4.1.1 HDMI 2.1 Source Example with DDC Snoop and DDC Buffer Enabled

When using TDP1204's DDC buffer with snooping enabled, this example can be used. In this example, adaptive EQ for HDMI 2.1 is disabled.

This example will initialize the following:

- Limited redriver mode with DC-coupled output
- TX slew rate for each data rate
- CTLE used for each data rate
- Receiver EQ setting for each lane (clock, D0, D1, and D2)
- TX voltage swing for each lane (clock, D0, D1, and D2)
- TX pre-emphasis or de-emphasis for HDMI 1.4 and 2.0

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x00), // Rate snoop and TXFFE snoop enabled.
(0x0B, 0x23), // 3G and 6G slew rate control
(0x0C, 0x70), // HDMI clock and 8G10G12G tx slew rate control
(0x0D, 0x22), // Limited mode, DC-coupled TX, 0 dB DCG, Auto Term, disable CTLE bypass
(0x0E, 0x97), // HDMI14, 2.0 and 2.1 CTLE selection
(0x10, 0x03), // Enabled DDC DCC correction and DDC buffer
(0x12, 0x03), // Clock lane VOD and TXFFE
(0x13, 0x00), // Clock lane EQ.
(0x14, 0x03), // D0 lane VOD and TXFFE.
(0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
(0x16, 0x03), // D1 lane VOD and TXFFE.
(0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
(0x18, 0x03), // D2 lane VOD and TXFFE.
(0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
(0x09, 0x00), // Take out of PD state. Should be done after initialization is complete.
```

8.4.1.2 HDMI 2.1 Source Example with DDC Snoop Disabled and DDC Buffer Disabled

When using an external discrete DDC buffer with snooping disabled, this example can be used. In this example, adaptive EQ for HDMI 2.1 is disabled. Also, this example assumes the source only wants to support TXFFE0 level when operating in HDMI 2.1 FRL mode.

This example will initialize the following:

- Limited redriver mode with DC-coupled output
- TX slew rate for each data rate
- CTLE used for each data rate

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x05), // Rate snoop disabled and TXFFE controlled by 35h, 41h, and 42h
(0x0B, 0x23), // 3G and 6G tx slew rate control
(0x0C, 0x70), // HDMI clock and 8G10G12G TX slew rate control
(0x0E, 0x97), // HDMI 1.4, 2.0 and 2.1 CTLE selection
(0x11, 0x00), // Disable all four lanes.
(0x09, 0x00), // Take out of PD state. Should be done after initialization is complete.

// Selection between HDMI modes (1.4, 2.0, and 2.1)
switch (HDMI_MODE) {
    case 'HDMI14_165' : // HDMI 1.4 configuration for less than 1.65 Gbps
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x20), // Limited mode, DC-coupled TX, 0dB DCG, Term open, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
```


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```
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI14_340' : // HDMI 1.4 configuration for greater than 1.65 Gbps
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x21), // Limited mode, DC-coupled TX, 0dB DCG, Term 300, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI20' :  // HDMI 2.0 configuration
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x02), // Set TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_3G' : // HDMI 2.1 3 Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x01), // Set to 3G FRL. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_6G_3lane' : // HDMI 2.1 6 Gbps FRL 3 lanes
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x02), // Set to 6G FRL and 3 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_6G_4lane' : // HDMI 2.1 6 Gbps FRL 4 lanes
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set to "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
```

```
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x03), // Set to 6G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_8G' : //HDMI 2.1 8 Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x04), // Set to 8G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_10G' : //HDMI 2.1 10 Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x05), // Set to 10G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_12G' : //HDMI 2.1 12 Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0 dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x06), // Set to 12G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
}
```

8.4.2 TDP1204 I²C Address Options

For further programmability, the TDP1204 can be controlled using I²C. The SCL/CFG0 and SDA/CFG1 terminals are used for I²C clock and I²C data respectively.

表 8-22. TDP1204 I²C Device Address Description

ADDR/EQ0 pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

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8.4.3 I²C Target Behavior

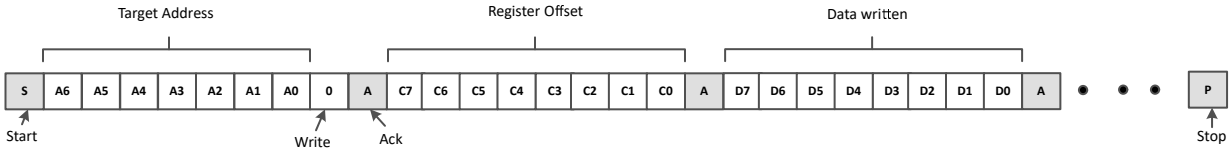


图 8-11. I²C Write with Data

The following procedure should be followed to write data to TDP1204 I²C registers (refer to 图 8-11):

1. The controller initiates a write operation by generating a start condition (S), followed by the TDP1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP1204 acknowledges the address cycle.
3. The controller presents the register offset within TDP1204 to be written, consisting of one byte of data, MSB-first.
4. The TDP1204 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I²C register.
6. The TDP1204 acknowledges the byte transfer.
7. The controller may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TDP1204.
8. The controller terminates the write operation by generating a stop condition (P).

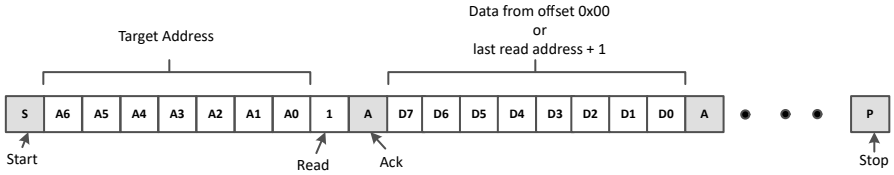


图 8-12. I2C Read Without Repeated Start

The following procedure should be followed to read the TDP1204 I²C registers without a repeated Start (refer to 图 8-12).

1. The controller initiates a read operation by generating a start condition (S), followed by the TDP1204 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TDP1204 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TDP1204 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TDP1204 shall start at the register offset specified in the write.
5. The TDP1204 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
6. If an ACK is received, then the TDP1204 transmits the next byte of data as long as controller provides the clock. If a NAK is received, then the TDP1204 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).

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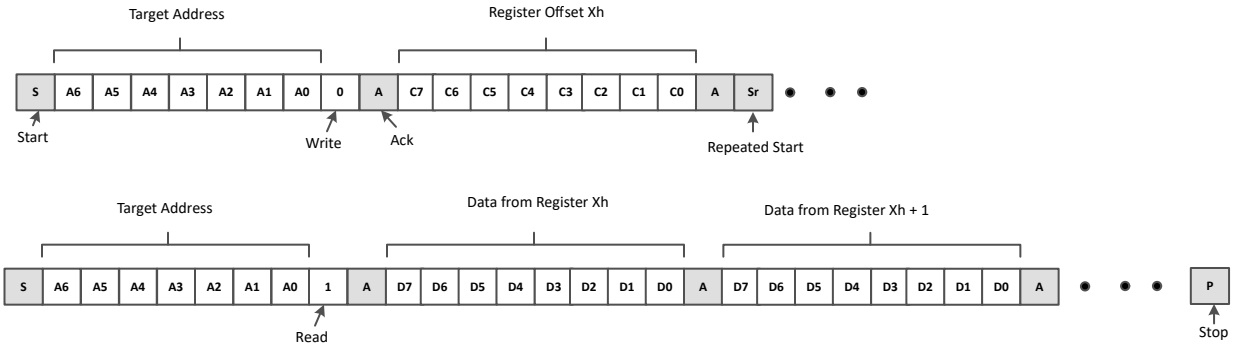


图 8-13. I2C Read with Repeated Start

The following procedure should be followed to read the TDP1204 I^{2}C registers with a repeated Start (refer to 图 8-13).

1. The controller initiates a read operation by generating a start condition (S), followed by the TDP1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP1204 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TDP1204 to be written, consisting of one byte of data, MSB-first.
4. The TDP1204 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TDP1204 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TDP1204 acknowledges the 7-bit address cycle.
8. The TDP1204 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TDP1204 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I^{2}C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, then the TDP1204 transmits the next byte of data as long as controller provides the clock. If a NAK is received, then the TDP1204 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).

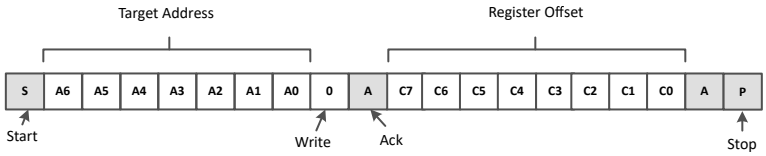


图 8-14. I2C Write Without Data

The following procedure should be followed for setting a starting sub-address for I^{2}C reads (refer to 图 8-14).

1. The controller initiates a write operation by generating a start condition (S), followed by the TDP1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP1204 acknowledges the address cycle.
3. The controller presents the register offset within TDP1204 to be written, consisting of one byte of data, MSB-first.
4. The TDP1204 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

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备注

图 8-12 that if no register offset is included for the read procedure after initial power-up, then reads start at register offset 00h and continue byte by byte through the registers until the I2C controller terminates the read operation. During a read operation, the TDP1204 auto-increments the I^2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C controller.

8.5 Register Maps

8.5.1 TDP1204 Registers

表 8-23 lists the memory-mapped registers for the TDP1204 registers. All register offset addresses not listed in 表 8-23 should be considered as reserved locations and the register contents should not be modified.

表 8-23. TDP1204 Registers

Offset	Acronym	Register Name	Section
8h	REV_ID	Revision ID	Go
9h	PD_RST	Power Down and Reset control	Go
Ah	MISC_CONTROL	Misc Control	Go
Bh	GBL_SLEW_CTRL	Global TX Slew control for data lanes in HDMI1.4 and 2.0	Go
Ch	GBL_SLEW_CTRL2	Global TX Slew control for data and clock	Go
Dh	GBL_CTRL1	Global control	Go
Eh	GBL_CTLE_CTRL	Global CTLE control	Go
10h	DDC_CFG	DDC Buffer controls	Go
11h	LANE_ENABLE	Lane enables	Go
12h	CLK_CONFIG1	CLK lane TX swing and FFE control	Go
13h	CLK_CONFIG2	CLK lane RX EQ control	Go
14h	D0_CONFIG1	D0 lane TX swing and FFE control	Go
15h	D0_CONFIG2	D0 lane RX EQ control	Go
16h	D1_CONFIG1	D1 lane TX swing and FFE control	Go
17h	D1_CONFIG2	D1 lane RX EQ control	Go
18h	D2_CONFIG1	D2 lane TX swing and FFE control	Go
19h	D2_CONFIG2	D2 lane RX EQ control	Go
1Ah	SIGDET_TH_CFG	SIGDET voltage threshold control	Go
1Ch	GBL_STATUS	Global Powerdown and Standby Status	Go
1Dh	AEQ_CONTROL1	Adaptive EQ control1	Go
1Eh	AEQ_CONTROL2	Adaptive EQ control2	Go
20h	SCDC_TMDS_CONFIG	SCDC TMDS Clock Ratio	Go
31h	SCDC_SINK_CONFIG	SCDC SNK FRL FFE and Rate	Go
35h	SCDC_SRC_TEST	SCDC Test	Go
41h	SCDC_STATUS10	Lanes 0 and 1 FRL Training Status	Go
42h	SCDC_STATUS32	Lanes 2 and 3 FRL Training Status	Go
50h	AEQ_STATUS	Adaptive EQ Status	Go
51h	AEQ_STATUS2	Adaptive EQ Status	Go

Complex bit access types are encoded to fit into small table cells. 表 8-24 shows the codes that are used for access types in this section.

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表 8-24. TDP1204 Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WtoP	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.1.1 REV_ID Register (Offset = 8h) [Reset = 03h]

REV_ID is shown in 表 8-25.

Return to the Summary Table.

表 8-25. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REV_ID	RH	3h	Device revision.

8.5.1.2 PD_RST Register (Offset = 9h) [Reset = 01h]

PD_RST is shown in 表 8-26.

Return to the Summary Table.

表 8-26. PD_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RST	HWtoP	0h	Writing a 1 to this field resets all fields
6	SCDC_SOFT_RST	HWtoP	0h	Writing a 1 to this field resets the fields in the SCDC registers 20h, 31h, 35h, 41h and 42h.
5	RESERVED	R	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R	0h	Reserved
2	HPD_PWRDWN_DISABLE	R/W	0h	Mode to ignore HPD pin and always enter active state unless PD_EN is high 0h = Automatically enter power down based on HPD_IN 1h = Always remain in active state or Standby
1	STANDBY_DISABLE	R/W	0h	When high, Standby state is disabled and the device will immediately enter active mode with all lanes enabled when not in power down. When low, the device will enter Standby state when exiting power down and wait for incoming data before entering active mode. 0h = Standby state enabled 1h = Standby state disabled

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表 8-26. PD_RST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PD_EN	R/W	1h	I2C power down. Software should clear this field after it has completed initialization. HPD_OUT will be asserted low when this field is set. 0h = Normal operation 1h = Forced power down by I2C

8.5.1.3 MISC_CONTROL Register (Offset = Ah) [Reset = 08h]

MISC_CONTROL is shown in 表 8-27.

Return to the Summary Table.

表 8-27. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LANE_SWAP	R/W	0h	This field swaps the input and output lanes. 0h = No lanes swapped 1h = Both input and output lanes swapped
6	RESERVED	R/W	0h	Reserved
5	RX_TERM_DISABLE	R/W	0h	When set will disable Rx termination. 0h = Enabled when HPD_IN high. 1h = Disable
4	HPD_OUT_SEL	R/W	0h	Selects whether HPD_OUT is push/pull or open-drain. 0h = Push Pull 1h = Open Drain
3	EQ_SNOOP_CTRL	R/W	1h	Control whether Rx EQ is adjusted in response to snooped TXFFE when TXFFE snooping is enabled through registers 41h and 42h. 0h = Rx EQ automatically adjusted for TXFFE 1h = Rx EQ is fixed
2	RATE_SNOOP_CTRL	R/W	0h	Control snooping of HDMI rates. When snooping is disabled, correct HDMI rate must be written through I2C to registers 20h and 31h. 0h = Snooping enabled 1h = Snooping disabled
1-0	TXFFE_SNOOP_CTRL	R/W	0h	Control snooping of TXFFE 0h = DDC snooping through registers 35h, 41h and 42h 1h = DDC snooping disabled. TXFFE controlled through I2C writes to 35h, 41h and 42h 2h = DDC snooping disabled. TXFFE controlled through writes to CLK_TXFFE, D0_TXFFE, D1_TXFFE, and D2_TXFFE 3h = DDC snooping disabled. TXFFE controlled through writes to CLK_TXFFE, D0_TXFFE, D1_TXFFE, and D2_TXFFE

8.5.1.4 GBL_SLEW_CTRL Register (Offset = Bh) [Reset = 34h]

GBL_SLEW_CTRL is shown in 表 8-28.

Return to the Summary Table.

表 8-28. GBL_SLEW_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	SLEW_3G	R/W	3h	Field controls slew rate for HDMI 1.4 data lane and HDMI 2.1 3 Gbps FRL data lanes. 0h = slowest edge rate 7h = fastest edge rate
3	RESERVED	R	0h	Reserved

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表 8-28. GBL_SLEW_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SLEW_6G	R/W	4h	Field controls slew rate for HDMI 2.0 data lanes and HDMI 2.1 6 Gbps FRL data lanes. 0h = slowest edge rate 7h = fastest edge rate

8.5.1.5 GBL_SLEW_CTRL2 Register (Offset = Ch) [Reset = 71h]

GBL_SLEW_CTRL2 is shown in 表 8-29.

Return to the Summary Table.

表 8-29. GBL_SLEW_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	SLEW_8G10G12G	R/W	7h	Field controls slew rate for data lanes for 8 Gbps, 10 Gbps and 12 Gbps FRL datarates 0h = slowest edge rate 7h = fastest edge rate
3	RESERVED	R	0h	Reserved
2-0	SLEW_CLK	R/W	1h	Field control slew rate of clock lane in HDMI 1.4b and HDMI 2.0 modes. 0h = slowest edge rate 7h = fastest edge rate

8.5.1.6 GBL_CTRL1 Register (Offset = Dh) [Reset = 22h]

GBL_CTRL1 is shown in 表 8-30.

Return to the Summary Table.

表 8-30. GBL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL_LINR_EN	R/W	0h	Global control for selecting between linear redriver or limited redriver. 0h = Limited 1h = Linear
6	TX_AC_EN	R/W	0h	Controls selection of ac-coupled or dc-coupled TX termination. When AC-coupled is enabled, 50 Ω termination on both P and N to VCC will be enabled. 0h = dc-coupled 1h = ac-coupled
5-4	GLOBAL_DCG	R/W	2h	CTLE DCGain for all lane. 0h = −3 dB 1h = −3 dB 2h = 0 dB 3h = +1 dB
3	TXTERM_AUTO_HDMI14	R/W	0h	Selects between no termination and 300 Ωs when TERM = 2h and operating in HDMI1.4. 0h = No termination for clock less than or equal to 165 MHz and 300 Ω for clock greater than 225 MHz 1h = 300 Ω
2	CTLEBYP_EN	R/W	0h	Selects whether or not CTLE bypass is enabled or not when GLOBAL_DCG is set to 2h and EQ set to 0h. 0h = CTLE bypass disabled 1h = CTLE bypass enabled

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表 8-30. GBL_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	TERM	R/W	2h	TX termination control 0h = No termination 1h = 300 Ω 2h = Automatic based HDMI mode 3h = 100 Ω

8.5.1.7 GBL_CTLE_CTRL Register (Offset = Eh) [Reset = 3Fh]

GBL_CTLE_CTRL is shown in 表 8-31.

Return to the Summary Table.

表 8-31. GBL_CTLE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GLOBAL_CTLEBW	R/W	0h	CTLE bandwidth control. 0 is lowest and 3h is highest.
5-4	HDMI14_CTLE_SEL	R/W	3h	Selects the CTLE used when datarate is HDMI 1.4. Value programmed into this field will apply to data lanes only. Clock lane will always use 3 Gbps CTLE. 0h = 3 Gbps CTLE 1h = 6 Gbps CTLE 2h = Auto select based on snoop datarate 3h = 12 Gbps CTLE
3-2	HDMI20_CTLE_SEL	R/W	3h	Selects the CTLE used when datarate is HDMI 2.0. Value programmed into this field will apply to data lanes only. Clock lane will always use 3 Gbps CTLE. 0h = 3 Gbps CTLE 1h = 6 Gbps CTLE 2h = Auto select based on snoop datarate 3h = 12 Gbps CTLE
1-0	HDMI21_CTLE_SEL	R/W	3h	Selects the CTLE used when datarate is HDMI 2.1. Value programmed into this field will apply to all four lanes. 0h = 3 Gbps CTLE 1h = 6 Gbps CTLE 2h = Auto select based on snoop datarate 3h = 12 Gbps CTLE

8.5.1.8 DDC_CFG Register (Offset = 10h) [Reset = 02h]

DDC_CFG is shown in 表 8-32.

Return to the Summary Table.

表 8-32. DDC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	DDC_LV_DCC_EN	R/W	1h	Controls whether duty cycle correction is enabled for DDC LV side. 0h = DCC disabled 1h = DCC enabled
0	DDCBUF_EN	R/W	0h	Controls whether or not DDC buffer is enabled. Regardless of the state of this field, the device will always disable the DDC buffer anytime HPD_IN is low or when PD_EN field is 1. 0h = DDC Buffer Disabled 1h = DDC Buffer Enabled

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8.5.1.9 LANE_ENABLE Register (Offset = 11h) [Reset = 5Fh]

LANE_ENABLE is shown in 表 8-33.

Return to the Summary Table.

表 8-33. LANE_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HDMI20_VOD	R/W	1h	VOD control for limited redriver in HDMI 2.0 0h = Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD 1h = Default (1000 mV) 2h = Default − 5% 3h = Default + 5%
5-4	HDMI14_VOD	R/W	1h	VOD control for limited redriver in HDMI 1.4 0h = Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD 1h = Default (1000 mV) 2h = Default − 5% 3h = Default − 10%
3	CLK_LANE_EN	R/W	1h	Enable for CLK lane 0h = Disabled 1h = Enabled
2	D0_LANE_EN	R/W	1h	Enable for D0 lane 0h = Disabled 1h = Enabled
1	D1_LANE_EN	R/W	1h	Enable for D0 lane 0h = Disabled 1h = Enabled
0	D2_LANE_EN	R/W	1h	Enable for D0 lane 0h = Disabled 1h = Enabled

8.5.1.10 CLK_CONFIG1 Register (Offset = 12h) [Reset = 03h]

CLK_CONFIG1 is shown in 表 8-34.

Return to the Summary Table.

表 8-34. CLK_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	CLK_TXFFE	R/W	0h	TXFFE control for CLK lane. This field is only honored in HDMI 2.1. 0h = 0.0 dB 1h = 3.5 dB 2h = 6.0 dB 3h = Reserved 4h = −1.5 dB 5h = −2.5 dB 6h = −3.5 dB 7h = −4.8 dB
3	RESERVED	R	0h	Reserved
2-0	CLK_VOD	R/W	3h	Differential Swing control for CLK lane. 0h = Limited −15% Linear 800 mV 1h = Limited −10% Linear 900 mV 2h = Limited − 5% Linear 1000 mV 3h = Limited 800 mV Linear 1200 mV 4h = Limited +5% Linear Reserved 5h = Limited +10% Linear Reserved 6h = Limited +15% Linear Reserved 7h = Limited +20% Linear Reserved

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8.5.1.11 CLK_CONFIG2 Register (Offset = 13h) [Reset = 00h]

CLK_CONFIG2 is shown in 表 8-35.

Return to the Summary Table.

表 8-35. CLK_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	CLK_EQ	R/W	0h	EQ control for CLK lane. This field is only honored in HDMI 2.1. 0h = Min EQ Fh = Max EQ

8.5.1.12 D0_CONFIG1 Register (Offset = 14h) [Reset = 03h]

D0_CONFIG1 is shown in 表 8-36.

Return to the Summary Table.

表 8-36. D0_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	D0_TXFFE	R/W	0h	TXFFE control for D0 lane. 0h = 0.0 dB 1h = 3.5 dB 2h = 6.0 dB 3h = Reserved 4h = −1.5 dB 5h = −2.5 dB 6h = −3.5 dB 7h = −4.8 dB
3	RESERVED	R	0h	Reserved
2-0	D0_VOD	R/W	3h	Differential Swing control for D0 lane. 0h = Limited −15% Linear 800 mV 1h = Limited −10% Linear 900 mV 2h = Limited - 5% Linear 1000 mV 3h = Limited 1000 mV Linear 1200 mV 4h = Limited +5% Linear Reserved 5h = Limited +10% Linear Reserved 6h = Limited +15% Linear Reserved 7h = Limited +20% Linear Reserved

8.5.1.13 D0_CONFIG2 Register (Offset = 15h) [Reset = 00h]

D0_CONFIG2 is shown in 表 8-37.

Return to the Summary Table.

表 8-37. D0_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	D0_EQ	R/W	0h	EQ control for D0 lane. 0h = Min EQ Fh = Max EQ

8.5.1.14 D1_CONFIG1 Register (Offset = 16h) [Reset = 03h]

D1_CONFIG1 is shown in 表 8-38.

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Return to the Summary Table.

表 8-38. D1_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	D1_TXFFE	R/W	0h	TXFFE control for D1 lane. 0h = 0.0 dB 1h = 3.5 dB 2h = 6.0 dB 3h = Reserved 4h = −1.5 dB 5h = −2.5 dB 6h = −3.5 dB 7h = −4.8 dB
3	RESERVED	R	0h	Reserved
2-0	D1_VOD	R/W	3h	Differential Swing control for D1 lane. 0h = Limited −15% Linear 800 mV 1h = Limited −10% Linear 900 mV 2h = Limited − 5% Linear 1000 mV 3h = Limited 1000 mV Linear 1200 mV 4h = Limited +5% Linear Reserved 5h = Limited +10% Linear Reserved 6h = Limited +15% Linear Reserved 7h = Limited +20% Linear Reserved

8.5.1.15 D1_CONFIG2 Register (Offset = 17h) [Reset = 00h]

D1_CONFIG2 is shown in 表 8-39.

Return to the Summary Table.

表 8-39. D1_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	D1_EQ	R/W	0h	EQ control for D1 lane 0h = Min EQ Fh = Max EQ

8.5.1.16 D2_CONFIG1 Register (Offset = 18h) [Reset = 03h]

D2_CONFIG1 is shown in 表 8-40.

Return to the Summary Table.

表 8-40. D2_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	D2_TXFFE	R/W	0h	TXFFE control for D2 lane 0h = 0.0 dB 1h = 3.5 dB 2h = 6.0 dB 3h = Reserved 4h = −1.5 dB 5h = −2.5 dB 6h = −3.5 dB 7h = −4.8 dB
3	RESERVED	R	0h	Reserved

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表 8-40. D2_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	D2_VOD	R/W	3h	Differential Swing control for D2 lane. 0h = Limited −15% Linear 800 mV 1h = Limited -10% Linear 900 mV 2h = Limited - 5% Linear 1000 mV 3h = Limited 1000 mV Linear 1200 mV 4h = Limited +5% Linear Reserved 5h = Limited +10% Linear Reserved 6h = Limited +15% Linear Reserved 7h = Limited +20% Linear Reserved

8.5.1.17 D2_CONFIG2 Register (Offset = 19h) [Reset = 00h]

D2_CONFIG2 is shown in 表 8-41.

Return to the Summary Table.

表 8-41. D2_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	D2_EQ	R/W	0h	EQ control for D2 lane. 0h = Min EQ Fh = Max EQ

8.5.1.18 SIGDET_TH_CFG Register (Offset = 1Ah) [Reset = 44h]

SIGDET_TH_CFG is shown in 表 8-42.

Return to the Summary Table.

表 8-42. SIGDET_TH_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	CFG_SIGDET_HYST	R/W	4h	Controls the SIGDET hysteresis. Value programmed into this field plus value programmed into CFG_SIGDET_VTH field defines the SIGDET assert threshold. 0h = 0 mV 1h = 12 mV 2h = 25 mV 3h = 37 mV 4h = 55 mV 5h = 63 mV 6h = 75 mV 7h = 90 mV
3	RESERVED	R	0h	Reserved
2-0	CFG_SIGDET_VTH	R/W	4h	Controls the SIGDET de-assert voltage threshold. 0h = 58 mV 1h = 60 mV 2h = 72 mV 3h = 84 mV 4h = 95 mV 5h = 108 mV 6h = 120 mV 7h = 135 mV

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8.5.1.19 GBL_STATUS Register (Offset = 1Ch) [Reset = 00h]

GBL_STATUS is shown in 表 8-43.

Return to the Summary Table.

表 8-43. GBL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PD_STATUS	RH	0h	Power Down status
6	STANDBY_STATUS	RH	0h	Standby Status
5-0	RESERVED	R	0h	Reserved

8.5.1.20 AEQ_CONTROL1 Register (Offset = 1Dh) [Reset = F3h]

AEQ_CONTROL1 is shown in 表 8-44.

Return to the Summary Table.

表 8-44. AEQ_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FULLAEQ_UPPER_EQ	R/W	Fh	Maximum EQ value to check for full AEQ mode
3-2	AEQ_PATTERN_CTRL	R/W	0h	Control how link training pattern snooping for EQ adaptation 0h = Require a read of pattern register 41h/42h after a rate change. Allow eq adaptation for patterns 0, 5, 6, 7, and 8. 1h = Require a read of pattern register 41h/42h after a rate change. Allow eq adaptation for patterns 5, 6, 7, and 8. 2h = Allow eq adaptation for patterns 0, 5, 6, 7, and 8. No need for read after rate change 3h = Allow eq adaptation for patterns 5, 6, 7, and 8. No need for read after rate change.
1	AEQ_START_CTRL	R/W	1h	Control whether starts based on signal detect or both signal detect and FLT_UPDATE cleared 0h = Only require signal detect 1h = Require signal detect and clearing of FLT_UPDATE
0	AEQ_TX_DELAY_EN	R/W	1h	Control whether TX remains disabled during EQ adaptation 0h = TX active during adaptation 1h = TX disabled during adaptation

8.5.1.21 AEQ_CONTROL2 Register (Offset = 1Eh) [Reset = 00h]

AEQ_CONTROL2 is shown in 表 8-45.

Return to the Summary Table.

表 8-45. AEQ_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AEQ_MODE	R/W	0h	Selects between two Adaption modes 0h = AEQ with hits counted at mideye for every EQ. 1h = AEQ with hits counted at mideye only for EQ equal 0.
6	AEQ_EN	R/W	0h	Controls whether or not adaptive EQ is enabled. 0h = AEQ disabled 1h = AEQ enabled
5-4	RESERVED	R/W	0h	Reserved
3	OVER_EQ_SIGN	R/W	0h	Selects the sign for OVER_EQ_CTRL field. 0h = positive 1h = negative

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表 8-45. AEQ_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	OVER_EQ_CTRL	R/W	0h	This field will increase or decrease the AEQ by value programmed into this field. For example, full AEQ value is 6 and this field is programmed to 2 and OVER_EQ_SIGN = 0, then EQ value used will be 8. This field is only used in Full AEQ mode. 0h = 0 or −8 1h = 1 or −7 2h = 2 or −6 3h = 3 or −5 4h = 4 or −4 5h = 5 or −3 6h = 6 or −2 7h = 7 or −1

8.5.1.22 SCDC_TMDS_CONFIG Register (Offset = 20h) [Reset = 00h]

SCDC_TMDS_CONFIG is shown in 表 8-46.

Return to the Summary Table.

表 8-46. SCDC_TMDS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	TMDS_CLK_RATIO	RH/W	0h	TMDS Bit Period to TMDS Clock Period Ratio. Reads last value snooped through DDC read/write or I2C write. 0h = 1/10 (HDMI 1.4b) 1h = 1/40 (HDMI 2.0)
0	RESERVED	R	0h	Reserved

8.5.1.23 SCDC_SINK_CONFIG Register (Offset = 31h) [Reset = 00h]

SCDC_SINK_CONFIG is shown in 表 8-47.

Return to the Summary Table.

表 8-47. SCDC_SINK_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FFE_LEVELS	RH/W	0h	Indicates the maximum TXFFE level supported for the current FRL rate. Read last value snooped through DDC read/write or I2C write. 0h = Only TXFFE0 supported 1h = TXFFE0-1 supported 2h = TXFFE0-2 supported 3h = TXFFE0-3 supported
3-0	FRL_RATE	RH/W	0h	Selects FRL rate and lane count. Read last value snooped through DDC read/write or I2C write. 0h = Disable FRL 1h = 3 Gbps on 3 lanes 2h = 6 Gbps on 3 lanes 3h = 6 Gbps on 4 lanes 4h = 8 Gbps on 4 lanes 5h = 10 Gbps on 4 lanes 6h = 12 Gbps on 4 lanes

8.5.1.24 SCDC_SRC_TEST Register (Offset = 35h) [Reset = 00h]

SCDC_SRC_TEST is shown in 表 8-48.

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Return to the Summary Table.

表 8-48. SCDC_SRC_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLT_NO_TIMEOUT	RH/W	0h	Set by sink test equipment to have source not time out during FRL link training 0h = Normal operation 1h = Source does not timeout
4	RESERVED	R	0h	Reserved
3	TX_NO_FFE	RH/W	0h	Test mode to disable FFE. Read last value snooped through DDC read/write or I2C write. 0h = Normal TXFFE 1h = TX sent with no FFE
2	TX_DEEMPH_ONLY	RH/W	0h	Test mode to enable de-emphasis only. Read last value snooped through DDC read/write or I2C write. 0h = Normal TXFFE 1h = TX sent de-emphasis only
1	TX_PRESHOOT_ONLY	RH/W	0h	Test mode to enable pre-shoot only. Read last value snooped through DDC read/write or I2C write. 0h = Normal TXFFE 1h = TX sent with pre-shoot only
0	RESERVED	R	0h	Reserved

8.5.1.25 SCDC_STATUS10 Register (Offset = 41h) [Reset = 00h]

SCDC_STATUS10 is shown in 表 8-49.

Return to the Summary Table.

表 8-49. SCDC_STATUS10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LN1_LTP_REQ	RH/W	0h	Link training pattern request for lane 1. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0.
3-0	LN0_LTP_REQ	RH/W	0h	Link training pattern request for lane 0. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0.

8.5.1.26 SCDC_STATUS32 Register (Offset = 42h) [Reset = 00h]

SCDC_STATUS32 is shown in 表 8-50.

Return to the Summary Table.

表 8-50. SCDC_STATUS32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LN3_LTP_REQ	RH/W	0h	Link training pattern request for lane 3. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0.

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表 8-50. SCDC_STATUS32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	LN2_LTP_REQ	RH/W	0h	Link training pattern request for lane 2. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0.

8.5.1.27 AEQ_STATUS Register (Offset = 50h) [Reset = 80h]

AEQ_STATUS is shown in 表 8-51.

Return to the Summary Table.

表 8-51. AEQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AEQDONE_STAT	RH	1h	This field is low while AEQ is active and high when it is done. It is valid when FRL training and AEQ_EN = 1 or when FORCE_AEQ_EN = 1 and HW has reset FORCE_AEQ back to 0. 0h = AEQ is running 1h = AEQ is done
6	AEQ_HC_OVERFLOW	RH	0h	13-bit AEQ hit counter overflow status
5	RESERVED	R	0h	Reserved
4	RXD1_DONE_STAT	RH	0h	This flag is set after DAC wait timer expires.
3-0	RXD1_AEQ_STAT	RH	0h	Optimal EQ determined by FSM after the completion of Full AEQ. This field will include the value programmed into OVER_EQ_CTRL field.

8.5.1.28 AEQ_STATUS2 Register (Offset = 51h) [Reset = 00h]

AEQ_STATUS2 is shown in 表 8-52.

Return to the Summary Table.

表 8-52. AEQ_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	VOD_RANGE_STAT	RH	0h	VOD range selected by the last AEQ run
3-0	AEQ_EYE_STAT	RH	0h	EYE status from the last AEQ run. Relative to the maximum limit of 15.

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

TDP1204 is designed to accept AC or DC-coupled HDMI input signals. The device provides signal conditioning and level shifting functions to drive a compliant HDMI source connector. The device can be used in an HDMI sink application such as monitor or TV. The TDP1204 can also be used as an DP/HDMI redriver in an embedded application. In many major PC or gaming systems APU/GPU will provide AC-coupled HDMI signals. TDP1204 is suitable for such platforms.

9.1 Application Information

The TDP1204 is designed to work in source applications such as Blu-ray™ DVD player, gaming system, desktops, notebooks, or audio video receivers (AVR) and in sink applications such as TV or monitors. The following sections provide design considerations for various types of applications.

9.2 Typical Source-Side Application

图 9-1 shows a schematic representation of what is considered a standard source implementation.

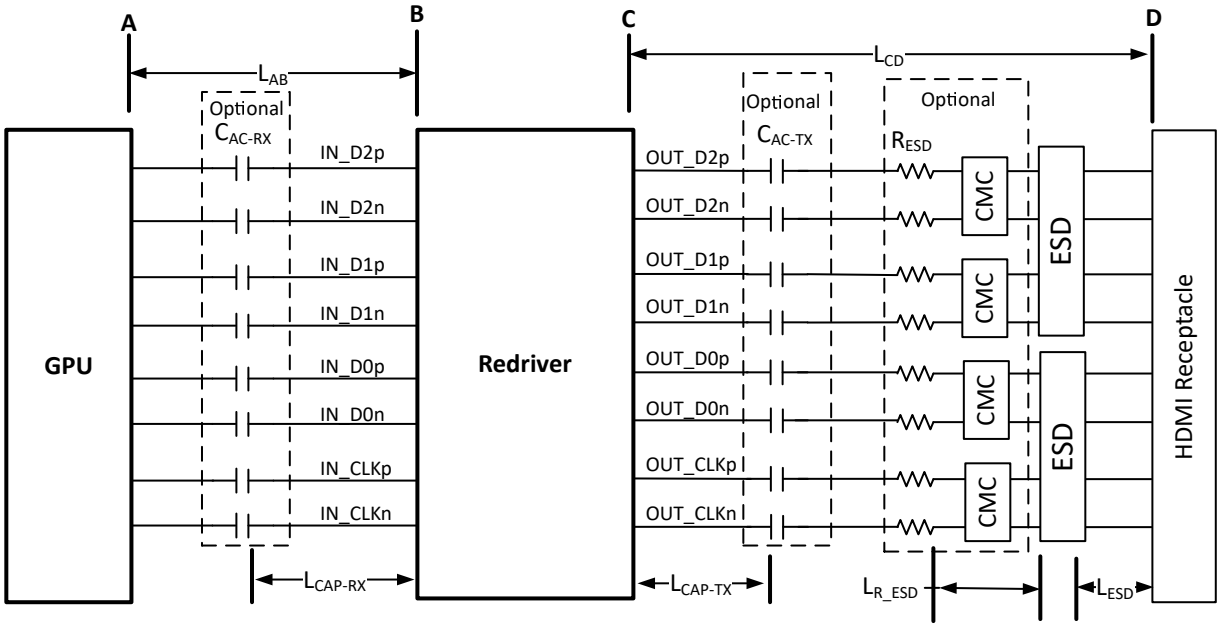


图 9-1. TDP1204 in Source Side Application

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9.2.1 Design Requirements

The TDP1204 can be designed into many different applications. In all the applications there are certain requirements for the system to work properly. The EN pin must have a 0.1-µF capacitor to ground. The processor can drive the EN pin, but the EN pin needs to change states (low to high) after the voltage rails have stabilized. Using I^2C is the best way to configure the device, but pin strapping is also provided as I^2C and is not available in all cases. As sources may have many different naming conventions, it is necessary to confirm that the link between the source and the TDP1204 are correctly mapped. A Swap function is provided for the input pins in case signaling is reversed between the source and receptacle. 表 9-1 lists information on expected values to perform properly.

For this design example, the TDP1204 is assumed to be configured for pin-strap mode. If I2C mode is desired, the MODE pin should be set to "F" and software must configure TDP1204. For how to configure TDP1204, refer to 节 8.4.1.

表 9-1. Design Parameters

Design Parameter	Value
V_{CC}	3.3-V
V_{IO} (1.2-V, 1.8-V, or 3.3-V LVCMOS levels)	1.8-V
Maximum HDMI 2.1 FRL Datarate (3, 6, 8, 10, or 12-Gbps)	12-Gbps
Pin-strap or I2C mode (if I2C, then MODE = "F").	Pin-strap
Pin Strap Mode.(MODE = "0", "R" or "1").	Mode = "0" (Fixed EQ with DDC Buffer support)
DDC Snoop Feature. (Y/N). Required when in pin strap. Optional in I2C mode.	Yes
SWAP function (Y / N). In pin strap mode controlled by SDA/CFG1 pin.	No. SDA/CFG1 pin = L.
DDC Level Shifter Support (Y / N)	Yes
HPD_IN to HPD_OUT Level Shifter Support (Y / N)	Yes, HPD_OUT is used. If no, then HPD_OUT can be left floating.
Pre-Channel Length (表 9-2 provides the length restrictions)	Length = 8 inches (≅ 7.2-dB at 6-GHz insertion loss)
Post-Channel Length (表 9-2 provides the length restrictions)	Length = 2 inches (≅ 1.8-dB at 6-GHz insertion loss)
Limited or linear redriver mode?	Limited redriver (LINEAR_EN pin = "0").
TX is DC or AC-coupled to HDMI receptacle?	DC-coupled. AC_EN pin = Low.
GPU Launch Voltage (500 mV to 1200 mV) if using limited redriver mode. If using linear redriver mode, then refer to the GPU requirements listed in 表 8-4.	500-mV
GPU HDMI 2.1 pre-shoot and de-emphasis levels used if using redriver in limited mode	If MODE = "0" or "R", GPU's TX FFE pre-shoot and de-emphasis levels shall be set to 0-dB for all four TXFFE levels If MODE = "1", then GPU TXFFE pre-shoot and de-emphasis levels shall meet the requirements listed in 表 8-4.
CTLE HDMI Datarate Map (Map A, Map B, or Map C)	Map C
RX EQ (16 possible values. Value chosen based on pre-channel length).	EQ1 pin: "R" ADDR/EQ0 pin: "R" (7.5-dB)
TX Pre-emphasis. In pre-strap mode controlled by TXPRE pin.	Default 0-dB of pre-emphasis. Float TXPRE pin.
TX Swing. In pre-strap mode controlled by TXSWG pin.	Default TX swing level. Float TXSWG pin.

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表 9-2. Source Layout and Component Placement Constraints

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{ESD}	External series resistor between ESD component and TDP1204		0		2.5	Ω
L_{AB} (1) (2)	PCB trace length from GPU to TDP1204	At 12-Gbps	1		10	inches
$L_{INTRA-AB}$	Intra-pair skew from GPU to TDP1204				5	mil
L_{CD} (1)	PCB trace length from TDP1204 to receptacle	At 12-Gbps	0.75		2	inches
$L_{INTRA-CD}$	Intra-pair skew from TDP1204 to receptacle				5	mil
L_{CAP-RX}	PCB trace length from TDP1204 to optional external C_{AC-RX} capacitor		0.3			inches
L_{CAP-TX}	PCB trace length from TDP1204 to optional external C_{AC-TX} capacitor		0.3			inches
L_{ESD}	PCB trace length from ESD component to receptacle				0.5	inches
L_{R_ESD}	PCB trace length from R_{ESD} to ESD component				0.25	inches
$L_{INTER-PAIR}$ (3)	Inter-pair skew between all four channels (D0, D1, D2, and CLK)				1	inches
IL_{PCB}	PCB trace insertion loss		0.1		0.17	dB / inch / GHz
Z_{PCB_AB}	Differential impedance of L_{AB}		75		110	Ω
Z_{PCB_CD}	Differential impedance of L_{CD}		90		110	Ω
VIA_{AB}	Number of vias between GPU and TDP1204				2	VIA
VIA_{CD}	Number of vias between HDMI connector and TDP1204				1	VIA
XTALK	Differential crosstalk between adjacent differential pairs on PCB.	≦ 3 GHz			−24	dB

(1) Maximum distance assumes PCB trace insertion loss meets IL_{PCB} requirement. If PCB trace insertion loss exceeds the maximum limit, then distance needs be reduced.
(2) Minimum distance assumes PCB trace insertion loss meets IL_{PCB} requirement. If PCB trace insertion loss is less than the minimum limit, then distance needs to be increased.
(3) Calculation of channel length is the sum of L_{AB} and L_{CD}.

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9.2.2 Detailed Design Procedure

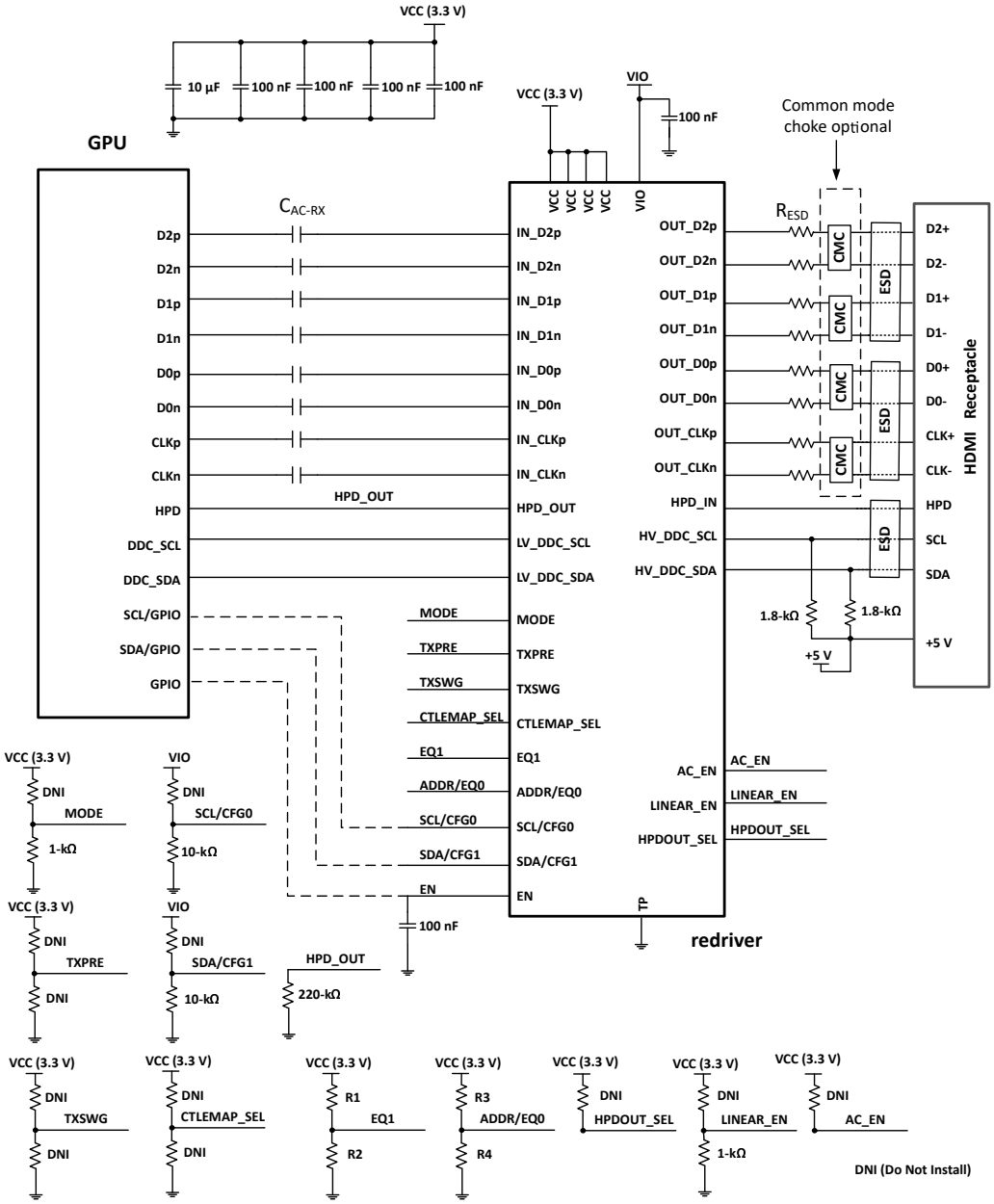


图 9-2. TDP1204 in Source Application Schematics

9.2.2.1 Pre-Channel (L_{AB})

The TDP1204 can support up to 12-dB at 6-GHz of insertion loss. The loss profile between the GPU and the TDP1204 input (referred to the pre-channel as shown in 图 9-1) should be less than the TDP1204 maximum receiver equalization. 图 9-3 shows the loss profile of FR4 trace at different lengths. The TDP1204 EQ0 and EQ1 pins should be configured to match the pre-channel insertion loss. 表 8-6 lists the EQ0 and EQ1 configuration options.

The GPU transmitter differential output voltage swing must be large enough so that the TDP1204's $V_{ID(DC)}$ and $V_{ID(EYE)}$ requirements are met. The $V_{ID(EYE)}$ is the eye height after the contribution of ISI jitter only. Because a redriver can only compensate for ISI jitter, all non-ISI sources of jitter (random, sinusoidal, and so forth) will be passed through TDP1204. If the system designer requires the worse case channel length of 10 inches, then the GPU transmitter differential voltage swing without de-emphasis should be at least 1000 mVpp to meet the $V_{ID(DC)}$ and $V_{ID(EYE)}$ requirements of the TDP1204. A GPU transmitter, which incorporates de-emphasis, can meet the requirement with less than 1000 mVpp.

9.2.2.2 Post-Channel (L_{CD})

图 9-1 shows the post-channel, which should be 2 inches or less. If ESD devices are used, then it may be necessary to overcome the insertion loss of the ESD device by increasing the TDP1204 transmitter voltage swing. 表 8-17 lists how this is done by configuring the TXSWG pin to the appropriate value.

If post-channel is greater than 2 inches, then transmitter pre-emphasis may need to be employed. 表 8-15 lists how this is done by configuring the TDP1204 TXPRE pin to the appropriate setting. Adjusting the TDP1204 transmitter voltage swing may also be necessary.

9.2.2.3 Common Mode Choke

It may be necessary to incorporate a common mode choke (CMC) to reduce EMI. The purpose of a CMC is to have a minimal impact to the differential signal while attenuating common mode noise thereby reducing radiated emissions. The CMC should be placed between the TDP1204 and the ESD device.

表 9-3. Recommended Common Mode Chokes

Manufacturer	Part Number
Murata	DLM0QSB120HY2
Murata	DLM0NSB120HY2
Murata	NFG0QHB542HS2

9.2.2.4 ESD Protection

It may be necessary to incorporate an ESD component to protect the TDP1204 from electrostatic discharge (ESD). It is recommended that the ESD protection component has a breakdown voltage of ≥4.5 V and a clamp voltage of ≤4.3 V. A clamp voltage greater than 4.3 V will require a R_{ESD} on each high-speed differential pin. The ESD component should be placed near the HDMI connector.

表 9-4. Recommended ESD Protection Component

Manufacturer	Part Number
NXP	PUSB3FR4

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9.2.3 Application Curves

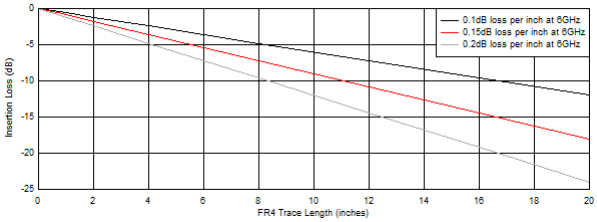


图 9-3. FR4 Trace Insertion Loss at 6 GHz

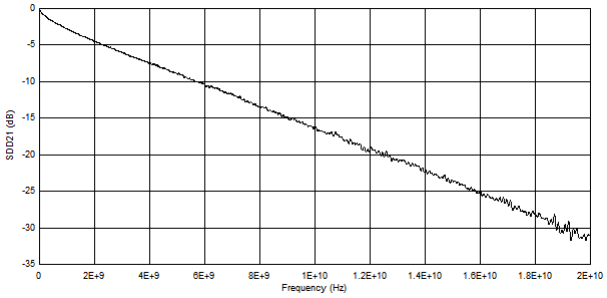


图 9-4. Pre-Channel Insertion Loss at TTP2

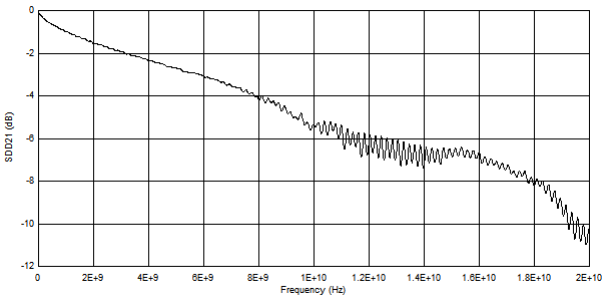


图 9-5. Post-Channel Insertion Loss at TTP4

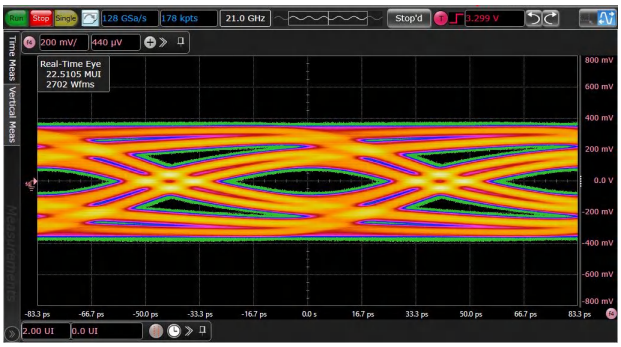


图 9-6. 12 Gbps Input Eye at TTP2 After Pre-channel

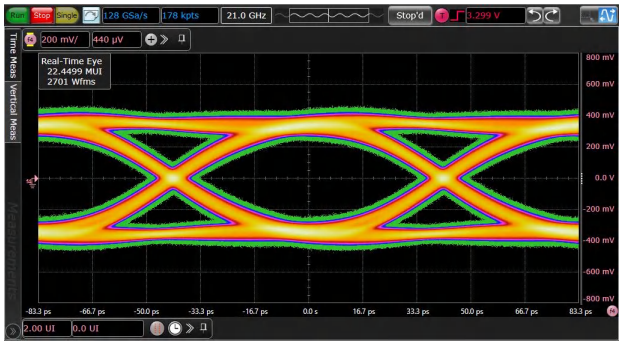


图 9-7. 12 Gbps Output Eye at TTP4 After Pre and Post Channels

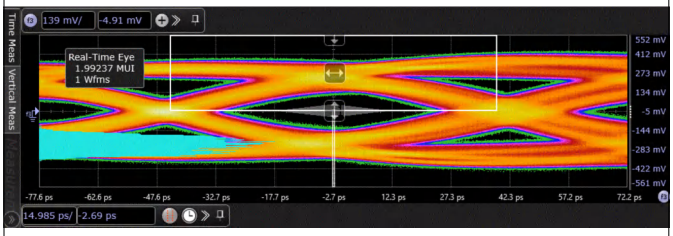


图 9-8. 12 Gbps Output Eye at TTP4_EQ After Pre and Post Channels

9.3 Typical Sink-Side Application

图 9-9 shows a schematic representation of what is considered a standard sink implementation.

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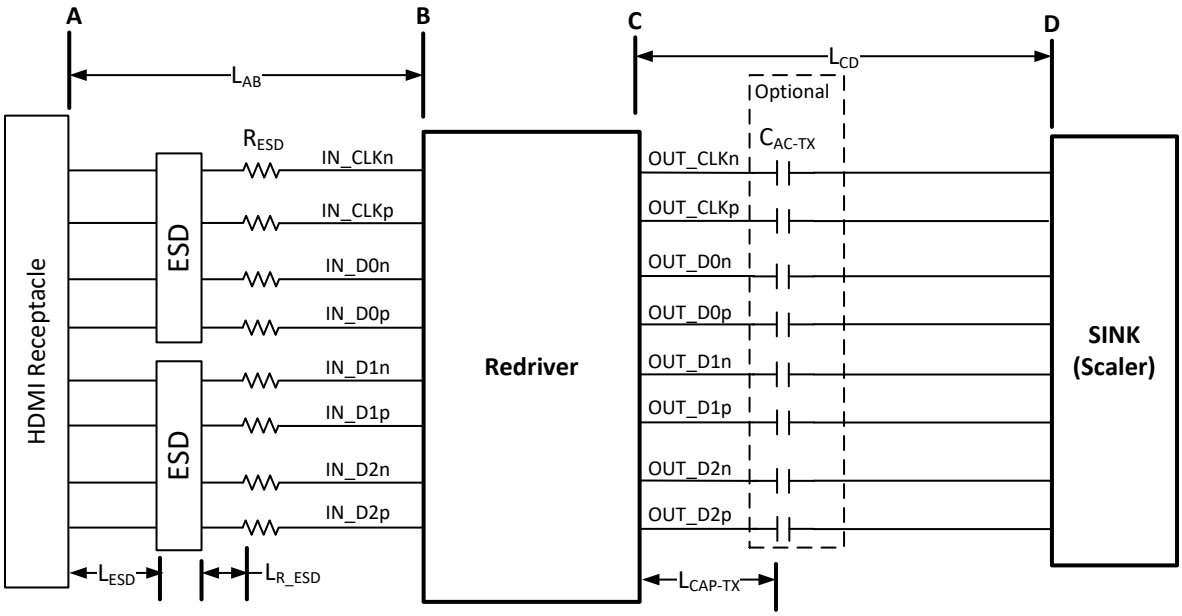


图 9-9. TDP1204 in Sink Side Application

9.3.1 Design Requirements

表 9-5. Design Parameters

Design Parameter	Value
V_{CC}	3.3-V (±5%)
V_{IO} (1.2-V, 1.8-V, or 3.3-V LVCMOS levels)	1.8-V
Maximum HDMI 2.1 FRL Datarate (6, 8, 10, or 12-Gbps)	12-Gbps
Pin-strap or I2C mode (if I2C, then MODE = "F").	Pin-strap
Pin Strap Mode.(MODE = "0", "R" or "1").	Mode = "1" (Adaptive EQ with DDC Buffer support)
DDC Snoop Feature. (Y/N). Required when in pin strap. Optional in I2C mode.	Yes
SWAP function (Y / N). In pin strap mode controlled by SDA/CFG1 pin.	Yes. SDA/CFG1 pin = H.
DDC Level Shifter Support (Y / N)	Yes
HPD_IN to HPD_OUT Level Shifter Support (Y / N)	No, then HPD_OUT can be left floating.
Pre-Channel Length (表 9-6 lists the length restrictions)	Length = 1 inches; Width = 4 mil. (≅ 1-dB at 6-GHz insertion loss)
Post-Channel Length (表 9-6 lists the length restrictions)	Length = 6 inches; Width = 4 mil (≅ 6-dB at 6-GHz insertion loss)
Limited or linear redriver mode?	Linear redriver (LINEAR_EN pin = "F") recommended in sink application
TX is DC or AC-coupled to HDMI receptacle?	AC-coupled. AC_EN pin = High.
RX EQ (16 possible values. Value chosen based on pre-channel length).	EQ1 pin: "0" ADDR/EQ0 pin: "1" (2.7-dB)
CTLE Map (Map A, Map B or Map C). In pre-strap controlled by CTLEMAP_SEL pin.	For Sink application recommend Map B or C.
TX pre-emphasis. In pre-strap mode controlled by TXPRE pin. TX pre-emphasis control not supported in linear redriver mode.	Float TXPRE pin.
TX Swing. In pre-strap mode controlled by TXSWG pin.	Default TX swing level. Float TXSWG pin.

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表 9-6. Sink Layout and Component Placement Constraints

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{ESD}	External series resistor between ESD component and TDP1204		0		2.5	Ω
L_{AB} (1) (2)	PCB trace length from receptacle to TDP1204		0.75		2	inches
$L_{INTRA-AB}$	Intra-pair skew from receptacle to TDP1204				2	mil
L_{CD} (1)	PCB trace length from TDP1204 to sink		1		6	inches
$L_{INTRA-CD}$	Intra-pair skew from TDP1204 to sink				2	mil
L_{CAP-TX}	PCB trace length from TDP1204 to external C_{AC-TX} capacitor		0.3			inches
L_{ESD}	PCB trace length from ESD component to receptacle				0.5	inches
L_{R_ESD}	PCB trace length from R_{ESD} to ESD component				0.25	inches
$L_{INTER-PAIR}$ (3)	Inter-pair skew between all four channels (D0, D1, D2, and CLK)				0.10	inches
IL_{PCB}	PCB trace insertion loss		0.1		0.17	dB / inch / GHz
Z_{PCB_AB}	Differential impedance of L_{AB}		90		110	Ω
Z_{PCB_CD}	Differential impedance of L_{CD}		90		110	Ω
VIA_{AB}	Number of vias between receptacle and TDP1204				1	VIA
VIA_{CD}	Number of vias between sink and TDP1204				2	VIA
XTALK	Differential crosstalk between adjacent differential pairs on PCB.	≦ 3-GHz			−24	dB

(1) Maximum distance assumes PCB trace insertion loss meets IL_{PCB} requirement. If PCB trace insertion loss exceeds the maximum limit, then distance needs to be reduced.
(2) Minimum distance assumes PCB trace insertion loss meets IL_{PCB} requirement. If PCB trace insertion loss is less than the minimum limit, then distance needs to be increased.
(3) Calculation of channel length is the sum of L_{AB} and L_{CD}.

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9.3.2 Detailed Design Procedures

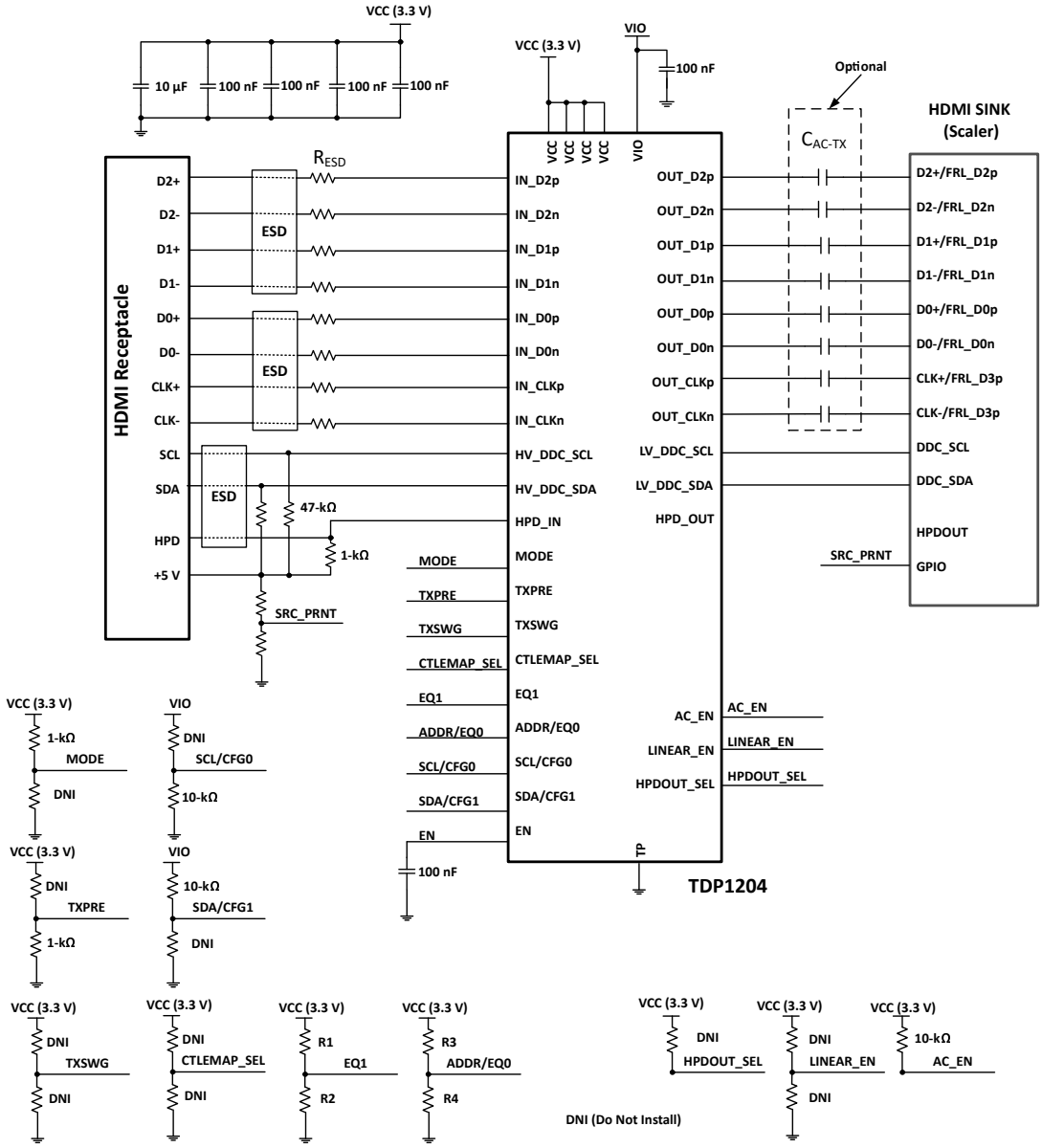


图 9-10. TDP1204 in Sink Application Schematics

9.4 Power Supply Recommendations

9.4.1 Supply Decoupling

Texas Instruments recommends a single bulk capacitor of 10-µF on the V_{CC} supply. Along with the bulk capacitor, Texas Instruments recommends a 0.1-µF decoupling capacitor on each TDP1204 V_{CC} pin that is placed as close to the V_{CC} pin as possible. 图 9-2 shows an example.

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9.5 Layout

9.5.1 Layout Guidelines

For the TDP1204 on a high-K board, it is required to solder the PowerPAD™ onto the thermal land to ground. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the TDP1204 can operate over the full temperature range by soldering the PowerPAD onto the thermal land. For the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\theta JA}$ = 30.9°C/W allowing 950-mW power dissipation at 70°C ambient temperature. For information about a general PCB design guide for PowerPAD packages, refer to the *PowerPAD Thermally Enhanced Package* application report. TI recommends using a four layer stack up at a minimum to accomplish a low-EMI PCB design. TI recommends four layers as the TDP1204 is a single voltage rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the HDMI connectors to the Redriver inputs and outputs. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed single layer establishes controlled impedance for transmission link interconnects and provides an excellent low-inductance path for the return current flow.
- Placing a power plane next to the ground plane creates an additional high-frequency bypass capacitance.
- Routing slower seed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high frequency bypass capacitance significantly.
- To minimize crosstalk between adjacent differential pairs, the distance between the differential pairs should be at least five times longer than the trace width (5W rule). For the clock differential pair, the distance should be increased to 8W or 10W.

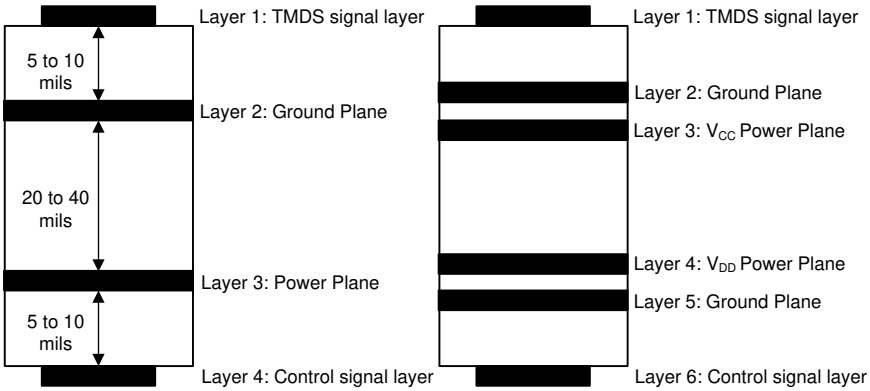


图 9-11. Recommended 4 or 6-Layer PCB Stack

9.5.2 Layout Example

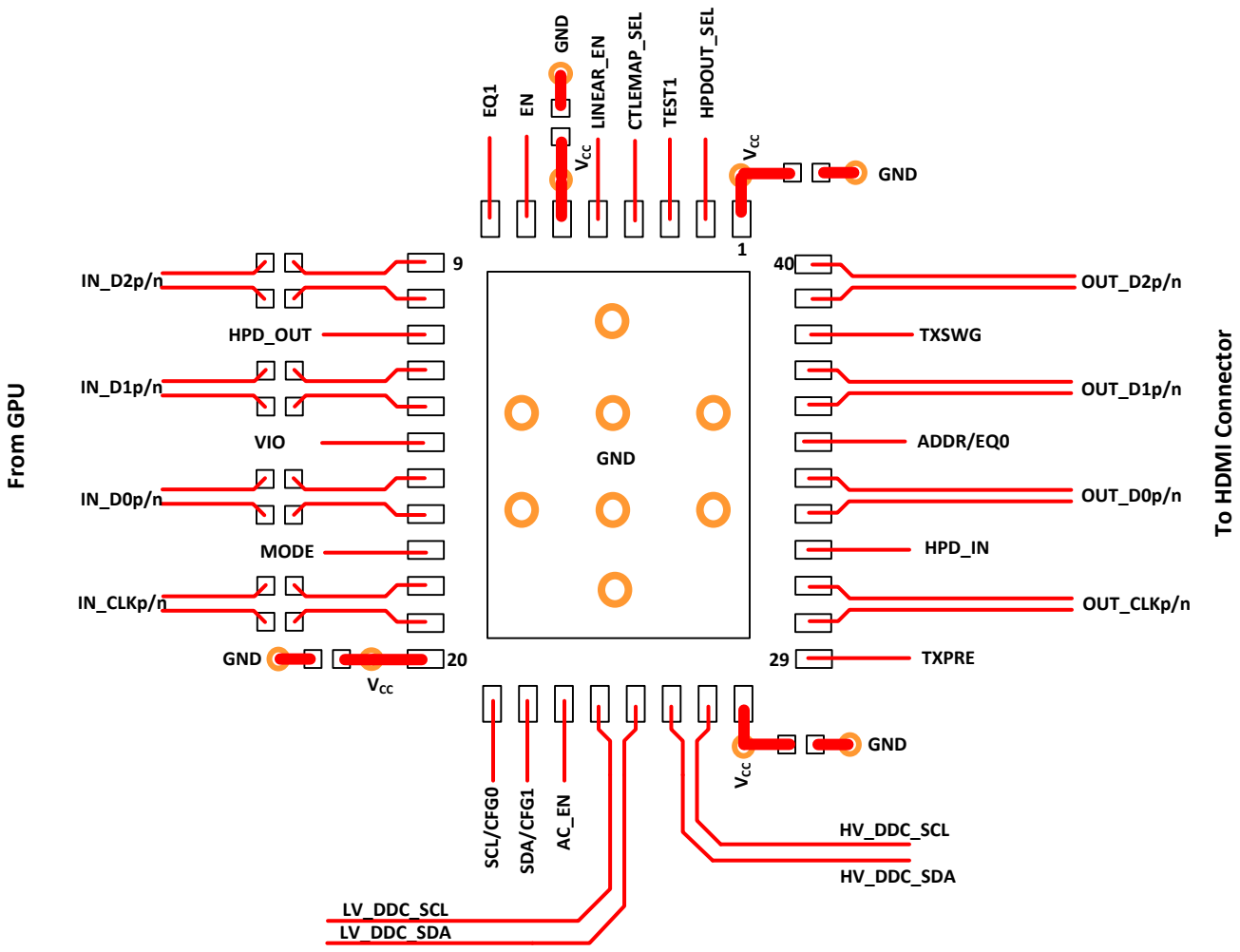


图 9-12. Source Example Layout

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10 器件和文档支持

10.1 文档支持

10.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*PowerPAD 热增强型封装* 应用报告

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
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10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDP1204IRNQR	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP04
TDP1204IRNQR.B	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP04
TDP1204IRNQT	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP04
TDP1204IRNQT.B	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP04
TDP1204RNQR	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP04
TDP1204RNQR.B	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP04
TDP1204RNQT	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP04
TDP1204RNQT.B	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP04

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

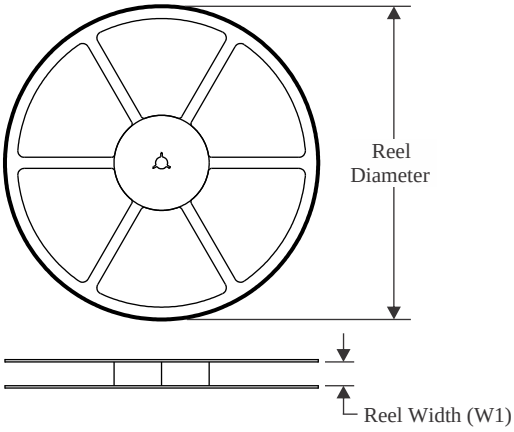
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

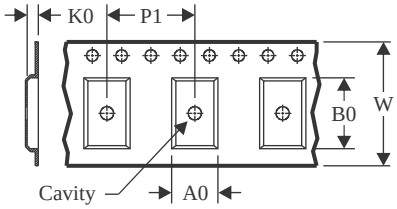
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

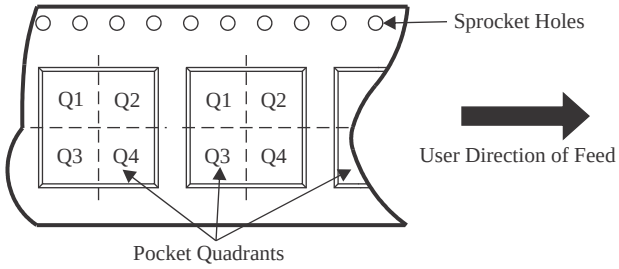


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

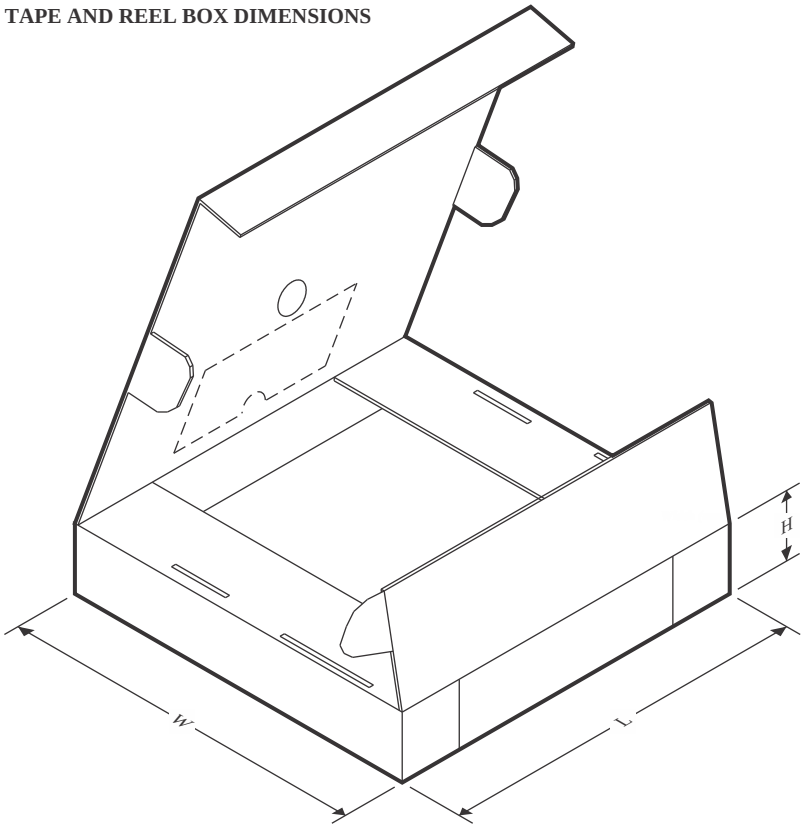
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDP1204IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP1204IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP1204RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP1204RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

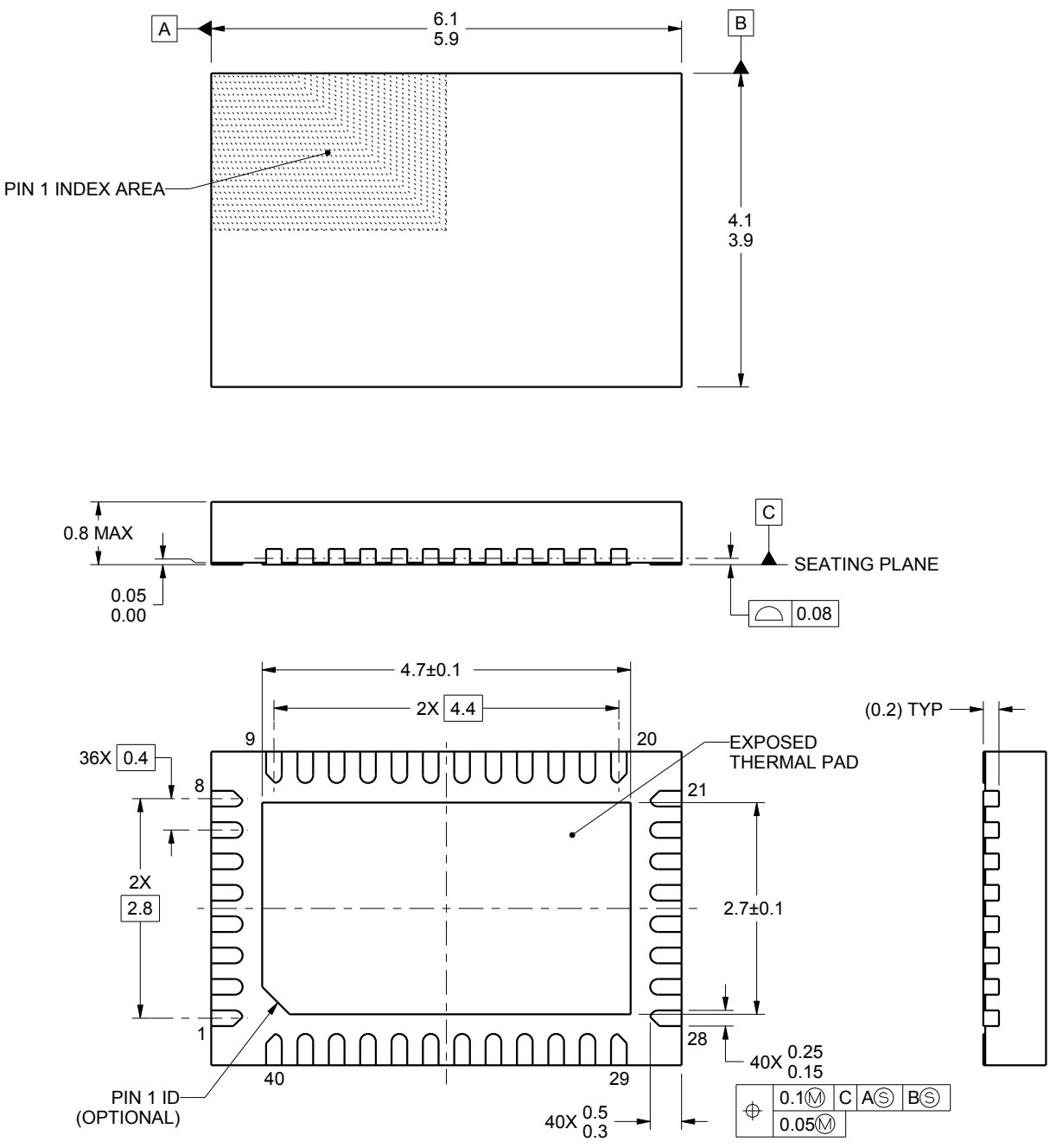
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDP1204IRNQR	WQFN	RNQ	40	3000	360.0	360.0	36.0
TDP1204IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0
TDP1204RNQR	WQFN	RNQ	40	3000	360.0	360.0	36.0
TDP1204RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

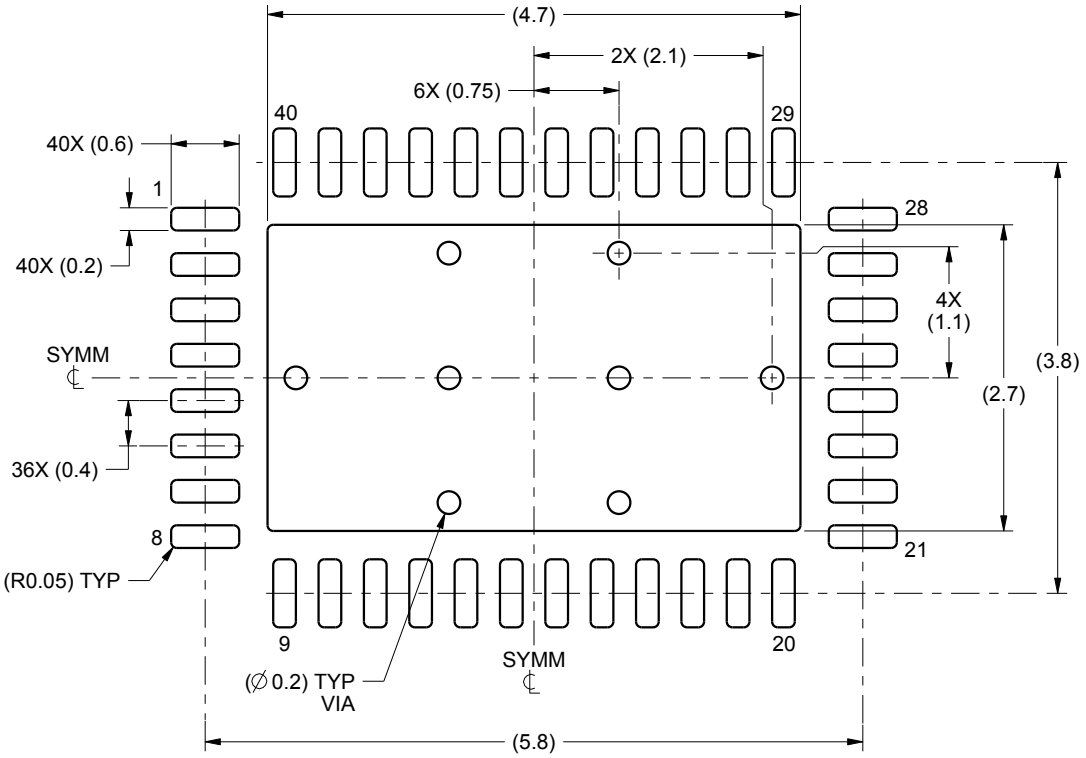
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

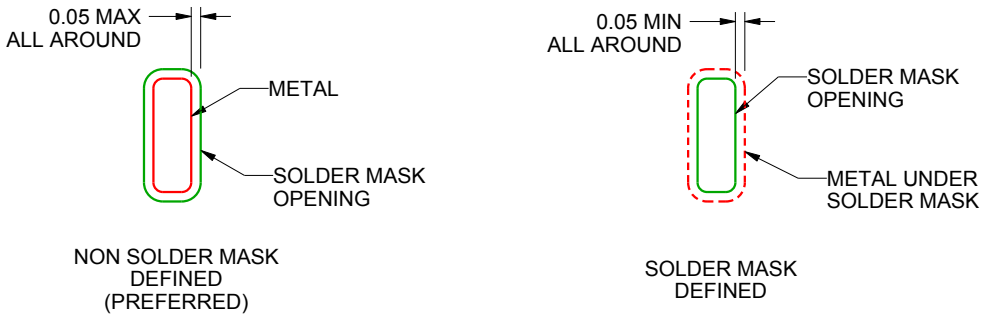


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

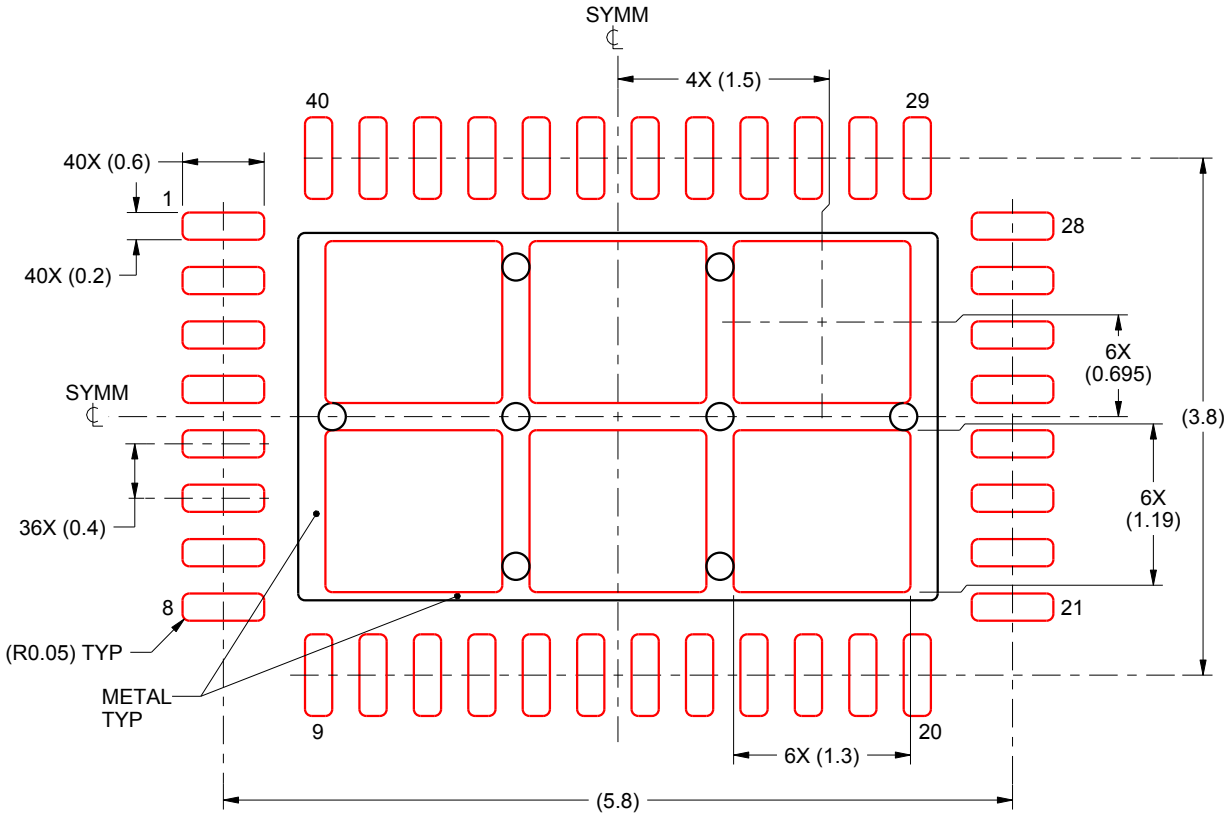


SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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