TCA9800 电平转换 I²C 总线缓冲器/中继器

1 特性

- 双通道双向缓冲器
- 在 B 侧集成了电流源，不需要外部 B 侧电阻器
- 超低功耗
- 无静态电压偏移，低 V_{OL}
- 与 I²C 总线和 SMBus 兼容
- 在 A 侧上，工作电源电压范围为 0.8V 至 3.6V
- 在 B 侧上，工作电源电压范围为 1.65V 至 3.6V
- 高电平有效中继器使能输入
- A 侧断电高阻抗 I²C 总线引脚
- 断电反射功率保护 I²C 总线引脚
- 支持时钟拉伸和多主仲裁
- 0.5mA 至 3mA 的电流源选项系列

2 应用

- 服务器
- 路由器（路由设备）
- 工业设备
- 个人计算机
- 功耗敏感型 应用

3 说明

TCA9800 是一款适用于 I²C 总线和 SMBus/PMBus 系统的双通道双向缓冲器。它在低电压（低至 0.8V）和较高电压（1.65V 至 3.6V）之间提供双向电平转换。TCA9800 在器件 B 侧 具有 一个内部电流源，因而 B 侧不需要外部上拉电阻器。该电流源还提供改进的上升时间和超低功耗。

TCA9800 能够在不使用静态电压偏移或增量偏移的情况下提供真正的缓冲（而不是 pass-FET 解决方案）。这意味着 TCA9800 的 A 侧和 B 侧上的 V_{OL} 极低（约为 0.2V），有助于消除由于固定的 V_{IL} 阈值导致的通信问题。TCA9800 的另一个重要特性是没有电源定序要求或电源依赖性。V_{CCA} 可以大于、小于或等于 V_{CCB}。这使得系统设计人员可以灵活地使用 TCA9800。

TCA9800 是由四种器件组成的产品系列中的一部分，每种器件有不同的电流源强度（请参见*器件比较表*）。

器件信息(1)

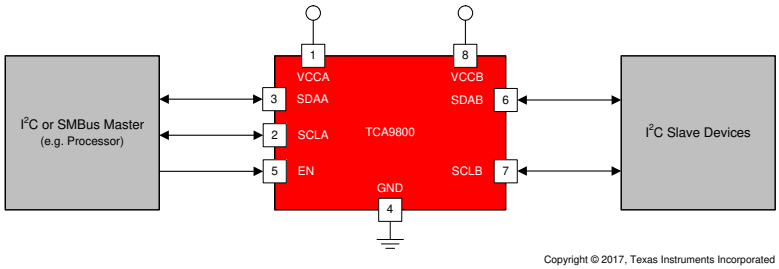
器件型号	封装	封装尺寸（标称值）
TCA9800	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件比较

器件型号	I_{CS}：电流源值（典型值）
TCA9800	0.54mA
TCA9801	1.1mA
TCA9802	2.2mA
TCA9803	3.3mA

简化原理图



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4 修订历史记录

Changes from Revision A (March 2017) to Revision B **Page**

- Added last sentence: "When enable is a logic LOW while VCCB is powered on, the internal current source on B side is still enabled...." to the *Active-High Repeater Enable Input* section ... 12

Changes from Original (March 2017) to Revision A **Page**

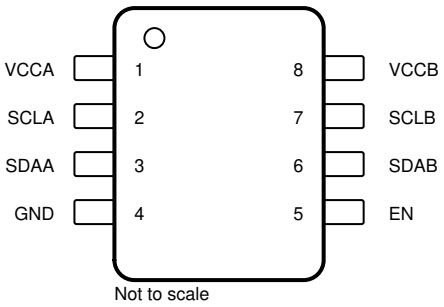
- Updated I_{CS} typical values in *Device Comparison Table* ... 3

5 Device Comparison Table

Part Number	I_{CS}: Current Source Value (Typical)
TCA9800	0.54 mA
TCA9801	1.1 mA
TCA9802	2.2 mA
TCA9803	3.3 mA

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.8 V to 3.6 V)
2	SCLA	I/O	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor, even if unused
3	SDAA	I/O	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor, even if unused
4	GND	—	Ground
5	EN	I	Active-high repeater enable input, referenced to V_{CCA}
6	SDAB	I/O	Serial data bus, B-side. Do NOT connect to V_{CCB} through a pull-up resistor for proper operation. If unused, leave floating
7	SCLB	I/O	Serial clock bus, B-side. Do NOT connect to V_{CCB} through a pull-up resistor for proper operation. If unused, leave floating
8	VCCB	Supply	B-side and device supply voltage (1.65 V to 3.6 V)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage on A-side	–0.5	4	V
V_{CCB}	Supply voltage on B-side	–0.5	4	V
V_{EN}	Enable input voltage	–0.5	4	V
$V_{I/O}$	I^2C bus voltage	–0.5	4	V
I_{OL}	Maximum SDAA, SCLA I_{OL} current		20	mA
I_{IK}	Input clamp current (SDAB/SCLB)		–20	mA
	Input clamp current (EN, VCCA, VCCB, SDAA, SCLA)		–20	mA
I_{OK}	Output clamp current (SDAB/SCLB)		–20	mA
	Output clamp current (EN, VCCA, VCCB, SDAA, SCLA)		–20	mA
Operating junction temperature	T_J		130	°C
Storage temperature	T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Operating free-air temperature		–40	125	°C
V_{CCA}	Supply voltage		0.8	3.6	V
V_{CCB}	Supply voltage		1.65	3.6	V
$V_{I/O}$	Input-output voltage	SDAA, SCLA	0	3.6	V
		SDAB, SCLB	0	3.6	
		EN	0	3.6	

7.4 Thermal Information

THERMAL METRIC(1)		TCA9800 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	102.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OUTPUT CHARACTERISTICS							
V_{OL}	Low-level output voltage	SDAA, SCLA	I_{OL} = 6 mA, V_{ILB} = 0 V		0.04	0.13	V
		SDAB, SCLB	V_{IA} = 0 V		0.22	0.26	
I_{EXT-I} (2)	Allowed input leakage current of I_{CS}		SDAB, SCLB	0		200	µA
I_{EXT-O} (2)	Allowed output leakage current of I_{CS}		SDAB, SCLB	0		100	µA
I_{CS}	Current source value				0.54		mA
	Current source tolerance			–25		25	%
INPUT CHARACTERISTICS							
R_{EN}	Enable pin pull-up			150	250	450	kΩ
V_{IH}	High-level input voltage		SDAA, SCLA	0.7 × V_{CCA}		V_{CCA}	V
			SDAB, SCLB(3)	0.7 × V_{CCB}		V_{CCB}	
			EN	0.7 × V_{CCA}		V_{CCA}	
V_{IL}	Low-level input voltage		SDAA, SCLA	0		0.3 × V_{CCA}	V
			SDAB, SCLB(4) (3)	0		0.3 × V_{CCB}	
			EN	0		0.3 × V_{CCA}	
I_{ILC}	Low-level input current contention		SDAB, SCLB(4)	300			µA
R_{ILC}	Low-level allowed pull-down resistance		SDAB, SCLB(3)			150	Ω
C_{BUS}	Bus capacitance limit		SDAB, SCLB(5)	0		400	pF
DC CHARACTERISTICS							
UVLO	Under-voltage lock out	V_{CCA}	V_{CCA} rising and falling; V_{CCB} = 1.65 or 3.6 V	0.3	0.55	0.8	V
		V_{CCB}	V_{CCB} rising; V_{CCA} = 0.8 or 3.6 V	1.3	1.51	1.6	
			V_{CCB} falling; V_{CCA} = 0.8 or 3.6 V	1.2	1.4	1.6	
I_{CCA}	Quiescent supply current for V_{CCA}	SDAA = SCLA = V_{CCA} or GND, SDAB = SCLB = open, EN = V_{CCA}	V_{CCA} = 0.8 V		0.1	7	µA
			V_{CCA} = 1.8 V		0.1	8	
			V_{CCA} = 2.5 V		0.2	9	
			V_{CCA} = 3.6 V		0.2	12	
I_{CCB}	Quiescent supply current for V_{CCB}	Both channels high, SDAA = SCLA = pulled up to V_{CCA}, SDAB = SCLB = open, EN = V_{CCA}	V_{CCB} = 1.8 V		16	40	µA
			V_{CCB} = 2.5 V		19	44	
			V_{CCB} = 3.6 V		24	52	
		Both channels low, SDAA = SCLA = GND. SDAB = SCLB = open, EN = V_{CCA}	V_{CCB} = 1.8 V		1.2	1.6	mA
			V_{CCB} = 2.5 V		1.2	1.6	
			V_{CCB} = 3.6 V		1.2	1.7	

(1) All typical values are at nominal supply voltage (1.8 V) and T_A = 25 °C unless otherwise specified.
(2) SDAB, SCLB may not sink current from external sources. It is required that no source of external current be used on these pins for proper device operation due to the internal current source.
(3) Parameter specified by design. Not tested in production.
(4) V_{IL} specification is for the first low-level seen by the SDAB and SCLB pins. I_{ILC} must also be satisfied in order to be interpreted as a low.
(5) SDAB, SCLB have a maximum supported capacitive load for device operation. If this load capacitance maximum is violated, the device does not function properly. SDAA, SCLA have no maximum capacitance limit.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{CCA} + I_{CCB}$	Total quiescent supply current		$V_{CCA} = V_{CCB} = 1.8$ V, SDAA/SCLA = V_{CCA}, SDAB/SCLB = V_{CCB}		18		µA
I_I	Input leakage current	SDAA, SCLA	$V_I = V_{CCA}$, EN = GND			±10	µA
			V_I = GND, EN = GND			±10	
		SDAB, SCLB	V_{CCB} = 0 V, V_I = 3.6 V			±10	
C_{IO}	I/O Capacitance	SDAA, SCLA	V_I = 0 V or 3.3 V, f = 1 MHz		2	10	pF
		SDAB, SCLB	V_{CCB} = GND, V_I = 0 V, f = 1 MHz		8		

7.6 Timing Requirements

PARAMETER			MIN	TYP	MAX	UNIT
$f_{SCL(MAX)}$	Max SCL clock frequency		100			kHz
t_r (1)	Rise time	Port A		57	70	ns
		Port B; V_{CCB} = 1.65 V		66	110	
		Port B; V_{CCB} = 2.5 V		100	170	
		Port B; V_{CCB} = 3.6 V		144	270	
t_f (1)	Fall time	Port A		9	30	ns
		Port B		35	85	
t_{PHL} (1)	Propagation delay high-to-low	Port A to Port B		75	200	ns
		Port B to Port A		85	250	
t_{PLH} (1)	Propagation delay low-to-high	Port A to Port B		40	150	ns
		Port B to Port A		100	350	

(1) Times are specified with loads of 1.35 kΩ and 50 pF on A-side and 50 pF on B-side. Different load resistance and capacitance alter the rise and fall times, thereby changing the propagation delay.

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{startup}$	Startup time		72	340	µs
t_{en}	Enable time		280	1000	ns
t_{dis}	Disable time		740	1800	ns

7.8 Typical Characteristics

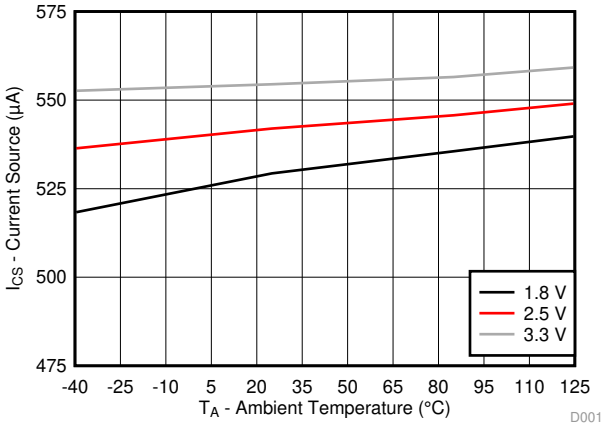


Figure 1. Current Source vs Ambient Temperature for Different V_{CCB}

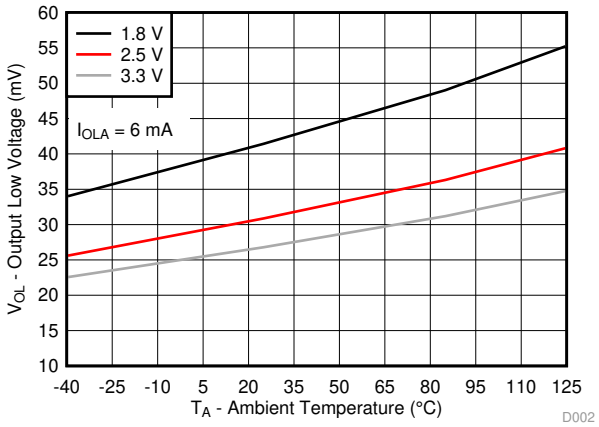


Figure 2. A-Side Output Low Voltage vs Ambient Temperature for Different V_{CCB} (I_{OLA} = 6 mA)

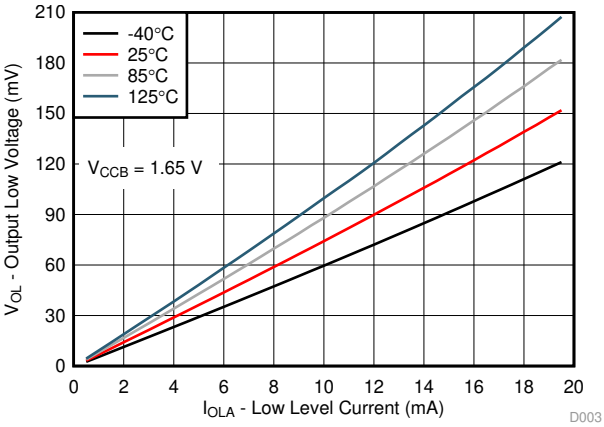


Figure 3. A-Side Output Low Voltage vs Low Level Current for Different T_A (V_{CCB} = 1.65 V)

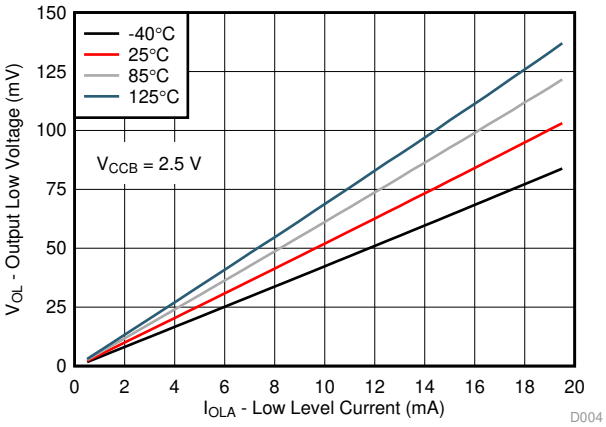


Figure 4. A-Side Output Low Voltage vs Low Level Current for Different T_A (V_{CCB} = 2.5 V)

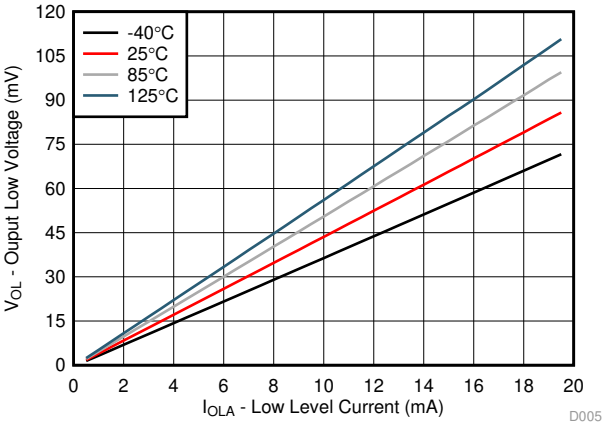


Figure 5. A-Side Output Low Voltage vs Low Level Current for Different T_A (V_{CCB} = 3.6 V)

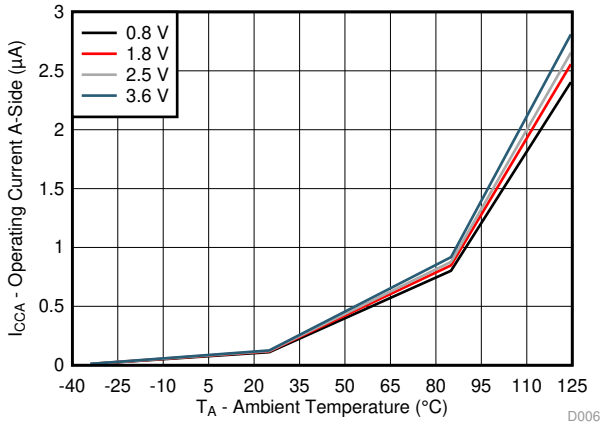


Figure 6. Operating Current A-Side vs Ambient Temperature for Different V_{CCA} (A-Side = V_{CCA} & GND)

Typical Characteristics (continued)

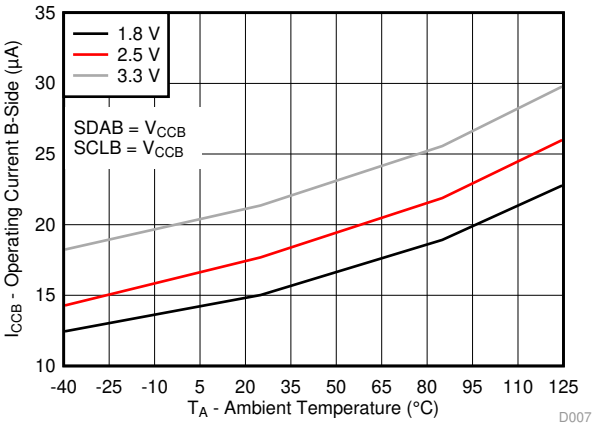


Figure 7. Operating Current B-Side vs Ambient Temperature for Different V_{CCB} (B-Side = V_{CCB})

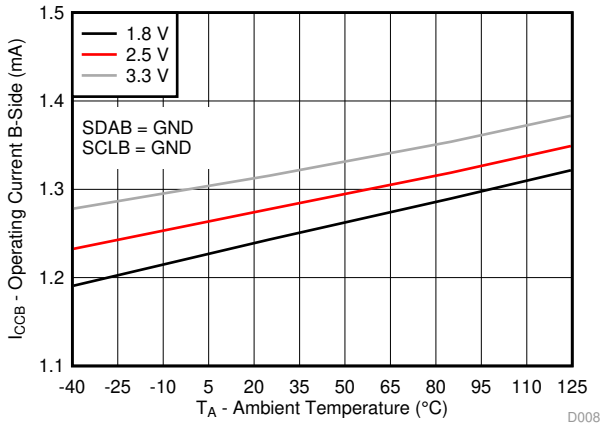


Figure 8. Operating Current B-Side vs Ambient Temperature for Different V_{CCB} (B-Side = GND)

8 Parameter Measurement Information

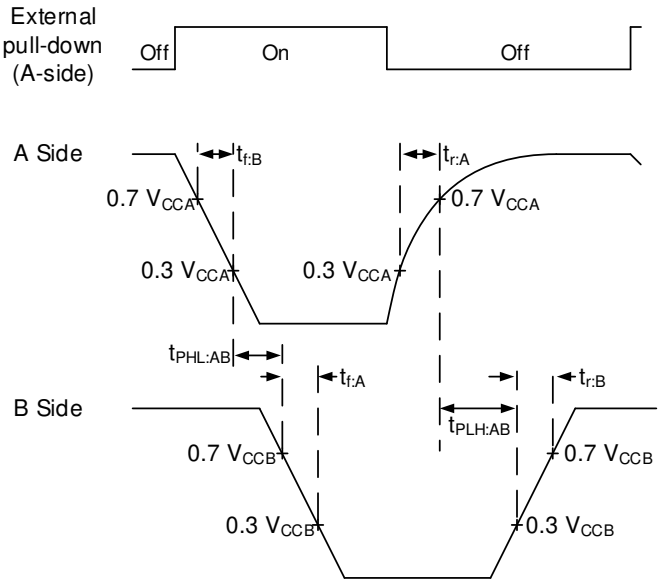
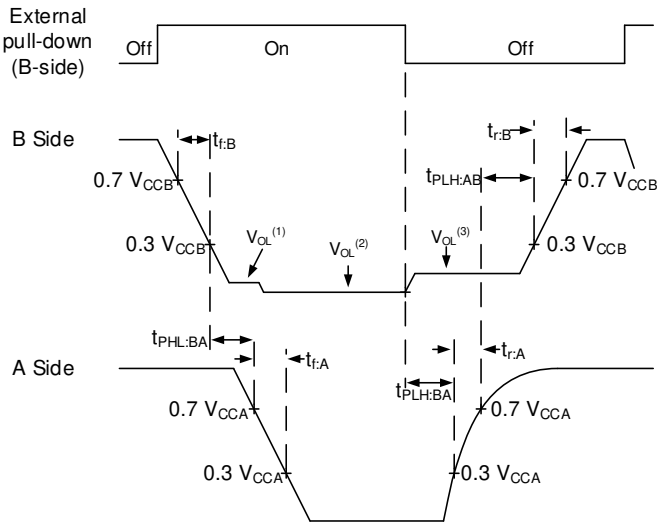
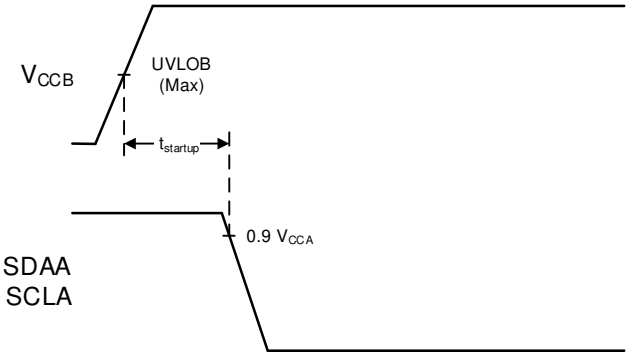


Figure 9. Propagation Delay and Transition Times for A-Side to B-Side



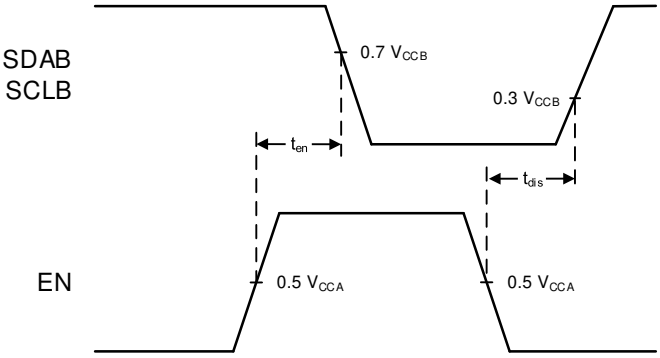
1) The V_{OL} of only the external device, pulling down on the bus
2) The V_{OL} of both the external device and the TCA980x translator
3) The V_{OL} of only the TCA980x, after the external device releases

Figure 10. Propagation Delay for B-Side to A-Side



1) V_{CCA} is powered, SDAB/SCLB are connected to GND

Figure 11. Startup Time ($t_{startup}$)



1) V_{CCA} is powered, SDAA/SCLA are connected to GND

Figure 12. Enable and Disable Time (t_{en} and t_{dis})

9 Detailed Description

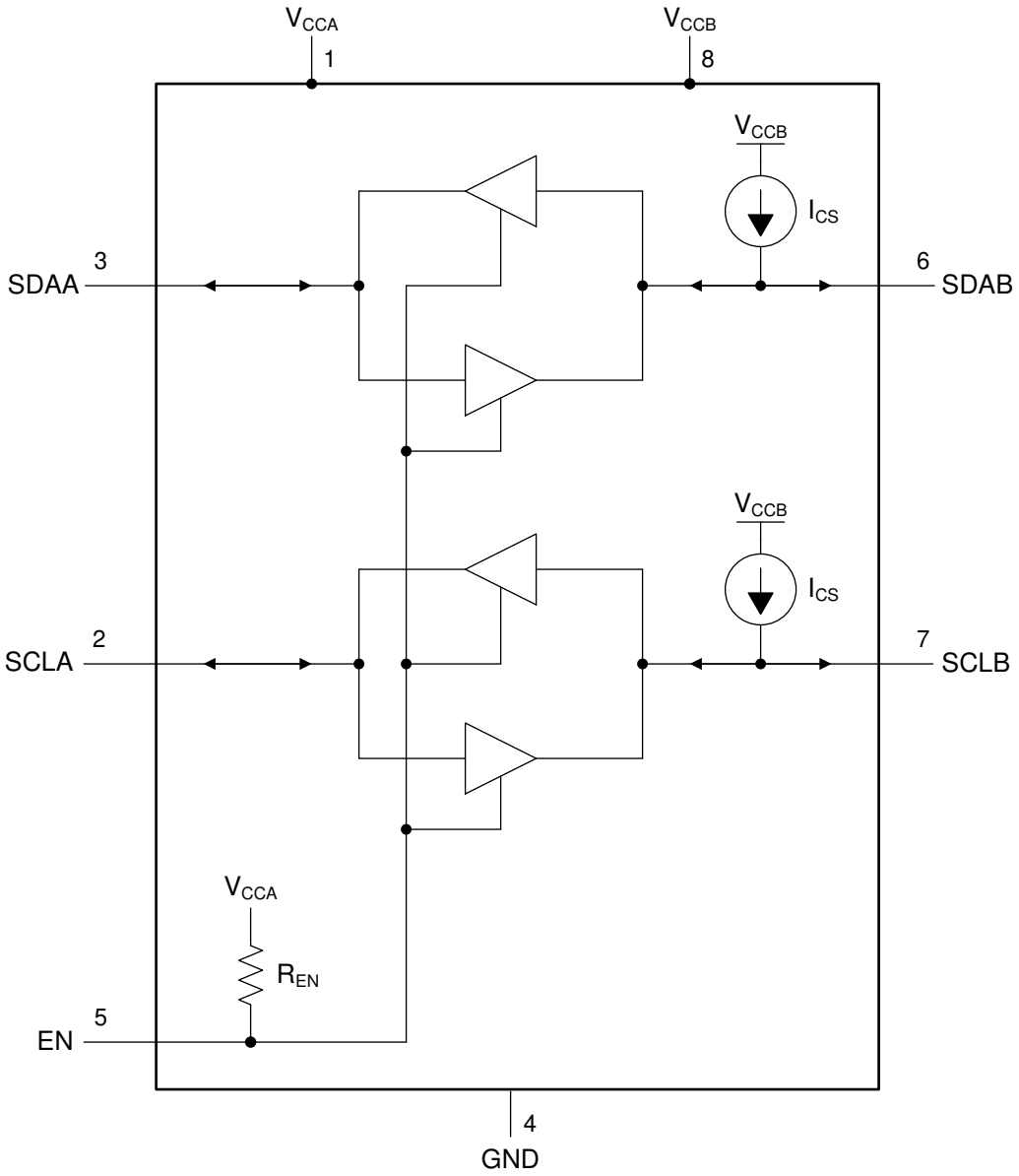
9.1 Overview

The TCA9800 is a dual-channel bidirectional buffer intended for I^2C bus and SMBus/PMBus systems. It provides bidirectional level shifting (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (1.65 V to 3.6 V). The TCA9800 features an internal current source on the B-side of the device, allowing the removal of external pull-up resistors on the B-side. The current source also provides an improved rise time and ultra-low power consumption.

The TCA9800 is able to provide true buffering (rather than a pass-FET solution) without using a static voltage offset or incremental offset. This means that the V_{OL} on both the A and B sides of the TCA9800 are very low (approximately 0.2 V), helping to eliminate communication issues as a result of fixed V_{IL} thresholds. Another key feature of the TCA9800 is that there are no power sequencing requirements, or power supply dependencies. V_{CCA} can be greater than, less than, or equal to V_{CCB}. This gives the system designer flexibility with how the TCA9800 is used.

The TCA9800 is part of a four device family with varying current source strengths (see the *Device Comparison Table*).

9.2 Functional Block Diagram



For proper device operation, no external current sources (pull-up resistors) must be used on the SDAB and SCLB ports

9.3 Feature Description

9.3.1 Integrated Current Source

The TCA980x family has an integrated current source on the B side. By using an integrated current source, the device is able to measure current to determine if an external device is pulling down on the bus or not. This innovative detection method removes the need for a static voltage offset on the B side.

9.3.2 Ultra-Low Power Consumption

The TCA980x family features ultra low power consumption, to help maximum battery life, or cut down on power dissipation in sensitive applications.

9.3.3 No Static-Voltage Offset

The TCA980x family has no static-voltage offset, which are commonly used in buffered translators to prevent a device lock-up situation where the buffer's own output low could trip the input low threshold. The removal of the static voltage offset is significant because it allows the device to have low a low V_{OL} on the B side, which helps prevents communication issues that arise from connecting a static-voltage offset output device to an input with an input low threshold which is below the static voltage V_{OL}.

9.3.4 Active-High Repeater Enable Input

The TCA980x has an active-high enable (EN) input with an internal pull-up to VCCA, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input must change state only when the global bus and repeater port are in an idle state. to prevent system or communication failures. When enable is a logic LOW while VCCB is powered on, the internal current source on B side is still enabled. The enable pin does not disable the internal current source.

9.3.5 Powered Off High Impedance I^2C Bus Pins on A-Side

The SCLA and SDAA pins enters a high impedance state when either VCCA or VCCB fall below their UVLO voltages. These pins are safe to continue having I^2C communication on, even when the device is disabled or has no power.

The SCLB and SDAB pins remain powered by their current source (I_{CS}), even when VCCA is below UVLO. When VCCB falls below UVLO, the current source turns off, and a weak pull-up is connected to prevent the B-pins from floating. This is intended behavior, because no external pull-up resistors are to be used on the SDAB or SCLB pins. This behavior prevents the bus pins from floating, and allows it to follow VCCB.

9.3.6 Powered-Off Back-Power Protection for I^2C Bus Pins

All I^2C bus pins has protection circuitry to prevent current from flowing to the VCC pins from the I^2C bus pins.

9.3.7 Clock Stretching and Multiple Master Arbitration Support

The TCA980x family supports clock stretching and multiple master arbitration methods, and helps to minimize overshoot during these hand offs between master and slave (or multiple masters).

9.4 Device Functional Modes

Table 1 shows the TCA980x function table.

Table 1. Enable Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

Table 2 lists the TCA980x B-Side current source functions.

Table 2. B-Side Current Source Function Table

VCCB	FUNCTION
L	Current sources disabled, weak pull-up is connected with back-power protection
H	Current sources enabled

9.4.1 Device Operation Considerations

9.4.1.1 B-Side Input Low (V_{IL}/I_{ILC}/R_{ILC})

The TCA980x family utilizes the current source on the B side to determine whether an external device is driving the bus low, or if it is driving the bus low itself. As such, there are some parameters that must be met to ensure a successful transmission of a low from the B-side to the A-side. These parameters are listed in Table 3.

Table 3. B-side Input Low-Level Parameters

PARAMETER		SHORT DESCRIPTION	DETAILED INFORMATION
V_{IL}	Low-level input voltage	The input voltage that is interpreted as a low. On the B-side, I_{ILC} must also be satisfied to maintain a low	See the *V_{ILC} & I_{ILC}* section
I_{ILC}	Low-level input current (contention)	The minimum amount of current that an external device must be sinking from the TCA980x to transmit a low. V_{IL} must also be satisfied	See the *V_{ILC} & I_{ILC}* section
R_{ILC}	Low-level allowed pull-down resistance	The maximum allowed pull-down resistance of an external device in order to successful transmit a low	See the *R_{ILC}* section

9.4.1.1.1 V_{ILC} & I_{ILC}

The I_{ILC} parameter is the minimum amount of current that the external device must sink from the TCA980x in order for the TCA980x to accept the low on the B-side.

In order for the TCA980x to accept a low on the B-side, both V_{IL} and I_{ILC} parameters must be satisfied. In an idle bus condition (both A and B sides are high), meeting the V_{IL} threshold with an external device pull-down meets the I_{ILC} requirement, since the pull-down has to sink the entire I_{CS} (current source value) current before the voltage on the pin falls.

In a contention situation (the A-side is being driven low externally, and the B-side is driven low by the TCA980x), the V_{IL} requirement is already satisfied by the TCA980x alone (Since the output low voltage is less than the V_{IL} threshold). In order for a device on the B-side to over-drive the A-side, it must sink the I_{ILC} value for the TCA980x to accept that the low is now being driven by the B-side. This helps reduce or eliminate overshoot during the hand off between a slave an master during a clock-stretching event, or an acknowledge.

External pull-up resistors on the B-side are not allowed for this reason. As the additional current provided by them may hinder an external device from being able to satisfy the TCA980x's I_{ILC} requirement. For more information on this and allowed external current into the device, see the *Input and Output Leakage Current (I_{EXT-I}/I_{EXT-O})* section.

9.4.1.1.2 R_{ILC}

The R_{ILC} parameter describes the maximum allowed pull-down resistance. This parameter comes from the combination of I_{ILC} and I_{CS}, and states the maximum resistance that can satisfy the I_{ILC} parameter. Note that series resistors on the bus are going to affect this, as seen with other types of buffers (voltage delta across the series resistor. This increases the effective V_{OL} of the external device pulling the bus low).

The calculated resistance of the internal pull-down FET of an external device can be calculated from the V_{OL} and I_{OL} measurements of the external device in question using Equation 1. Take care to consider any series resistors placed in the path from the TCA980x to any external device. Note that R_{PD} is the calculated resistance of the internal pull-down FET, and not a resistor to ground. This is for determining if the external device's output characteristics meet the TCA980x R_{ILC} requirement (150 Ω).

$$R_{PD} = V_{OL} / I_{OL} \quad (1)$$

9.4.1.2 *Input and Output Leakage Current (I_{EXT-I}/I_{EXT-O})*

The Input external current (I_{EXT-I}) and output external current (I_{EXT-O}) parameters describe the amount of parasitic current either injected into the device or pulled from the device (such as leakage from ESD cells) without affecting device operation as shown in Table 4.

Table 4. B-Side Input and Output Leakage Current

PARAMETER		SHORT DESCRIPTION	DETAILED INFORMATION
I_{EXT-I}	Input leakage current	Current that is external, but pulled up to supply, leaking current into the TCA980x B-side. An example is a leaky ESD cell from VCC, or an external pull-up resistor.	See the *I_{EXT-I}* section
I_{EXT-O}	Output leakage current	Current that is pulled from the TCA980x B-side. ESD cells are the most common form of output leakage. Care must be taken not to violate this spec, otherwise the leakage current can create a false low.	See the *I_{EXT-O}* section

9.4.1.2.1 I_{EXT-I}

I_{EXT-I} is a current source that is external to the TCA980x B-side, but leaks current into the device. This type of input leakage may not exceed the I_{EXT-I} maximum spec, or else the minimum I_{ILC} value does not apply.

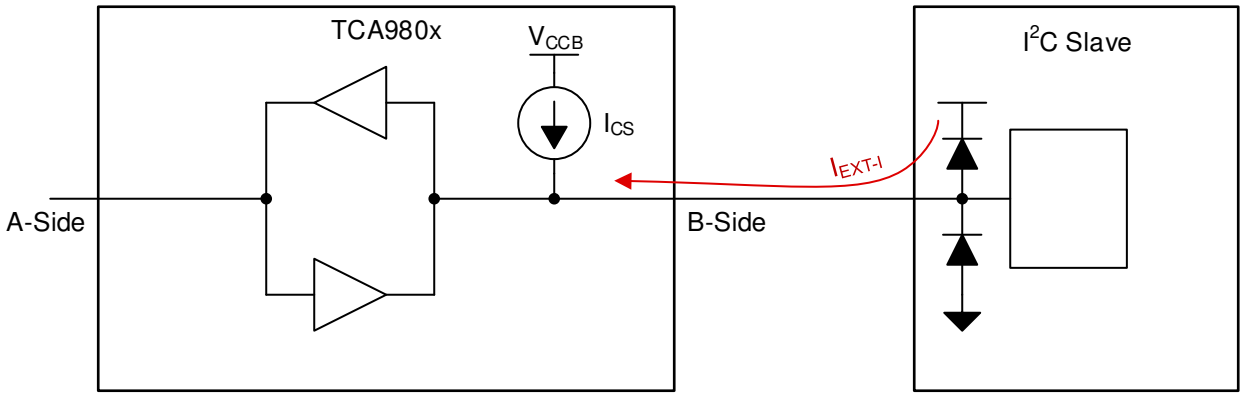


Figure 13. I_{EXT-I} Example

As shown in Figure 13, I_{EXT-I} is a source of additional current into the device, shown as a leaky ESD cell. The user must keep I_{EXT-I} as close to 0 as possible, since the TCA980x has a current source as a pull-up internally, and uses this current source to help detect which side is driving a low. As I_{EXT-I} increases, it increases the minimum I_{ILC} value, requiring that an external device sink more current from the TCA980x in order to transmit a low. There must be no external pull-up resistor on the B-side to contribute to I_{EXT-I}.

9.4.1.2.2 I_{EXT-O}

I_{EXT-O} is an unintentional current from the TCA980x's internal current source that is external. Leaking ESD cells are a common contributor to leakage current. This type of input leakage may not exceed the I_{EXT-O} maximum spec, or else the TCA980x can interpret this excessive current as an external device transmitting a low, causing the bus to latch. It is important to consider the total sum of I^2C slave device's leakage to ground, and that it does not violate I_{EXT-O}. An example showing a typical I_{EXT-O} leakage path through an ESD cell is shown in Figure 14.

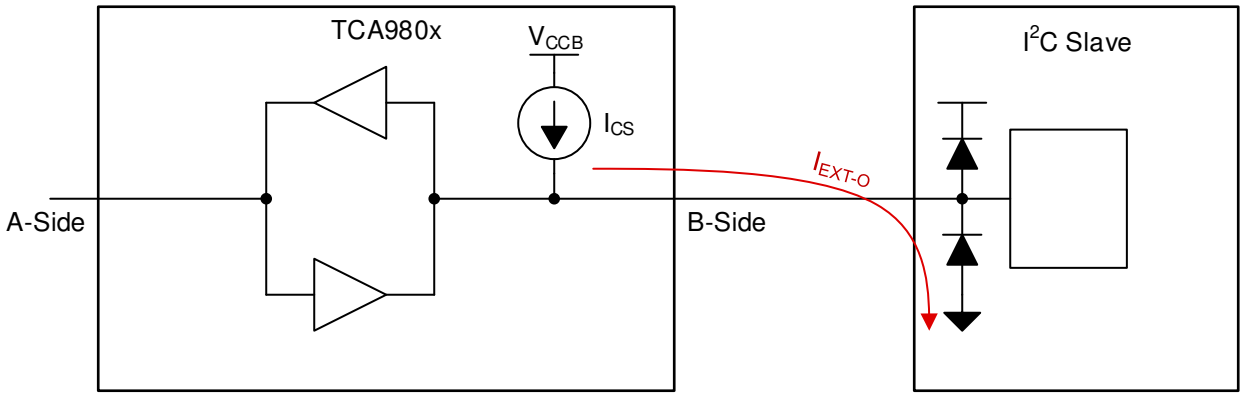


Figure 14. I_{EXT-O} Example

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Device Selection Guide

The TCA980x family has 4 different variants, with different strengths of the internal current source as shown in Table 5.

Table 5. TCA980x Family

Part Number	I_{CS}: Current Source Value
TCA9800	0.54 mA
TCA9801	1.1 mA
TCA9802	2.2 mA
TCA9803	3.3 mA

It is acceptable to select the TCA9803 as the default, since it is able to drive 400-pF bus capacitance loads at 400 kHz. For system designers looking to optimize selection, see the *Detailed Design Procedure* section for single device for detailed examples of how to select a part number for a specific application.

10.1.2 Special Considerations for the B-side

The TCA980x supports many types of connections between other TCA980x and other buffers/translators. Care must be taken to ensure that all of the B-side requirements be satisfied. For example, FET/pass-gate based translators typically cannot be used on the B-side, because they require pull-up resistors on both sides, and when one side is pulling low, the FET/switch closes, likely causing I_{EXT-I} to be violated (See the *I_{EXT-I}* section for more information).

The *FET or Pass-Gate Translators* and *Buffered Translators/Level-shifters* sections list some use-cases that are not supported or require special considerations when connected to the B-ports, note that these considerations only apply to the B-side of the TCA980x family.

10.1.2.1 FET or Pass-Gate Translators

Some translators are based on pass-gates for translation support. In most of the use cases, external pull-up resistors are required to pull the bus to the voltage rail.

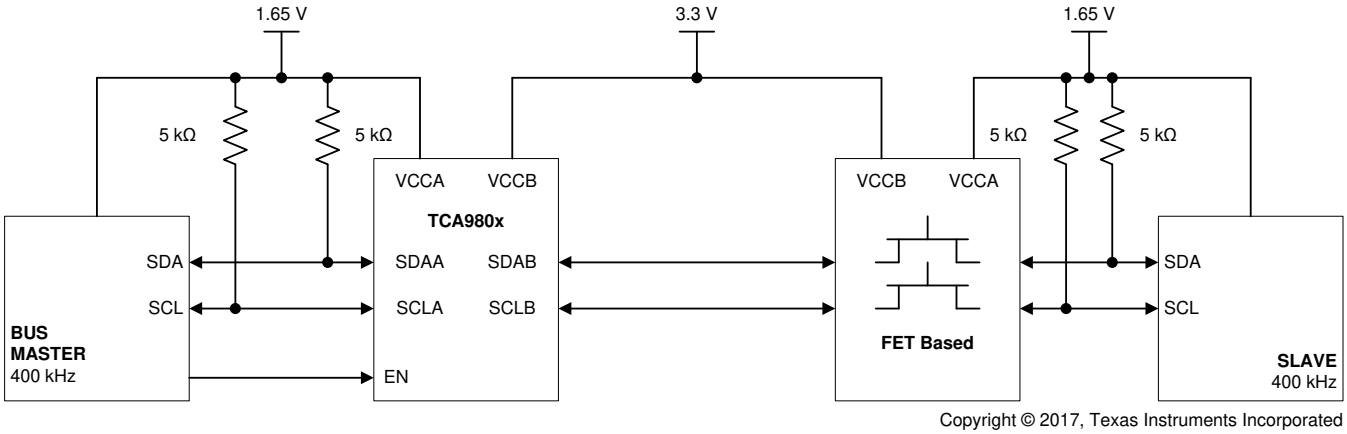


Figure 15. Incorrect B-Side Pass-Gate Based Translator Use Case

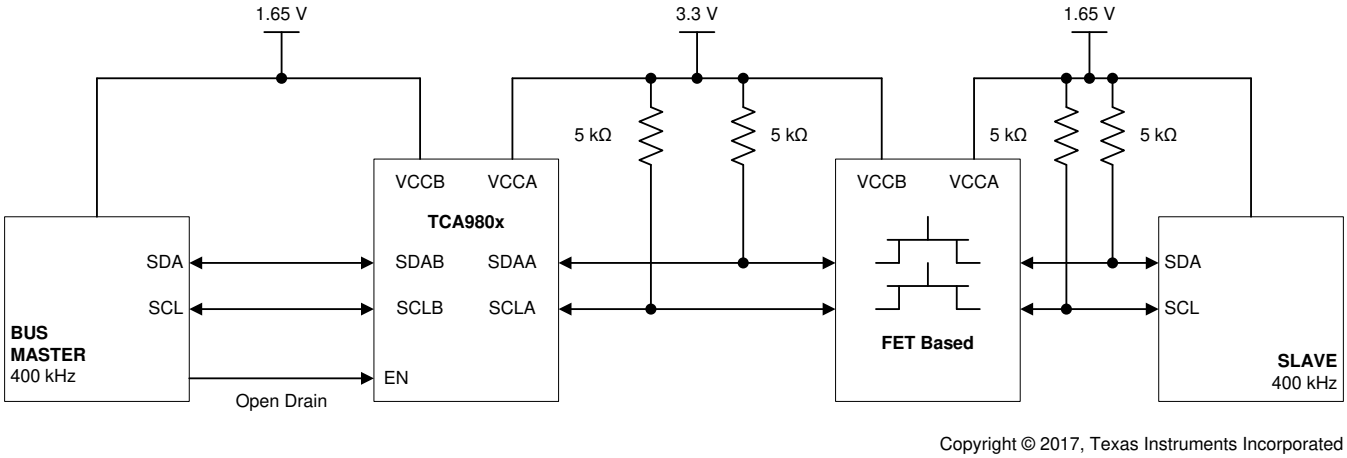


Figure 16. A-Side Pass-Gate Based Translator Use Case

As shown in Figure 15, it may appear that this use case is valid, but actually it is not. When either the TCA980x B-side or the slave pull down on the bus, the FET isolating the bus closes (low R_{DS_ON}) and current from the 5-kΩ resistor is observed by the TCA980x, violating I_{EXT-I}. See the *I_{EXT-I}* section for more information.

Figure 16 shows the correct way to pair with a FET base translator (connecting to the A-side).

Rather than using a FET-based translator, it is recommended that a buffered translator be used, such as another TCA980x or a TCA9517. See the *Typical Application* section for single device for more information on concerns with B-side connections to buffered translators.

10.1.2.2 Buffered Translators/Level-shifters

The TCA980x family supports connections with buffered translators, but care must be taken to ensure that no operating conditions be violated. In a general sense, the following must be avoided on the B-side ports of the TCA980x:

- Sources of current other than the individual TCA980x (B-side of the other TCA980x, external pull-up resistors, current sources, rise time accelerators, etc)
- Static-voltage offset buffer outputs (B-side of the TCA9517, etc)
- Outputs with R_{ILC} (equivalent pull-down resistance) > 150 Ω

It is important to note that these special operating requirements apply only to the B-side ports of the TCA980x. For example, the TCA9517 B-side can be safely connected to the A-side of the TCA980x, but not to the B-side of the TCA980x. However, it is OK to connect the A-side of the TCA9517 to the B-side (or A-side) of the TCA980x, because the A-side does not have a static voltage offset based output.

Figure 17 shows an example of the incorrect connection on the B-side to a buffer with a static voltage offset output. The reason this is unacceptable is because the equivalent output resistance of the output buffer is greater than the maximum R_{ILC} allowed. See the *R_{ILC}* section for more information.

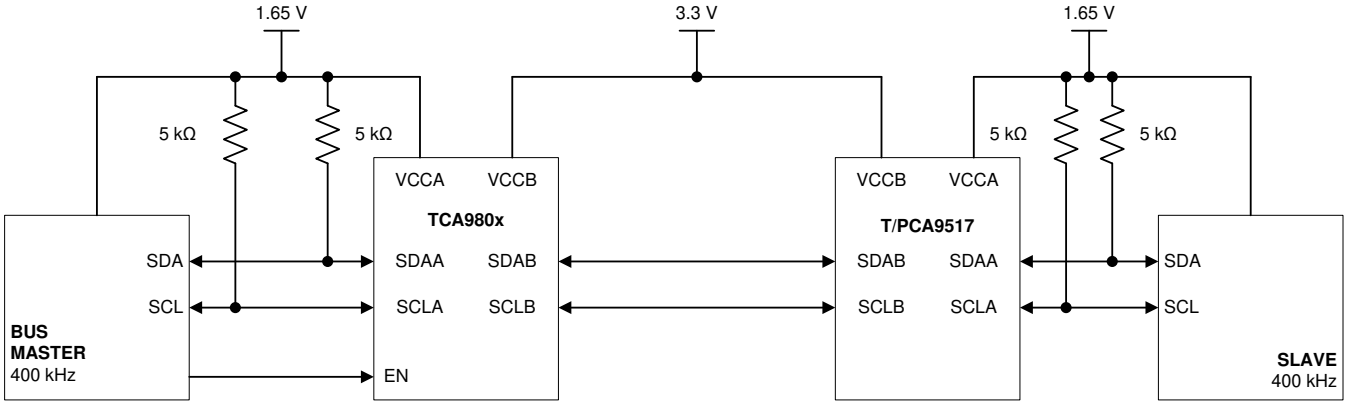


Figure 17. Incorrect B-Side Static Voltage Offset Buffer Connection

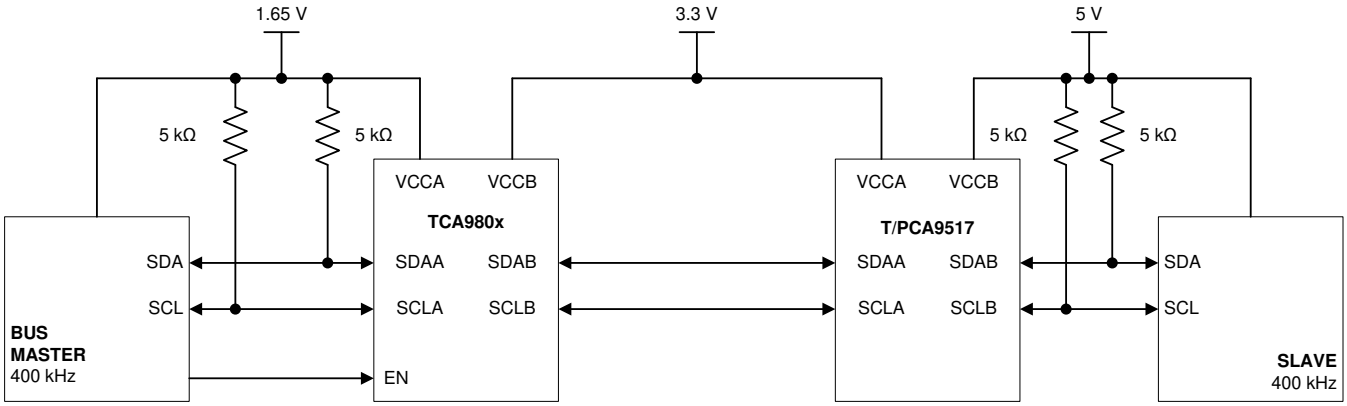


Figure 18. Correct Connection With Other Buffers

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

As shown in Figure 18, this connection is acceptable for use on the B-side ports of the TCA980x, because the equivalent R_{ILC} of the A-side of this example buffer is less than 150 Ω.

10.2 Typical Application

10.2.1 Single Device

The typical application for the TCA980x family is to be used as a buffering translator, where the V_{CCA} and V_{CCB} are at different values in order to level-shift the I^2C bus voltages.

Typical Application (continued)

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the I_{EXT-I} section.

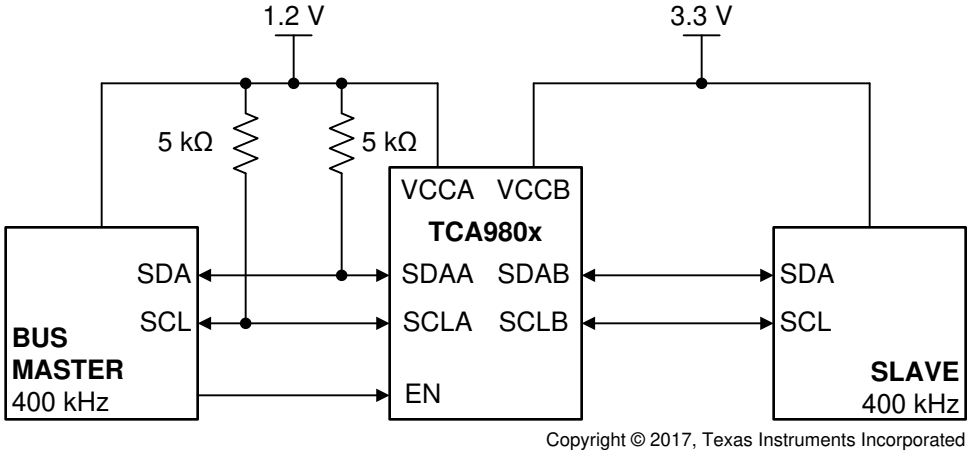


Figure 19. Typical Level-Shifting Application Example (Master on A-side)

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

As shown in Figure 20, the I^2C master can be on the B-side, and that it is ok to have $V_{CCA} > V_{CCB}$. The only requirements are that no external source of current (pull-up resistor or current source) be on the B-pins of the TCA980x, and that both V_{CCA}/V_{CCB} values are within the recommended range. As a note, since the EN pin is referenced to the VCCA supply voltage, when the master is on the A-side, the system designer must ensure that the enable pin voltage is pulled up to V_{CCA} (either with an external or the internal pull-up resistor) to ensure that the device is enabled.

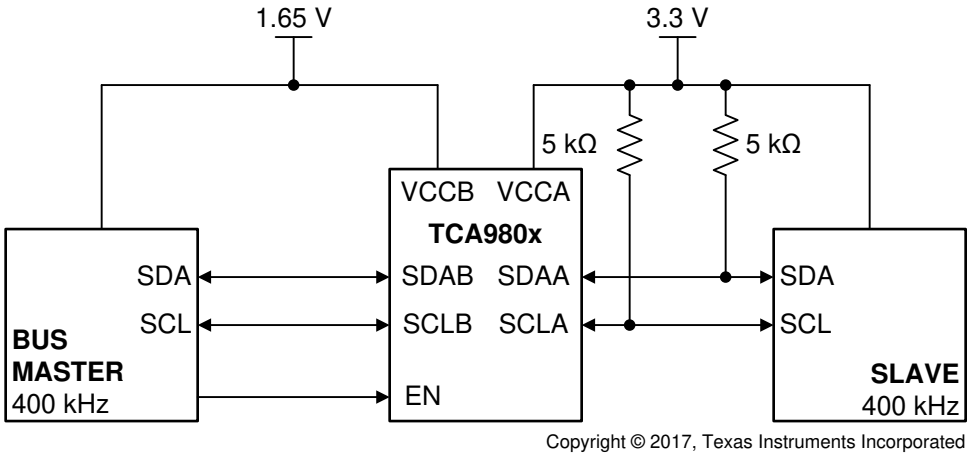


Figure 20. Typical Level-Shifting Application Example (Master on B-side)

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

Typical Application (continued)

10.2.1.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in Table 6 must be known. The setup in Figure 19 is used for these example design requirements.

C_L is the capacitance of the bus, including the pin capacitance of each slave device connected, and the capacitance of the board trace. It is possible to estimate the bus capacitance by summing up the pin capacitances of each slave device on the node (using 10-pF per slave is a safe estimate, since this is the maximum allowed per the I^2C specification), but trace capacitance requires an estimation through simulation or by getting the capacitance per unit length from the board manufacturer.

Table 6. Design Requirements

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	100 pF
t_r	Rise time	up to 300 ns	≤ 150 ns
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	1.2 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	3.3 V
f_{SCL}	I^2C clock frequency		400 kHz

10.2.1.2 Detailed Design Procedure

Selection of the correct device is important for designers wanting optimize power consumption while transmitting.

Selecting the pull-up resistor required for the A-side is well documented already, see the *I2C Bus Pullup Resistor Calculation* application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Since the B-ports of the TCA980x family have an integrated current source, the rise time is easily calculated with Equation 2. The graphs in the *Application Curves* section show the maximum capacitance load that each device can drive (based on minimum I_{CS} value) to achieve a desired rise time, for different V_{CCB} voltages.

$$t_r = C_L \frac{(0.4 \times V_{CCB})}{I_{CS}} \tag{2}$$

The target design requirements example is intended for 400-kHz I^2C, so the appropriate selection graph to use is Figure 22, and specifically Figure 27 since VCCB supply voltage is 3.3 V. In Figure 21, the graph has the appropriate regions shaded to help illustrate how to select the appropriate device. When looking at the general selection graphs, note that voltage line shifts evenly between the 1.65 V and 3.6 V traces in the general selection graphs. For example, if VCCB in another example is 2.5 V, then the selection graph is based on a line in the middle of the 1.65 V and the 3.6 V trace.

As shown in Figure 21, the shaded region is the appropriate region based on design requirements listed in Table 6. Any line that touches this shaded region is able to meet the design requirements. In this example, the TCA9803 and the TCA9802 both are able to satisfy the design requirements, since they both touch the shaded region. The TCA9800 and the TCA9801 both fall below the shaded region. While the TCA9801 is able to meet a rise time of about 190 ns at 100 pF (acceptable by the fast-mode rise time requirements), the design target in this example was ≤ 150 ns. This is a consideration a system designer can make, sacrificing rise time for a lower-power device, but in this example, the 150 ns limit is going to be upheld).

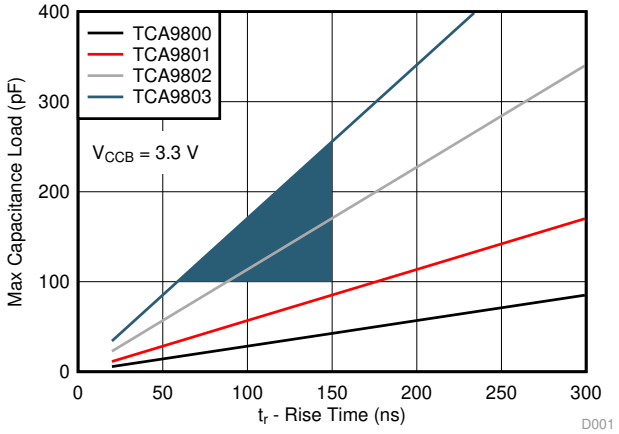


Figure 21. Selection Guide Based on Example Design Requirements

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

Based on the selection graph shown above, the TCA9802 is selected, since it is the lowest-power device's trace (grey trace) which touches the shaded region. The TCA9803 may also be used without any consequences.

10.2.1.3 Application Curves

The application curves can be used to select the appropriate part for a given design requirement, or to estimate the rise-time.

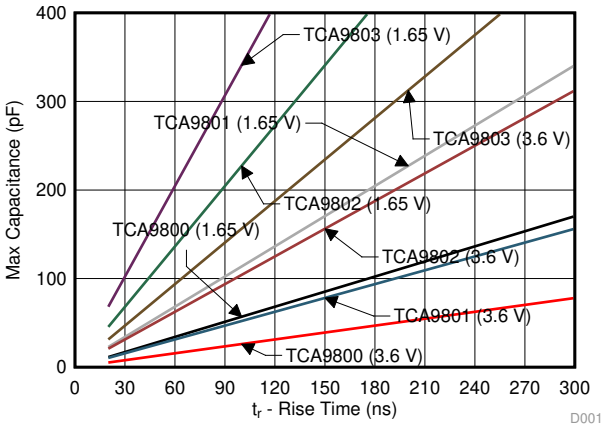


Figure 22. Maximum Load Capacitance vs Rise Time (400-kHz I^2C)

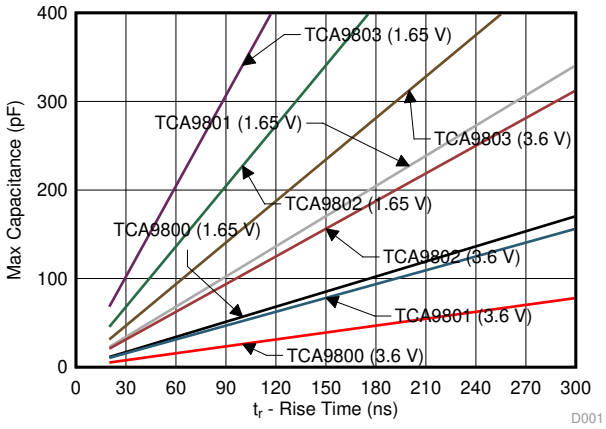


Figure 23. Maximum Load Capacitance vs Rise Time (100-kHz I^2C)

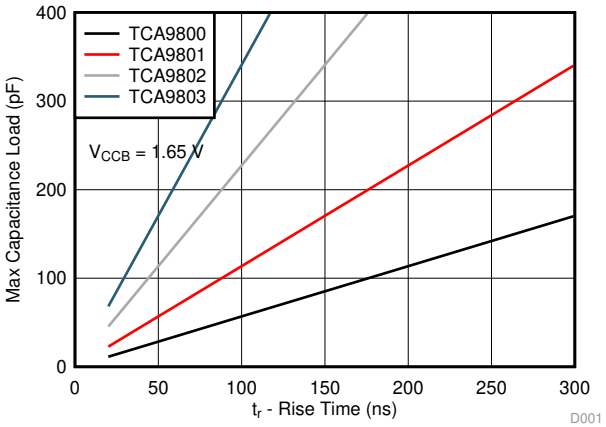


Figure 24. Maximum Load Capacitance vs Rise Time (400-kHz I^2C, V_{CCB} = 1.65 V)

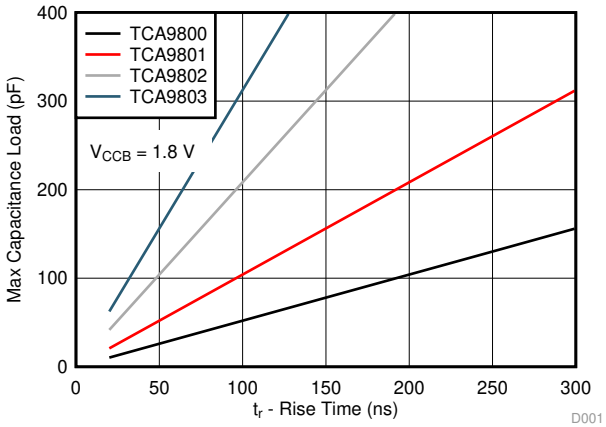


Figure 25. Maximum Load Capacitance vs Rise Time (400-kHz I^2C, V_{CCB} = 1.8 V)

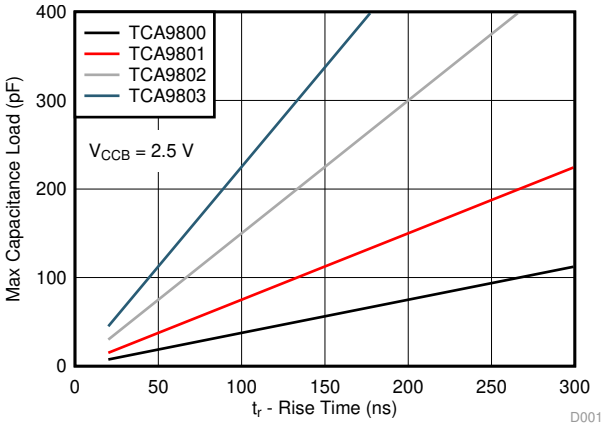


Figure 26. Maximum Load Capacitance vs Rise Time (400-kHz I^2C, V_{CCB} = 2.5 V)

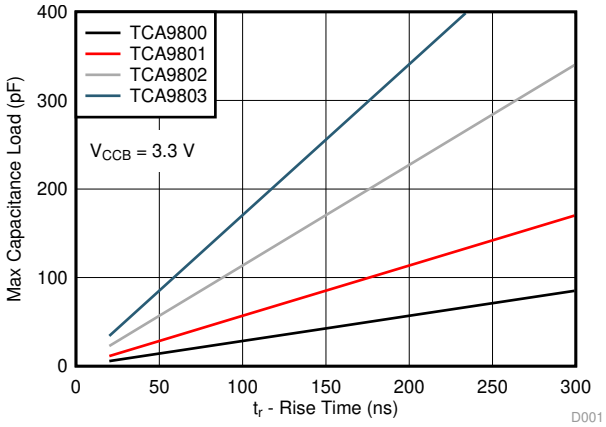


Figure 27. Maximum Load Capacitance vs Rise Time (400-kHz I^2C, V_{CCB} = 3.3 V)

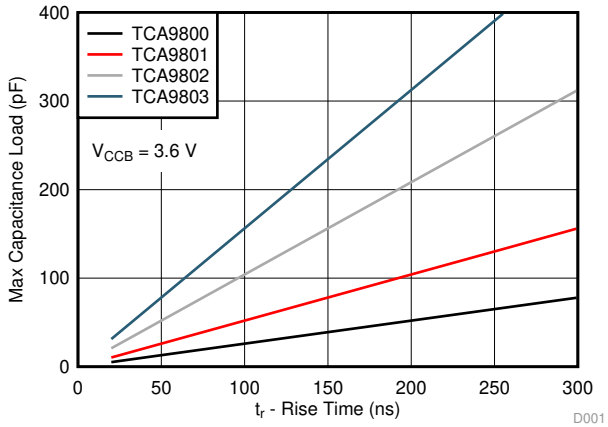


Figure 28. Maximum Load Capacitance vs Rise Time (400-kHz I²C, V_{CCB} = 3.6 V)

10.2.2 Buffering Without Level-Shifting

The TCA980x family supports buffering use cases which do not need level-shifting or voltage-translation.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the *I_{EXT-I}* section.

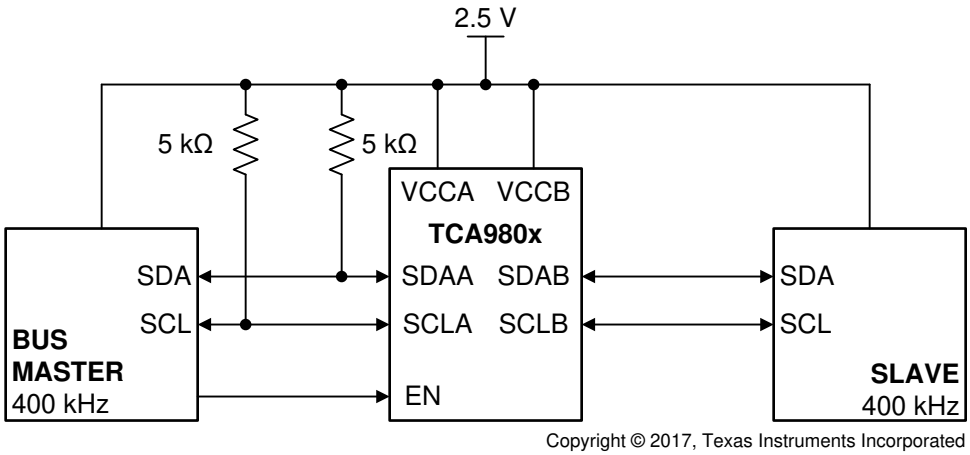


Figure 29. Buffering Use Case Without Level-Shifting

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

10.2.2.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in Table 7 must be known. The setup in Figure 29 is used for these example design requirements.

Table 7. Design Requirements

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	200 pF
t_r	Rise time	up to 300 ns	≤ 300 ns

Table 7. Design Requirements (continued)

Parameter	Description	Acceptable Range	Example Value/Target
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	2.5 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	2.5 V
f_{SCL}	I^2C clock frequency		400 kHz

10.2.2.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side is well documented already, see the *I2C Bus Pullup Resistor Calculation* application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Selection process of each device is identical to the procedure described in the *Device Selection Guide* section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the *Detailed Design Procedure* section for single device for detailed information.

As shown in Figure 30, the shaded region is the appropriate region based on design requirements listed in *Table 7*. Any line that touches this shaded region is able to meet the design requirements. In this example, the TCA9803, TCA9802, and TCA9801 are able to satisfy the design requirements, since they all touch the shaded region. The TCA9800 falls below the shaded region.

Based on the selection graph shown above, the TCA9801 is selected, since it is the lowest-power device which touches the shaded region (red trace). The TCA9803 or the TCA9802 may also be used without any consequences.

10.2.2.3 Application Curve

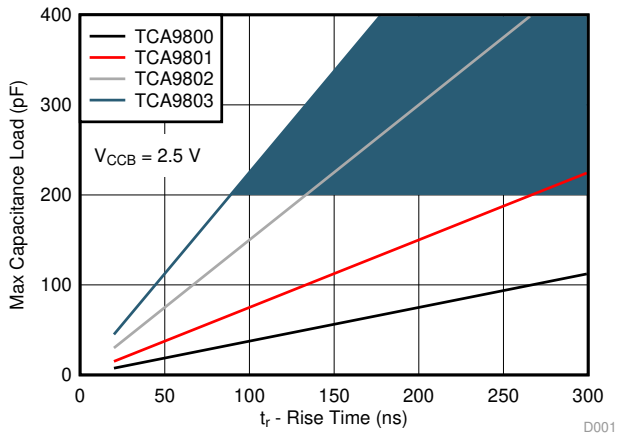


Figure 30. Selection Guide Based On Example Design Requirements

10.2.3 Parallel Device Use Case

The TCA980x family supports multiple TCA980x used in parallel. The A-sides of the TCA980x are allowed to be connected together.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation shown in the I_{EXT-I} section.

NOTE: B-sides of TCA980x devices may never be connected to each other, because the I_{EXT-I} specification limit is violated. See the I_{EXT-I} section for more information.

NOTE: The B-side may not be connected to another translator if it uses a static-voltage offset. The R_{ILC} spec is violated since the static voltage offset adjusts the output resistance to ground to be outside of the R_{ILC} spec requirement, causing the TCA980x to be unable to recognize a low.

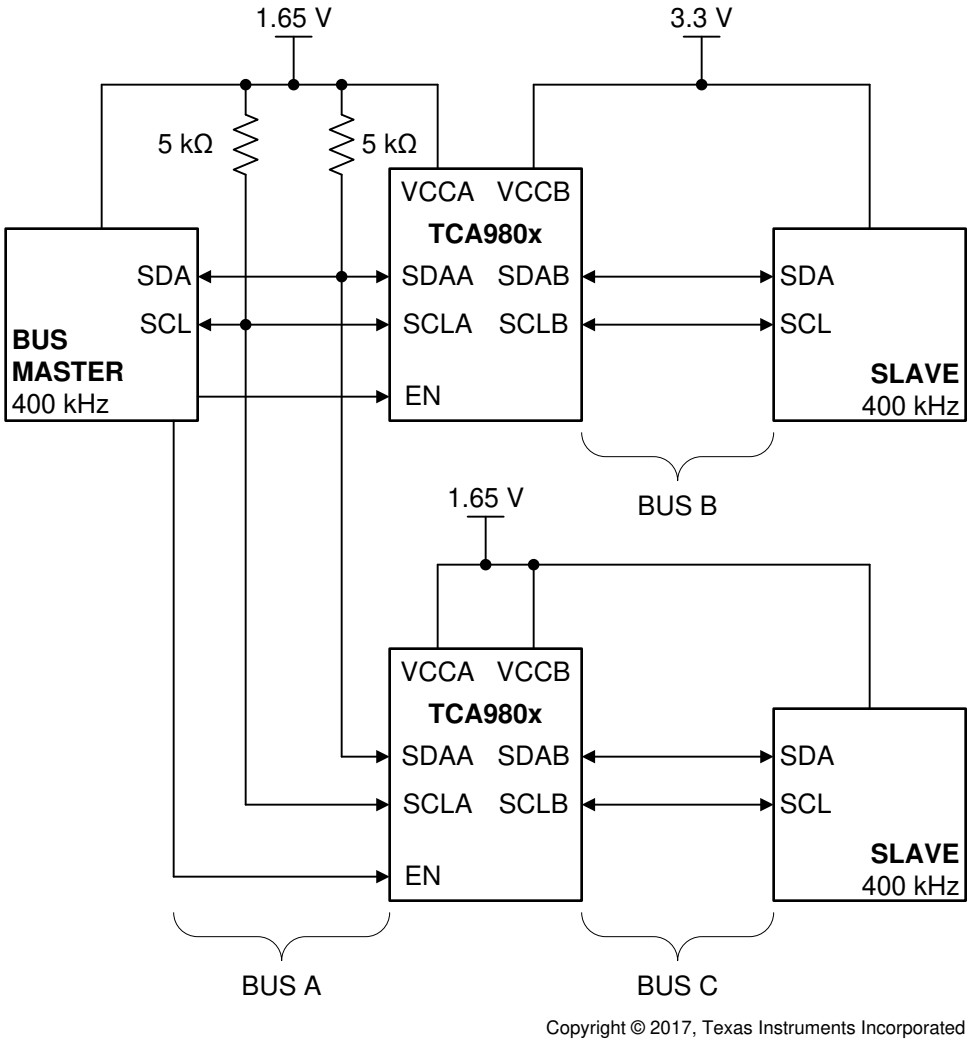


Figure 31. Parallel Use Case

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

10.2.3.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information shown in Table 8 and Table 9 must be known. The setup in Figure 31 is used for these example design requirements.

Table 8. Design Requirements for Bus B

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	300 pF
t_r	Rise time	up to 300 ns	≤ 300 ns
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	1.65 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	3.3 V

Table 8. Design Requirements for Bus B (continued)

Parameter	Description	Acceptable Range	Example Value/Target
f_{SCL}	I^2C clock frequency		400 kHz

Table 9. Design Requirements for Bus C

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	40 pF
t_r	Rise time	up to 300 ns	≤ 300 ns
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	1.65 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	1.65 V
f_{SCL}	I^2C clock frequency		400 kHz

10.2.3.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side (Bus A) is well documented already, see the *I2C Bus Pullup Resistor Calculation* application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Selection process of each device is identical to the procedure described in the *Device Selection Guide* section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the *Detailed Design Procedure* section for single device for detailed information.

Based on Figure 32, the TCA9802 or the TCA9803 are the devices which are able to meet the design requirements. The TCA9802 is the most optimized selection, but the TCA9803 can be used without issue.

Based on Figure 33, all 4 variants of the TCA980x family meet the design requirements. The TCA9800 is the most optimized selection, but any of the variants can be used without issue.

As the system designer, the choice can be made to go for the most optimized part selections (TCA9802 for bus B and TCA9800 for bus C), but it is also ok to use the TCA9802 or the TCA9803 on both busses, because they both satisfy the design requirements of both busses.

10.2.3.3 Application Curves

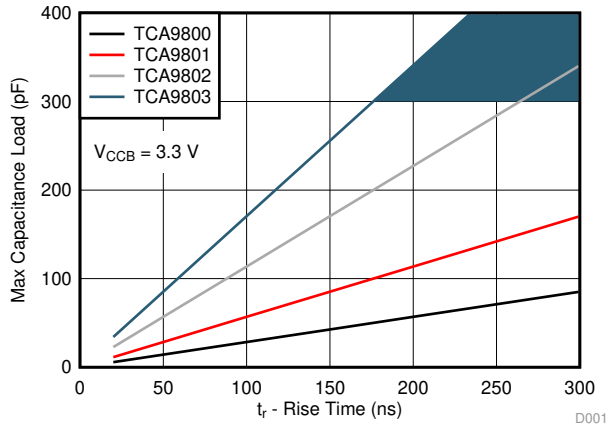


Figure 32. Selection Guide Based On Example Design Requirements for Bus B

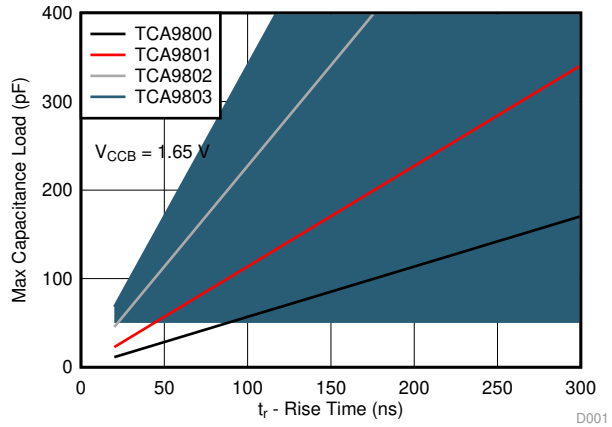


Figure 33. Selection Guide Based On Example Design Requirements for Bus C

10.2.4 Series Device Use Case

The TCA980x family supports multiple TCA980x used in series. It is acceptable to connect A sides together, or have A sides connect to B sides, but B-sides may never be connected together.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the I_{EXT-I} section.

NOTE: B-sides of TCA980x devices may never be connected to each other, because the I_{EXT-I} specification limit is violated. See the I_{EXT-I} for more information.

NOTE: The B-side may not be connected to another translator if it uses a static-voltage offset. The R_{ILC} spec is violated since the static voltage offset adjusts the output resistance to ground to be outside of the R_{ILC} spec requirement, causing the TCA980x to be unable to recognize a low.

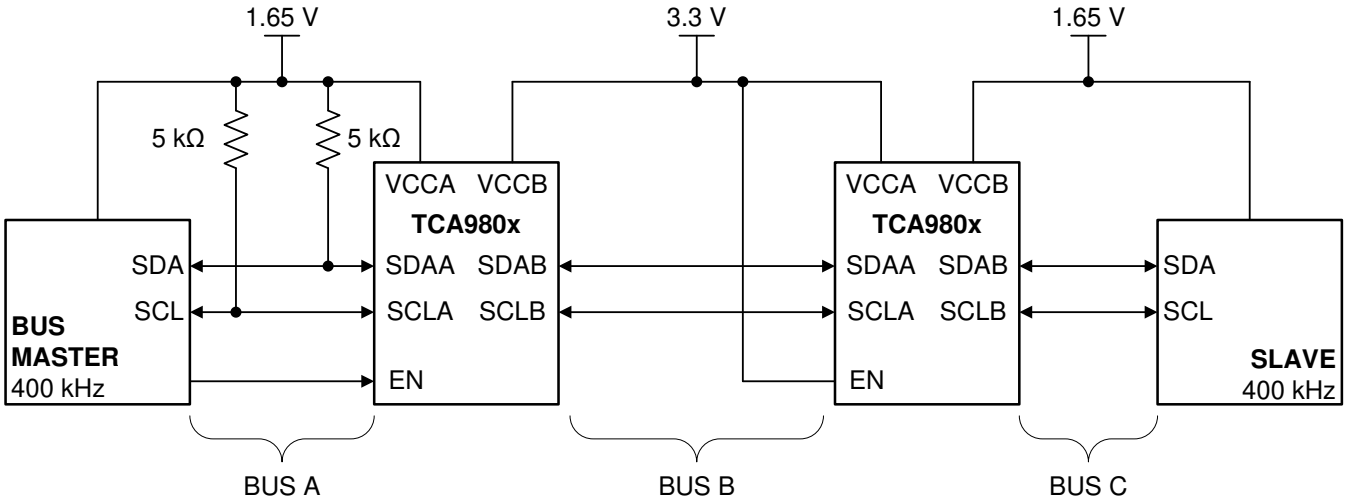


Figure 34. Series Use Case

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 µF and 0.1 µF) must be placed close to each power supply pin.

10.2.4.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in Table 10 and Table 11 must be known. The setup in Figure 34 is used for these example design requirements.

Table 10. Design Requirements for Bus B / 1st TCA980x

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	300 pF
t_r	Rise time	up to 300 ns	≤ 200 ns
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	1.65 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	3.3 V
f_{SCL}	I^2C clock frequency		400 kHz

Table 11. Design Requirements for Bus C / 2nd TCA980x

Parameter	Description	Acceptable Range	Example Value/Target
C_L	Load capacitance (bus capacitance) on B-side	up to 400 pF	100 pF
t_r	Rise time	up to 300 ns	≤ 250 ns
V_{CCA}	VCCA supply voltage	0.8 V-3.6 V	3.3 V
V_{CCB}	VCCB supply voltage	1.65 V-3.6 V	1.65 V
f_{SCL}	I^2C clock frequency		400 kHz

10.2.4.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side (Bus A) is well documented already, see the *I2C Bus Pullup Resistor Calculation* application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Selection process of each device is identical to the procedure described in the *Device Selection Guide* section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the *Detailed Design Procedure* section for single device for detailed information.

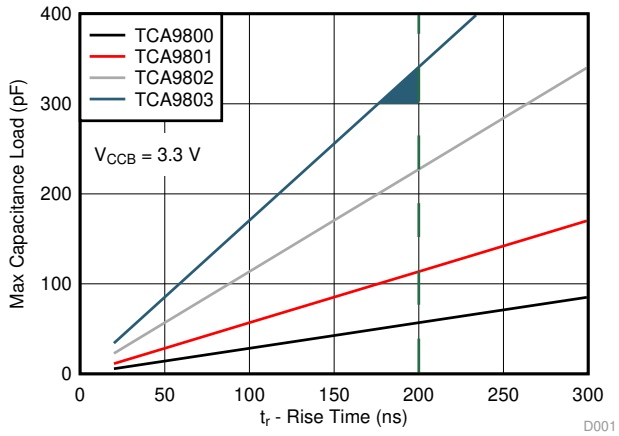


Figure 35. Selection Guide Based On Example Design Requirements for Bus B

Based on Figure 35, the TCA9803 is the only device which can satisfy the design requirements. Had the rise time requirement been ≤ 300 ns, then the TCA9802 also works, but the design requirement was 200 ns.

Based on Figure 36, all 4 variants of the TCA980x family meet the design requirements. The TCA9800 is the most optimized selection, but any of the variants can be used without issue.

As the system designer, the choice can be made to go for the most optimized part selections (TCA9803 for bus B and TCA9800 for bus C), but it is also ok to use the TCA9803 on both busses, because it can satisfy the design requirements of both busses.

10.2.4.3 Application Curve

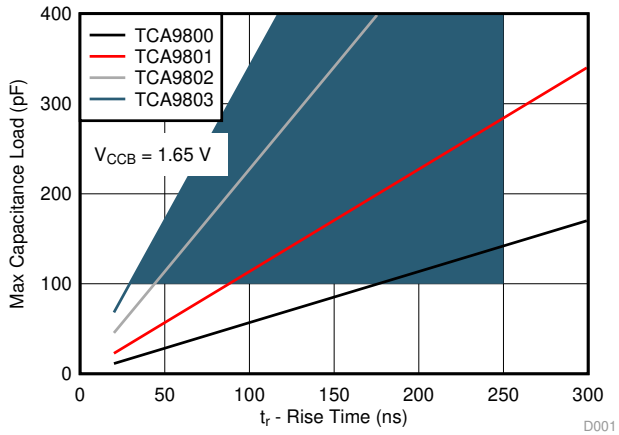


Figure 36. Selection Guide Based on Example Design Requirements for Bus C

11 Power Supply Recommendations

The following need to be ensured when designing with the TCA980x family:

- V_{CCA} is within the recommended voltage range
- V_{CCB} is within the recommended voltage range

There are no supply sequencing requirements, V_{CCA} may ramp before, after, or at the same time as V_{CCB}.

There are no supply dependency requirements. V_{CCA} may be greater than, less than, or equal to V_{CCB}. Each supply has its own requirement of voltage range, but there is no required relationship between V_{CCA} and V_{CCB} values.

It is recommended that decoupling capacitors be used on the power supplies (0.1 µF and 1 µF) and that they be placed as close as possible to the VCCA and VCCB pins.

12 Layout

12.1 Layout Guidelines

There are no special considerations required for most I^2C translators, but there are common practices which are always recommended.

It is recommended that decoupling capacitors be used on the power supplies (0.1 µF and 1 µF) and that they be placed as close as possible to the VCCA and VCCB pins.

12.2 Layout Example

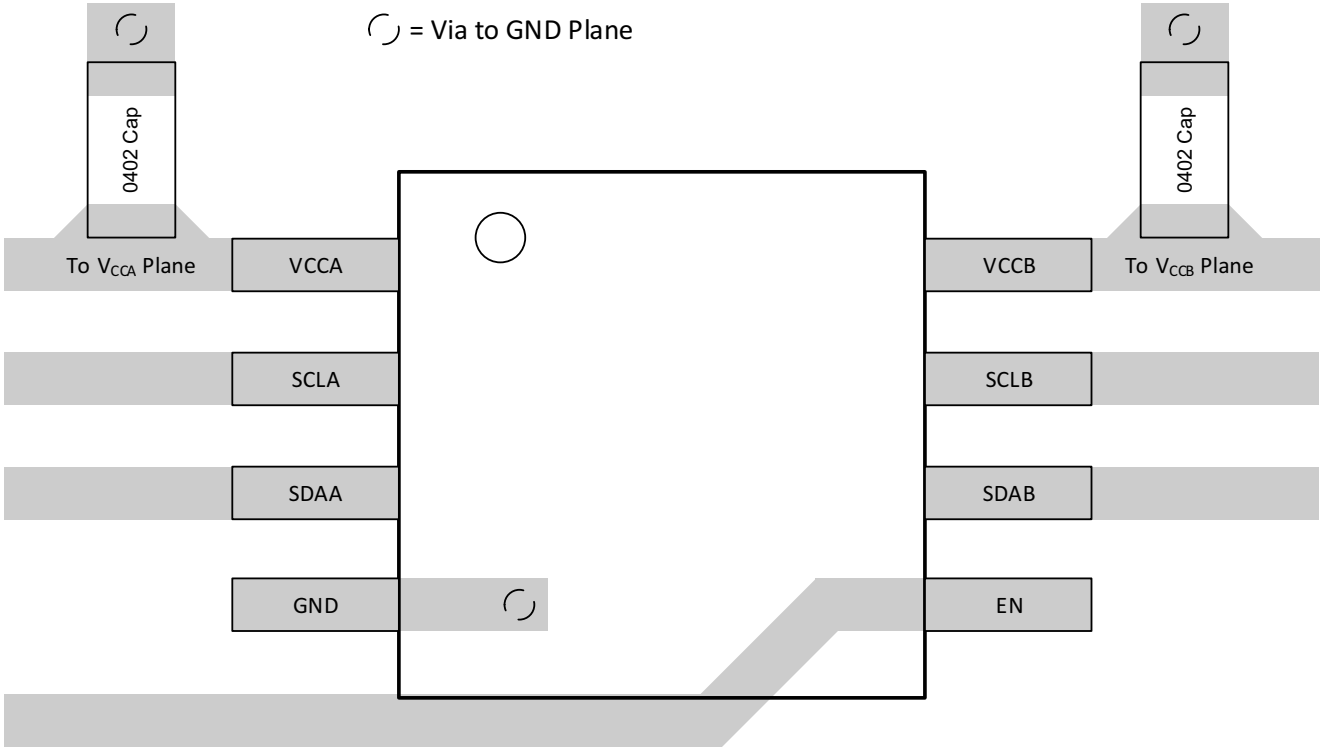


Figure 37. TCA980x DGK Layout Example

13 器件和文档支持

13.1 文档支持

相关文档请参见以下部分：

- *《I2C 总线上拉电阻计算》*
- *《I2C 总线在采用中继器时的最高时钟频率》*
- *《逻辑器件简介》*
- *《理解 I2C 总线》*
- *《为新设计挑选合适的 I2C 器件》*

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 商标

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9800DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	15B
TCA9800DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15B
TCA9800DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	15B
TCA9800DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

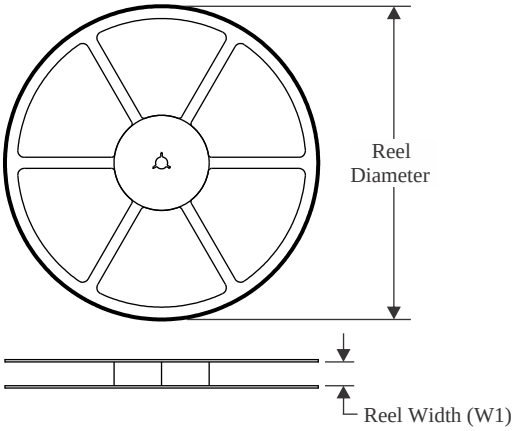
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

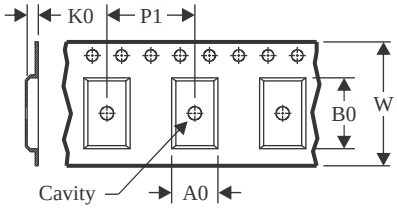
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

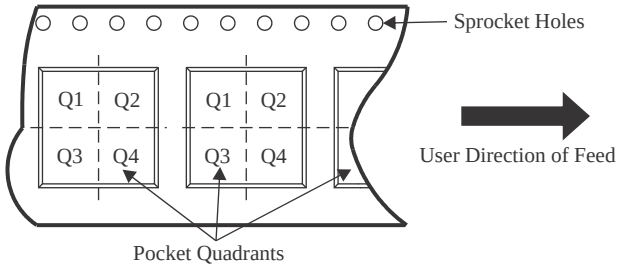


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

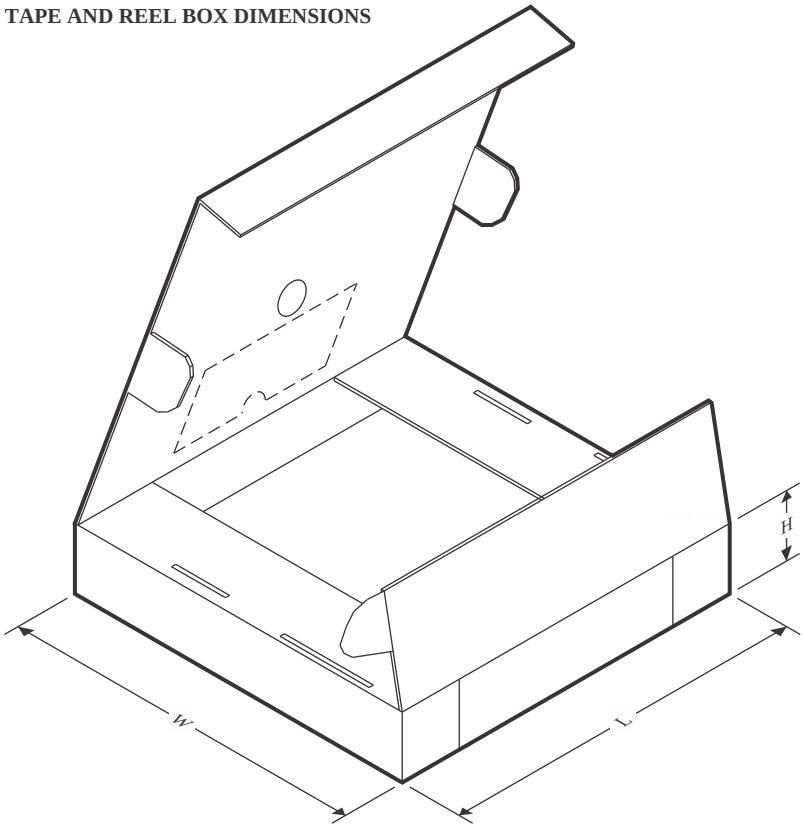
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9800DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9800DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

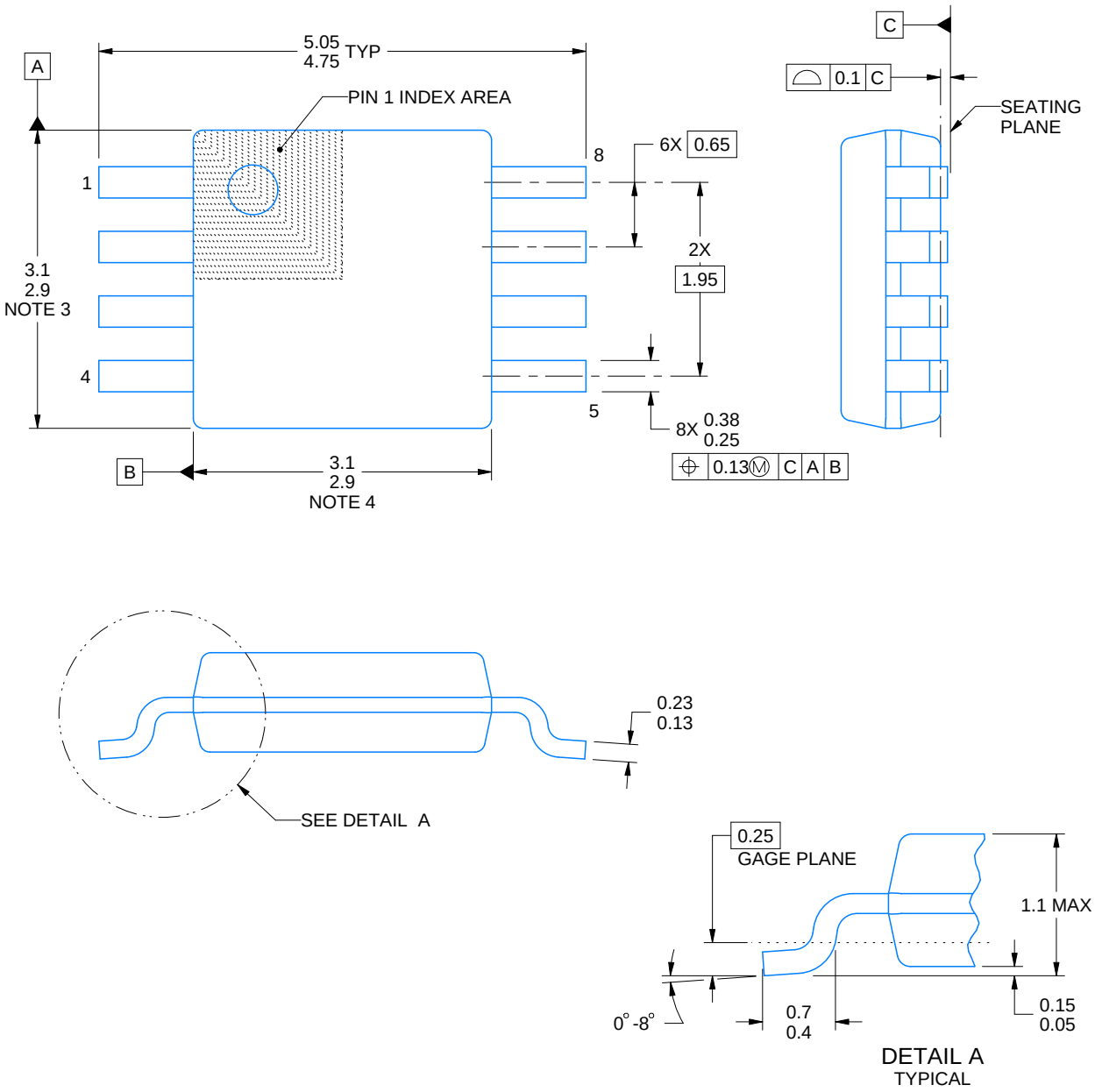
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9800DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TCA9800DGKT	VSSOP	DGK	8	250	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

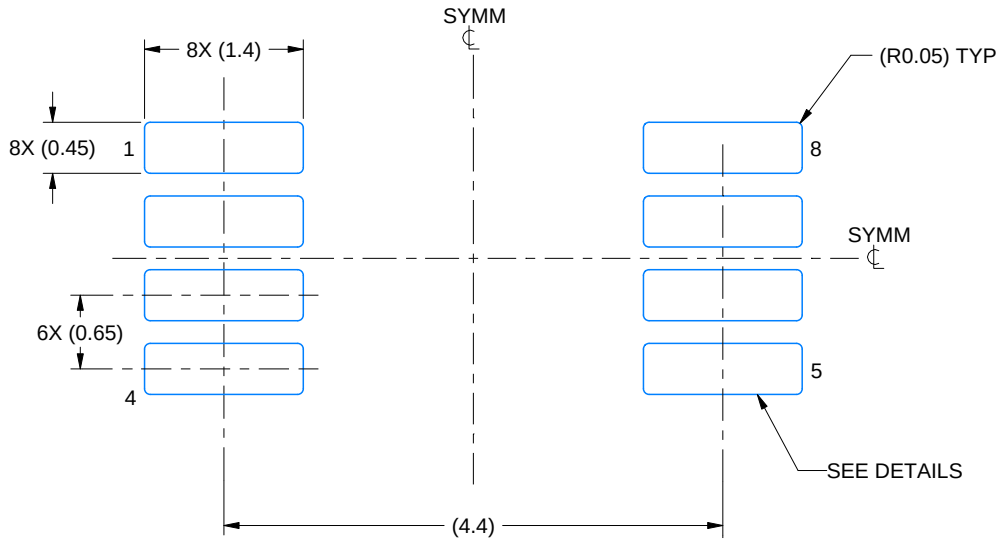
SMALL OUTLINE PACKAGE



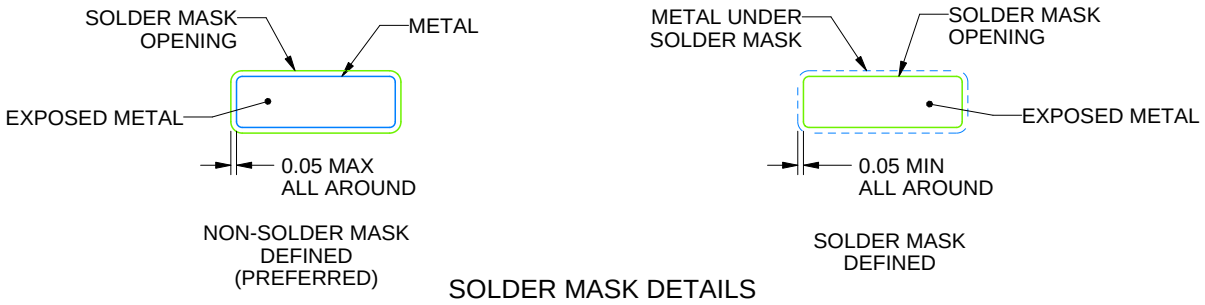
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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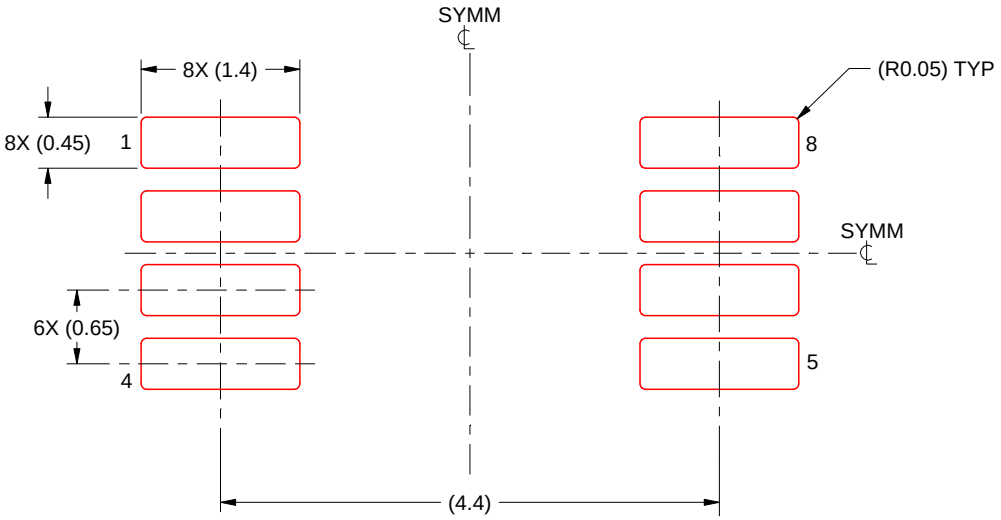
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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