

## TCA9517 电平转换 I<sup>2</sup>C 总线中继器

### 1 特性

- 双通道双向缓冲器
- 与 I<sup>2</sup>C 总线和系统管理总线 (SMBus) 兼容
- 在 A 侧上, 运行电源电压范围为 0.9V 至 5.5V
- 在 B 侧上, 运行电源电压范围为 2.7V 至 5.5V
- 从 0.9V-5.5V 到 2.7V-5.5V 的电压电平转换
- 针对 PCA9515B 的封装和功能替代产品
- 高电平有效中继器启用输入
- 漏极开路 I<sup>2</sup>C I/O
- 5.5V 耐压 I<sup>2</sup>C 和使能输入支持混合模式信号操作
- 适用于标准模式和快速模式 I<sup>2</sup>C 器件和多重主器件
- 器件断电时 I<sup>2</sup>C 引脚呈高阻态
- 锁断性能超过 100mA, 符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 5500V 人体放电模式 (A114-A)
  - 200V 机器放电模式 (A115-A)
  - 1000V 组件充电模式 (C101)

### 2 应用

- 服务器
- 路由器 (电信交换设备)
- 工业设备
- 具有多个 I<sup>2</sup>C 从器件和/或印刷电路板 (PCB) 走线较长的产品

### 3 说明

TCA9517 是一款具有电平转换功能的双向缓冲器, 适用于 I<sup>2</sup>C 和 SMBus 系统。此器件可在混合模式应用中提供低电压 (低至 0.9V) 和较高电压 (2.7V 至 5.5V) 间的双向电压电平转换 (上行转换/下行转换)。应用中的杂音问题。该器件能够扩展 I<sup>2</sup>C 和 SMBus 系统, 甚至在电平转换期间也不会影响系统性能。

TCA9517 可缓冲 I<sup>2</sup>C 总线上的串行数据 (SDA) 和串行时钟 (SCL) 信号, 因此允许 I<sup>2</sup>C 应用中的两条总线连接高达 400pF 的总线电容。

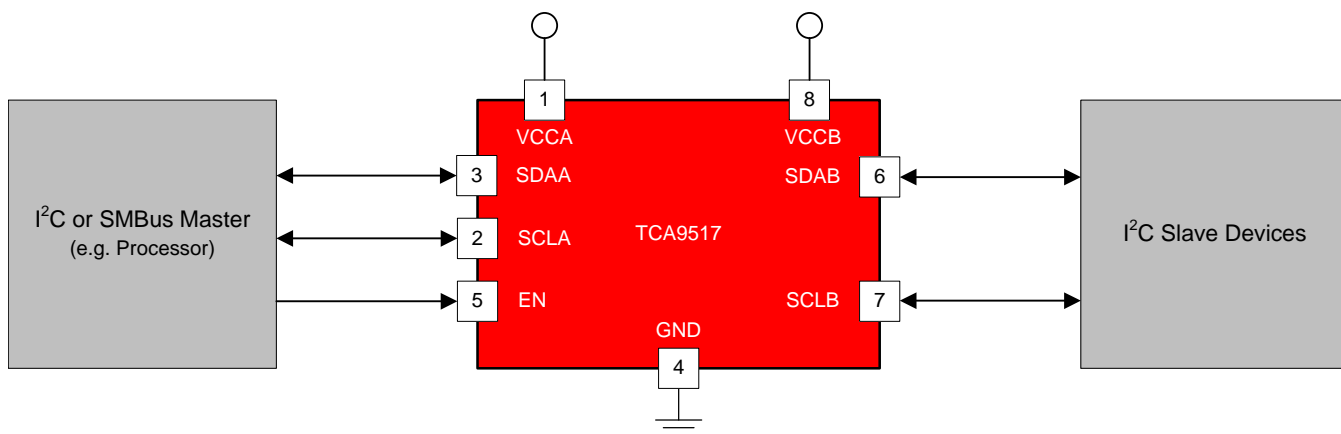
TCA9517 具有两类驱动器: A 侧驱动器和 B 侧驱动器。所有输入和 I/O 均可耐受 5.5V 过压, 甚至在器件断电时 ( $V_{CCB}$  和/或  $V_{CCA} = 0V$ ) 也如此。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TCA9517	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化的原理图



## 目录

<b>1</b>	特性 .....	<b>1</b>	9.1	Overview .....	<b>10</b>
<b>2</b>	应用 .....	<b>1</b>	9.2	Functional Block Diagram .....	<b>10</b>
<b>3</b>	说明 .....	<b>1</b>	9.3	Feature Description .....	<b>11</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	9.4	Device Functional Modes .....	<b>11</b>
<b>5</b>	说明 (续) .....	<b>3</b>	<b>10</b>	<b>Application and Implementation</b> .....	<b>12</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>4</b>	10.1	Application Information .....	<b>12</b>
<b>7</b>	<b>Specifications</b> .....	<b>4</b>	10.2	Typical Application .....	<b>12</b>
7.1	Absolute Maximum Ratings .....	<b>4</b>	<b>11</b>	<b>Power Supply Recommendations</b> .....	<b>15</b>
7.2	ESD Ratings .....	<b>5</b>	<b>12</b>	<b>Layout</b> .....	<b>16</b>
7.3	Recommended Operating Conditions .....	<b>5</b>	12.1	Layout Guidelines .....	<b>16</b>
7.4	Thermal Information .....	<b>5</b>	12.2	Layout Example .....	<b>16</b>
7.5	Electrical Characteristics .....	<b>6</b>	<b>13</b>	<b>器件和文档支持</b> .....	<b>17</b>
7.6	Timing Requirements .....	<b>6</b>	13.1	社区资源 .....	<b>17</b>
7.7	I <sup>2</sup> C Interface Switching Characteristics .....	<b>7</b>	13.2	商标 .....	<b>17</b>
7.8	Typical Characteristics .....	<b>8</b>	13.3	静电放电警告 .....	<b>17</b>
<b>8</b>	<b>Parameter Measurement Information</b> .....	<b>9</b>	13.4	Glossary .....	<b>17</b>
<b>9</b>	<b>Detailed Description</b> .....	<b>10</b>	<b>14</b>	<b>机械、封装和可订购信息</b> .....	<b>17</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision C (June 2015) to Revision D Page

- Deleted  $V_{CCA} < V_{CCB}$  from the *Design Requirements* list ..... **12**

### Changes from Revision B (May 2013) to Revision C Page

- 已添加 引脚配置和功能部分、ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 ..... **1**
- 删除了订购信息表。 ..... **3**

### Changes from Revision A (April 2013) to Revision B Page

- 更新了订购信息表的顶部标记列。 ..... **1**

### Changes from Original (December 2012) to Revision A Page

- 在文档中增加了 D 封装。 ..... **1**
- 更新了订购信息表的顶部标记列。 ..... **1**

## 5 说明（续）

**B** 侧上的缓冲器设计类型使其无法与使用静态电压偏移的器件串联使用。这是因为这类器件并不将经缓冲的低电平信号识别为有效低电平，并且不再将其作为经缓冲的低电平进行传送。

**B** 侧驱动器运行电压介于 **2.7V** 至 **5.5V** 之间。针对这个内部缓冲器的输出低电平大约为 **0.5V**，但是当输出在内部被驱动为低电平时，输入电压必须比输出低电平低 **70mV** 或者更多。更高的电压低信号被称为经缓冲的低电平。当 **B** 侧 I/O 被内部驱动为低电平时，输入并不将此低电平识别为低电平。当输入低电平状态被释放时，这一特性防止了锁定情况的发生。

**A** 侧驱动器运行电压介于 **0.9V** 至 **5.5V** 之间并且能够驱动更大电流。它们不需要经缓冲的低电平特性（或者静态偏移电压）。这意味着，**B** 侧上的低电平信号将转换为 **A** 侧上接近 **0V** 的低电平，以适应低压逻辑的较小电压摆幅。**A** 侧上的输出下拉电阻会驱动一个“硬”低电平，输入电平会设置在  $0.3 \times V_{CCA}$  以满足低压侧电源电压低至 **0.9V** 的系统对于较低低电平的需求。

可将 **A** 侧作为公共总线，将两个或两个以上的 **TCA9517** 的 **A** 侧连接在一起，从而实现多个拓扑结构（请参阅 [图 8](#) 和 [图 9](#)）。此外，还可以将 **A** 侧直接连接至任意具有静态或动态偏移电压的其他缓冲器。可以将多个 **TCA9517** 串联在一起（相邻器件间通过 **A** 侧和 **B** 侧相连），偏移电压不会增大，只是需要考虑飞行时间延迟。由于 **B** 侧缓冲低电压的原因，**TCA9517** 不能通过 **B** 侧相连。**B** 侧不能连接配有上升时间加速器的器件。

**VCCA** 只能用于为 **A** 侧输入比较器提供  $0.3 \times V_{CCA}$  参考电压，或者用于电源正常状态检测电路。**TCA9517** 逻辑和所有 I/O 均由 **VCCB** 引脚供电。

当与标准 **I<sup>2</sup>C** 系统一同工作时，需要用上拉电阻在经缓冲的总线上提供逻辑高电平。**TCA9517** 具有 **I<sup>2</sup>C** 总线的标准漏极开路配置。这些上拉电阻器的尺寸由系统决定，然而，中继器的每一侧都必须有一个上拉电阻器。此器件专为与标准模式及快速模式 **I<sup>2</sup>C** 器件（而不单是 **SMBus** 器件）一起工作而设计。在可以接受标准模式器件和多个主控器的通用型 **IC** 系统中，标准模式 **I<sup>2</sup>C** 器件的额定值仅为 **3mA**。在特定条件下，可以采用更高的终止电流。

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9 V to 5.5 V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to $V_{CCA}$ through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to $V_{CCA}$ through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to $V_{CCB}$ through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to $V_{CCB}$ through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7 V to 5.5 V)

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCB}$	Supply voltage range	-0.5	7	V
$V_{CCA}$	Supply voltage range	-0.5	7	V
$V_I$	Enable input voltage range <sup>(2)</sup>	-0.5	7	V
$V_{I/O}$	I <sup>2</sup> C bus voltage range <sup>(2)</sup>	-0.5	7	V
$I_{IK}$	Input clamp current		-50	mA
$I_{OK}$	Output clamp current		-50	
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±5500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (A115-A)	±200

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage, A-side bus	0.9 <sup>(1)</sup>	5.5	V
V <sub>CCB</sub>	Supply voltage, B-side bus	2.7	5.5	V
V <sub>IH</sub>	High-level input voltage	SDAA, SCLA	0.7 × V <sub>CCA</sub>	5.5
		SDAB, SCLB	0.7 × V <sub>CCB</sub>	5.5
		EN	0.7 × V <sub>CCB</sub>	5.5
V <sub>IL</sub>	Low-level input voltage	SDAA, SCLA	0.3 × V <sub>CCA</sub>	V
		SDAB, SCLB <sup>(2)</sup>	0.3 × V <sub>CCB</sub>	
		EN	0.3 × V <sub>CCB</sub>	
I <sub>OL</sub>	Low-level output current		6	mA
T <sub>A</sub>	Operating free-air temperature	−40	85	°C

(1) Low-level supply voltage

(2) V<sub>IL</sub> specification is for the first low level seen by the SDAB and SCLB lines. V<sub>ILC</sub> is for the second and subsequent low levels seen by the SDAB and SCLB lines. See [V<sub>ILC</sub> and Pullup Resistor Sizing](#) for V<sub>ILC</sub> application information

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TCA9517		UNIT	
	DGK (VSSOP)	D (SOIC)		
	8 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	187.6	133.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	59.3	87.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	108.6	74.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.4	36.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	106.9	73.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

 $V_{CCB} = 2.7\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CCB}$	MIN	TYP	MAX	UNIT	
$V_{IK}$	Input clamp voltage	$I_I = -18\text{ mA}$	2.7 V to 5.5 V			-1.2	V	
$V_{OL}$	Low-level output voltage	SDAB, SCLB $I_{OL} = 100\ \mu\text{A}$ or $6\text{ mA}$ , $V_{ILA} = V_{ILB} = 0\text{ V}$	2.7 V to 5.5 V	0.45	0.52	0.6	V	
		SDAA, SCLA $I_{OL} = 6\text{ mA}$			0.1	0.2		
$V_{OL} - V_{ILC}$	Low-level input voltage below low-level output voltage	SDAB, SCLB ensured by design	2.7 V to 5.5 V		70		mV	
$V_{ILC}$	SDA and SCL low-level input voltage contention	SDAB, SCLB	2.7 V to 5.5 V		0.4		V	
$I_{CC}$	Quiescent supply current for $V_{CCA}$	Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA	
		Both channels high, SDAA = SCLA = $V_{CCA}$ and SDAB = SCLB = $V_{CCB}$ and EN = $V_{CCB}$	5.5 V		1.5	5		
		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5		
$I_{CC}$	Quiescent supply current	In contention, SDAA = SCLA = GND and SDAB = SCLB = GND	5.5 V		3	5	mA	
$I_I$	Input leakage current	SDAB, SCLB	2.7 V to 5.5 V	$V_I = V_{CCB}$		$\pm 1$	$\mu\text{A}$	
				$V_I = 0.2\text{ V}$		10		
		SDAA, SCLA		$V_I = V_{CCB}$		$\pm 1$		
				$V_I = 0.2\text{ V}$		10		
		EN		$V_I = V_{CCB}$		$\pm 1$		
				$V_I = 0.2\text{ V}$		-10 -30		
$I_{OH}$	High-level output leakage current	SDAB, SCLB	2.7 V to 5.5 V	$V_O = 3.6\text{ V}$		10	$\mu\text{A}$	
		SDAA, SCLA			10			
$C_I$	Input capacitance	EN	3.3 V		6	10	pF	
		SCLA, SCLB	3.3 V		8	13		
$C_{IO}$	Input/output capacitance	SDAA, SDAB	3.3 V		8	13	pF	
			0 V		7	11		

## 7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$t_{su}$	Setup time, EN high before Start condition <sup>(1)</sup>	100		ns
$t_h$	Hold time, EN high after Stop condition <sup>(1)</sup>	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

## 7.7 I<sup>2</sup>C Interface Switching Characteristics

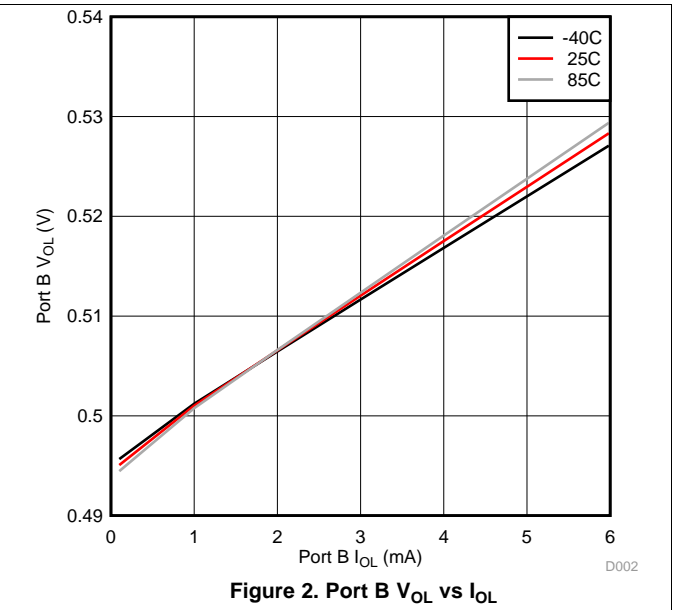
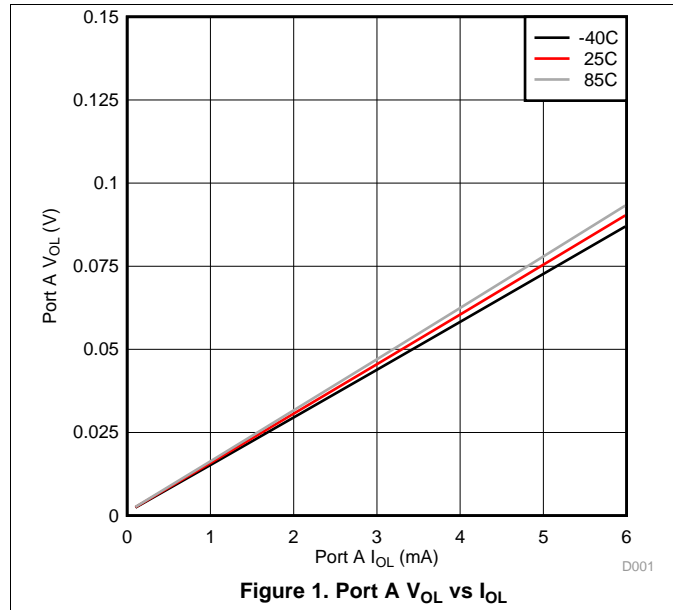
 $V_{CCB} = 2.7\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP <sup>(3)</sup>	MAX	UNIT	
$t_{PLZ}$	Propagation delay	SDAB, SCLB <sup>(4)</sup> (see Figure 6)	SDAA, SCLA <sup>(4)</sup> (see Figure 6)		80	141	250	ns	
		SDAA, SCLA <sup>(5)</sup> (see Figure 5)	SDAB, SCLB <sup>(5)</sup> (see Figure 5)		25	74	110		
$t_{PZL}$	Propagation delay	SDAB, SCLB	SDAA, SCLA	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 4)	30	76 <sup>(6)</sup>	110	ns	
				$V_{CCA} \geq 3\text{ V}$ (see Figure 4)	10	86	230		
		SDAA, SCLA <sup>(5)</sup> (see Figure 5)	SDAB, SCLB <sup>(5)</sup> (see Figure 5)		60	107	230		
$t_{TLH}$	Transition time	B-side to A side	80%	20%	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 5)	10	12	15	ns
					$V_{CCA} \geq 3\text{ V}$ (see Figure 5)	40	42	45	
						110	125	140	
$t_{THL}$	Transition time	B-side to A side	80%	20%	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 5)	1	52 <sup>(6)</sup>	105	ns
					$V_{CCA} \geq 3\text{ V}$ (see Figure 5)	20	67	175	
						30	48	90	
	A side to B-side (see Figure 4)								

- (1) Times are specified with loads of 1.35-k $\Omega$  pull-up resistance and 50-pF load capacitance on the B-side and 167- $\Omega$  pull-up and 57-pF load capacitance on the A side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
- (2) pull-up voltages are  $V_{CCA}$  on the A side and  $V_{CCB}$  on the B-side.
- (3) Typical values were measured with  $V_{CCA} = V_{CCB} = 3.3\text{ V}$  at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.
- (4) The  $t_{PLH}$  delay data from B to A side is measured at 0.4 V on the B-side to 0.5  $V_{CCA}$  on the A side when  $V_{CCA}$  is less than 2 V, and 1.5 V on the A side if  $V_{CCA}$  is greater than 2 V.
- (5) The proportional delay data from A to B-side is measured at 0.3  $V_{CCA}$  on the A side to 1.5 V on the B-side.
- (6) Typical value measured with  $V_{CCA} = 2.7\text{ V}$  at  $T_A = 25^\circ\text{C}$

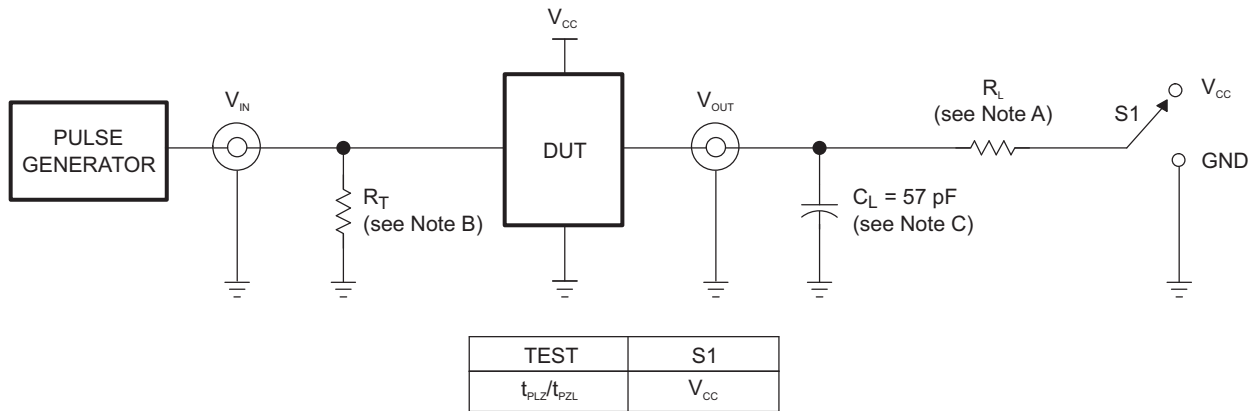
## 7.8 Typical Characteristics

$V_{CCA} = 0.9\text{ V}$ ,  $V_{CCB} = 2.7\text{ V}$





## 8 Parameter Measurement Information



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

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- A.  $R_L = 167 \Omega$  (0.9 V to 2.7 V) and  $R_L = 450 \Omega$  (3.0 V to 5.5 V) on the A side and 1.35 k $\Omega$  on the B-side
- B.  $R_T$  termination resistance should be equal to  $Z_{OUT}$  of pulse generators.
- C.  $C_L$  includes probe and jig capacitance.
- D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq 1$  V/ns.
- E. The outputs are measured one at a time, with one transition per measurement.
- F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- G.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- H.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

Figure 3. Test Circuit

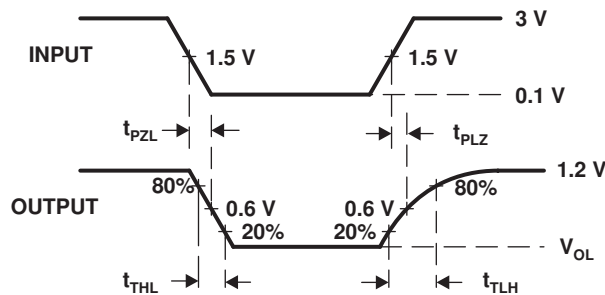


Figure 4. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

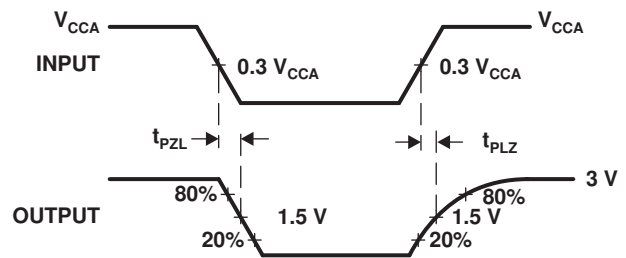


Figure 5. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

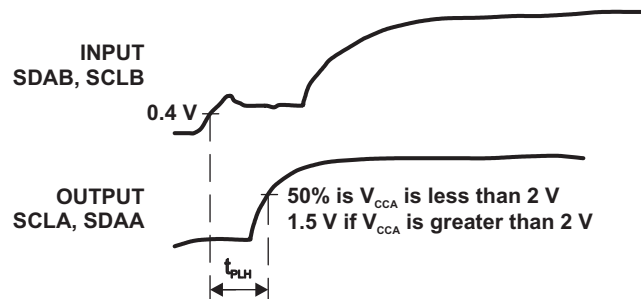


Figure 6. Waveform 3 – Propagation Delay for B-side to A-side

## 9 Detailed Description

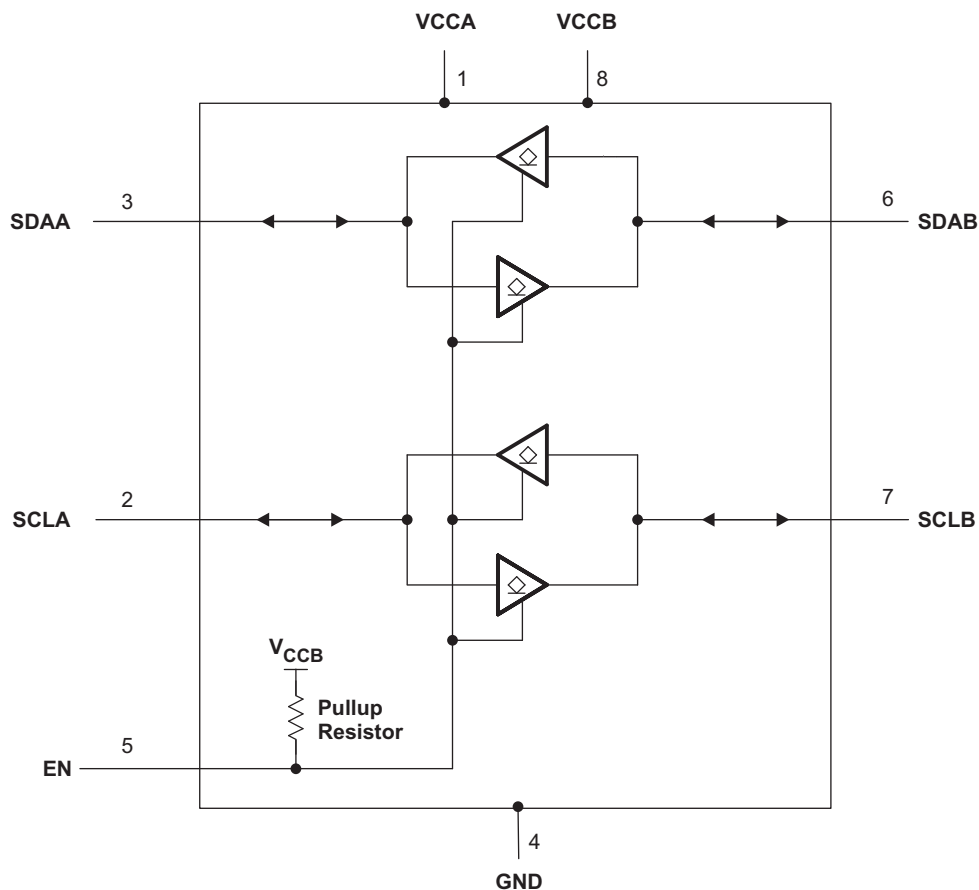
### 9.1 Overview

The TCA9517 is a bidirectional buffer with level shifting capabilities for I<sup>2</sup>C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I<sup>2</sup>C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I<sup>2</sup>C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I<sup>2</sup>C application.

The TCA9517 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered ( $V_{CCB}$  and/or  $V_{CCA} = 0$  V).

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Two-Channel Bidirectional Buffer

The TCA9517 is a two-channel bidirectional buffer with level-shifting capabilities

### 9.3.2 Active-High Repeater-Enable Input

The TCA9517 has an active-high enable (EN) input with an internal pull-up to  $V_{CCB}$ , which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

### 9.3.3 $V_{OL}$ B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

### 9.3.4 Standard Mode and Fast Mode Support

The TCA9517 supports standard mode as well as fast mode I<sup>2</sup>C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

### 9.3.5 Clock Stretching Support

The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

## 9.4 Device Functional Modes

**Table 1. Function Table**

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

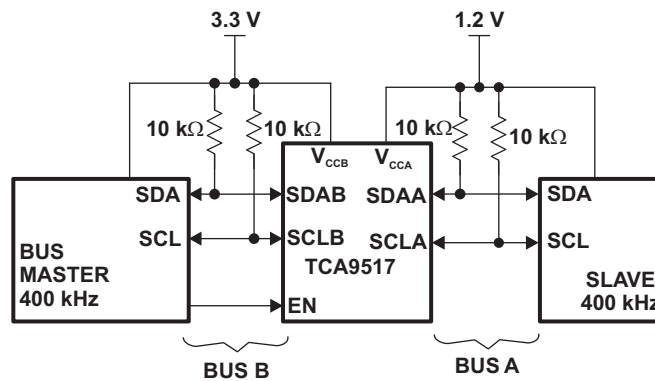
A typical application is shown in [Figure 7](#). In this example, the system master is running on a 3.3 V I<sup>2</sup>C bus, and the slave is connected to a 1.2 V I<sup>2</sup>C bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the TCA9517 is pulled low by a driver on the I<sup>2</sup>C bus, a comparator detects the falling edge when it goes below  $0.3 \times V_{CCA}$  and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to [Figure 9](#) and [Figure 10](#). If the bus master in [Figure 7](#) were to write to the slave through the TCA9517, waveforms shown in [Figure 9](#) would be observed on the A bus. This looks like a normal I<sup>2</sup>C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517, the clock and data lines would have a positive offset from ground equal to the  $V_{OL}$  of the TCA9517. After the eighth clock pulse, the data line is pulled to the  $V_{OL}$  of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517 for a short delay, while the A-bus side rises above  $0.3 \times V_{CCA}$  and then continues high.

### 10.2 Typical Application



**Figure 7. Typical Application Schematic**

#### 10.2.1 Design Requirements

For the level translating application, the following should be true:

- $V_{CCA} = 0.9 \text{ V to } 5.5 \text{ V}$
- $V_{CCB} = 2.7 \text{ to } 5.5 \text{ V}$
- B-side ports must not be connected together

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Clock Stretching Support

The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

#### 10.2.2.2 $V_{ILC}$ and Pullup Resistor Sizing

For the TCA9517 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level ( $V_{ILC}$ ). This means that the  $V_{OL}$  of any device on the B-side must be below 0.4 V.

$V_{OL}$  of a device can be adjusted by changing the  $I_{OL}$  through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

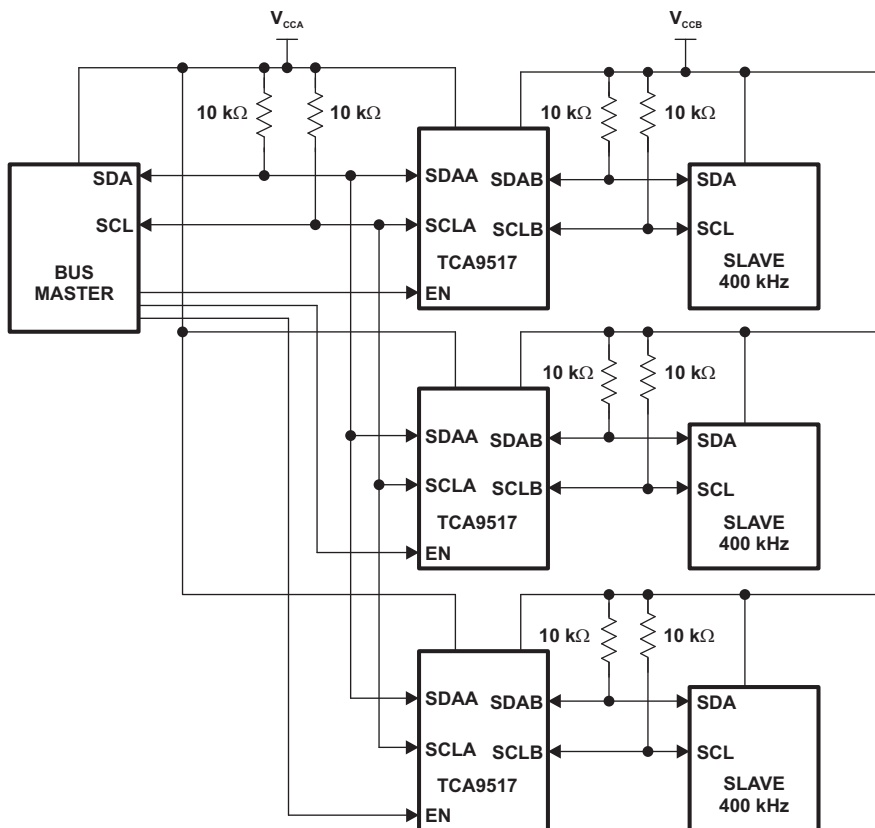


Figure 8. Typical Star Application

Multiple A sides of TCA9517 s can be connected in a star configuration, allowing all nodes to communicate with each other.

Typical Application (continued)

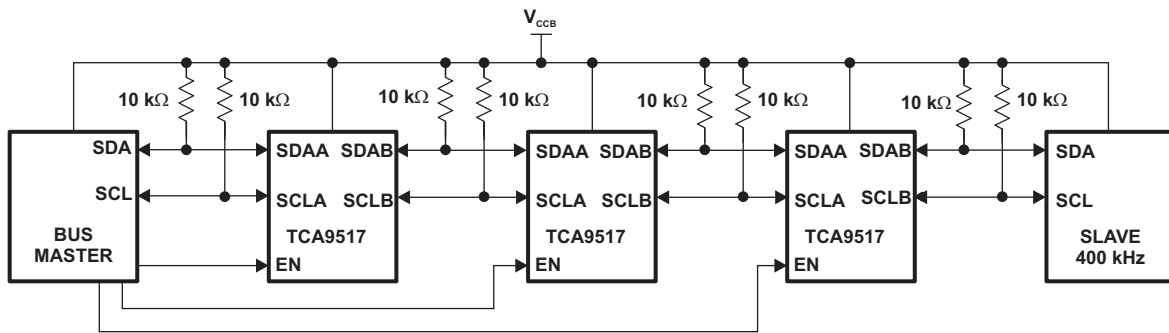


Figure 9. Typical Series Application

To further extend the I<sup>2</sup>C bus for long traces/cables, multiple TCA9517 s can be connected in series as long as the A-side is connected to the B-side. I<sup>2</sup>C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

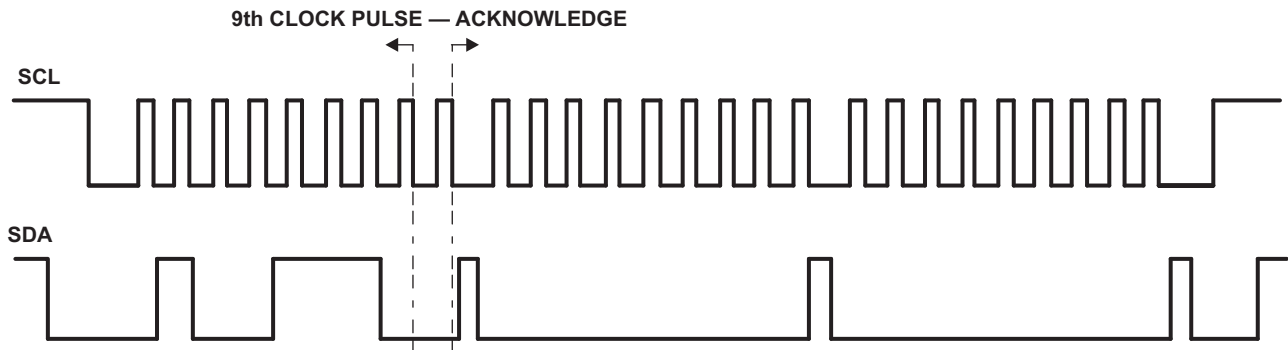


Figure 10. Bus A (0.9 V to 5.5 V Bus) Waveform

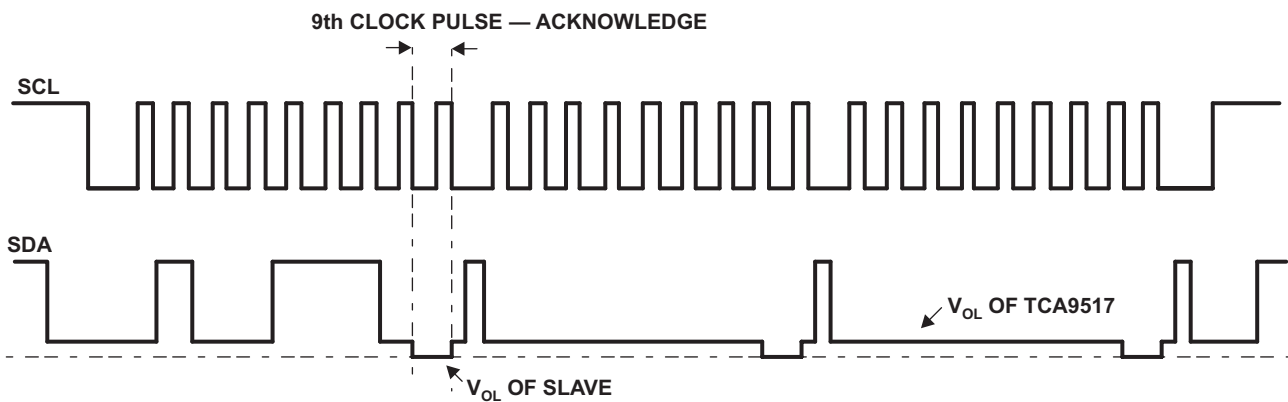
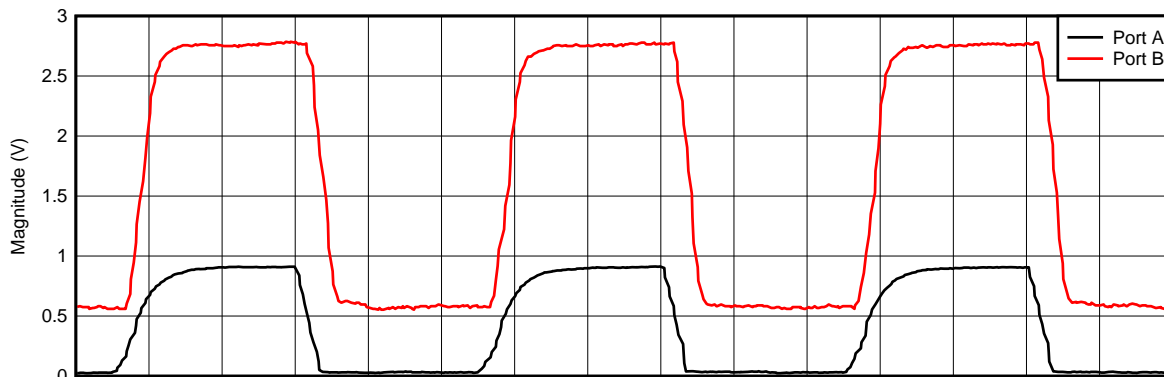


Figure 11. Bus B (2.7 V to 5.5 V Bus) Waveform

**Typical Application (continued)**

**10.2.3 Application Curve**



D003

**Figure 12. Voltage Translation at 400 kHz,  $V_{CCA} = 0.9\text{ V}$ ,  $V_{CCB} = 2.7\text{ V}$**

**11 Power Supply Recommendations**

$V_{CCB}$  and  $V_{CCA}$  can be applied in any sequence at power up. The TCA9517 includes a power-up circuit that keeps the output drivers turned off until  $V_{CCB}$  is above 2.5 V and the  $V_{CCA}$  is above 0.8 V. After power up and with the EN high, a low level on the A-side (below  $0.3 \times V_{CCA}$ ) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above  $0.3 \times V_{CCA}$ , the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below  $0.3 \times V_{CCB}$ , the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above  $0.7 \times V_{CCB}$ . If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above  $0.3 \times V_{CCA}$ .

TI recommends using a decoupling capacitor and placing it close to the  $V_{CCA}$  and  $V_{CCB}$  pins of a value of about 100 nF.

## 12 Layout

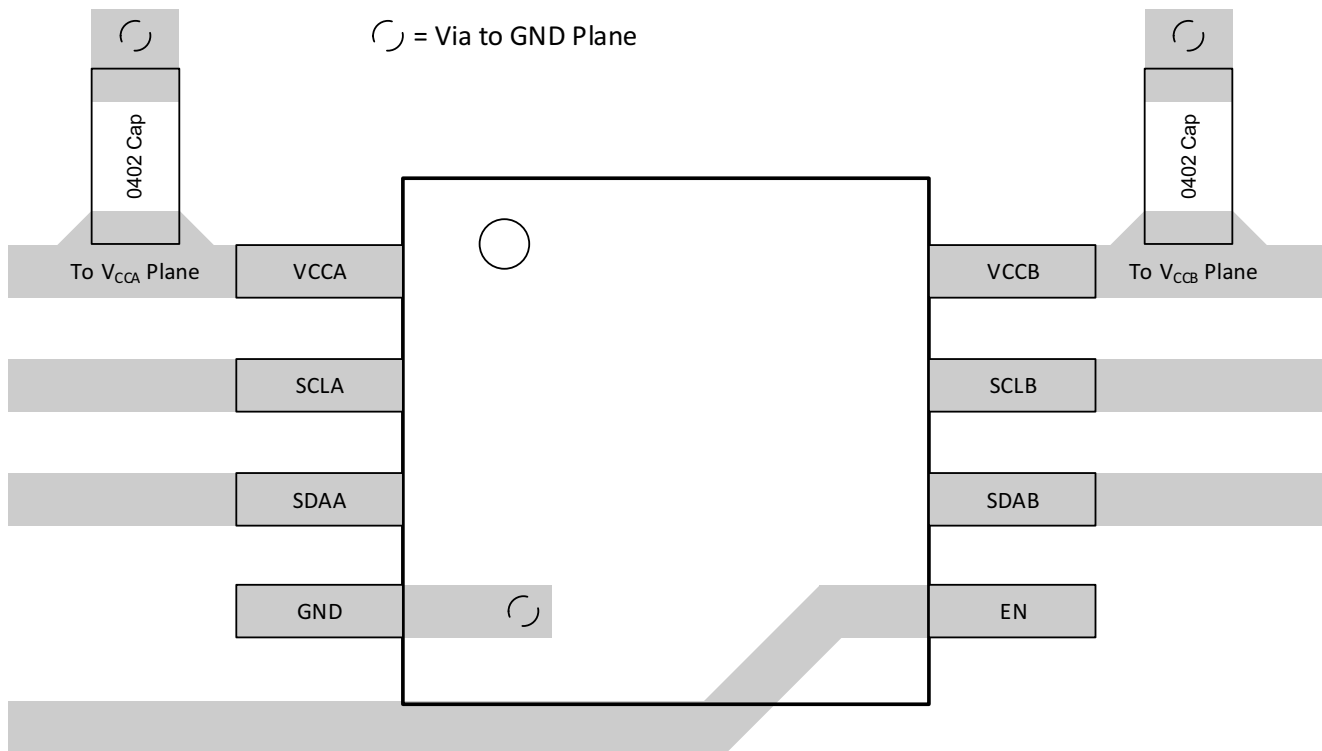
### 12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517 .

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

### 12.2 Layout Example

Figure 13 shows an example layout of the DGK package.



**Figure 13. TCA9517A Layout Example**



## 13 器件和文档支持

### 13.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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### 13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 13.4 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9517DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	-40 to 85	AYK	<a href="#">Samples</a>
TCA9517DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW517	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TCA9517 :**

- Automotive : [TCA9517-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9517DR	SOIC	D	8	2500	340.5	336.1	25.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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