

TAS6501-Q1 具有电流检测和实时负载诊断功能的 15W、2MHz 数字输入单通道汽车级无散热器 D 类音频放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
 - 温度等级 1：-40°C 至 +125°C，T_A
- 常规运行
 - 4.5V 至 19V 电源电压，40V 负载突降
 - 支持 1.8V 和 3.3V I/O
 - I²C 控制，具有 8 个地址选项
 - 14.4V 下的空闲功率损耗低于 0.5W，最大 PVDD 关断损耗低于 5uA
- 通过 I²S 或 TDM 进行输出电流检测
 - 无需外部电路
- 实时负载诊断
 - 播放音频时监控输出条件
 - 开路负载、短路负载、电源短路、接地短路检测
- 集成 DSP 处理
 - 热监控和折返
 - PVDD 监控和折返
 - 削波检测
 - 低延迟路径，在 48kHz 时信号延迟减少 70% 以上
- 直流和交流备用负载诊断
- 音频输入
 - I²S 和 TDM 支持高达 TDM16
 - 输入采样率：16、32、44.1、48、96、192kHz
- 音频输出
 - 384kHz 至 2MHz 可配置输出开关频率
 - 15W (14.4V、4Ω、10% THD+N)
- 音频性能
 - THD+N < 0.02% (4Ω, 1W, 1kHz)
 - 105dB 的信噪比 (SNR)
 - 输出噪声：14.4V 时为 41 μV_{RMS}，A 加权
- 保护
 - 输出短路保护
 - Speaker Guard™ Pro 功率限制器
 - 可配置的过热警告和关断
 - I²C 温度和电源电压读数
 - 直流失调电压，欠压和过压
- 可轻松满足 CISPR25-L5 EMC 规范要求
 - 高级展频

2 应用

- 声学车辆警报系统 (AVAS)
- 紧急呼叫 (eCall)
- 汽车音响主机
- 远程信息处理控制单元
- 汽车仪表组显示器

3 说明

TAS6501-Q1 是一款单通道、数字输入、D 类音频放大器，支持 2MHz 开关频率，可实现成本和尺寸优化的单通道音频放大器设计。该器件的工作电压范围为 4.5V 至 19V，可提供高达 15W (14.4V、4Ω、10% THD+N) 的功率。该器件集成了直流和交流负载诊断功能，可在启用输出级之前确定所连接负载的状态。此外，该器件还可以在 PLAY 模式下使用实时负载诊断（无论是否有音频）来监控输出负载状况，该诊断独立于主机和音频输入运行。

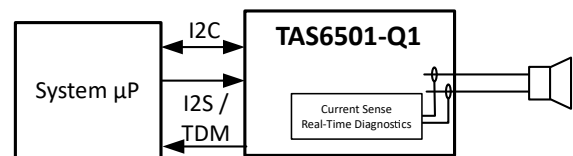
TAS6501-Q1 可以监测器件的输出电流、PVDD 电压和温度，并可以通过 TDM 或 I²S 报告这些数据。TAS6501-Q1 的集成 DSP 可实现高级保护功能，例如 PVDD 折返、热折返和 Speaker Guard™ Pro 功率限制器。该 DSP 还支持一个额外的低延迟信号路径，在 48kHz 条件下为时间敏感型有源噪声消除 (ANC) 和道路噪声消除 (RNC) 应用提供最高快 70% 的信号处理速度。

该器件采用焊盘朝下的小型 TSSOP 和 QFN (具有可湿性侧面) 封装，可实现无散热器的音频放大器设计。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TAS6501-Q1	HTSSOP (28)	6.4mm × 9.7mm
	VQFN (24)	4mm × 4mm

- (1) 有关更多信息，请参阅“机械、封装和可订购信息”。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



简图



4 器件比较

表 4-1. 相关的 D 类音频放大器

器件	通道电流限制 (典型值)	输出功率 / 10% THD+N
		4 Ω / 14.4V
TAS6501-Q1	3.7A	15W
TAS6511-Q1	7.3A	30W

5 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发设计的工具和软件。

5.1 器件支持

5.2 文档支持

5.2.1 相关文档

5.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

5.5 商标

TI E2E™ is a trademark of Texas Instruments.

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5.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

日期	修订版本	注释
September 2025	*	初始发行版

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS6501QPWPRQ1	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6501
TAS6501QRGERQ1	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TAS6501

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

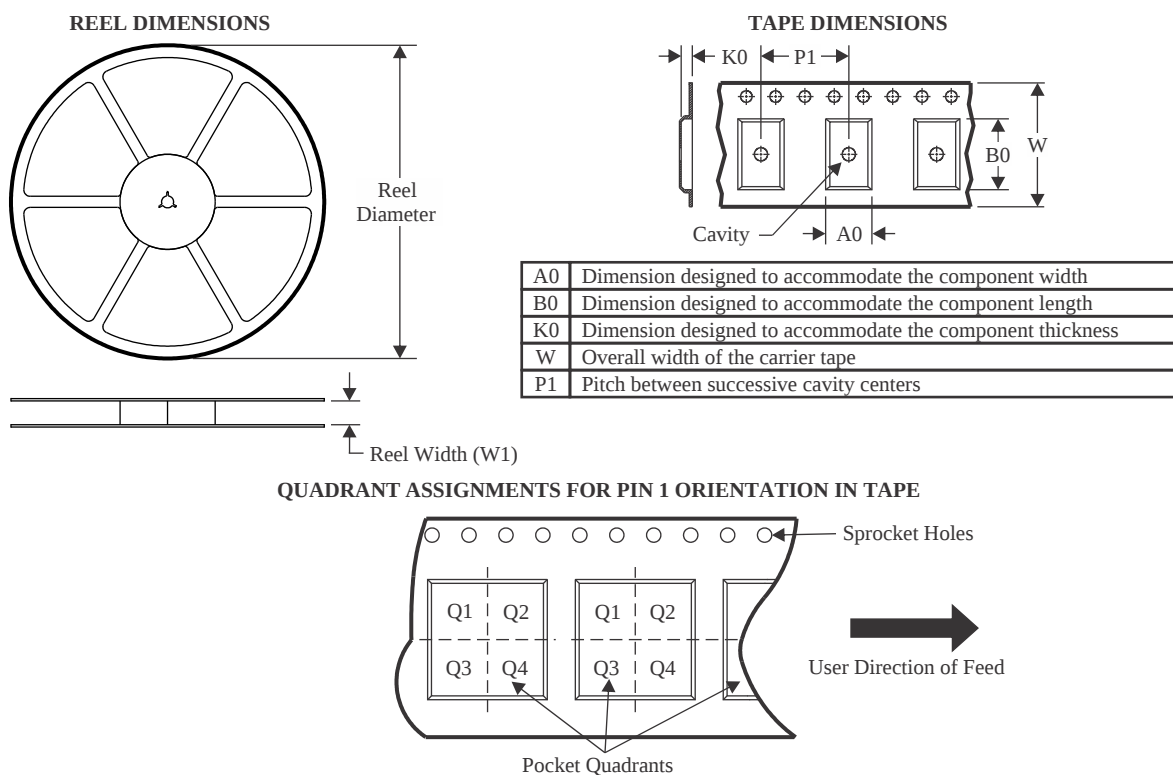
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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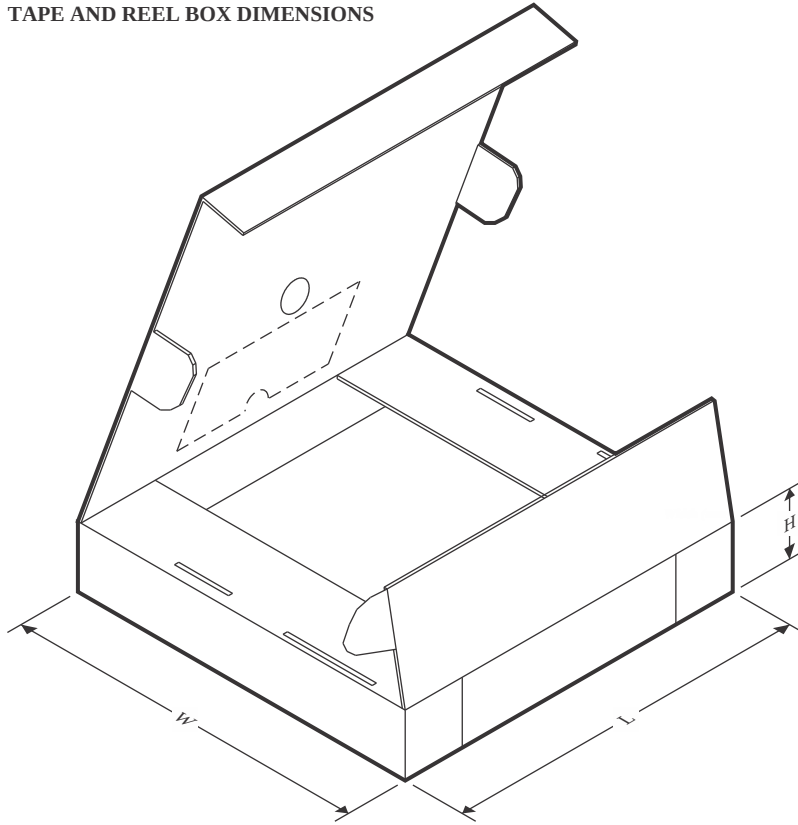
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6501QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TAS6501QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6501QPWPRQ1	HTSSOP	PWP	28	2000	353.0	353.0	32.0
TAS6501QRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

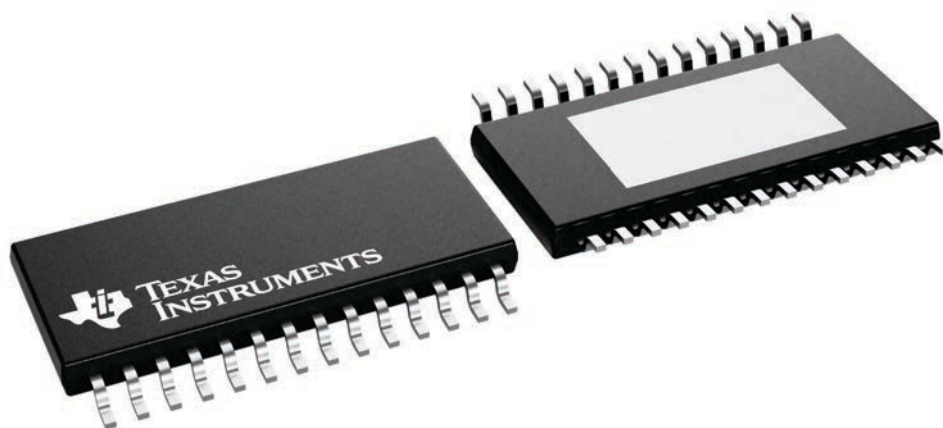
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

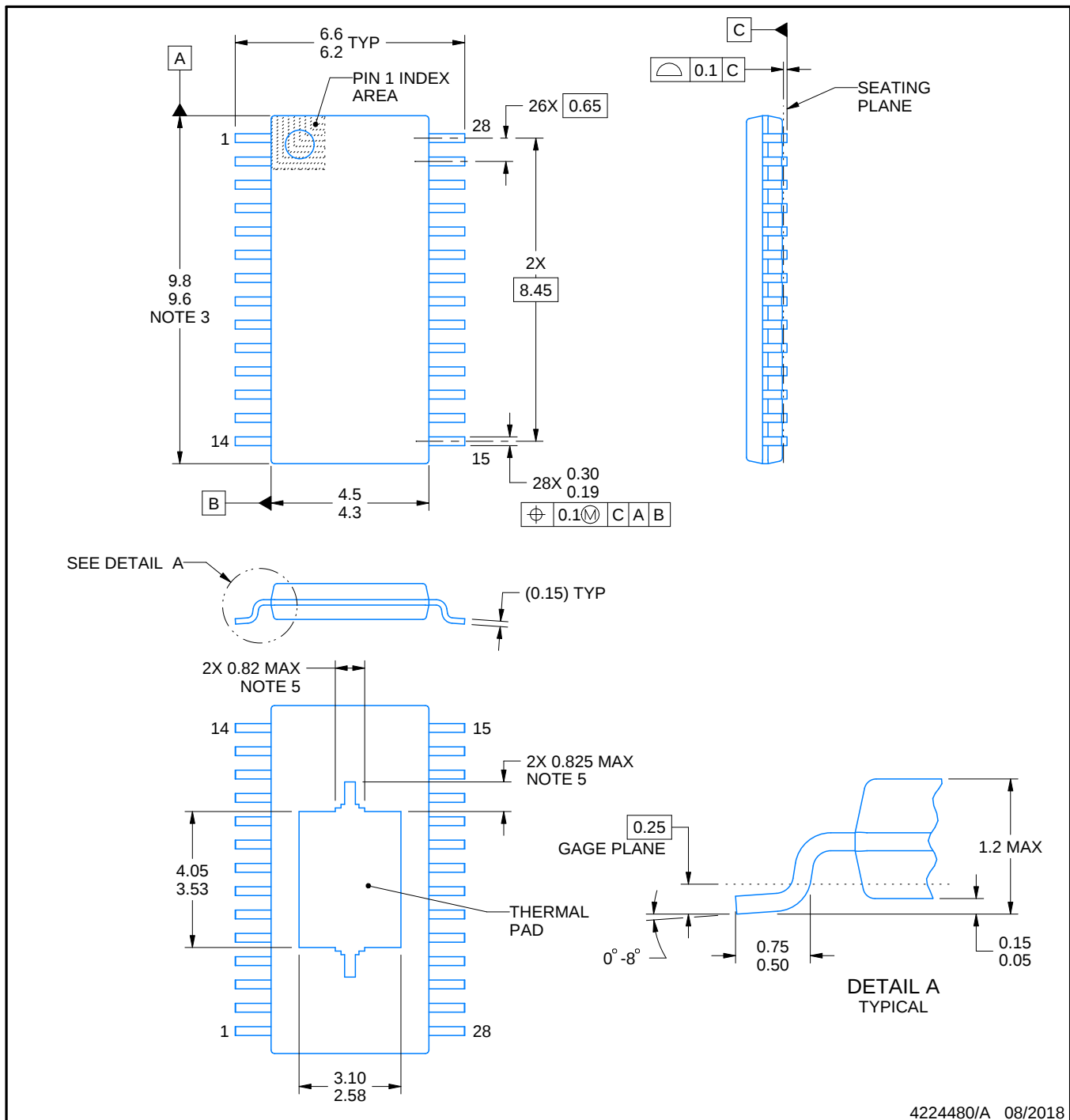
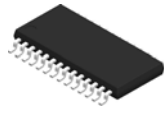
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

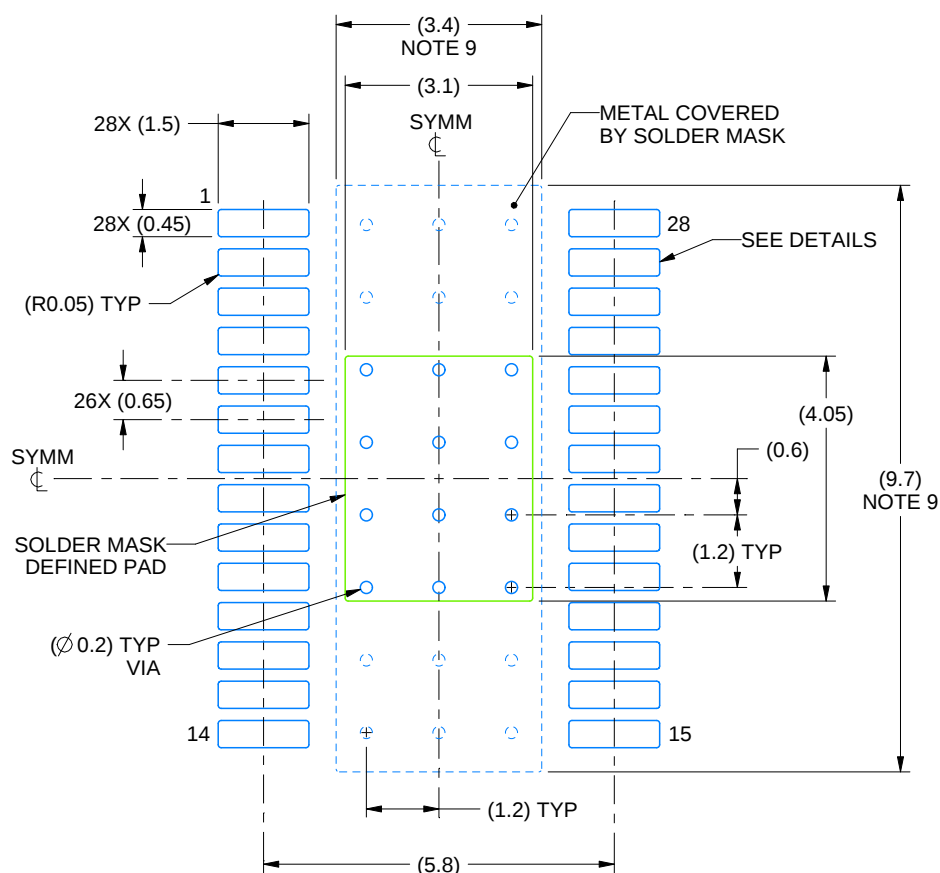
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

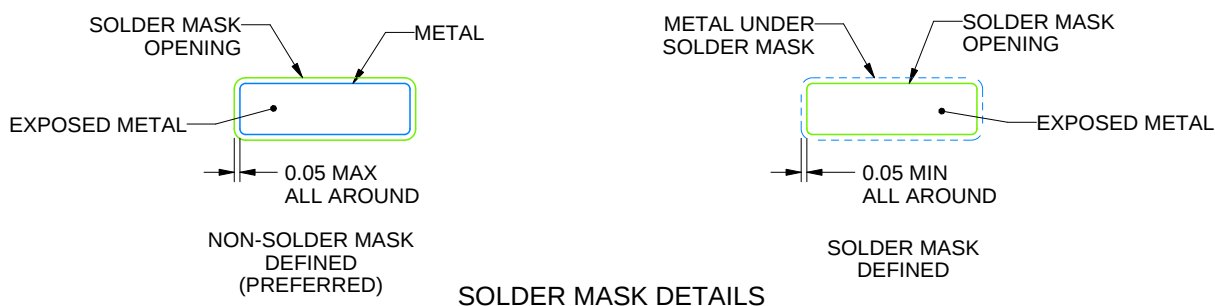
PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



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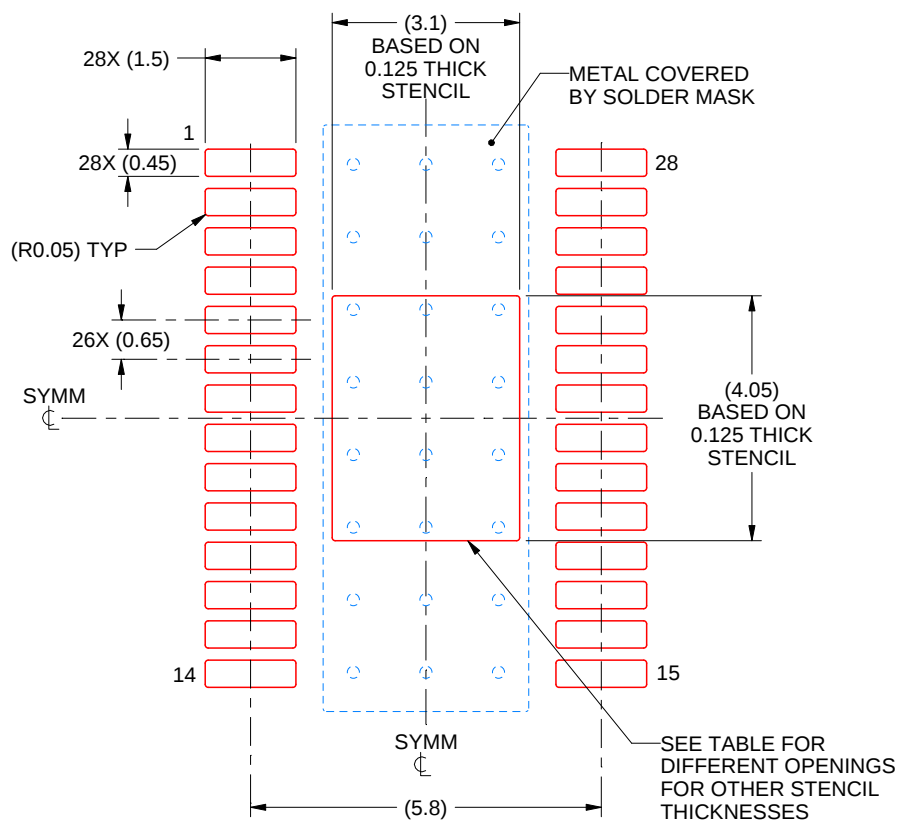
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

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NOTES: (continued)

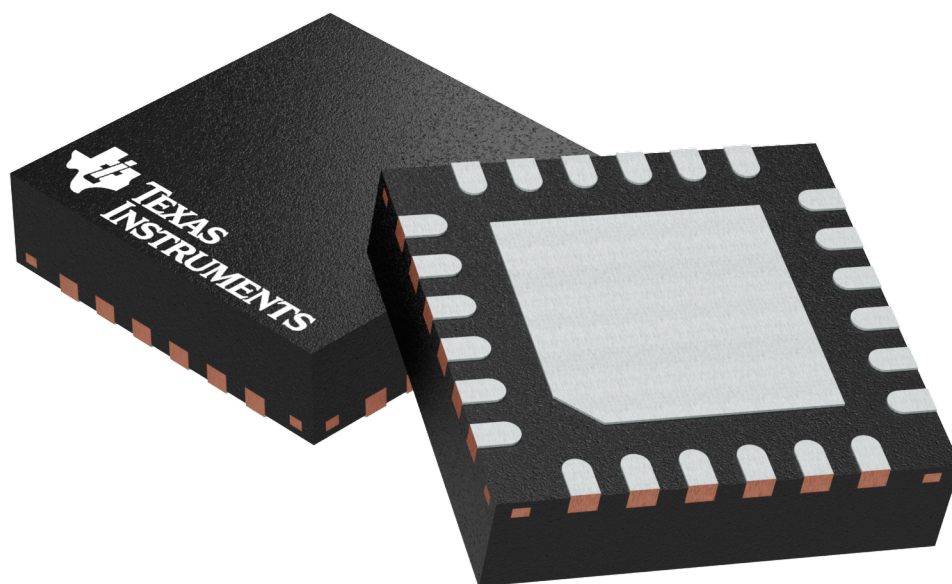
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RGE 24

GENERIC PACKAGE VIEW

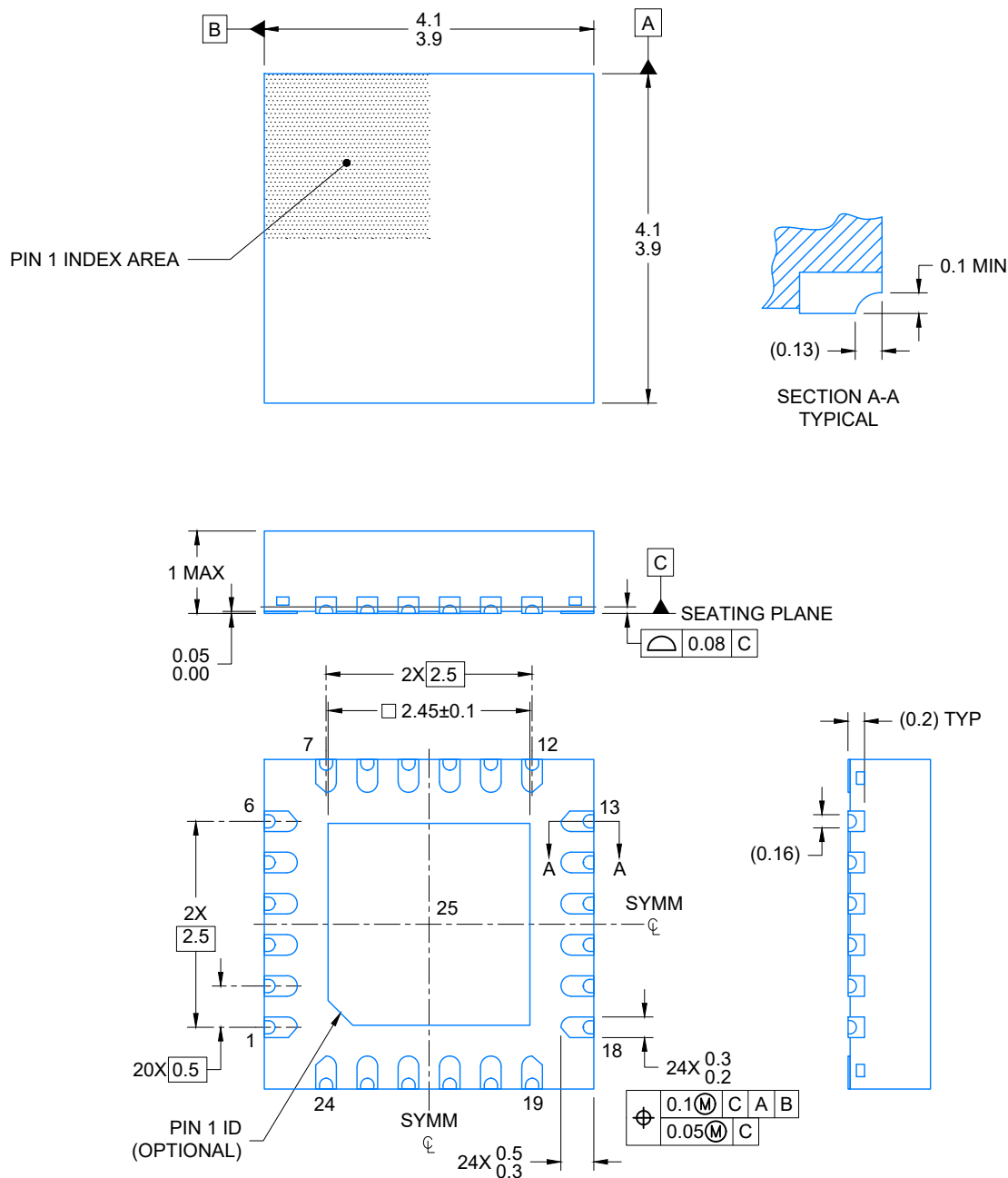
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

VQFN - 1 mm max height

24X (0.6)

24X (0.25)

20X (0.5)

2X (0.975)

6

(R0.05) TYP

2X (2.5)

2X (3.8)

(□ 2.45)

24

19

18

13

25

7

12

SYMM

SYMM

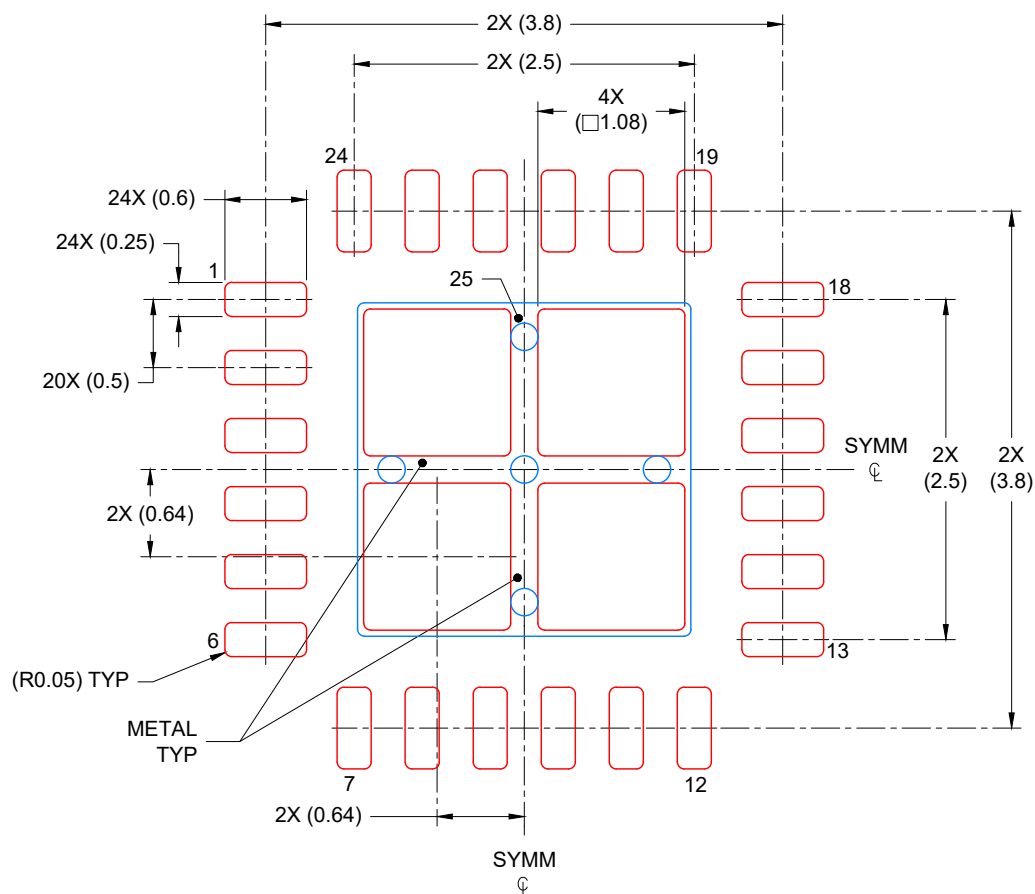
(Ø 0.2) VIA TYP

The diagram compares two PCB manufacturing methods:

- NON SOLDER MASK DEFINED (PREFERRED):** This method shows a rectangular opening in the solder mask. The opening is defined by a blue line, and the surrounding area is filled with green, representing the metal. A dimension line indicates a maximum clearance of 0.07 mm all around the opening. Labels include "0.07 MAX ALL AROUND", "METAL", and "SOLDER MASK OPENING".
- SOLDER MASK DEFINED:** This method shows a rectangular opening in the solder mask. The opening is defined by a green line, and the surrounding area is filled with blue, representing the metal. A dimension line indicates a minimum clearance of 0.07 mm all around the opening. Labels include "0.07 MIN ALL AROUND", "METAL UNDER SOLDER MASK", and "SOLDER MASK OPENING".

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4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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