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TEXAS INSTRUMENTS

TAS5806MD

ZHCSJT7 – MAY 2019

具有增强处理能力和 DirectPath™ HP 驱动器的 TAS5806MD 23W、无电感器、数字输入、立体声、闭环 D 类音频放大器

1 特性

- 支持多路输出配置：
  - 2.0 模式（8Ω、21V、THD+N=1%）下可提供 2 × 23W 的功率
  - 单声道模式（4Ω、21V、THD+N=1%）下可提供 45W 的功率
- 优异的音频性能
  - 1W、1kHz、PVDD = 12V 的条件下，THD+N ≤ 0.03%
  - SNR ≥ 107dB（A 加权），噪声级别 < 40µVrms
- 灵活的电源配置
  - PVDD：4.5V 至 26.4V
  - DVDD 和 I/O：1.8V 或 3.3V
- 灵活的音频 I/O
  - I²S、LJ、RJ、TDM、3 线数字音频接口（无需 MCLK）
  - 支持 32、44.1、48、88.2、96kHz 采样率
  - 用于音频监控、子通道或回声消除的 SDOUT
- 增强的音频处理能力
  - 多频带高级 DRC 和 AGL
  - 2×15 个 BQ、热折返、直流阻断
  - 输入混合器、输出交叉开关、电平计
  - 5 个 BQ + 单频带 DRC + THD 管理器（用于低音炮通道）
  - 声场定位器选项
- 集成式自保护功能
  - 邻近的引脚对引脚短路且无损坏
  - 过流错误
  - 过温警告和错误
  - 欠压、过压锁定（UVLO、OVLO）
- 可轻松进行系统集成
  - I²C 软件控制
  - 解决方案尺寸更小
    - 与开环器件相比，所需的无源器件更少
    - 对于 PVDD ≤ 14V 的大多数情况，可实现无电感器运行（铁氧体磁珠）
    - 立体声耳机和立体声线路驱动器通过 I²C 调节增益
    - DirectPath 技术不再需要大容量的隔直电容器

2 应用

- LCD 电视、OLED 电视
- 无线扬声器、智能扬声器（带语音助理）
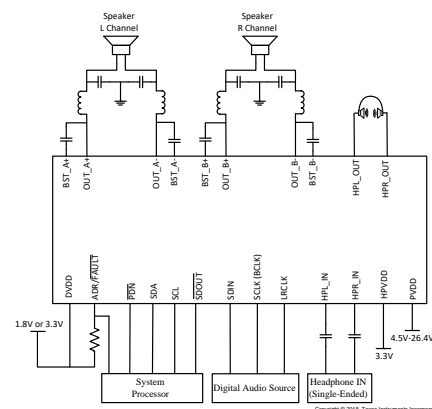- 条形音箱、有线扬声器、书架立体声系统
- AV 接收器、智能家居和物联网电器

3 说明

TAS5806MD 是一款高效立体声闭环 D 类放大器，可提供具有低功率耗散和丰富声音且具有成本效益的数字输入解决方案。该器件的集成音频处理器和 96kHz 架构支持高级音频处理流程（包括 SRC、每通道 15 个 BQ、音量控制、音频混合、3 频带 4 阶 DRC、全频带 AGL、THD 管理器和电平计）。

TAS5806MD 采用 TI 的专有混合调制方案，消耗极低的静态电流（13.5V PVDD 下为 16.5mA），从而能够延长便携式音频 应用中的电池寿命。凭借先进的 EMI 抑制技术，对低于 10W 的 应用，设计人员可利用廉价的铁氧体磁珠滤波器来减小其布板空间并降低系统成本。该器件配有集成 DirectPath™ 耳机放大器和线路驱动器，可提高系统级集成度并降低解决方案总成本。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TAS5806MD	TSSOP (38)	9.7mm × 4.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 5 月	*	初始发行版。

5 Device Comparison Table

ORDERABLE PART NUMBER	RECOMMENDED PVDD RANGE	$R_{DS(ON)}$ OPTION	Package	Headphone/Line Driver integrated
TAS5806MD	4.5 V to 26.4 V	180 mΩ	TSSOP38 (DCP)	YES
TAS5806M	4.5 V to 26.4 V	180 mΩ	TSSOP38 (DCP)	NO
TAS5805M	4.5 V to 26.4 V	180 mΩ	TSSOP28 (PWP)	NO
TAS5825M	4.5 V to 26.4 V	90 mΩ	QFN32 (RHB)	NO

6 Pin Configuration and Functions

DCP Package
38-Pin TSSOP
Top View

Pin	Name		Pin	Name
1	BST_A-		38	BST_B-
2	OUT_A-		37	OUT_B-
3	PGND		36	PGND
4	BST_A+		35	BST_B+
5	OUT_A+		34	OUT_B+
6	PVDD		33	PVDD
7	PVDD		32	PVDD
8	DGND		31	AGND
9	DVDD		30	AVDD
10	ADR/$\overline{FAULT}$		29	$\overline{PDN}$
11	VR_DIG		28	SCL
12	DGND		27	SDA
13	LRCLK		26	SDOUT
14	SCLK		25	CPP
15	SDIN		24	NC
16	HP_GND		23	CPN
17	HPVDD		22	HPVSS
18	HPR_IN		21	HPL_OUT
19	HPL_IN		20	HPR_OUT

Thermal Pad

Not to scale
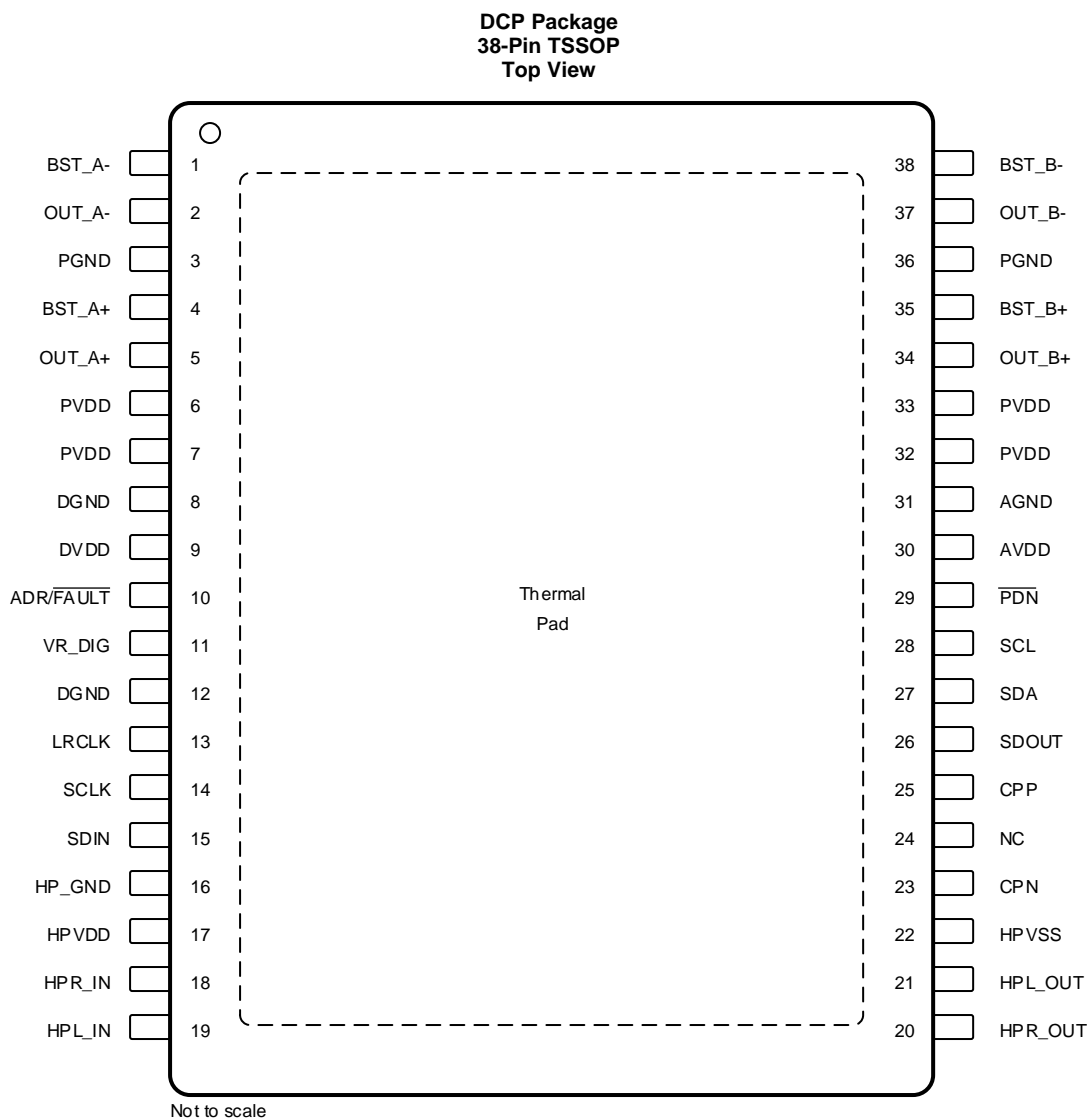
Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BST_A-	1	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
OUT_A-	2	AO	Negative pin for differential speaker amplifier output A-
PGND	3, 36	G	Ground reference for power device circuitry. Connect this pin to system ground.
BST_A+	4	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
OUT_A+	5	AO	Positive pin for differential speaker amplifier output A+
PVDD	6, 7, 32, 33.	P	PVDD voltage input
DGND	8, 12	G	Digital ground
DVDD	9	P	3.3-V or 1.8-V digital power supply
ADR/$\overline{\text{FAULT}}$	10	DIO	Different I^2 C device address can be set by selecting different pull up resistor to DVDD, see Table 3 for details. After power up, ADR/$\overline{\text{FAULT}}$ can be redefine as $\overline{\text{FAULT}}$, go to Page0, Book0, set register 0x61 = 0x0b first, then set register 0x60 = 0x01
VR_DIG	11	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
LRCLK	13	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^{2}S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
SCLK	14	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
SDIN	15	DI	Data line to the serial data port
HP_GND	16	G	Headphone Ground
HPVDD	17	P	Headphone Positive Power Supply
HPR_IN	18	AI	Headphone In Right
HPL_IN	19	AI	Headphone In Left
HPR_OUT	20	AO	Headphone Out Right
HPL_OUT	21	AO	Headphone Out Left
HPVSS	22	P	Headphone Negative Power Supply (Generated Internally)
CPN	23		Negative connection point for charge pump fly cap
NC	24		No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
CPP	25		Positive connection point for charge pump fly cap
SDOUT	26	DO	Serial Audio data output, the source data can select as Pre-DSP or Post DSP, by setting the register 0x30h.
SDA	27	DI/O	I2C serial control data interface input/output
SCL	28	DI	I2C serial control clock input
$\overline{\text{PDN}}$	29	DI	Power Down, active-low. $\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators. Low, Power Down Device; High, Enable Device.
AVDD	30	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices
AGND	31	G	Analog ground
OUT_B+	34	AO	Positive pin for differential speaker amplifier output B+
BST_B+	35	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
OUT_B-	37	AO	Negative pin for differential speaker amplifier output B
BST_B-	38	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
PowerPAD™		P	Connect to the system Ground

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)

7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) [1]

		MIN	MAX	UNIT
DVDD, HPVDD	Low-voltage digital supply	−0.3	3.9	V
PVDD	PVDD supply	−0.3	30	V
Input Voltage	HPL_IN, HPR_IN	-(HPVDD + 0.5)	+(HPVDD + 0.5)	V
$V_{I(DigIn)}$	DVDD referenced digital inputs [2]	−0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	−0.3	32	V
T_A	Ambient operating temperature,	−25	85	°C
T_{stg}	Storage temperature	−40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) DVDD referenced digital pins include: ADR/$\overline{FAULT}$, LRCLK, SCLK, SCL, SDA, SDIN, $\overline{PDN}$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	HPVDD	3	3.3	3.63	V
		DVDD	1.62		3.63	
		PVDD	4.5		26.4	
R_{SPK}	Minimum speaker load	BTL Mode (4.5V<PVDD<16V)	3.2	4		Ω
		BTL Mode (16V<PVDD<24V)	4.8	6		Ω
		PBLT Mode (4.5V<PVDD<16V)	1.6	2		Ω
		PBLT Mode (16V<PVDD<24V)	2.4	3		Ω
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1	4.7		µH
R_hp_L	Headphone-mode load impedance (HPL/HPR)		16	32		Ω
R_ln_L	Line-driver-mode load impedance (HPL/HPR)		1	10		kΩ

7.4 Thermal Information

		TAS5806MD TSSOP (DCP) 38 PINS			UNIT
THERMAL METRIC[1]		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5806MDEVM-4 4-LAYER PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	-	29.2	23.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	-	18	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	-	9.6	-	°C/W
ψ_{JT}	Junction-to-top characterization parameter	-	0.8	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	-	9.5	8.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	2.4	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Free-air room temperature 25°C, DVDD=3.3V, 1SPW Modulation Mode with LC filter, BD Modulation Mode with Ferrite bead filter (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
$|I_{IH}|$	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	µA
$|I_{IL}|$	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = 0$ V			−10	µA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	$I_{OH} = 2$ mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	$I_{OH} = −2$ mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)						
t_{off}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD. Measured at 0 dB input(1FS)	4.95		29.5	V
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 29.5 Vp		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier			384		kHz
				768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization.		180		mΩ
OCE_{THRES}	Over-Current Error Threshold	Any short to supply, ground, or other channels		5		A
	Over-Current cycle-by-cycle limit			4.2		A
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold			28		V
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold			4.2		V
OTE_{THRES}	Over temperature error threshold			160		°C
$OTE_{Hysteresis}$	Over temperature error hysteresis			10		°C
OTW_{THRES}	Over temperature warning level 3	Read by register 0x73 bit3		135		°C
SPEAKER AMPLIFIER (STEREO BTL)						

Electrical Characteristics (continued)

Free-air room temperature 25°C, DVDD=3.3V, 1SPW Modulation Mode with LC filter, BD Modulation Mode with Ferrite bead filter (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Quiescent supply current on DVDD	$\overline{PDN}$=2V, DVDD=3.3V, Play mode		18		mA
		$\overline{PDN}$=2V, DVDD=3.3V, Sleep mode		0.75		mA
		$\overline{PDN}$=2V, DVDD=3.3V, Deep Sleep mode		0.75		mA
		$\overline{PDN}$=0V, DVDD=3.3V, Shutdown mode		5.5		µA
I_{CC}	Quiescent supply current on PVDD	$\overline{PDN}$=2V, V_{PVDD}=13.5V, LC filter=10uH+0.68uF, Fsw=768kHz, BD Modulation, Play mode, BTL mode		32.5		mA
		$\overline{PDN}$=2V, V_{PVDD}=13.5V, LC filter=22uH+0.68uF, Fsw=384kHz, Hybrid or 1SPW Modulation, Play mode, BTL Mode		16.5		mA
		$\overline{PDN}$=2V, V_{PVDD}=13.5V, Output Hiz Mode		10.4		mA
		$\overline{PDN}$=2V, V_{PVDD}=13.5V, Sleep Mode		7.2		mA
		$\overline{PDN}$=2V, V_{PVDD}=13.5V, Deep Sleep Mode		120		µA
		$\overline{PDN}$=0V, V_{PVDD}=13.5V, Shutdown Mode		7.2		µA
$|Vos|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 Vp gain, V_{PVDD} = 24 V	-6.5		6.5	mV
$P_{O(SPK)}$	Output power (per channel)	V_{PVDD} = 12 V, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 10%		12		W
		V_{PVDD} = 12 V, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 1%		9.9		W
$P_{O(SPK)}$	Output power (per channel)	V_{PVDD} = 18 V, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 10%		25		W
		V_{PVDD} = 18 V, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 1%		21		W
$P_{O(SPK)}$	Output power (per channel)	V_{PVDD} = 21 V, R_{SPK} = 8 Ω, f = 1 kHz THD+N = 10%		27.5		W
		V_{PVDD} = 21 V, R_{SPK} = 8 Ω, f = 1 kHz THD+N = 1%		23		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 KHz, R_{SPK} = 6 Ω)	V_{PVDD} = 12 V, SPK_GAIN = 29.5 Vp, LC-filter		0.03%		
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 Vp, LC-filter		0.03%		
$I_{CN(SPK)}$	Idle channel noise	A-weighted (AES17), V_{PVDD} = 12 V, LC-filter, R_{SPK} = 6 Ω		37		µVrms
		A-weighted (AES17), V_{PVDD} = 24 V, LC-filter, R_{SPK} = 6 Ω		38		
DR	Dynamic range	A-Weighted, -60 dBFS method. V_{PVDD} = 24 V, SPK_GAIN = 29.5 Vp, R_{SPK} = 6 Ω		112		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24V		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=14.4V		107.5		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V_{rms}, V_{PVDD} = 14.4 V, input audio signal = digital zero		72		dB
X-talk$_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 KHz		100		dB
SPEAKER AMPLIFIER (MONO PBTL)						
$|V_{OS}|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 Vp gain, V_{PVDD} = 24 V	−8		8	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 12 V, R_{SPK} = 4Ω, f = 1KHz, THD+N = 1%		15.4		W
		V_{PVDD} = 12 V, R_{SPK} = 4 Ω, f = 1KHz, THD+N = 10%		18.5		W
		V_{PVDD} = 18 V, R_{SPK} = 4 Ω, f = 1KHz, THD+N = 1%		33.6		W
		V_{PVDD} = 18 V, R_{SPK} = 4 Ω, f = 1KHz, THD+N = 10%		41		W

Electrical Characteristics (continued)

Free-air room temperature 25°C, DVDD=3.3V, 1SPW Modulation Mode with LC filter, BD Modulation Mode with Ferrite bead filter (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N$_{SPK}$	Total harmonic distortion and noise (P$_O$ = 1 W, f = 1 KHz	V$_{PVDD}$ = 12 V, LC-filter, R$_{SPK}$ = 4 Ω		0.015%		
		V$_{PVDD}$ = 24 V, LC-filter R$_{SPK}$ = 4 Ω		0.015%		
DR	Dynamic range	A-Weighted, -60 dBFS method. V$_{PVDD}$ = 24 V, SPK_GAIN = 29.5 Vp		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V$_{PVDD}$=13.5V		108		dB
		A-Weighted, referenced to 1% THD+N Output Level, V$_{PVDD}$=24V		111		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V$_{rms}$, V$_{PVDD}$ = 19 V, input audio signal = digital zero		72		dB
Headphone Amplifier						
P$_o$(hp)	Headphone power output per channel	HPVDD = 3.3 V (Rhp = 32 Ω; THD = 1%)	30	40		mW
SNR_hp	Signal -to-noise ratio (headphone mode)	Rhp = 32 Ω		101		dB
SNR_ln	Signal-to-noise ratio (line driver mode)	2-V$_{RMS}$ output		105		dB
f$_{cp}$	Charge-pump switching frequency			360		kHz

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I²C Bus Timing – Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
I²C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns

7.7 Typical Characteristics

7.7.1 Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5806MDEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM Modulation mode set to 1 SPW mode with Class D Bandwidth =120 kHz for 576kHz Fsw and Class D Bandwidth = 175 kHz for 768 kHz Fsw (Listed in Register 0x53) unless otherwise noted.
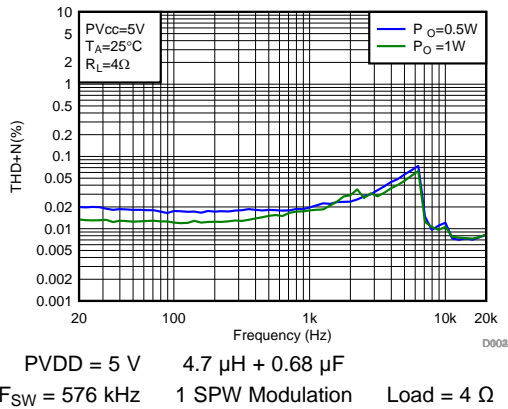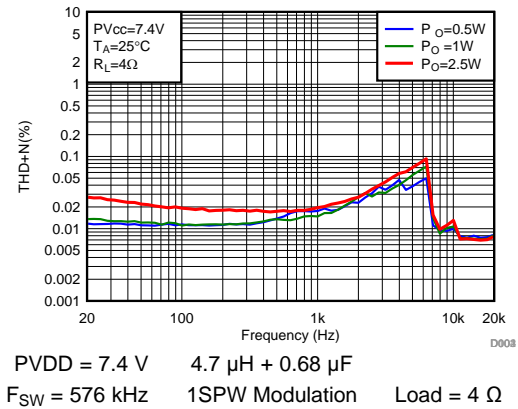
PVDD = 5 V   4.7 µH + 0.68 µF

F_{SW} = 576 kHz   1 SPW Modulation   Load = 4 Ω

图 1. THD+N vs Frequency-BTL

PVDD = 7.4 V   4.7 µH + 0.68 µF

F_{SW} = 576 kHz   1SPW Modulation   Load = 4 Ω

图 2. THD+N vs Frequency-BTL

PVDD = 12 V   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   1SPW Modulation   Load = 4 Ω

图 3. THD+N vs Frequency-BTL

PVDD = 12 V   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   1SPW Modulation   Load = 6 Ω

图 4. THD+N vs Frequency-BTL

PVDD = 18 V   10 µH + 0.68 µF

F_{SW} = 768 kHz   1SPW Modulation   Load = 6 Ω

图 5. THD+N vs Frequency-BTL

PVDD = 24 V   10 µH + 0.68 µF
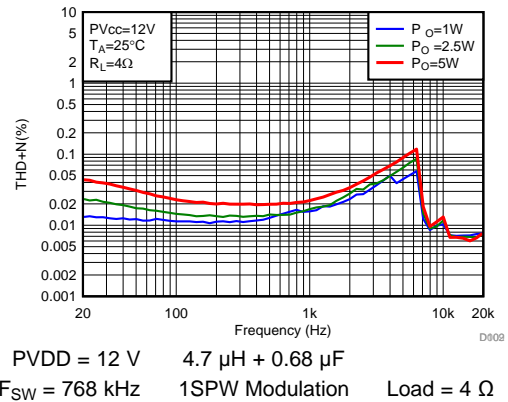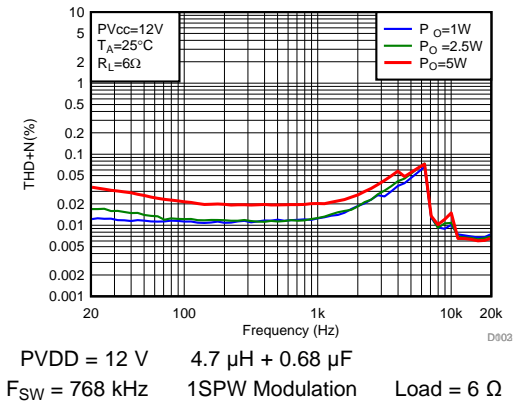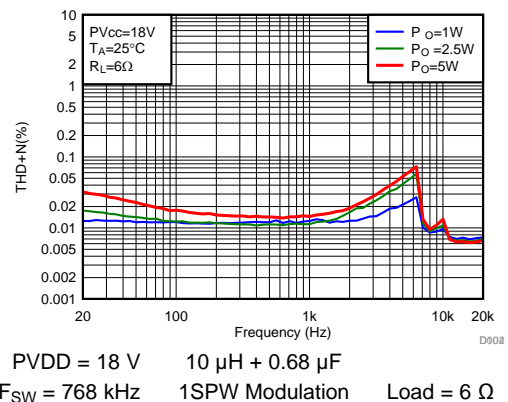
F_{SW} = 768 kHz   1SPW Modulation   Load = 6 Ω
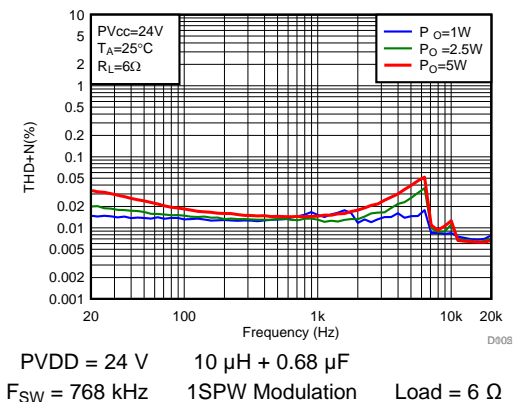
图 6. THD+N vs Frequency-BTL

Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (接下页)

PVDD = 12 V   4.7 µH + 0.68 µF
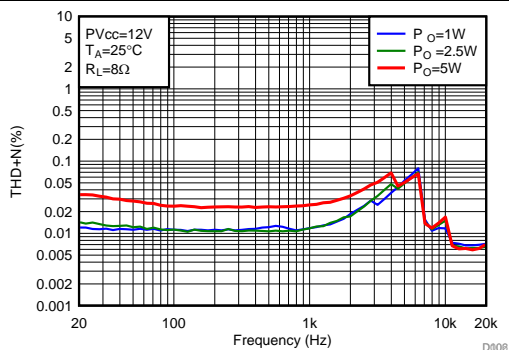
F_{SW} = 768 kHz   1SPW Modulation   Load = 8 Ω
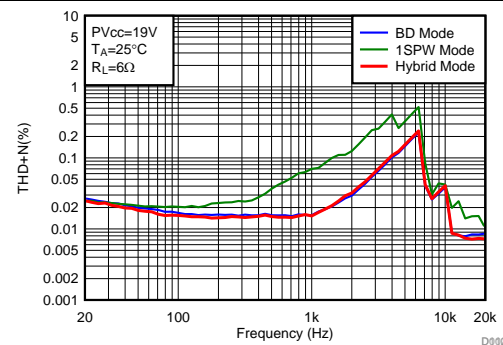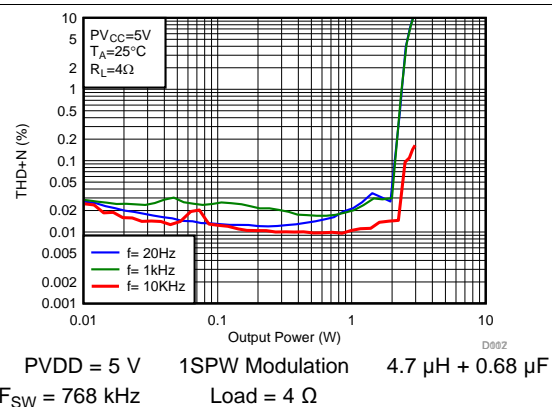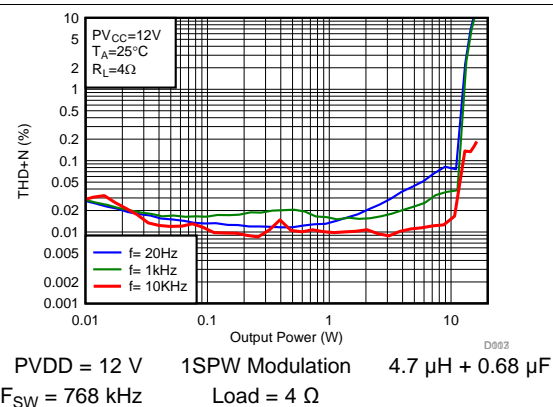
图 7. THD+N vs Frequency-BTL

PVDD = 18 V   10 µH + 0.68 µF
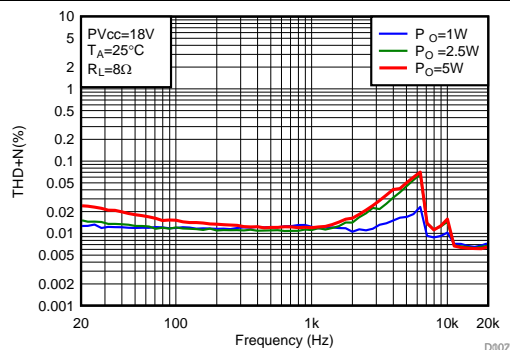
F_{SW} = 768 kHz   1SPW Modulation   Load = 8 Ω

图 8. THD+N vs Frequency-BTL

PVDD = 24 V   10 µH + 0.68 µF
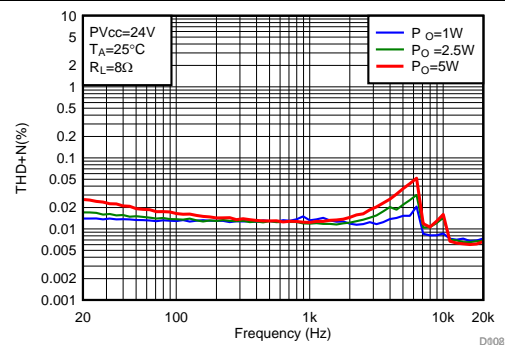
F_{SW} = 768 kHz   1SPW Modulation   Load = 8 Ω

图 9. THD+N vs Frequency-BTL

PVDD = 19 V   Hybrid, BD P_O = 5 W

F_{SW} = 384 kHz   1 SPW Modulation   Load = 6 Ω

图 10. THD+N vs Frequency-BTL

PVDD = 5 V   1SPW Modulation   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 4 Ω

图 11. THD+N vs Output Power-BTL

PVDD = 12 V   1SPW Modulation   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 4 Ω

图 12. THD+N vs Output Power-BTL
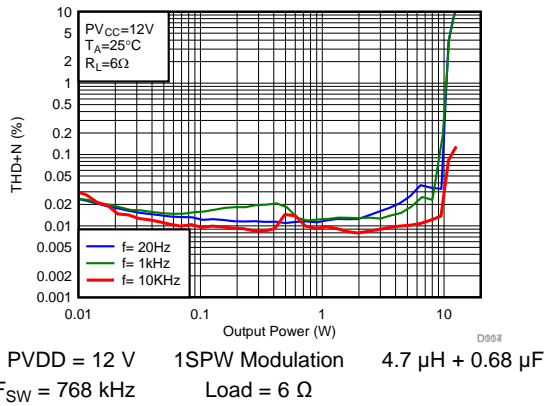
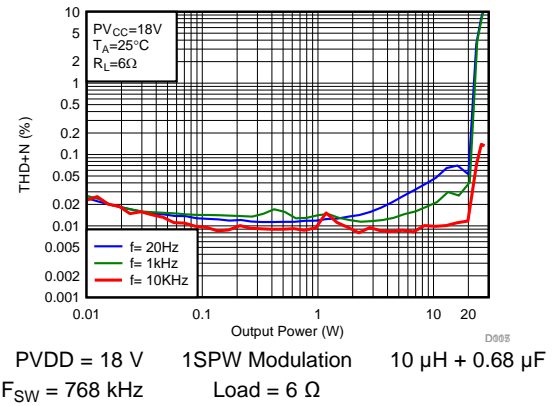## Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (接下页)

PVDD = 12 V   1SPW Modulation   4.7 μH + 0.68 μF

F_{SW} = 768 kHz   Load = 6 Ω

图 13. THD+N vs Output Power-BTL

PVDD = 18 V   1SPW Modulation   10 μH + 0.68 μF

F_{SW} = 768 kHz   Load = 6 Ω

图 14. THD+N vs Output Power-BTL

PVDD = 24 V   1SPW Modulation   10 μH + 0.68 μF

F_{SW} = 768 kHz   Load = 6 Ω

图 15. THD+N vs Output Power-BTL

PVDD = 12 V   1SPW Modulation   10 μH + 0.68 μF

F_{SW} = 768 kHz   Load = 8 Ω

图 16. THD+N vs Output Power-BTL

PVDD = 18 V   1SPW Modulation   10 μH + 0.68 μF

F_{SW} = 768 kHz   Load = 8 Ω

图 17. THD+N vs Output Power-BTL

PVDD = 24 V   1SPW Modulation   10 μH + 0.68 μF

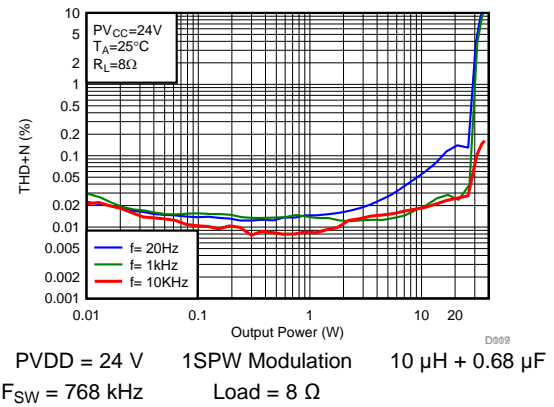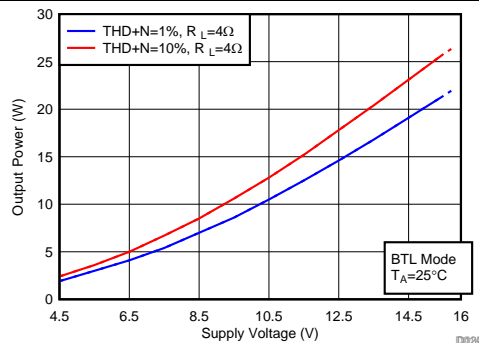F_{SW} = 768 kHz   Load = 8 Ω
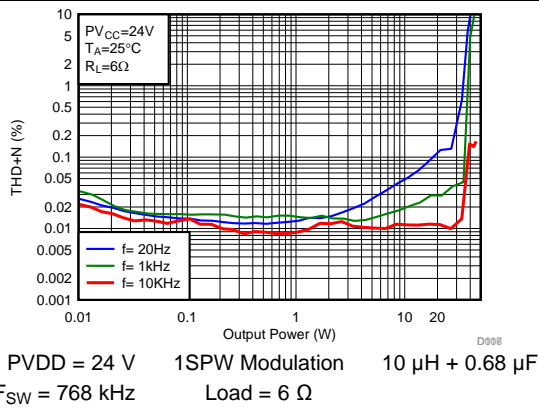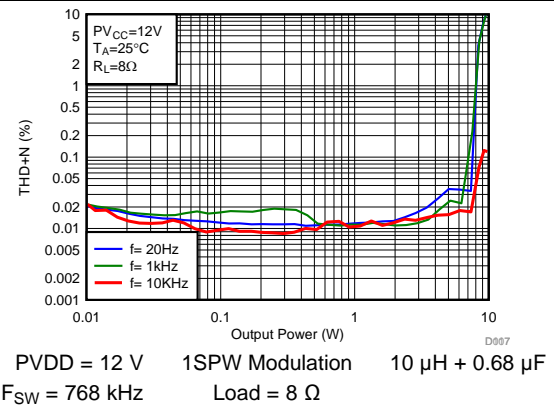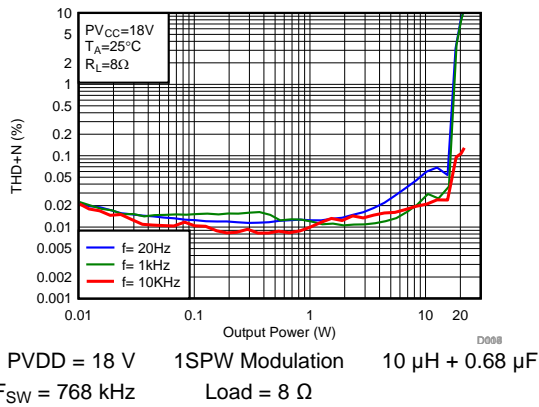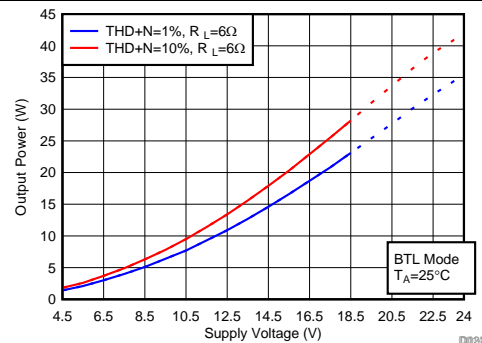
图 18. THD+N vs Output Power-BTL

Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (接下页)

Dashed lines represent thermally limited region for the continuous output power.

PVDD = 4.5V~16V   1SPW Modulation   4.7 µH + 0.68 µF
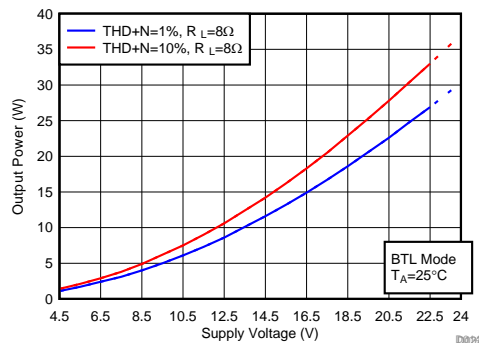
F_{SW} = 768 kHz   Load = 4 Ω

图 19. Output Power vs Supply Voltage

Dashed lines represent thermally limited region for the continuous output power.

PVDD = 4.5V~24V   1SPW Modulation   10 µH + 0.68 µF

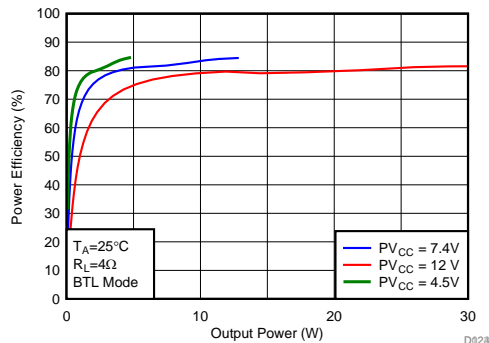F_{SW} = 768 kHz   Load = 6 Ω

图 20. Output Power vs Supply Voltage

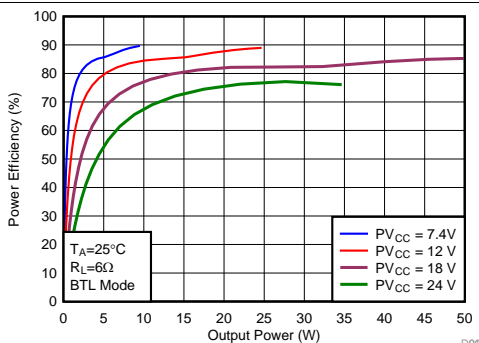Dashed lines represent thermally limited region for the continuous output power.

PVDD = 4.5V~24V   1SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 8 Ω

图 21. Output Power vs Supply Voltage
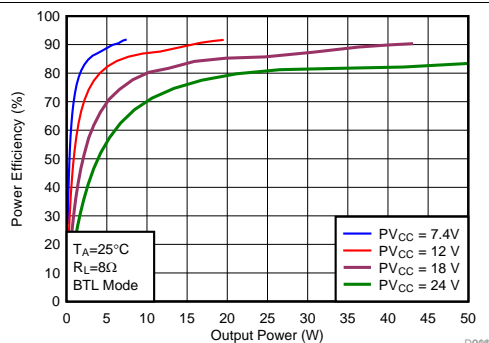

PVDD = 4.5 V, 7.4 V, 12 V   1 SPW Modulation

F_{SW} = 768 kHz   Load = 4 Ω   4.7 µH + 0.68 µF

图 22. Efficiency vs Supply Voltage

PVDD = 7.4 V, 12 V, 18 V, 24 V   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 6 Ω   1 SPW Modulation
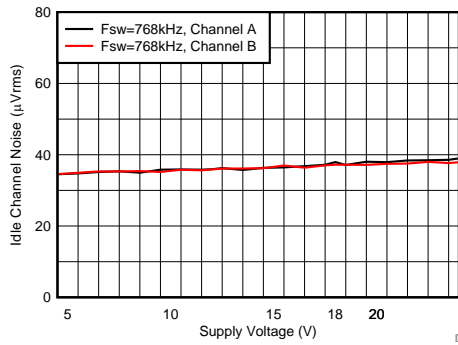
图 23. Efficiency vs Supply Voltage

PVDD = 7.4 V, 12 V, 18 V, 24 V   10 µH + 0.68 µF

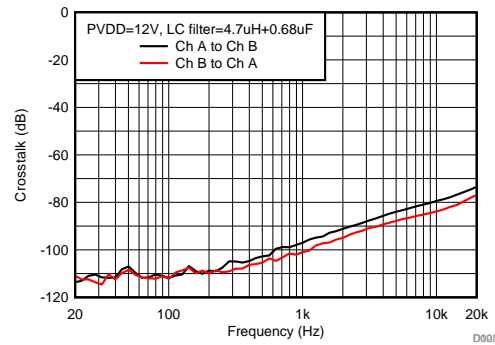F_{SW} = 768 kHz   Load = 8 Ω   1SPW Modulation

图 24. Efficiency vs Supply Voltage

Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (接下页)
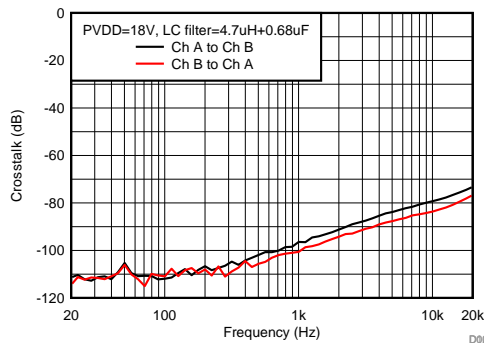

PVDD = 4.5V~24V   1 SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 8 Ω

图 25. Idle Channel Noise vs Supply Voltage

PVDD = 12 V   1 SPW Modulation   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 6 Ω P_O = 1 W

图 26. Crosstalk

PVDD = 18 V   1 SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 6 Ω P_O = 1 W

图 27. Crosstalk

PVDD = 24 V   1 SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 6 Ω P_O = 1 W

图 28. Crosstalk
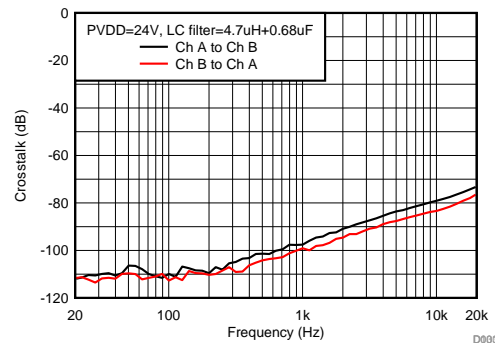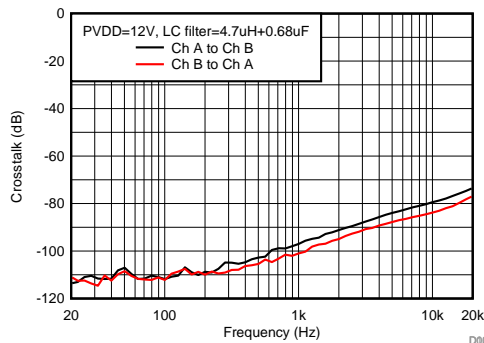

PVDD = 12 V   1 SPW Modulation   4.7 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 8 Ω P_O = 1 W

图 29. Crosstalk
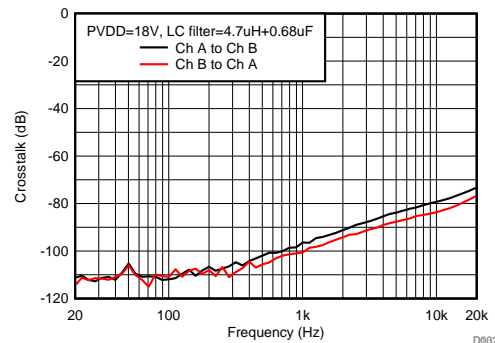
PVDD = 18 V   1 SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 8 Ω P_O = 1 W

图 30. Crosstalk

Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (接下页)

PVDD=24V, LC filter=4.7uH+0.68uF
—— Ch A to Ch B
—— Ch B to Ch A

Crosstalk (dB)
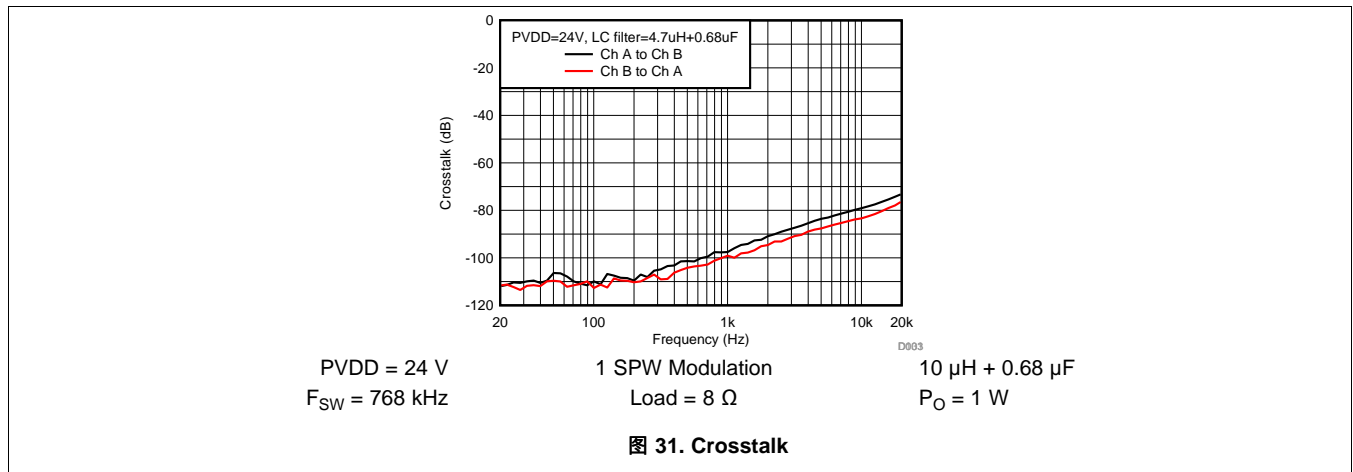
Frequency (Hz)

D003

PVDD = 24 V   1 SPW Modulation   10 µH + 0.68 µF

F_{SW} = 768 kHz   Load = 8 Ω P_O = 1 W

图 31. Crosstalk

7.7.2 Bridge Tied Load (BTL) Configuration Curves

Free-air room temperature 25°C (unless otherwise noted), Measurements were made using TAS806MDEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, with Class D Bandwidth=80kHz (Listed in Register 0x53), Spread Spectrum Enable, Ferrite bead + Capacitor as the output filter, BD Modulation, unless otherwise noted.
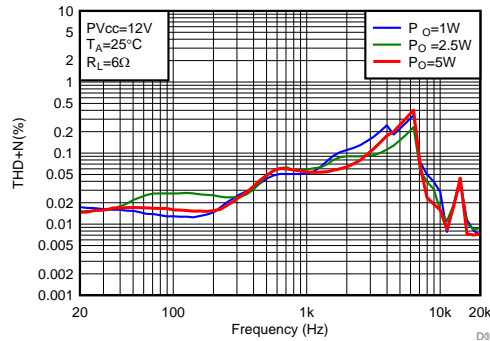
| PVDD = 12 V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 6 Ω |

图 32. THD+N vs Frequency
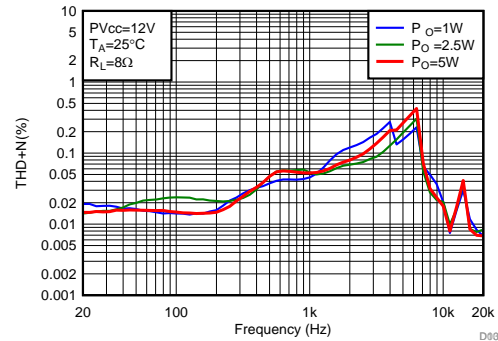
| PVDD = 12 V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 8 Ω |

图 33. THD+N vs Frequency
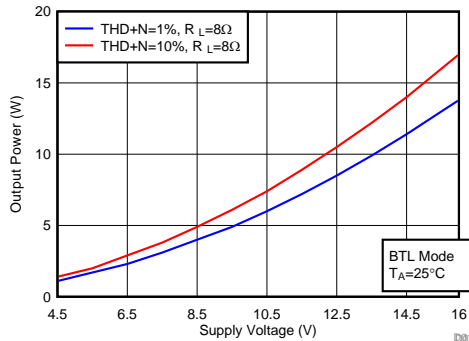
| PVDD = 4.5V~16V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 8 Ω |

图 34. Output Power vs Supply Voltage
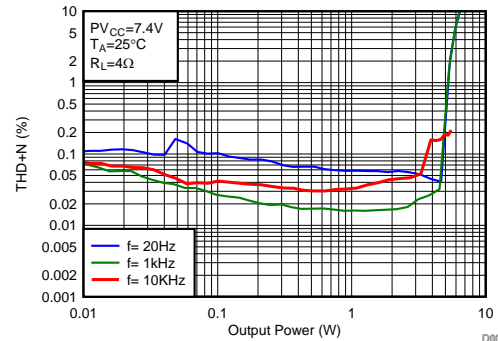
| PVDD = 7.4V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 4 Ω |

图 35. THD+N vs Output Power
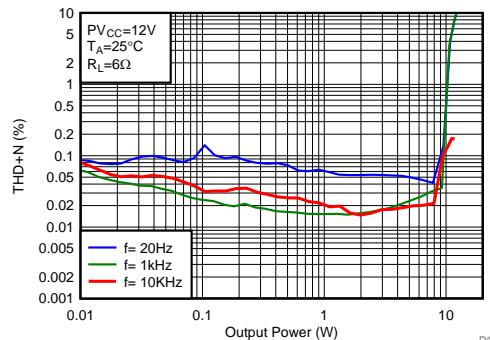
| PVDD = 12V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 6 Ω |

图 36. THD+N vs Output Power
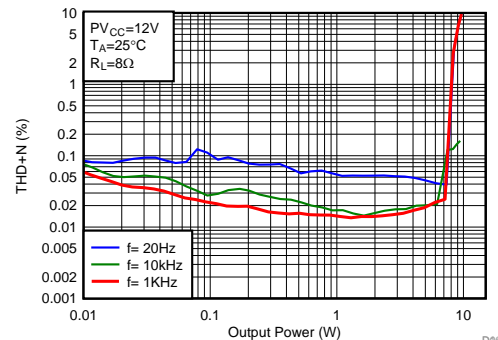
| PVDD = 12V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F$_{SW}$ = 384 kHz | BD Modulation | Load = 8 Ω |

图 37. THD+N vs Output Power

Bridge Tied Load (BTL) Configuration Curves (接下页)
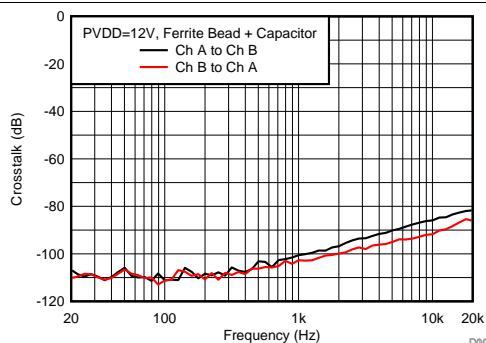
| PVDD = 12 V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F_{SW} = 384 kHz | BD Modulation | Load = 6 Ω, P_O = 1 W |

图 38. Crosstalk
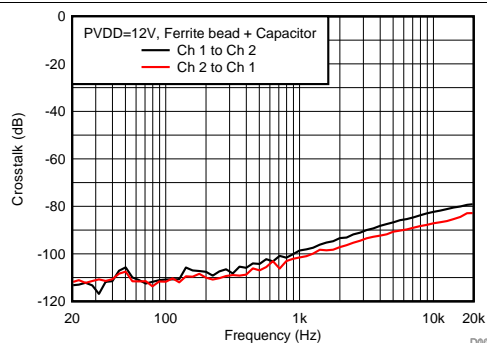
| PVDD = 12V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F_{SW} = 384 kHz | BD Modulation | Load = 8 Ω , P_O = 1 W |

图 39. Crosstalk
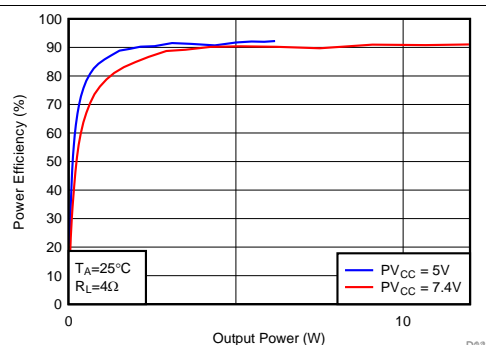
| PVDD = 5V, 7.4V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F_{SW} = 384 kHz | BD Modulation | Load = 4 Ω |

图 40. Efficiency vs Output Power
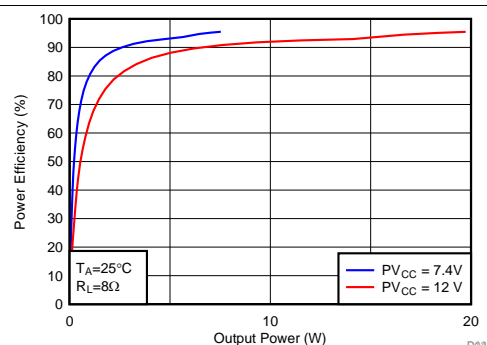
| PVDD = 7.4V, 12V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F_{SW} = 384 kHz | BD Modulation | Load = 8 Ω |

图 41. Efficiency vs Output Power
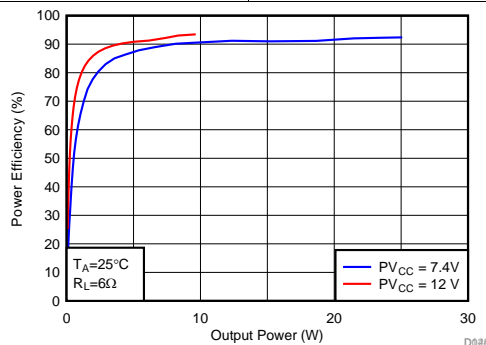
| PVDD = 7.4V, 12V | Ferrite bead + Capacitor | Spread Spectrum Enable |
| F_{SW} = 384 kHz | BD Modulation | Load = 6 Ω |

图 42. Efficiency vs Output Power

7.7.3 Parallel Bridge Tied Load (PBTL) Configuration

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5806MDEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576kHz, the LC filter used was 4.7 µH / 0.68 µF, 1SPW modulation with Class D Bandwidth =120kHz (Listed in Register 0x53) unless otherwise noted.
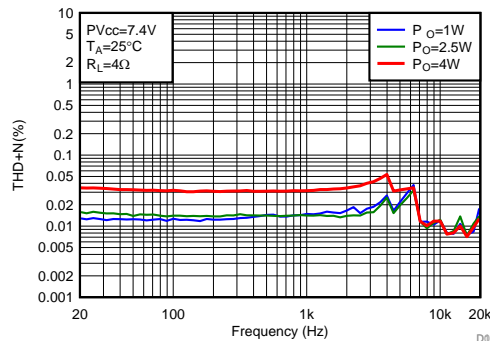
PVDD = 7.4 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 4 Ω

图 43. THD+N vs Frequency
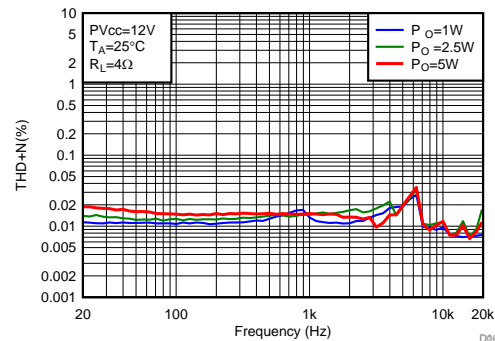
PVDD = 12 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 4 Ω

图 44. THD+N vs Frequency
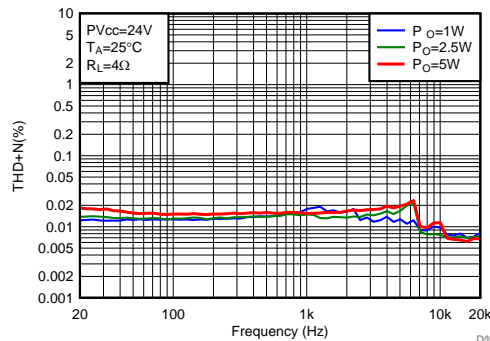
PVDD = 24 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 4 Ω

图 45. THD+N vs Frequency
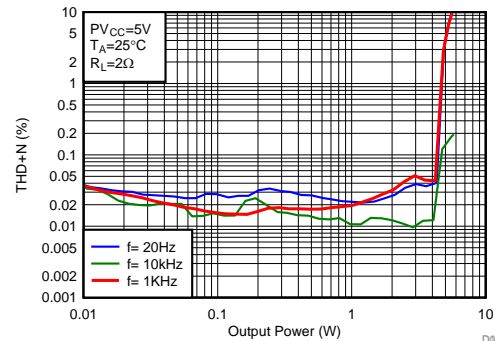
PVDD = 5 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 2 Ω

图 46. THD+N vs Output Power
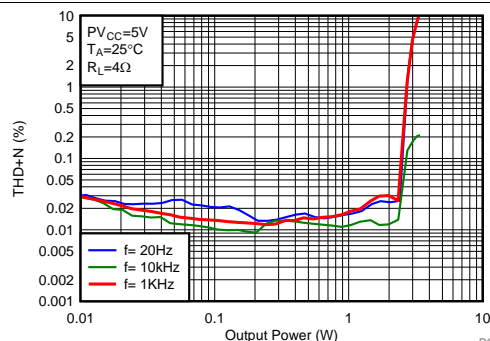
PVDD = 5 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 4 Ω

图 47. THD+N vs Output Power
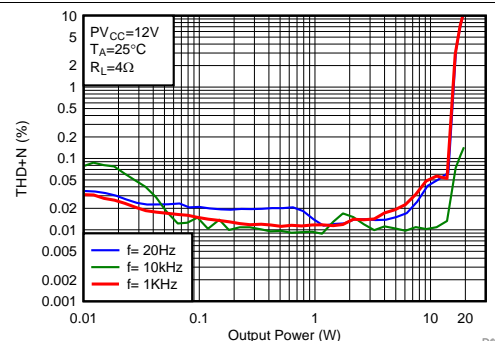
PVDD = 12 V   1SPW Modulation   4.7 µH + 0.68 µF
F_SW = 576 kHz   Load = 4 Ω

图 48. THD+N vs Output Power

Parallel Bridge Tied Load (PBTL) Configuration (接下页)
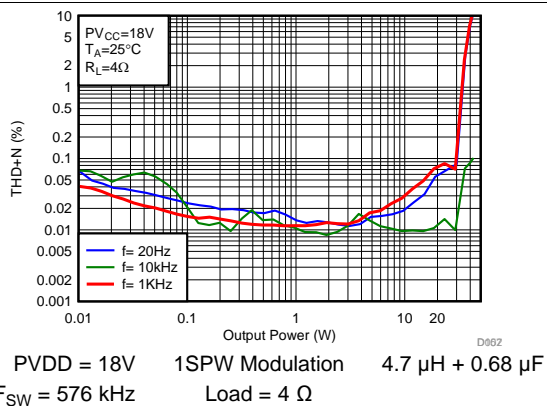
PVDD = 18V   1SPW Modulation   4.7 µH + 0.68 µF

F_SW = 576 kHz   Load = 4 Ω

图 49. THD+N vs Output Power

PVDD = 24V   1SPW Modulation   4.7 µH + 0.68 µF

F_SW = 576 kHz   Load = 4 Ω

图 50. THD+N vs Output Power

PVDD = 4.5V~24V   1SPW Modulation   4.7 µH + 0.68 µF

F_SW = 576 kHz   Load = 4 Ω

图 51. Idle Channel Noise vs Supply Voltage

PVDD = 5 V, 7.4 V, 12 V, 18 V, 24 V   1 SPW Modulation

F_SW = 576 kHz   Load = 4 Ω   4.7 µH + 0.68 µF
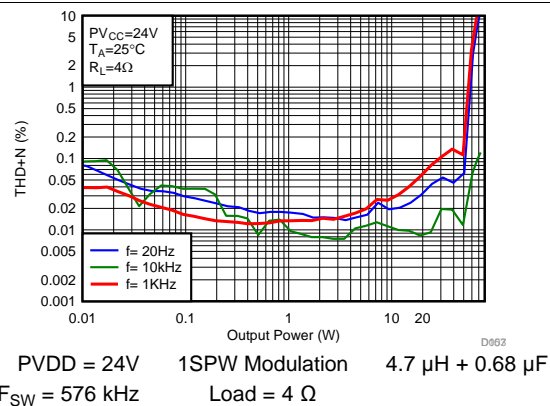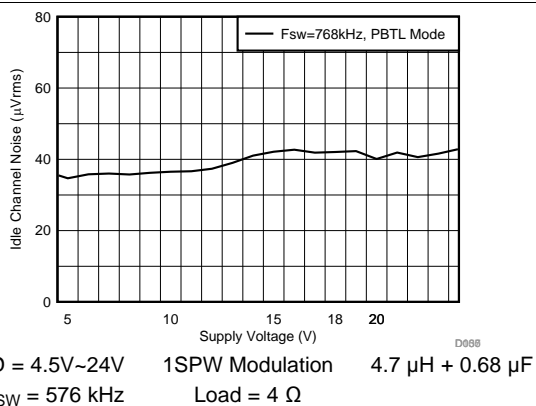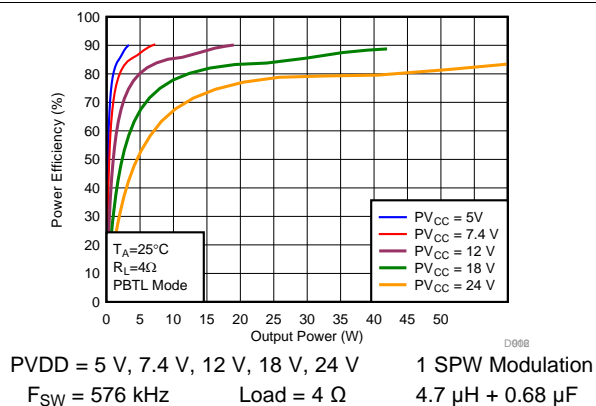
图 52. Efficiency vs Output Power

7.7.4 Headphone Driver

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5807MDREF board and Audio Precision System 2722 with Analog Analyzer filter set to 20 kHz brickwall filter. HPVDD = 3.3V. All measurement taken with audio frequency set to 1 kHz.
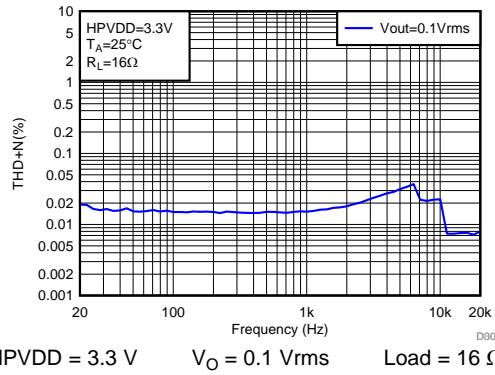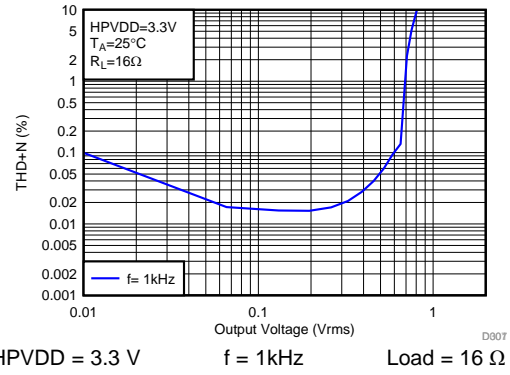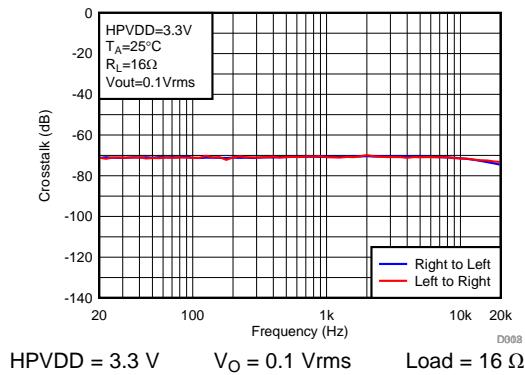
HPVDD = 3.3 V	V_O = 0.1 Vrms	Load = 16 Ω

图 53. THD+N vs Frequency

HPVDD = 3.3 V	f = 1kHz	Load = 16 Ω

图 54. THD+N vs Output Voltage

HPVDD = 3.3 V	V_O = 0.1 Vrms	Load = 16 Ω

图 55. Crosstalk vs Frequency

HPVDD = 3.3 V	V_O = 1 Vrms	Load = 32 Ω

图 56. THD+N vs Frequency

HPVDD = 3.3 V	f = 1 kHz	Load = 32 Ω

图 57. THD+N vs Output Voltage

HPVDD = 3.3 V	V_O = 1 Vrms	Load = 32 Ω
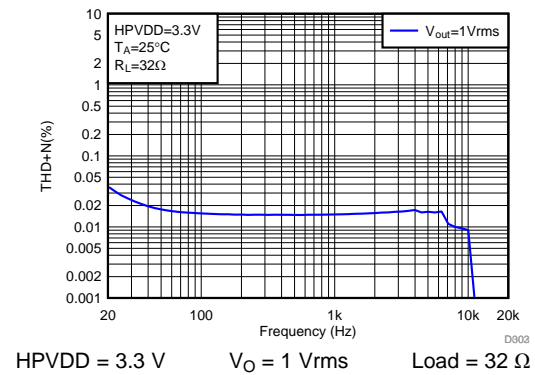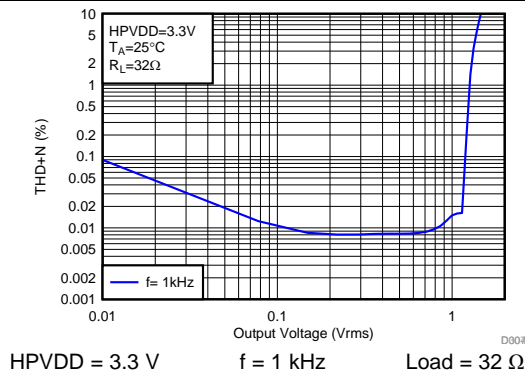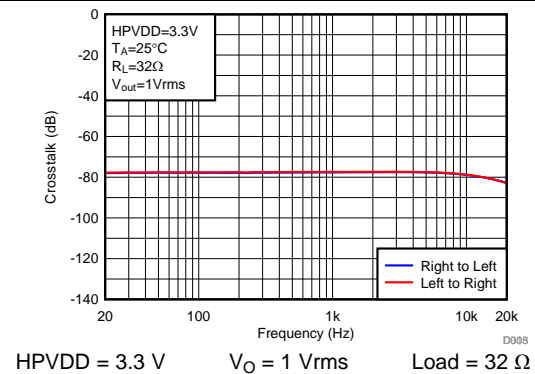
图 58. Crosstalk vs Frequency

7.7.5 Line Driver

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5807MDREF board and Audio Precision System 2722 with Analog Analyzer filter set to 20 kHz brickwall filter. HPVDD = 3.3 V. All measurements taken with audio frequency set to 1 kHz.
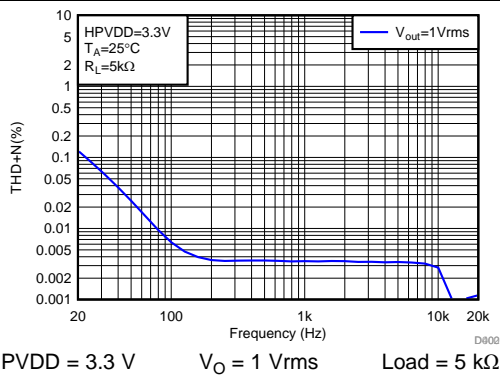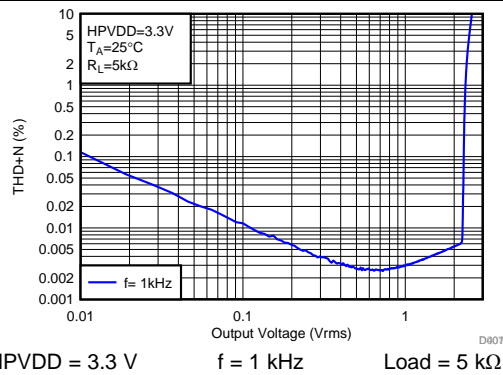
| HPVDD = 3.3 V | V$_O$ = 1 Vrms | Load = 5 kΩ |

图 59. THD+N vs Frequency

| HPVDD = 3.3 V | f = 1 kHz | Load = 5 kΩ |

图 60. THD+N vs Output Voltage

| HPVDD = 3.3 V | V$_O$ = 1 Vrms | Load = 5 kΩ |

图 61. Crosstalk vs Frequency

| HPVDD = 3.3 V | V$_O$ = 1 Vrms | Load = 10 kΩ |

图 62. THD+N vs Frequency

| HPVDD = 3.3 V | f = 1 kHz | Load = 10 kΩ |
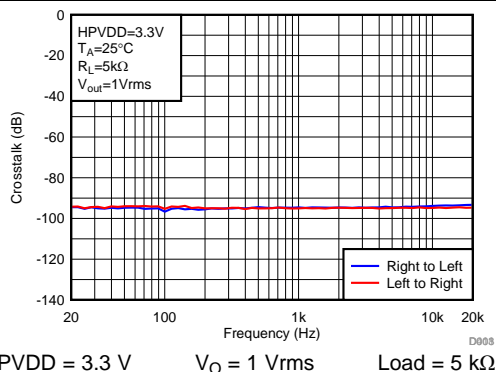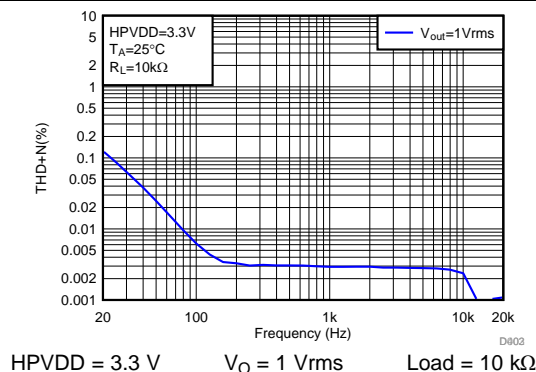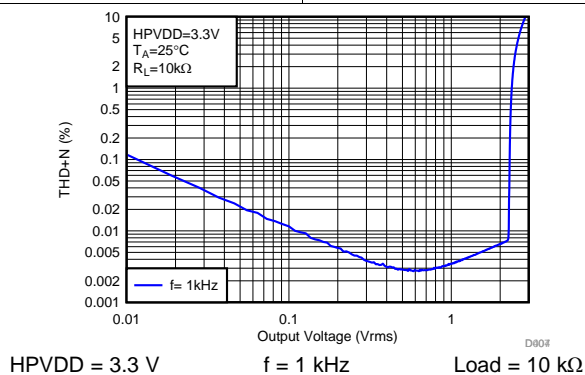
图 63. THD+N vs Output Voltage

8 Parametric Measurement Information
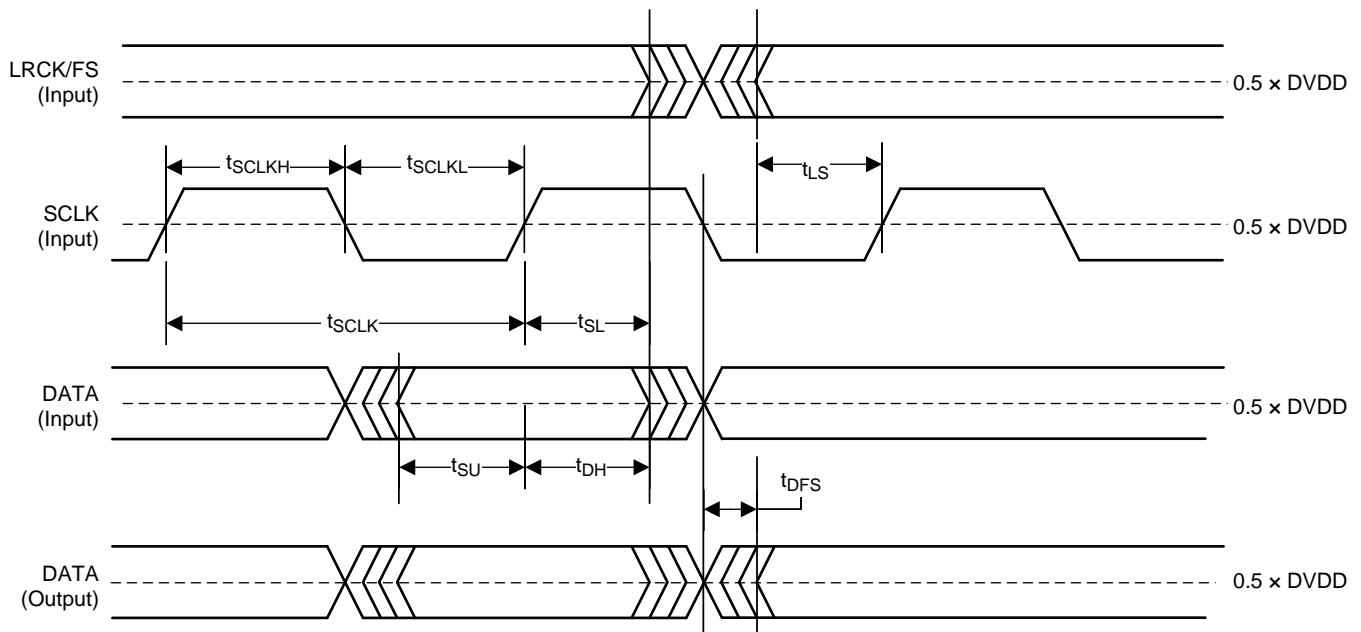
图 64. **Serial Audio Port Timing in Slave Mode**
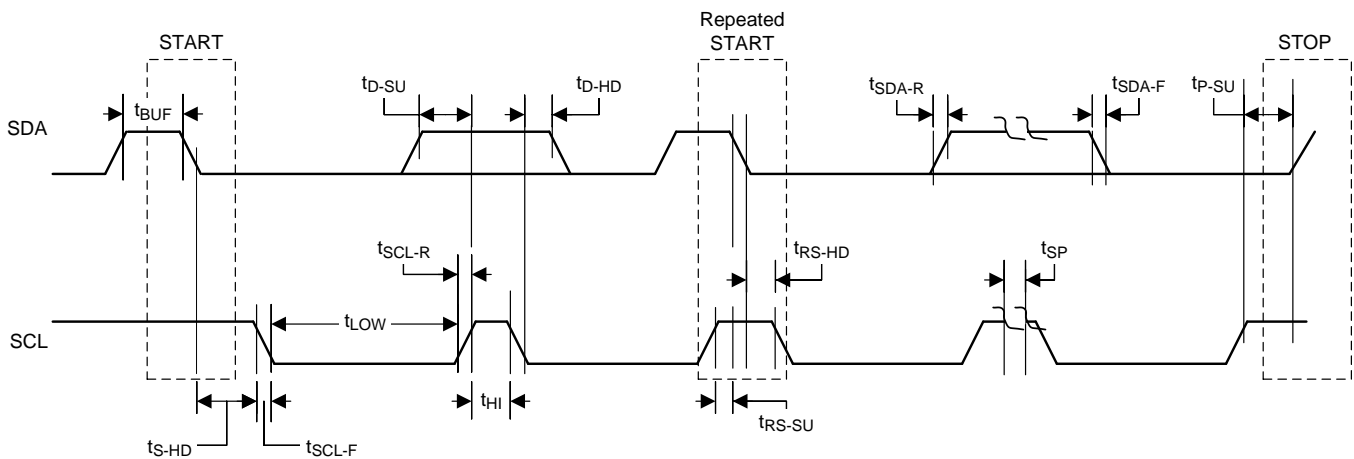
图 65. **I²C Communication Port Timing Diagram**

9 Detailed Description

9.1 Overview

The TAS5806MD device integrates 5 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and easy of use. The 5 main building blocks are listed as follows:

- A stereo audio DAC.
- An Audio DSP subsystem.
- A flexible close-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I²C control port for communication with the device
- An Integrated Directpath™ Headphone amplifier and line driver

The device requires only three power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. A HPVDD supply is required to power the charge pump for Headphone/Line driver. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Onel LDO converts PVDD to 5 V for AVDD and internal GVDD, another one converts DVDD to 1.5V for internal digital core.

9.2 Functional Block Diagram
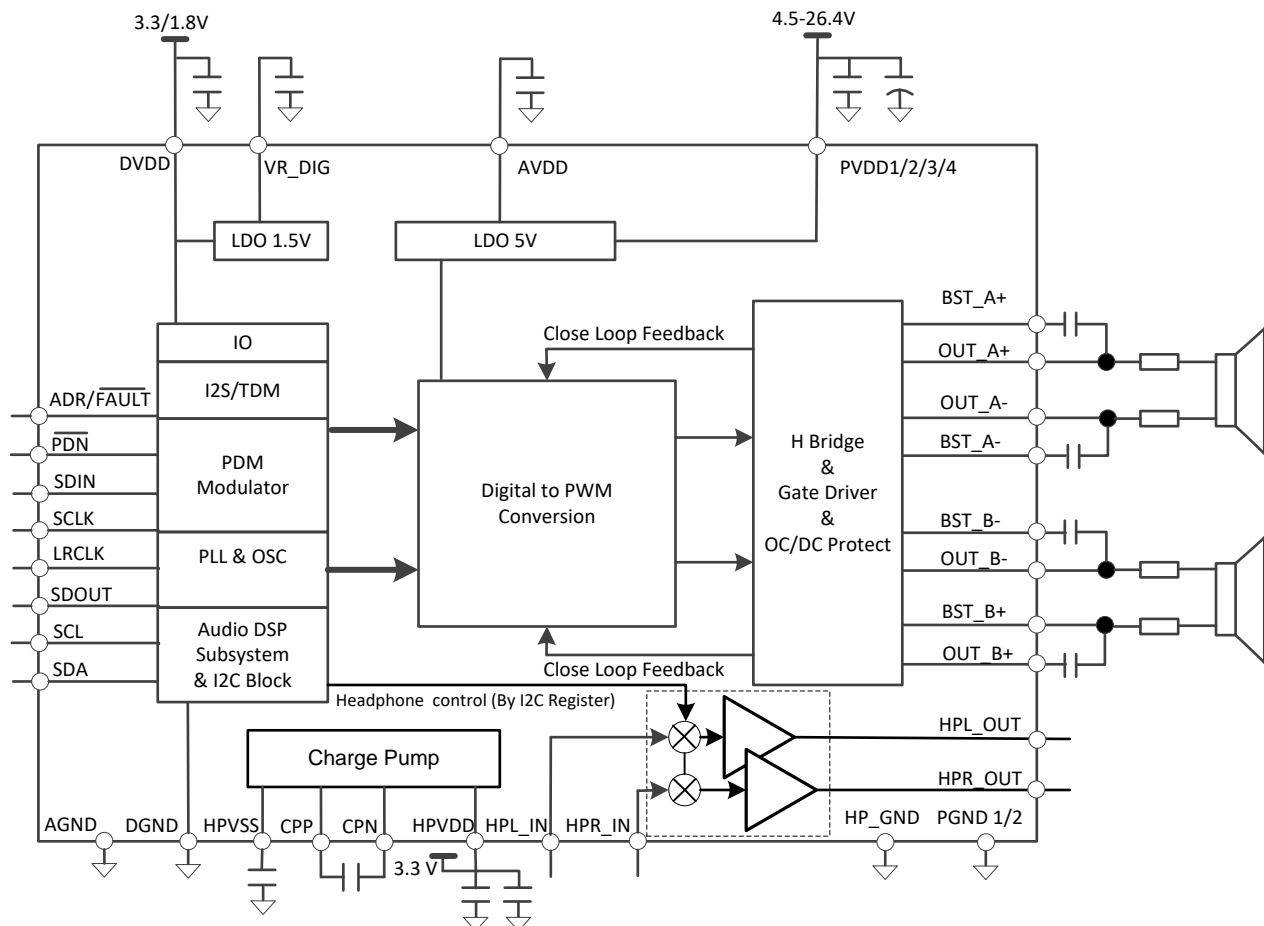
9.3 Feature Description

9.3.1 Power Supplies

To facilitate system design, TAS5806MD needs only a 3.3-V or 1.8-V supply in addition to the (typical) 12 V or 24 V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (AVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (AVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

9.3.2 Device Clocking

The TAS5806MD devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.
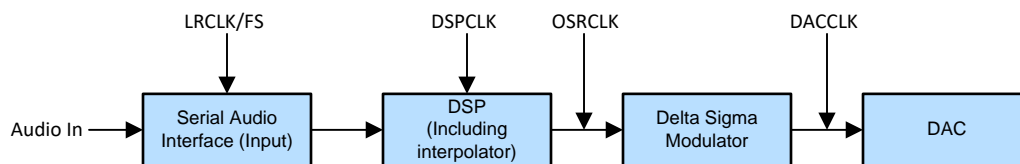
图 66. **Audio Flow with Respective Clocks**

图 66 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:
- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The TAS5806MD device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32 kHz, 44.1kHz – 48 kHz, 88.2 kHz – 96 kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

9.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5806MD device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

表 1. **Audio Data Formats, Bit Depths and Clock Rates**

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^{2}S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32

Feature Description (接下页)

表 1. Audio Data Formats, Bit Depths and Clock Rates (接下页)

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256

Before DSP register initialize with I²C during the startup , TAS5806MD requires stable I²S ready. When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

9.3.4 Clock Halt Auto-recovery

As some of host processor will Halt the I²S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

9.3.5 Sample Rate on the Fly Change

TAS5806MD supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32kHz to 48kHz or 96kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 100us before changing to the new sample rate.

9.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (P0-R51-D[5:4]). If the high width of LRCK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (P0-R51-D[3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 1 through Figure 6. The word length are selected via Register (P0-R51-D[1:0]). The offsets of data are selected via Register (P0-R51-D[7]) and Register (P0-R52-D[7:0]). Default setting is I2S and 24 bit word length.
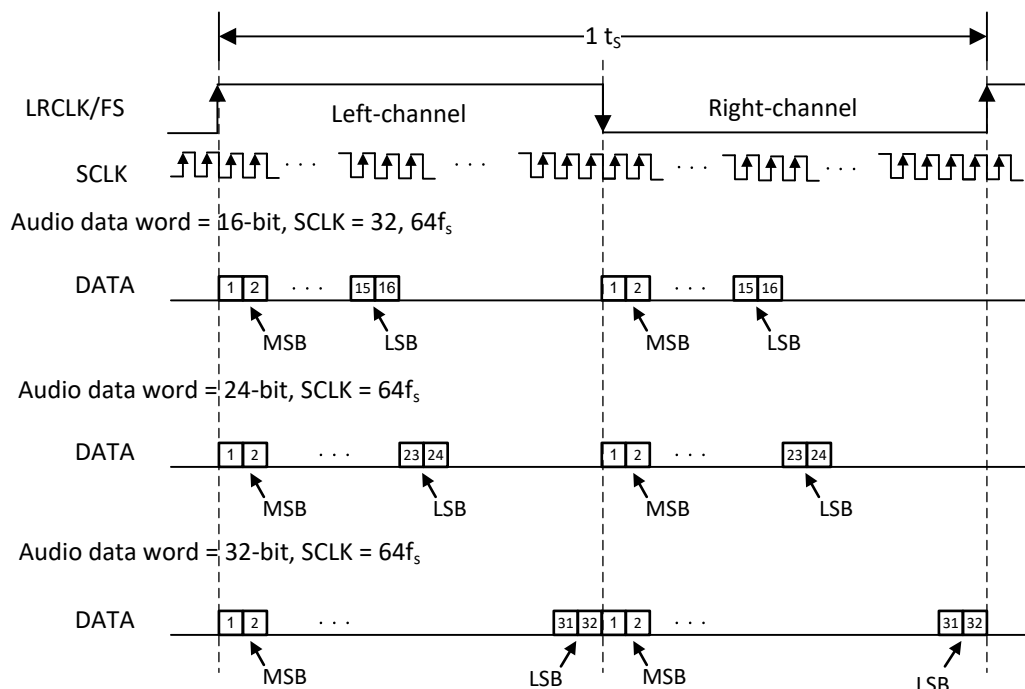
图 67. Left Justified Audio Data Format
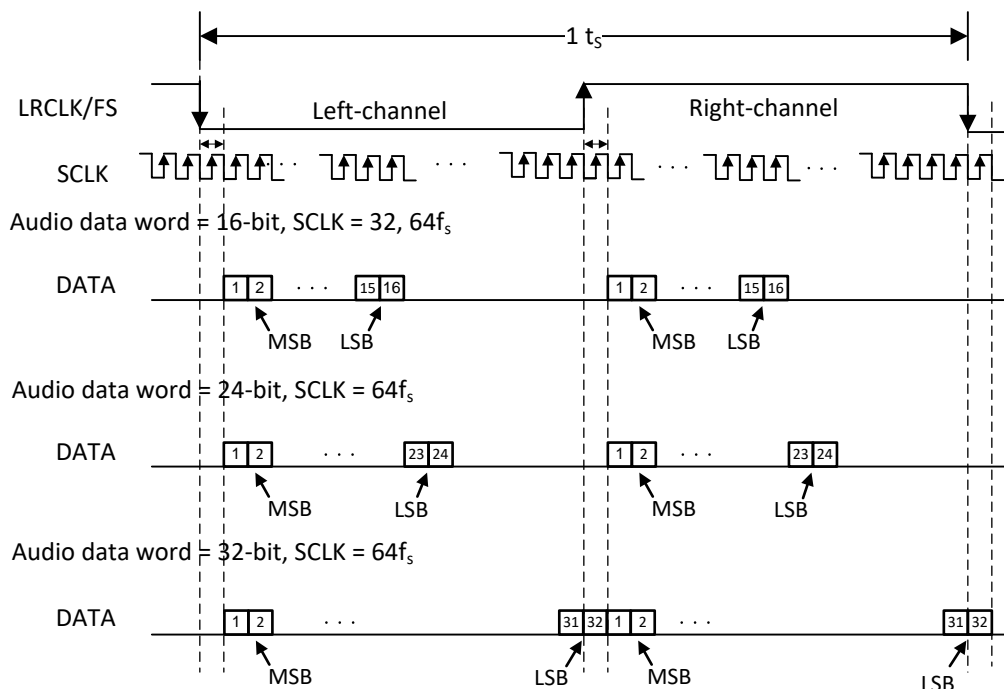
I^2S Data Format; L-channel = LOW, R-channel = HIGH

图 68. I^2S Audio Data Format
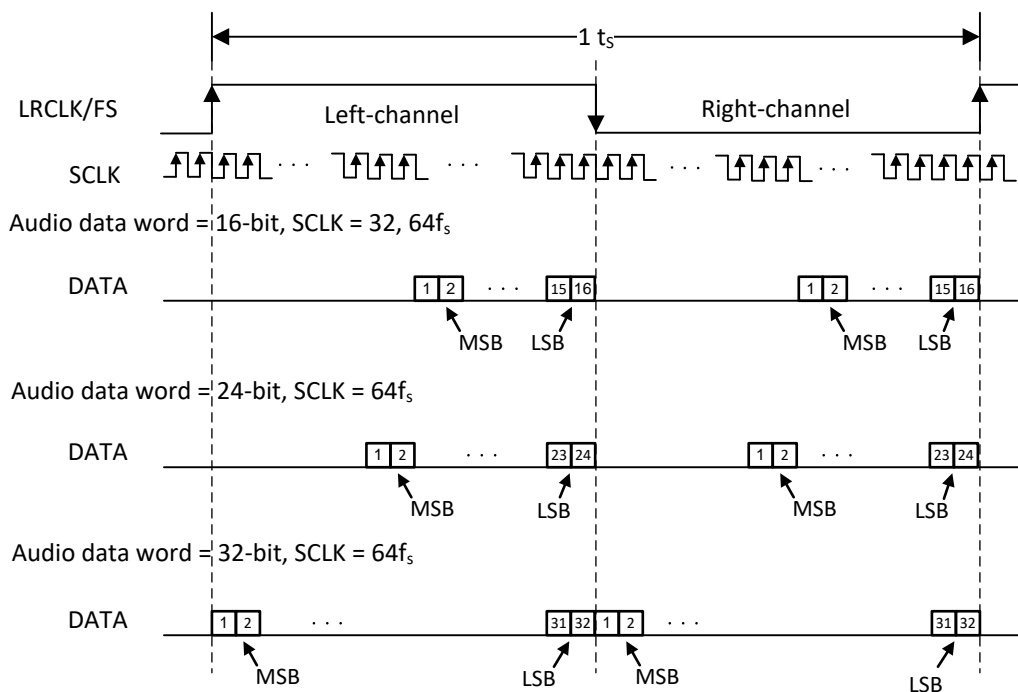
Right Justified Data Format; L-channel = HIGH, R-channel = LOW

图 69. Right Justified Audio Data Format
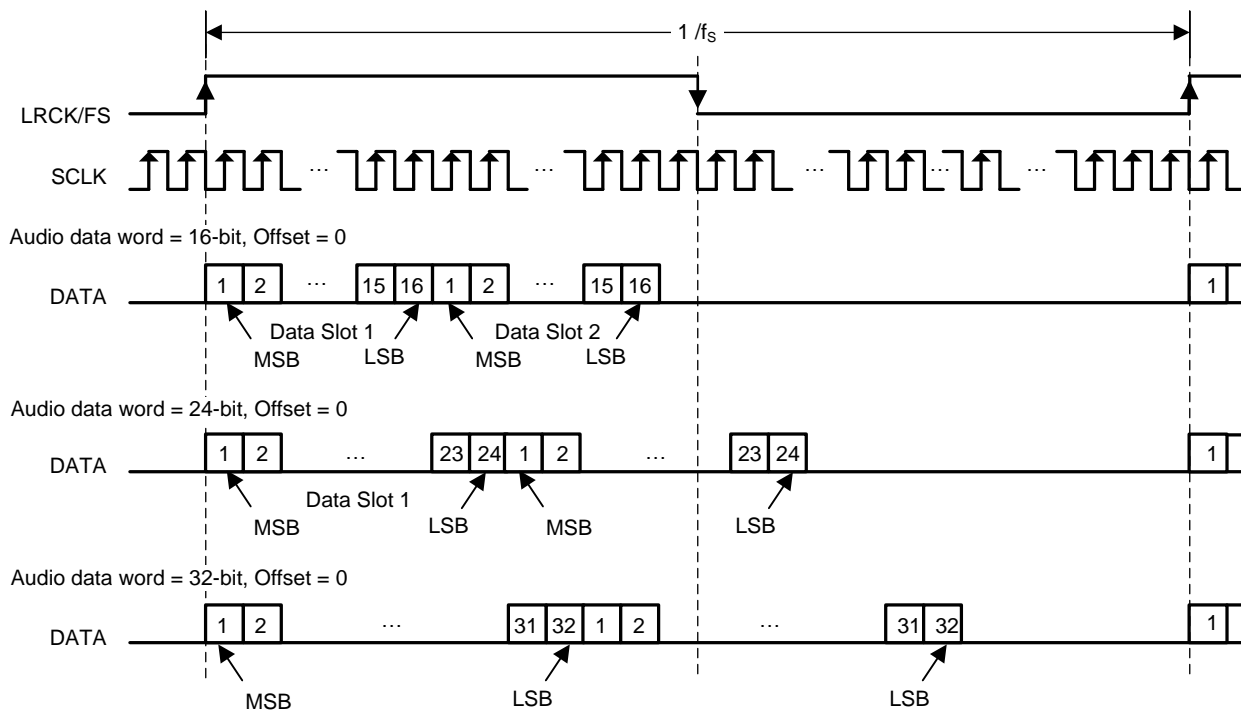
TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

图 70. TDM 1 Audio Data Format
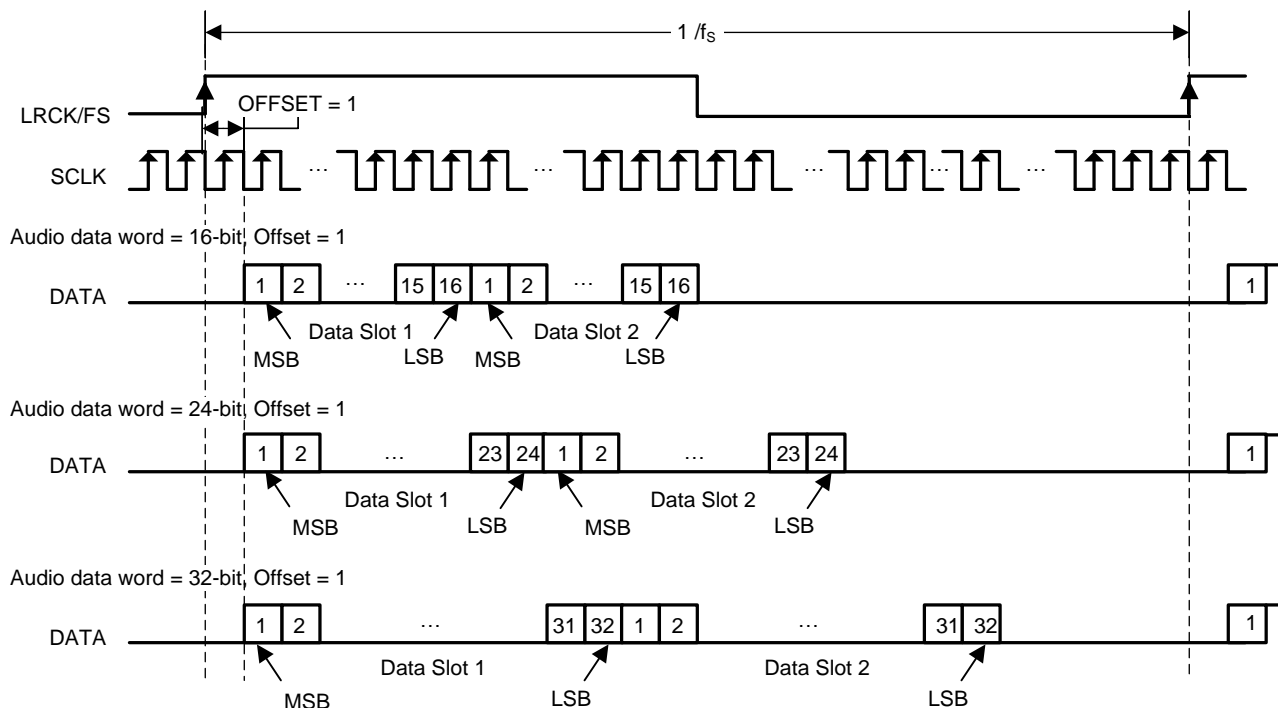
TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

图 71. TDM 2 Audio Data Format

The I2S slave timing is shown in .

9.3.7 Digital Audio Processing

TAS5806MD DSP has ROM fixed process flows which are same with TAS5805M for different applications, refer to application note, *TAS5805M Process Flows* for details.

9.3.8 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

9.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in 图 72, the audio path of the TAS5806MD consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

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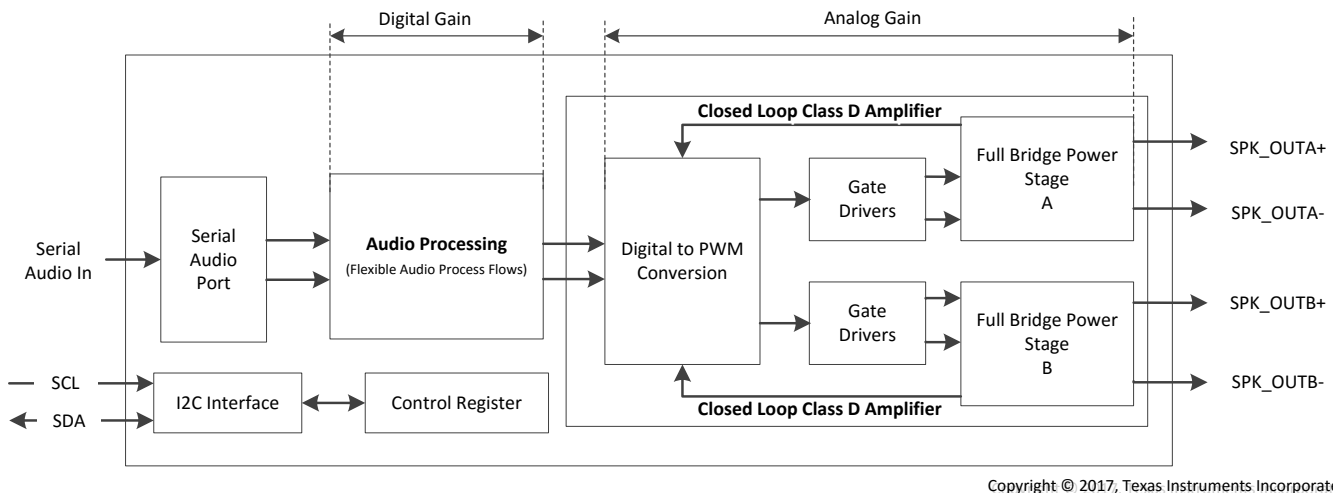
图 72. Speaker Amplifier Gain

As shown in 图 72, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default, it does not change. For all settings of the register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings ensure that the output signal is not clipping at different PVDD levels. 0dBFS output is 29.5-V peak output voltage

表 2. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
……..	……..	…….
11111	-15.5	4.95

9.4 Device Functional Modes

9.4.1 Software Control

The TAS5806MD device is configured via an I^2 C communication port.

The I2C Communication Protocol is detailed in the I^{2}C Communication Port section. The I^{2}C timing requirements are described in the I^{2}C Bus Timing – Standard and I^{2}C Bus Timing – Fast sections.

9.4.2 Speaker Amplifier Operating Modes

The TAS5806MD device can be used in two different amplifier configurations:
• BTL Mode
• PBTL Mode

9.4.2.1 BTL Mode

In BTL mode , the TAS5806MD device amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

9.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5806MD device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5806MD device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

9.4.3 Low EMI Modes

TAS5806MD employs several modes to minimize EMI during playing audio, and they can be used based on different applications.

9.4.3.1 Minimize EMI with Spread Spectrum

This device supports spread spectrum with triangle mode, Spread spectrum is used to minimize the EMI noise.

User need configure register SS_CTRL0 (0x6B) to Enable triangle mode and enable spread spectrum, and select spread spectrum frequency and range with SS_CTRL1 (0x6C). For 384kHz FSW which configured by DEVICE_CTRL1 (0x02), the spread spectrum frequency and range are described in Table 3.

表 3. Spread Spectrum Setting

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example-Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz, take I^{2}C device address 0x58 as an example:

w 58 6b 03 //Enable Spread Spectrum.

w 58 6c 03 //SS_TRI_CTRL[3:0]0011, Triangle Frequency = 24kHz, Spread Spectrum Range should be 25% (336kHz~432kHz).

9.4.3.2 Channel to Channel Phase shift

This device support channel to channel 180 degree PWM phase shift to minimize the EMI.

9.4.3.3 *Multi-Devices PWM Phase Synchronization*

This device support up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 devices, user can select phase 0/1/2/3 for each device by register PHASE_CTRL (0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I²S clock during the Startup Phase.

1. Halt I²S clock.
2. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x03 for device 0; Register 0x6A = 0x07 for device 1; Register 0x6A = 0x0B for device 2; Register 0x6A = 0x0F for device 3. There should be a 45 degree PWM phase shift between each device to minimize the EMI.
3. Configure each device into HIZ mode.
4. Provide I²S to each device. Phase synchronization for all 4 devices will be automatically done by internal sequence.
5. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
6. Device to Device PWM phase shift should be fixed with 45 degree.

9.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5806MD from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5806MD to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (135C typ), an internal AGL (Automatic Gain Limiter) will reduce the digital gain automatically. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5806MD App in PurePathTM Console3.

9.4.5 Headphone Control

TAS5806MD supports Headphone/Line driver control with I²C command which includes Headphone/Line driver gain control and Mute/Shutdown control.
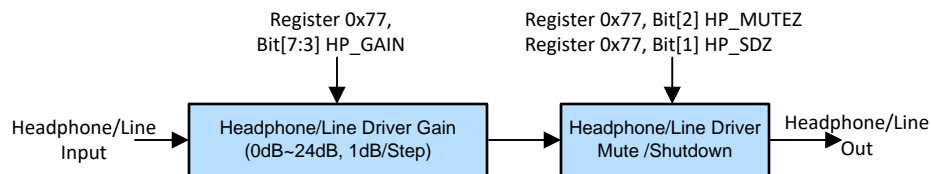
图 73. Headphone/Line driver control with I²C

9.4.6 Device State Control

TAS5806MD has 5 states with different power dissipation which listed in the Electrical Characteristics Table.

- Shutdown Mode. With PDN pin pull down to GND. All internal LDOs (1.5V for digital core, 5V for analog) are disabled, all registers will be cleared to default value.

注

Exit from Shutdown Mode and re-enter into Play mode, need reload all register configurations (which generated by PurePath Console3) again.

- Deep Sleep Mode. Deep Sleep Mode. Register 0x03h -D[1:0]=00, device stays in Deep Sleep Mode. In this mode, I2C block and 1.5V LDO for digital core still working, but internal 5V LDO (For AVDD and MOSFET gate driver) is disabled for low power dissipation. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, TAS5806MD can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Unlike the Shutdown Mode (Pulling PDN Low), entering or exiting Deep Sleep Mode, the DSP keeps active.
- Sleep Mode. Register 0x03h -D[1:0]=01, device stays in Sleep Mode. In this mode, I²C block, Digital core, DSP Memory , 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull PDN Low), enter or exit

Sleep Mode, DSP keeps active. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.

- Output Hiz Mode. Register 0x03h -D[1:0]=10, device stays in Hiz Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.

- Play Mode. Register 0x03h -D[1:0]=11, device stays in Play Mode.

9.4.7 Device Modulation

TAS5806MD has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for with Register 0x02 [1:0]-DAMP_MOD.

9.4.7.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.
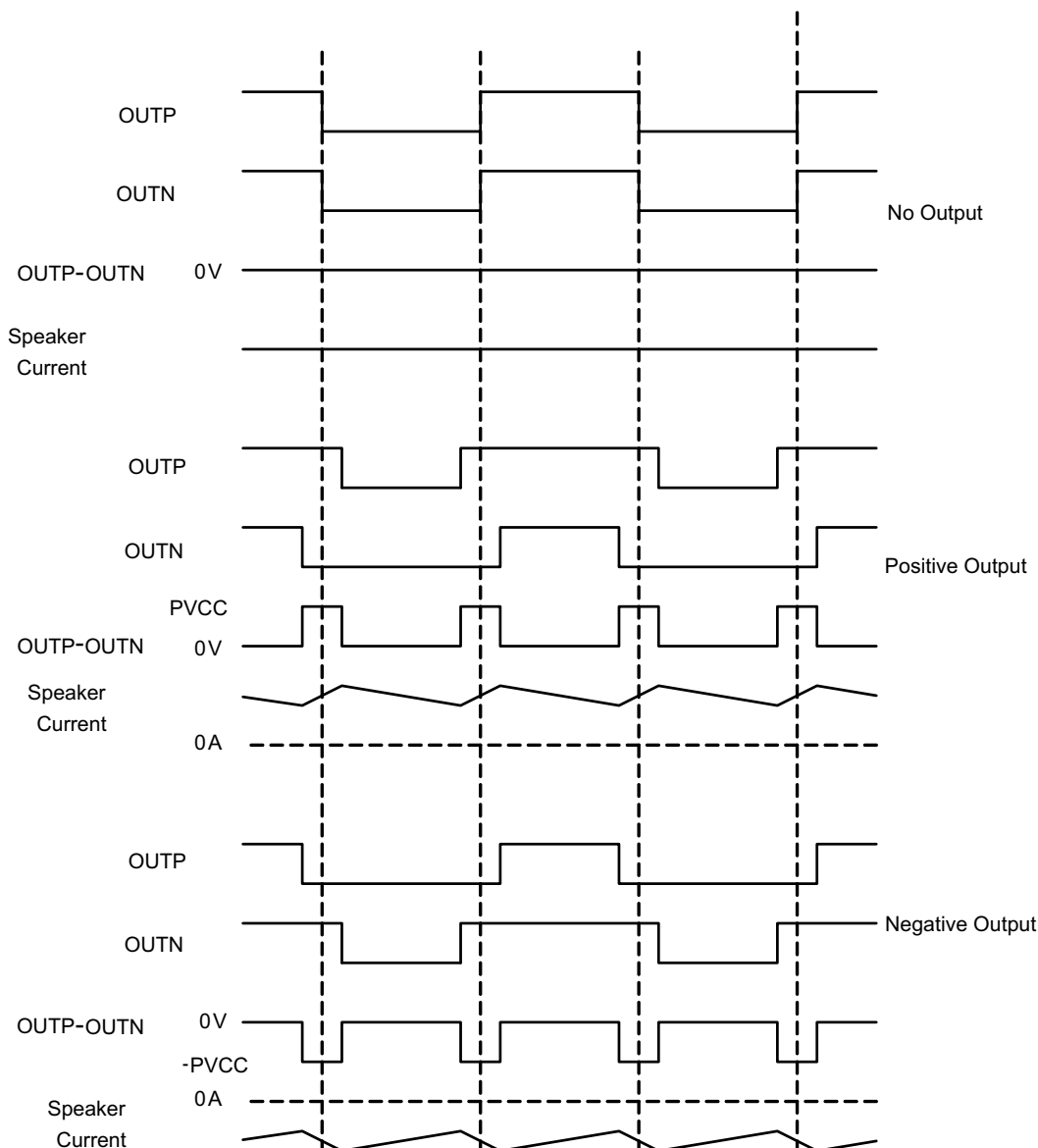
图 74. BD Mode Modulation

9.4.7.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~14% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.
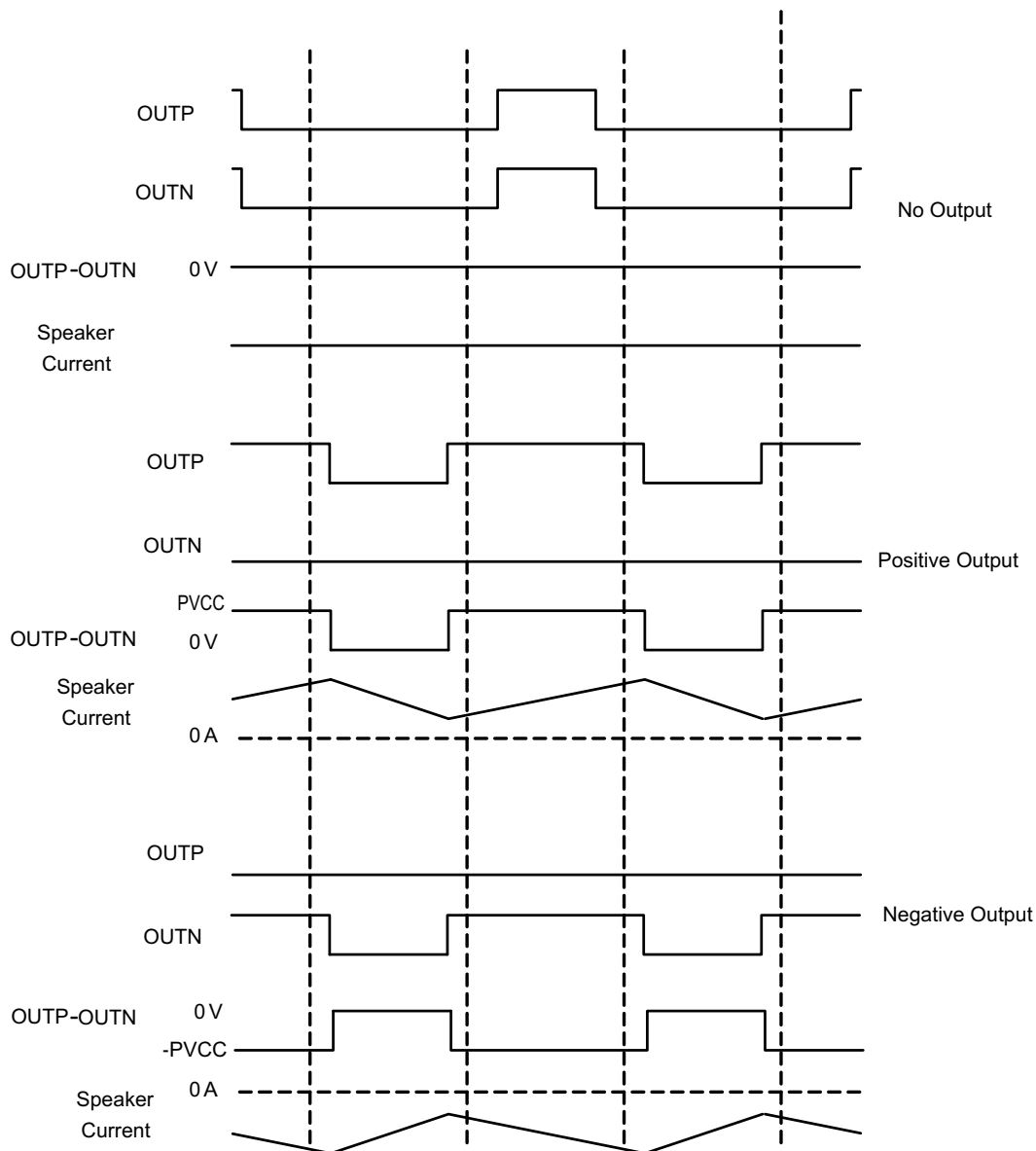
图 75. 1SPW Mode Modulation

9.4.7.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5806MD will detect the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the Hybrid Modulation.

注
To use the Hybrid Modulation, users need to enter the system's PVDD value on the TAS5806MD PPC3 App.

9.5 Programming and Control

9.5.1 I^2 C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the I^{2}C bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a slave device. Because the TAS5806MD register map and DSP memory spans multi pages, the user should change from page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255.

9.5.2 Slave Address

The TAS5806MD device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 01011(0x5x). The next two bits of address byte are the device select bits which can be user-defined by ADR/$\overline{\text{FAULT}}$ pin in 表 4.

表 4. I^2 C Slave Address Configuration

ADR/$\overline{\text{FAULT}}$ PIN Configuration	MSBs					User Define		LSB
4.7k Ω to DVDD	0	1	0	1	1	0	0	R/$\overline{\text{W}}$
15kΩ to DVDD	0	1	0	1	1	0	1	R/$\overline{\text{W}}$
47kΩ to DVDD	0	1	0	1	1	1	0	R/$\overline{\text{W}}$
120kΩ to DVDD	0	1	0	1	1	1	1	R/$\overline{\text{W}}$

9.5.2.1 Random Write

As shown in 图 76, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^{2}C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.
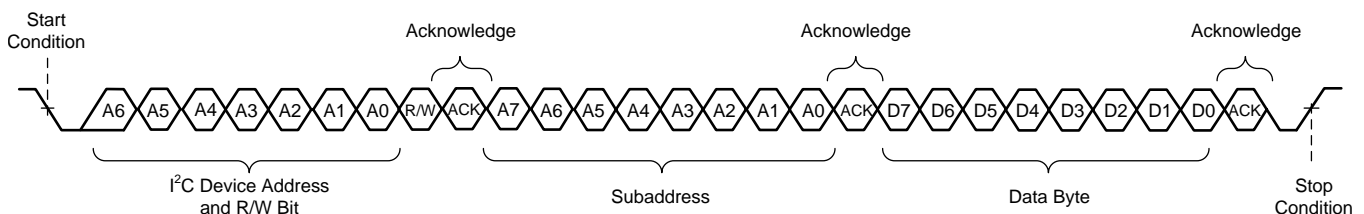
图 76. Random Write Transfer

9.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in 图 77. After receiving each data byte, the device responds with an acknowledge bit and the I^2 subaddress is automatically incremented by one.
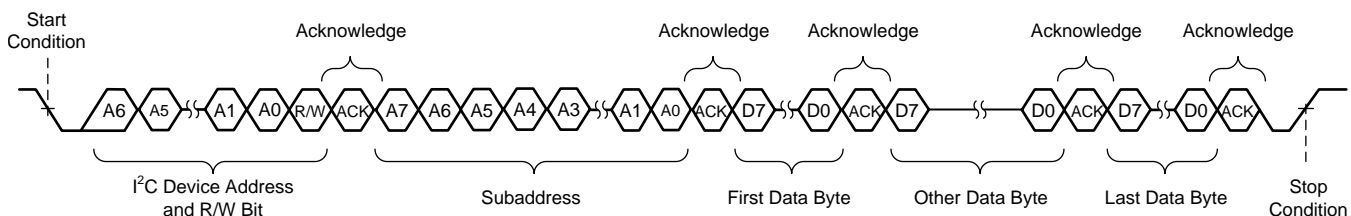
图 77. Sequential Write Transfer

9.5.2.3 Random Read

As shown in 图 78, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.
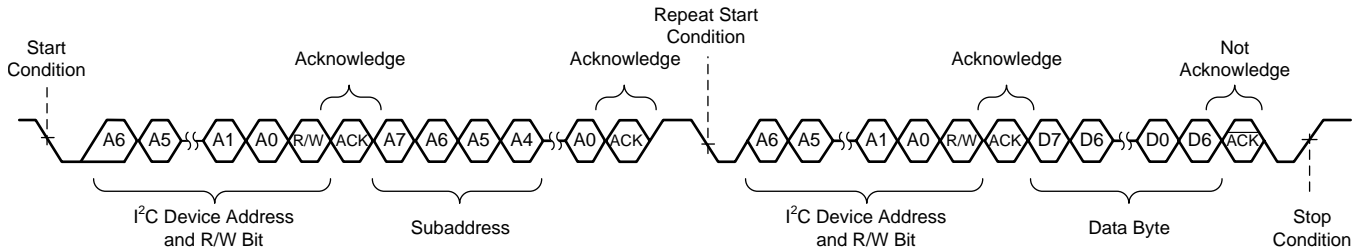
图 78. Random Read Transfer

9.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in 图 79. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.
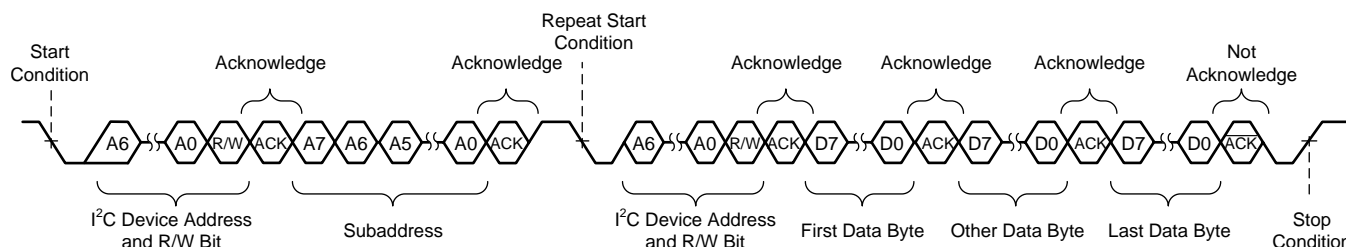
图 **79. Sequential Read Transfer**

9.5.2.5 DSP Memory Book, Page and BQ update

The TAS5806MD device supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device.

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

Because the TAS5806MD register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes.

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in Book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest.

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5805M Process Flows

9.5.2.6 Example Use

Example 1, The following is a sample script for configuring a device on I²C slave address 0x58 and set the device switching frequency to 768kHz with Class D loop bandwidth to 175kHz, 1SPW Modulation:

w 58 00 00 #Go to Page0

w 58 7f 00 #Change the Book to 0x00

w 58 00 00 #Go to Page 0x00

w 58 02 01 #Set switching frequency to 768kHz with 1SPW Modulation

w 58 53 60 #Set Class D Loop Bandwidth to 175kHz

Example 2, The following is a sample script for configuring a device on I2C slave address 0x58 and using the DSP host memory to change the digital volume to the default value of 0dB:

w 58 00 00 #Go to Page 0

w 58 7f 8c #Change the Book to 0x8C

w 58 00 2a #Go to Page 0x2a

w 58 24 00 80 00 00 #change digital volume to 0dB

9.5.2.7 *Checksum*

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

9.5.2.7.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, $(1 + x1 + x2 + x8)$). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I^{2}C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

9.5.2.7.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

9.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

9.5.3.1 Startup Procedures

1. Configure ADR/$\overline{\text{FAULT}}$ pin with proper setting for I²C device address.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once power supplies are stable, bring up $\overline{\text{PDN}}$ to High and wait 5ms at least, then start SCLK, LRCLK. .
4. Once I²S clocks are stable, set the device into HiZ state and enable DSP via the I2C control port.
5. Wait 5ms at least. Then initialize the DSP Coefficient, then set the device to Play state.
6. The device is now in normal operation.
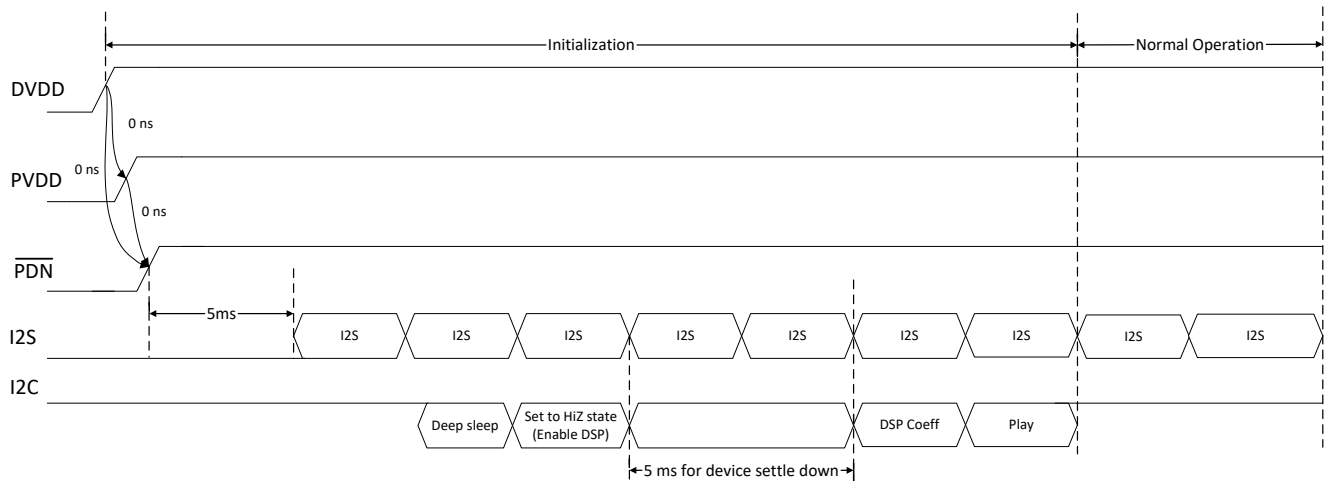
图 80. **Start-up Sequence**

9.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h -D[1:0]=10 (Hi-Z) via the I2C control port or Pull $\overline{\text{PDN}}$ low.
3. Wait at least 6 ms (this time depends on the LRCLK/FS rate ,digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.
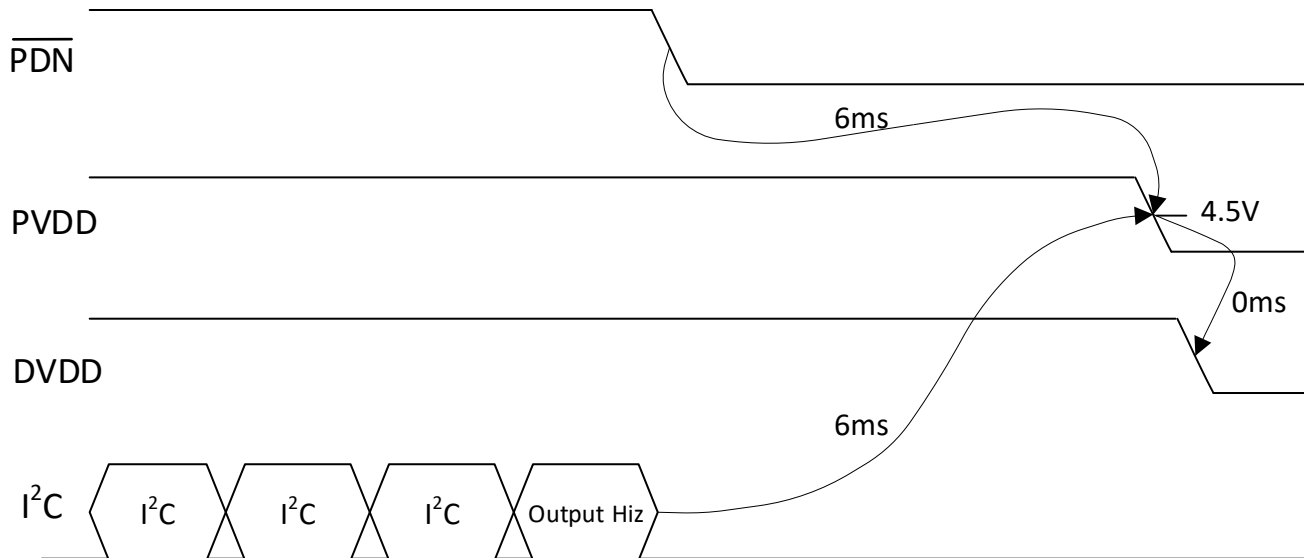
(1) Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{PDN}$ or by I²C.

(2) At least 6 ms delay needed based on LRCLK (Fs) = 48 kHz. Digital volume ramp down update every sample period, decreased by 0.5 dB for each update, digital volume = 24 dB. Change the value of register 0x4C and 0x4E or change the LRCLK rate, the delay changes.

图 81. Power-down Sequence

9.5.3.3 Protection and Monitoring

9.5.3.3.1 Overcurrent Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I²C. An OCSD event activates the fault pin, and the I² fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OSCD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

9.5.3.3.2 DC Detect

If the TAS5806MD device measures a DC offset in the output voltage, the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault.

9.6 Register Maps

9.6.1 CONTROL PORT Registers

Table 5 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Go
2h	DEVICE_CTRL_1	Register 2	Go
3h	DEVICE_CTRL_2	Register 3	Go
Fh	I2C_PAGE_AUTO_INC	Register 15	Go
28h	SIG_CH_CTRL	Register 40	Go
29h	CLOCK_DET_CTRL	Register 41	Go
30h	SDOUT_SEL	Register 48	Go
31h	I2S_CTRL	Register 49	Go
33h	SAP_CTRL1	Register 51	Go
34h	SAP_CTRL2	Register 52	Go
35h	SAP_CTRL3	Register 53	Go
37h	FS_MON	Register 55	Go
38h	BCK_MON	Register 56	Go
39h	CLKDET_STATUS	Register 57	Go
40h	CHANNEL_FORCE_HIZ	Register 58	Go
4Ch	DIG_VOL_CTRL	Register 76	Go
4Eh	DIG_VOL_CTRL2	Register 78	Go
4Fh	DIG_VOL_CTRL3	Register 79	Go
50h	AUTO_MUTE_CTRL	Register 80	Go
51h	AUTO_MUTE_TIME	Register 81	Go
53h	ANA_CTRL	Register 83	Go
54h	AGAIN	Register 84	Go
5Ch	BQ_WR_CTRL1	Register 92	Go
5Dh	DAC_CTRL	Register 93	Go
60h	ADR_PIN_CTRL	Register 96	Go
61h	ADR_PIN_CONFIG	Register 97	Go
66h	DSP_MISC	Register 102	Go
67h	DIE_ID	Register 103	Go
68h	POWER_STATE	Register 104	Go
69h	AUTOMUTE_STATE	Register 105	Go
6Ah	PHASE_CTRL	Register 106	Go
6Bh	SS_CTRL0	Register 107	Go
6Ch	SS_CTRL1	Register 108	Go
6Dh	SS_CTRL2	Register 109	Go
6Eh	SS_CTRL3	Register 110	Go
6Fh	SS_CTRL4	Register 111	Go
70h	CHAN_FAULT	Register 112	Go
71h	GLOBAL_FAULT1	Register 113	Go
72h	GLOBAL_FAULT2	Register 114	Go
73h	OT WARNING	Register 115	Go
74h	PIN_CONTROL1	Register 116	Go
75h	PIN_CONTROL2	Register 117	Go

Table 5. CONTROL PORT Registers (continued)

Offset	Acronym	Register Name	Section
76h	MISC_CONTROL	Register 118	Go
77h	HP_CONTROL	Register 119	Go
78h	FAULT_CLEAR	Register 120	Go

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.6.1.1 RESET_CTRL Register (Offset = 1h) [reset = 0x00]

RESET_CTRL is shown in Figure 82 and described in Table 7.

Return to Summary Table.

Figure 82. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
R/W			W	R			W

Table 7. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_MOD	W	0	WRITE CLEAR BIT Reset Modules WRITE CLEAR BIT Reset full digital core This bit resets full digital signal chain (Include DSP and Control Port Registers). Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. 0: Normal 1: Reset modules
3-1	RESERVED	R	000	This bit is reserved
0	RST_CONTROL_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the control port registers back to their initial values. The RAM content is not cleared. 0: Normal 1: Reset control port registers

9.6.1.2 *DEVICE_CTRL_1 Register (Offset = 2h) [reset = 0x00]*

DEVICE_CTRL_1 is shown in Figure 83 and described in Table 8.

Return to Summary Table.

Figure 83. DEVICE_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTL	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

Table 8. DEVICE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW 000:768K 001:384K 011:480K 100:576K 010:Reserved 101:Reserved 110:Reserved 111:Reserved
3	RESERVED	R/W	0	This bit is reserved
2	DAMP_PBTL	R/W	0	0: SET DAMP TO BTL MODE 1: SET DAMP TO PBTL MODE
1-0	DAMP_MOD	R/W	00	00:BD MODE 01:1SPW MODE 10:HYBRID MODE

9.6.1.3 DEVICE_CTRL_2 Register (Offset = 3h) [reset = 0x10]

DEVICE_CTRL_2 is shown in Figure 84 and described in Table 9.

Return to Summary Table.

Figure 84. DEVICE_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

Table 9. DEVICE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute Both Left /Right Channel This bit issues soft mute request for the left/right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	Device state control register 00: Deep Sleep 01: Sleep 10: Hiz (Set both A channel and B channel to Hiz) Notes: For separate channel Hiz, see details in Table 21 11: PLAY

9.6.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [reset = 0x00]

I2C_PAGE_AUTO_INC is shown in Figure 85 and described in Table 10.

Return to Summary Table.

Figure 85. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

Table 10. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

9.6.1.5 SIG_CH_CTRL Register (Offset = 28h) [reset = 0x00]

SIG_CH_CTRL is shown in Figure 86 and described in Table 11.

Return to Summary Table.

Figure 86. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCK_RATIO_CONFIGURE				FS_MODE			
R/W				R/W			

Table 11. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured BCK ratio, the number of BCK clocks in one audio frame. 0011: 32FS 0101: 64FS 0111: 128FS 1001: 256FS 1011: 512FS
3-0	FS_MODE	R/W	0000	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 0000: Auto detection 0110: 32KHz 1000: 44.1KHz 1001: 48KHz 1010: 88.2KHz 1011: 96KHz Others Reserved

9.6.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [reset = 0x00]

CLOCK_DET_CTRL is shown in Figure 87 and described in Table 12.

Return to Summary Table.

Figure 87. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_BCL K_RANGE	DIS_DET_FS	DIS_DET_BCL K	DIS_DET_MIS S	RESERVED	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 12. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	DIS_DET_BCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256KHz and 50MHz or an error will be reported. When ignored, a BCK range error will not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error.But CLKDET_STATUS will report fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_BCLK	R/W	0	Ignore BCK Detection This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. 0: Regard BCK detection 1: Ignore BCK detection
2	DIS_DET_MISS	R/W	0	Ignore BCK Missing Detection This bit controls whether to ignore the BCK missing detection. When ignored an BCK missing will not cause a clock error. 0: Regard BCK missing detection 1: Ignore BCK missing detection
1	RESERVED	R/W	0	This bit is reserved
0	RESERVED	R/W	0	This bit is reserved

9.6.1.7 SDOUT_SEL Register (Offset = 30h) [reset = 0h]

SDOUT_SEL is shown in Figure 88 and described in Table 13.

Return to Summary Table.

Figure 88. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
							R/W

Table 13. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED		0	This bit is reserved
0	SDOUT_SEL	R	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

9.6.1.8 I2S_CTRL Register (Offset = 31h) [reset = 0x00]

I2S_CTRL is shown in Figure 89 and described in Table 14.

Return to Summary Table.

Figure 89. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCK_INV	RESERVED		RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

Table 14. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	BCK_INV	R/W	0	BCK Polarity This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode
4-0	RESERVED	R/W	00000	This bit is reserved

9.6.1.9 SAP_CTRL1 Register (Offset = 33h) [reset = 0x02]

SAP_CTRL1 is shown in Figure 90 and described in Table 15.

Return to Summary Table.

Figure 90. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB	RESERVED	DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

Table 15. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: lrclk pulse < 8 SCLK. If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, these two bits need set to 01.
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

9.6.1.10 SAP_CTRL2 Register (Offset = 34h) [reset = 0x00]

SAP_CTRL2 is shown in Figure 91 and described in Table 16.

Return to Summary Table.

Figure 91. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

Table 16. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: offset = 0 BCK (no offset) 000000001: ofsset = 1 BCK 000000010: offset = 2 BCKs and 111111111: offset = 512 BCKs

9.6.1.11 SAP_CTRL3 Register (Offset = 35h) [reset = 0x11]

SAP_CTRL3 is shown in Figure 92 and described in Table 17.

Return to Summary Table.

Figure 92. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		LEFT_DAC_DPATH		RESERVED		RIGHT_DAC_DPATH	
R/W		R/W		R/W		R/W	

Table 17. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	LEFT_DAC_DPATH	R/W	01	Left DAC Data Path. These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	RESERVED	R/W	00	This bit is reserved
1-0	RIGHT_DAC_DPATH	R/W	01	Right DAC Data Path. These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

9.6.1.12 FS_MON Register (Offset = 37h) [reset = 0x00]

FS_MON is shown in Figure 93 and described in Table 18.

Return to Summary Table.

Figure 93. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS			
R/W		R		R			

Table 18. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	BCLK_RATIO_HIGH	R	00	2 msbs of detected BCK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 0000: FS Error 0110: 32KHz 1000: Reserved 1001: 48KHz 1011: 96KHz Others Reserved

9.6.1.13 BCK_MON Register (Offset = 38h) [reset = 0x00]

BCK_MON is shown in Figure 94 and described in Table 19.

Return to Summary Table.

Figure 94. BCK_MON Register

7	6	5	4	3	2	1	0
BCLK_RATIO_LOW							
R							

Table 19. BCK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK ratio, the number of BCK clocks in one audio frame. BCK = 32 FS~512 FS

9.6.1.14 CLKDET_STATUS Register (Offset = 39h) [reset = 0x00]

CLKDET_STATUS is shown in Figure 95 and described in Table 20.

Return to Summary Table.

Figure 95. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

Table 20. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	DET_STATUS	R	0	This bit indicates whether the BCLK is overrate or underrate
4	DET_STATUS	R	0	This bit indicates whether the PLL is overrate
3	DET_STATUS	R	0	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled.
2	DET_STATUS	R	0	This bit indicates whether the BCK is missing or not.
1	DET_STATUS	R	0	This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-512FS to be valid.
0	DET_STATUS	R	0	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag will be also asserted.

9.6.1.15 CHANNEL_FORCE_HIZ Register (Offset = 40h) [reset = 0x01]

CHANNEL_FORCE_HIZ is shown in Figure 96 and described in Table 21.

Return to Summary Table.

Figure 96. CHANNEL_FORCE_HIZ Register

7	6	5	4	3	2	1	0
RESERVED			CH_A_HIZ	CH_B_HIZ	RESERVED		
R/W			R/W	R/W	R/W		

Table 21. CHANNEL_FORCE_HIZ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	These bits are reserved
4	CH_A_HIZ	R/W	0	1: Force Channel A (L channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel A is now controlled by Register 0x03, see Table 9. Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
3	CH_B_HIZ	R/W	0	1: Force Channel B (R channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel B is now controlled by Register 0x03, see Table 9. Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
2-0	RESERVED	R/W	001	These bits are reserved.

9.6.1.16 DIG_VOL_CTL Register (Offset = 4Ch) [reset = 30h]

DIG_VOL_CTL is shown in Figure 97 and described in Table 22.

Return to Summary Table.

Figure 97. DIG_VOL_CTL Register

7	6	5	4	3	2	1	0
PGA							
R/W							

Table 22. DIG_VOL_CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA	R/W	00110000	Digital Volume These bits control both left and right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB .... and 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB .... 11111110: -103 dB 11111111: Mute

9.6.1.17 DIG_VOL_CTRL2 Register (Offset = 4Eh) [reset = 0x33]

DIG_VOL_CTRL2 is shown in Figure 98 and described in Table 23.

Return to Summary Table.

Figure 98. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

Table 23. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each updat 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

9.6.1.18 DIG_VOL_CTRL3 Register (Offset = 4Fh) [reset = 0x30]

DIG_VOL_CTRL3 is shown in Figure 99 and described in Table 24.

Return to Summary Table.

Figure 99. DIG_VOL_CTRL3 Register

7	6	5	4	3	2	1	0
FAST_RAMP_DOWN_SPEED		FAST_RAMP_DOWN_STEP		RESERVED			
R/W		R/W		R/W			

Table 24. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.19 AUTO_MUTE_CTRL Register (Offset = 50h) [reset = 0x07]

AUTO_MUTE_CTRL is shown in Figure 100 and described in Table 25.

Return to Summary Table.

Figure 100. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					REG_AUTO_MUTE_CTRL		
R/W					R/W		

Table 25. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2	REG_AUTO_MUTE_CTRL	R/W	1	0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted
1	REG_AUTO_MUTE_CTRL	R/W	1	0: Disable right channel auto mute 1: Enable right channel auto mute
0	REG_AUTO_MUTE_CTRL	R/W	1	0: Disable left channel auto mute 1: Enable left channel auto mute bit2: .

9.6.1.20 *AUTO_MUTE_TIME Register (Offset = 51h) [reset = 0x00]*

AUTO_MUTE_TIME is shown in Figure 101 and described in Table 26.

Return to Summary Table.

Figure 101. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

Table 26. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

9.6.1.21 ANA_CTRL Register (Offset = 53h) [reset = 0x00]

ANA_CTRL is shown in Figure 102 and described in Table 27.

Return to Summary Table.

Figure 102. ANA_CTRL Register

7	6	5	4	3	2	1	0
			ANA_CTRL				
			R/W				

Table 27. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	ANA_CTRL	R/W	00	Class-D bandwidth control. 00: 80kHz; 01: 100kHz; 10: 120kHz; 11: 175kHz. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance. With Fsw=384kHz, bandwidth should ≤ 120kHz.
4-0	RESERVED	R/W	0000	These bits are reserved

9.6.1.22 AGAIN Register (Offset = 54h) [reset = 0x00]

AGAIN is shown in Figure 103 and described in Table 28.

Return to Summary Table.

Figure 103. AGAIN Register

7	6	5	4	3	2	1	0
	RESERVED				ANA_GAIN		
	R/W				R/W		

Table 28. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control , with 0.5dB one step This bit controls the analog gain. 00000: 0 dB (29.5V peak voltage) 00001: -0.5db 11111: -15.5 dB

9.6.1.23 BQ_WR_CTRL1 Register (Offset = 5Ch) [reset = 0x00]

BQ_WR_CTRL1 is shown in Figure 104 and described in Table 29.

Return to Summary Table.

Figure 104. BQ_WR_CTRL1 Register

7	6	5	4	3	2	1	0
			RESERVED				BQ_WR_FIRST _COEF
			R/W				R/W

Table 29. BQ_WR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.

9.6.1.24 DAC_CTRL Register (Offset = 5Dh) [reset = 0xF8]

DAC_CTRL is shown in Figure 105 and described in Table 30.

Return to Summary Table.

Figure 105. DAC_CTRL Register

7	6	5	4	3	2	1	0
DAC_FREQUE NCY_SEL	DAC_DITHER_EN		DAC_DITHER			DAC_CTRL_DEM_SEL	
R/W	R/W		R/W			R/W	

Table 30. DAC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_FREQUENCY_SEL	R/W	1	DAC Frequency Select 0: 6.144MHz 1: 3.072MHz
6-5	DAC_DITHER_EN	R/W	11	DITHER_EN, 00: disable both stage dither 01: enable main stage dither 10: enable second stage dither 11: enbale both stage dither
4-2	DAC_DITHER	R/W	110	Dither level 100: -2^-7 101: -2^-8 110: -2^-9 111: -2^-10 000: -2^-13 001: -2^-14 010: -2^-15 011: -2^-16
1-0	DAC_CTRL_DEM_SEL	R/W	00	00: Enable DEM 11: Disable DEM

9.6.1.25 ADR_PIN_CTRL Register (Offset = 60h) [reset = 0h]

ADR_PIN_CTRL is shown in Figure 106 and described in Table 31.

Return to Summary Table.

Figure 106. ADR_PIN_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							ADR_OE
							R/W - 0x0

Table 31. ADR_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	ADR_OE	R/W	0	ADR Output Enable This bit sets the direction of the ADR pin 0: ADR is input 1: ADR is output

9.6.1.26 ADR_PIN_CONFIG Register (Offset = 61h) [reset = 0x00]

ADR_PIN_CONFIG is shown in Figure 107 and described in Table 32.

Return to Summary Table.

Figure 107. ADR_PIN_CONFIG Register

7	6	5	4	3	2	1	0
	RESERVED			ADR_PIN_CONFIG			
				R/W			

Table 32. ADR_PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	These bits are reserved
4-0	ADR_PIN_CONFIG	R/W	00000	00000: off (low)
				00011: Auto mute flag (asserted when both L and R channels are auto muted)
				00100: Auto mute flag for left channel 0101: Auto mute flag for right channel
				00110: Clock invalid flag (clock error or clock missing)
				00111: Reserved
				01001: Reserved
				01011: ADR as FAULTZ output

9.6.1.27 DSP_MISC Register (Offset = 66h) [reset = 0h]

DSP_MISC is shown in Figure 108 and described in Table 33.

Return to Summary Table.

Figure 108. DSP_MISC Register

7	6	5	4	3	2	1	0
			BYPASS_CONTROL				
			R/W				

Table 33. DSP_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	These bits are reserved
3	BYPASS CONTROL	R/W	0	1: Left and Right will have use unique coef 0->Right channel will share left channel coefficient
2	BYPASS CONTROL	R/W	0	1: bypass 128 tap FIR
1	BYPASS CONTROL	R/W	0	1: bypass DRC (Only bypass DRC in L/R channel)
0	BYPASS CONTROL	R/W	0	1: bypass EQ (Only bypass EQs in L/R channel)

9.6.1.28 DIE_ID Register (Offset = 67h) [reset = 0h]

DIE_ID is shown in Figure 109 and described in Table 34.

Return to Summary Table.

Figure 109. DIE_ID Register

7	6	5	4	3	2	1	0
			DIE_ID				
			R-0h				

Table 34. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	0h	DIE ID

9.6.1.29 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in Figure 110 and described in Table 35.

Return to Summary Table.

Figure 110. POWER_STATE Register

7	6	5	4	3	2	1	0
			STATE_RPT				
			R				

Table 35. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	0: Deep sleep 1: Sleep 2: HIZ 3: Play Others: reserved

9.6.1.30 AUTOMUTE_STATE Register (Offset = 69h) [reset = 0x00]

AUTOMUTE_STATE is shown in Figure 111 and described in Table 36.

Return to Summary Table.

Figure 111. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						ZERO_RIGHT_MON	ZERO_LEFT_MON
R						R	R

Table 36. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

9.6.1.31 PHASE_CTRL Register (Offset = 6Ah) [reset = 0x00]

PHASE_CTRL is shown in Figure 112 and described in Table 37.

Return to Summary Table.

Figure 112. PHASE_CTR Register

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		PHASE_SYNC_SEL	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

Table 37. PHASE_CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/W	00	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. 00: phase0 01: phase1 10: phase2 11: phase3
1	I2S_SYNC_EN	R/W	0	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0	0: RAMP phase sync disable 1: RAMP phase sync enable

9.6.1.32 SS_CTRL0 Register (Offset = 6Bh) [reset = 0x00]

SS_CTRL0 is shown in Figure 113 and described in Table 38.

Return to Summary Table.

Figure 113. SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SS_PRE_DIV_SEL	SS_MANUAL_MODE	RESERVED		SS_RDM_EN	SS_TRI_EN
R/W	R/W	R/W	R/W	R/W		R/W	R/W

Table 38. SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	Select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	Set ramp ss controller to manual mode
3-2	RESERVED	R/W	0	This bit is reserved
1	SS_RDM_EN	R/W	0	Random SS enable
0	SS_TRI_EN	R/W	0	Triangle SS enable

9.6.1.33 SS_CTRL1 Register (Offset = 6Ch) [reset = 0x00]

SS_CTRL1 is shown in Figure 114 and described in Table 39.

Return to Summary Table.

Figure 114. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	SS_RDM_CTRL			SS_TRI_CTRL			
R/W	R/W			R/W			

Table 39. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	Random SS range control
3-0	SS_TRI_CTRL	R/W	0000	Triangle SS frequency and range control

9.6.1.34 SS_CTRL2 Register (Offset = 6Dh) [reset = 0x50]

SS_CTRL2 is shown in Figure 115 and described in Table 40.

Return to Summary Table.

Figure 115. SS_CTRL2 Register

7	6	5	4	3	2	1	0
TM_FREQ_CTRL
R/W

Table 40. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	01010000	Control ramp frequency in manual mode, F=61440000/N

9.6.1.35 SS_CTRL3 Register (Offset = 6Eh) [reset = 0x11]

SS_CTRL3 is shown in Figure 116 and described in Table 41.

Return to Summary Table.

Figure 116. SS_CTRL3 Register

7	6	5	4	3	2	1	0
\multicolumn{4}{c	}{TM_DSTEP_CTRL}	\multicolumn{4}{c	}{TM_USTEP_CTRL}
\multicolumn{4}{c	}{R/W}	\multicolumn{4}{c	}{R/W}

Table 41. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	Control triangle mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	Control triangle mode spread spectrum rise step in ramp ss manual mode

9.6.1.36 SS_CTRL4 Register (Offset = 6Fh) [reset = 0x24]

SS_CTRL4 is shown in Figure 117 and described in Table 42.

Return to Summary Table.

Figure 117. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RESERVED	\multicolumn{2}{c	}{TM_AMP_CTRL}	\multicolumn{5}{c	}{SS_TM_PERIOD_BOUNDRY}
R/W	\multicolumn{2}{c	}{R/W}	\multicolumn{5}{c	}{R/W}

Table 42. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	Control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	Control triangle mode spread spectrum boundary in ramp ss manual mode

9.6.1.37 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in Figure 118 and described in Table 43.

Return to Summary Table.

Figure 118. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

Table 43. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	Left channel DC fault
2	CH2_DC_1	R	0	Right channel DC fault
1	CH1_OC_I	R	0	Left channel over current fault
0	CH2_OC_I	R	0	Right channel over current fault

9.6.1.38 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in Figure 119 and described in Table 44.

Return to Summary Table.

Figure 119. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR				CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R				R	R	R

Table 44. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0h	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0h	The recent BQ is written failed
5-3	RESERVED	R	0h	This bit is reserved
2	CLK_FAULT_I	R	0h	Clock fault
1	PVDD_OV_I	R	0h	PVDD OV fault
0	PVDD_UV_I	R	0h	PVDD UV fault

9.6.1.39 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in Figure 120 and described in Table 45.

Return to Summary Table.

Figure 120. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		OTSD_I
R					R		R

Table 45. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000	This bit is reserved
0	OTSD_I	R	0	Over temperature shut down fault

9.6.1.40 OT WARNING Register (Offset = 73h) [reset = 0x00]

OT_WARNING is shown in Figure 121 and described in Table 46.

Return to Summary Table.

Figure 121. OT_WARNING Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED			OTW	RESERVED	
R		R		R	R	R	R

Table 46. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	This bit is reserved
5-3	RESERVED	R	000	This bit is reserved
2	OTW	R	0	Over temperature warning ,135C
1-0	RESERVED	R	00	This bit is reserved

9.6.1.41 PIN_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN_CONTROL1 is shown in Figure 122 and described in Table 47.

Return to Summary Table.

Figure 122. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDD_UV	MASK_DVDD_OV	MASK_CLK_FAULT	MASK_PVDD_UV	MASK_PVDD_OV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 47. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	Mask OTSD fault report
6	MASK_DVDD_UV	R/W	0	Mask DVDD UV fault report
5	MASK_DVDD_OV	R/W	0	Mask DVDD OV fault report
4	MASK_CLK_FAULT	R/W	0	Mask clock fault report
3	MASK_PVDD_UV	R/W	0	Mask PVDD UV fault report
2	MASK_PVDD_OV	R/W	0	Mask PVDD OV fault report
1	MASK_DC	R/W	0	Mask DC fault report
0	MASK_OC	R/W	0	Mask OC fault report

9.6.1.42 PIN_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN_CONTROL2 is shown in Figure 123 and described in Table 48.

Return to Summary Table.

Figure 123. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED		CLKFLT_LATCH_EN	OTSD_LATCH_EN	OTW_LATCH_EN	MASK_OTW	RESERVED	
		R/W	R/W	R/W	R/W		

Table 48. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	11	This bit is reserved
5	CLKFLT_LATCH_EN	R/W	1	Enable clock fault latch
4	OTSD_LATCH_EN	R/W	1	Enable OTSD fault latch
3	OTW_LATCH_EN	R/W	1	Enable OT warning latch
2	MASK_OTW	R/W	0	Mask OT warning report
1-0	RESERVED	R/W	00	This bit is reserved

9.6.1.43 MISC_CONTROL Register (Offset = 76h) [reset = 0x00]

MISC_CONTROL is shown in Figure 124 and described in Table 49.

Return to Summary Table.

Figure 124. MISC_CONTROL Register

7	6	5	4	3	2	1	0
DET_STATUS_ LATCH	RESERVED		OTSD_AUTO_ REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

Table 49. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:Latch clock detection status 0:Don't latch clock detection status
6-5	RESERVED	R/W	00	This bit is reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.44 HP_CONTROL Register (Offset = 77h) [reset = 0x00]

HP_CONTROL is shown in Figure 125 and described in Table 50.

Return to Summary Table.

Figure 125. HP_CONTROL Register

7	6	5	4	3	2	1	0
HP_GAIN					HP_MUTEZ	HP_SDZ	HP_FAST_STA RT_UP
R/W					R/W	R/W	R/W

Table 50. HP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	HP_GAIN	R/W	00000	Headphone gain 0: 0dB 1: 1dB ... 24: 24dB 25~31: reserved
2	HP_MUTEZ	R/W	0	0: Mute Headphone 1: Un-mute Headphone
1	HP_SDZ	R/W	0	0: Shutdown Headphone 1: Enable Headphone
0	RESERVED	R/W	0	This bit is reserved

9.6.1.45 FAULT_CLEAR Register (Offset = 78h) [reset = 0x00]

FAULT_CLEAR is shown in Figure 126 and described in Table 51.

Return to Summary Table.

Figure 126. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR	RESERVED						
W	R/W						

Table 51. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT. Once write this bit to 1, device will clear analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

10 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5806MD device into the larger system.

10.1.1 Bootstrap Capacitors

The output stage of the TAS5806MD uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22-µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22-µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22-µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

10.1.2 Inductor Selections

It is required that the peak current is smaller than the OCP (Over current protection) value which is 5A, there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ.

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin(1/\sqrt{L \times C} \times \theta / F_{sw})$$

(1)

> **注**
>
> θ = 0.5 (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation)

表 52. Peak current during power up

PWM Modulation	PVDD	L (uH)	C (uF)	Fsw (kHz)	I_peak_power_up	Comments
BD Modulation (θ=0.5)	24	4.7	0.68	384 (80kHz BW)	6.07A (>5A OCP)	1. Lower Switching Frequency only permits low Class D Loop Bandwidth, which cause worse THD+N. 2. Lower Switching Frequency cause higher startup peak current, which needs Inductor supports higher saturation current. 3. BD Mode has more switching loss than 1SPW mode, so the thermal performance is worse with high PVDD, recommend 1SPW mode for high PVDD case (Typical >16V case). 4. Saturation current of Inductor needs >I_peak_power_up.
	24	10	0.68	384 (80kHz BW)	3A	
	12	4.7	0.68	384 (80kHz BW)	3.32A	
	12	10	0.68	384 (80kHz BW)	1.55A	
	24	4.7	0.68	768 (175kHz BW)	3.25A	
	24	10	0.68	768 (175kHz BW)	1.55A	

Application Information (接下页)

表 52. Peak current during power up (接下页)

PWM Modulation	PVDD	L (uH)	C (uF)	Fsw (kHz)	I$_{peak\_power\_up}$	Comments
1SPW Modulation (θ=0.14)	24	4.7	0.68	384 (80kHz BW)	1.84A	1. 1SPW mode with smaller duty cycle during start up cause smaller I$_{peak\_power\_up}$
	24	10	0.68	384 (80kHz BW)	0.87A	
	12	4.7	0.68	384 (80kHz BW)	0.92A	
	12	10	0.68	384 (80kHz BW)	0.44A	
	12	4.7	0.68	768 (175kHz BW)	0.46A	1. Even with same Inductor value, higher switching frequency cause smaller I$_{peak\_power\_up}$ which means some lower cost inductor with less saturation current is permitted. 2. 768kHz switching frequency,175kHz Loop Bandwidth with 1SPW mode is a good balance for both thermal and audio performance.
	24	4.7	0.68	768 (175kHz BW)	0.93A	
	24	10	0.68	768 (175kHz BW)	0.87A	

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping will cause PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1-\theta)/(F_{sw} \times L)$$

(2)

表 53. Peak current during PVDD clipping with Burst Signal

PWM Modulation	PVDD	L (uH)	Fsw (kHz)	I$_{peak\_clipping}$	Comments
1SPW	24	10	768	2.68A	For high PVDD case, 1SPW mode is a good option to improve thermal performance, but switching frequency can't be too low.
	24	10	576	3.58A	
	24	10	384	5.37A (>5A OCP)	
	12	10	768	1.34A	
	12	4.7	768	2.86A	
BD	24	10	768	1.56	
	24	10	384	3.12	
	12	10	768	0.78	
	12	4.7	768	1.66	

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{spea\,ker\_Load}}$$

(3)

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It's suggested that inductor's saturation current Isat, is larger than the amplifier's peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak\_power\_up}, I_{peak\_clipping}, I_{peak\_output\_power})$$

(4)

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in 表 54 to meet datasheet specifications. The minimum inductance is given in 表 54 .

表 54. LC filter recommendation

PVDD (V)	Switching Frequency (kHz)	Modulation Scheme	Recommended Minimum Inductance (µH) for LC filter design
≤12	384	BD	4.7 µH + 0.68 µF
>12			10 µH + 0.68 µF
≤12	384	1 SPW/Hybrid	10 µH + 0.68 µF
>12			15 µH + 0.68 µF

For higher switching frequency (Fsw), select inductors with minimum inductance to be 384 kHz/F_{sw} × L.

10.1.3 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1-µF or 0.1-µF capacitors as close as possible to the PVDD pins of the device.

10.1.4 Output EMI Filtering

The TAS5806MD device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

10.2 Typical Applications

10.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

图 127 shows the 2.0 (Stereo BTL) system application.
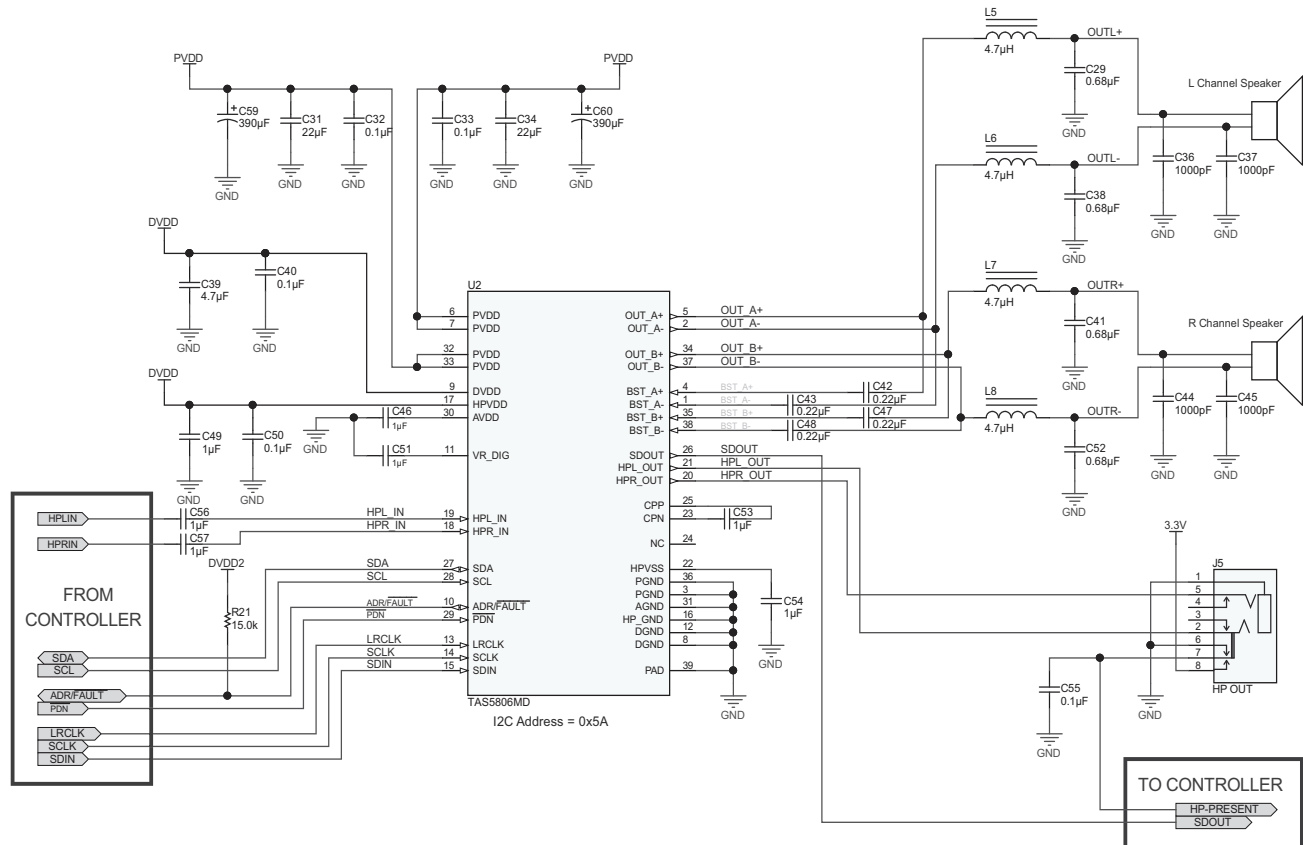
Typical Applications (接下页)

图 127. 2.0 (Stereo BTL) System Application Schematic

10.2.2 Design Requirements

- Power supplies:
  - 3.3-V or 1.8-V supply for DVDD.
  - 3.3V for HPVDD.
  - 4.5-V to 24-V supply for PVDD.
- Communication: host processor serving as I²C compliant master.
- Externa memory (Such as EEPROM or FLASH) used for coefficients.

Typical Applications (接下页)

10.2.3 Detailed Design Procedure

The design procedure can be used for Stereo 2.0, Mono, 2.1 system

10.2.3.1 Step 1: Hardware Integration

• Use the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
• Follow the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  – The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
  – For questions and support, go to the E2E forums (E2E.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

10.2.3.2 Step2: Speaker Tuning

Use the TAS5806MDEVM board and the TAS5806MD tuning software to configure the desired device settings.

10.2.3.3 Software Integration

Use the End System Integration feature of the TAS5806MD tuning software app to generate a baseline configuration file.

Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.

Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.
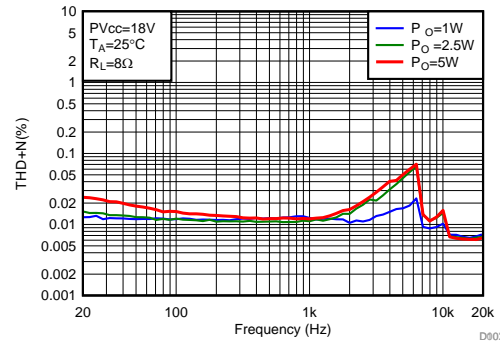
Typical Applications (接下页)

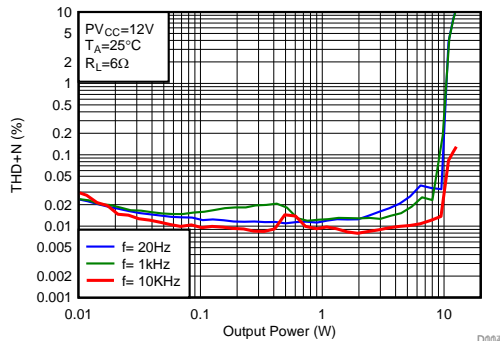### 10.2.4 Application Curves
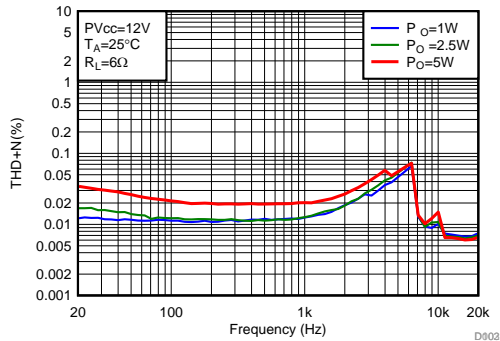
PVDD = 12 V   BTL Load = 6 Ω

Fsw = 768 kHz   LC filter = 4.7 µH + 0.68 µF

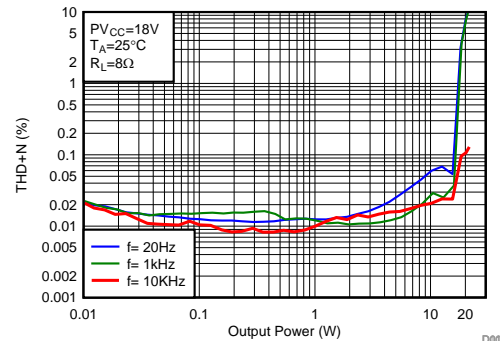**图 128. THD+N vs Frequency (1 SPW Mode, PVDD = 12 V, Load = 6 Ω, BTL Mode)**

PVDD = 18 V   BTL Load = 8 Ω

Fsw = 768 kHz   LC filter = 10 µH + 0.68 µF

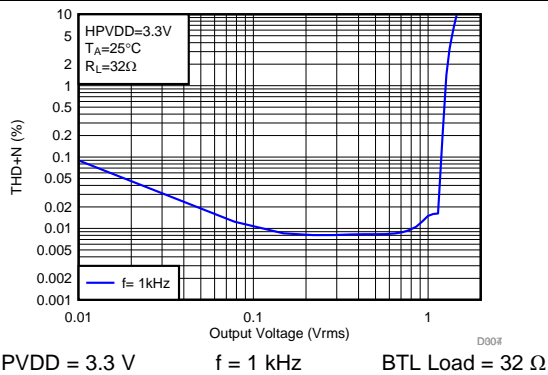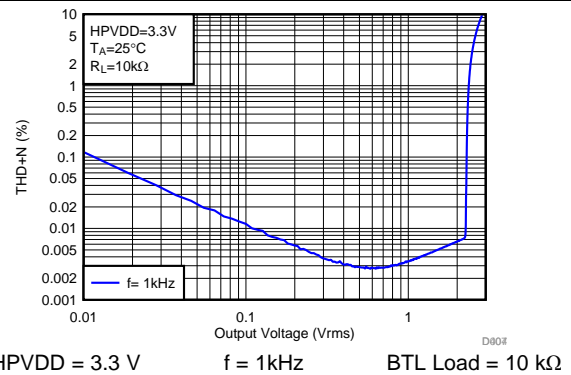**图 129. THD+N vs Frequency (1 SPW Mode, PVDD = 18 V, Load = 8 Ω, BTL Mode)**

PVDD = 12 V   BTL Load = 6 Ω

Fsw = 768 kHz   LC filter = 4.7 µH + 0.68 µF

图 130. THD+N vs Output Power (1SPW Mode, PVDD = 12 V, Load = 6 Ω, BTL Mode)

PVDD = 18 V   BTL Load = 8 Ω

Fsw = 768 kHz   LC filter = 10 µH + 0.68 µF

图 131. THD+N vs Output Power (1 SPW Mode, PVDD = 18 V, Load = 8 Ω, BTL Mode)

HPVDD = 3.3 V   f = 1 kHz   BTL Load = 32 Ω

图 132. THD+N vs Output Voltage (Headphone load = 32 Ω)

HPVDD = 3.3 V   f = 1kHz   BTL Load = 10 kΩ

图 133. THD+N vs Output Voltage (Line driver load = 10 kΩ)

Typical Applications (接下页)

10.2.5 Mono (PBTL) system

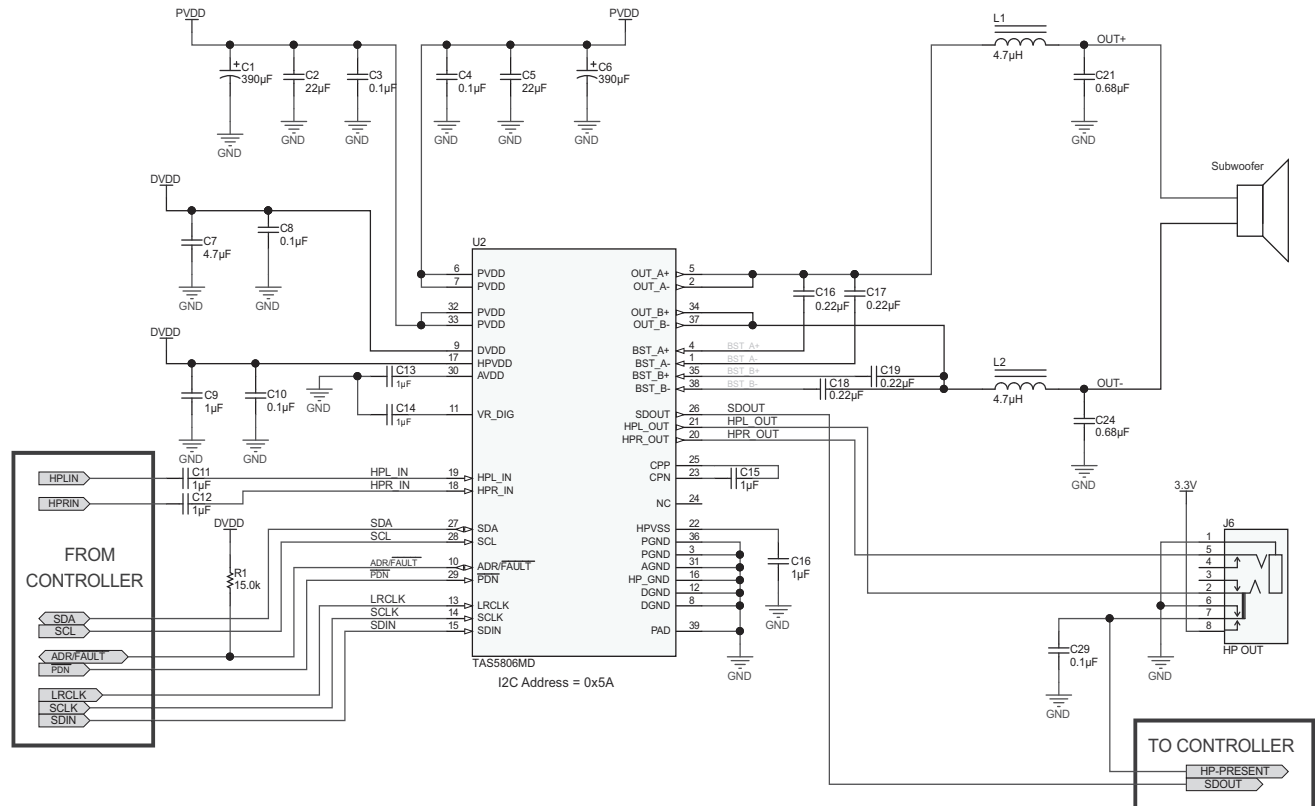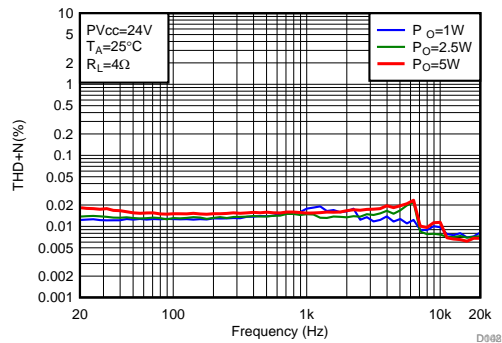In MONO application, TAS5806MD can be used as PBTL mode to drive sub-woofer with more output power.

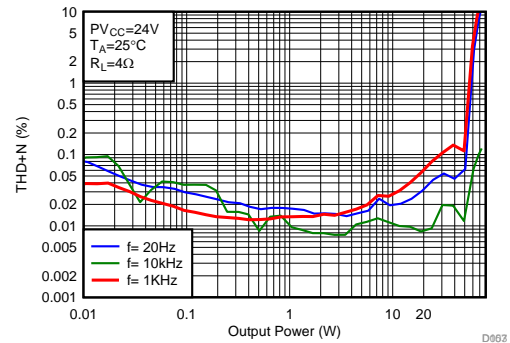图 134. **Mono (PBTL) System Application Schematic**

Typical Applications (接下页)

10.2.6 Application Curves

PVDD = 24 V	1 SPW Mode	PBTL Load = 4 Ω
Fsw = 576 kHz	LC filter = 4.7 µH + 0.68 µF	

图 135. **THD+N vs Frequency**

|		
PVDD = 24 V	1 SPW Mode	PBTL Load = 4 Ω
Fsw = 576 kHz	LC filter = 4.7 µH + 0.68 µF	

图 136. **THD+N vs Output Power**

11 Power Supply Recommendations

The TAS5806MD device requires three power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. One low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. Another low-voltage power supply which is calls HPVDD for headphone driver. The allowable voltage range for both PVDD, DVDD and HPVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required power-up sequence. The power supplies can be powered on in any order. But once the device has been initialized, PVDD must keep within the normal operation voltage. Once PVDD lower than 3.5V, all registers need re-initialize again.
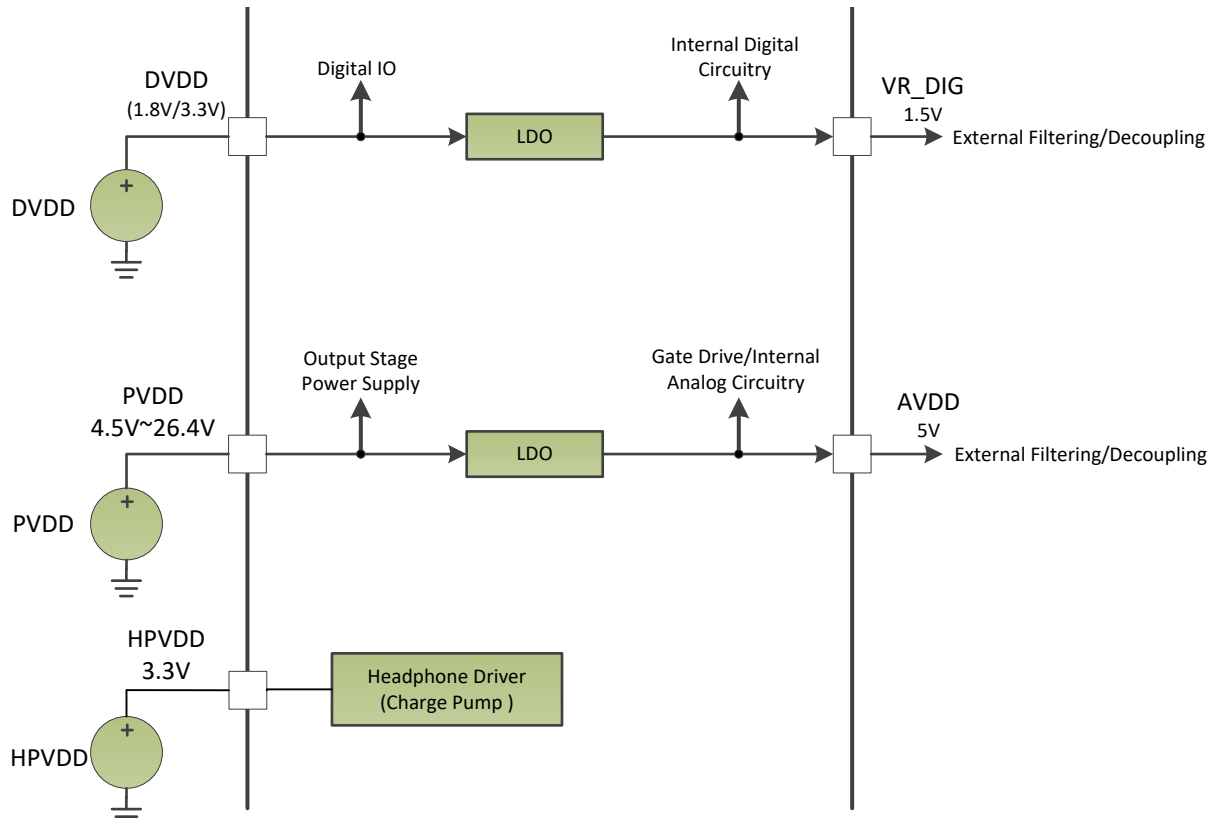
Copyright © 2018, Texas Instruments Incorporated

图 137. **Power Supply Function Block Diagram**

11.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in 图 137, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Application and Implementation* section and the *Layout Example* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5806MD device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the VR_DIG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuity. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

11.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5806MD MEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5806MD device *Application and Implementation*. Lack of proper decoupling, like that shown in the *Application and Implementation*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5806MD internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

12 Layout

12.1 Layout Guidelines

12.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the *Layout Example* section. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Example* section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

12.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD and PVDD. However, the capacitors on the PVDD net for the TAS5806MD device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5806MD device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the deice . For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

12.1.3 Optimizing Thermal Performance

Follow the layout example shown in the 图 138 to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

12.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5806MD device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5806MD device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5806MD device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5806MD device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane

Layout Guidelines (接下页)

from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

12.1.3.2 Stencil Pattern

The recommended drawings for the TAS5806MD device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

12.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5806MD device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5806MD device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5806MD device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Layout Example* section, this interface can benefit from improved thermal performance.

注

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias are as follows:
- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drull must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Example* section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5806MD device to open up the current path to and from the device.

12.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to

Layout Guidelines (接下页)

manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

12.2 Layout Example
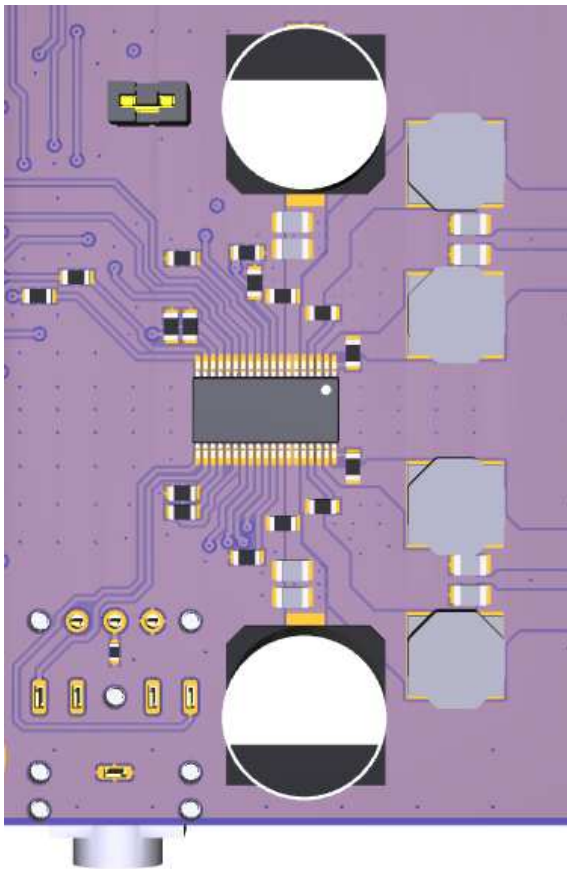
Top Layer 3D layout
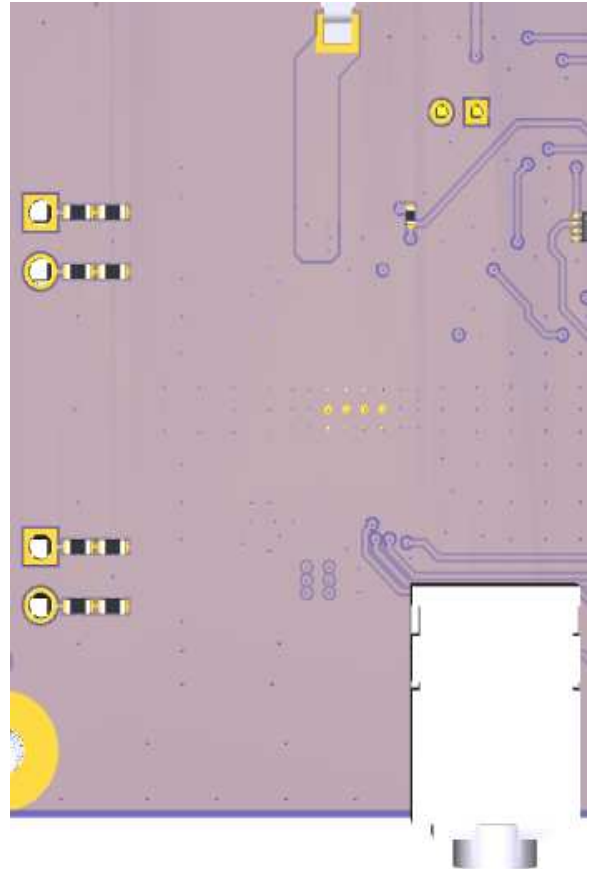
Bot Layer 3D layout

图 138. 2.0 (Stereo BTL) 3-D View

13 器件和文档支持

13.1 器件支持

13.1.1 器件命名规则

Glossary 部分列出的是一个通用的术语表，其中包括常用的缩写和词语，它们都是根据一个范围广泛的 TI 计划定义的，符合 JEDEC、IPC、IEEE 等行业标准。本部分提供的术语表定义了特定于本产品和文档、附属产品或本产品使用的支持工具和软件的词语和缩写。如对定义和术语有其他疑问，请访问 e2e 音频放大器论坛。

桥接式负载 (BTL) 是一种输出配置，其中扬声器的两端分别连接一个半桥。

DUT 是指*被测器件*，用于区分不同的器件。

闭环架构是一种拓扑结构，其中放大器监视输出端子、对比输出信号与输入信号，并尝试修正输出信号的非线性。

动态控件是指系统或最终用户在正常使用时可更改的控件。

GPIO 是通用输入/输出引脚。该引脚是一个高度可配置的双向数字引脚，可执行系统所需的多种功能。

主机处理器（也称系统处理器、标量、主机或系统控制器）是指用作中央系统控制器的器件，可为与其连接的器件提供控制信息，还可以从上游器件采集音频源数据并将其分配给其他器件。该器件通常配置音频路径中音频处理器件（如 TAS5806MD）的控件，从而根据频率响应、时间校准、目标声压级、系统安全工作区域和用户偏好优化扬声器的音频输出。

最大持续输出功率是指放大器在 25°C 运行环境温度下可持续（不关断）提供的最大输出功率。测试该参数时，要求温度达到热平衡点且不再升高

并联桥接式负载 (PBTL) 是一种输出配置，其中扬声器的两端分别连接一对并行放置的半桥

r$_{DS(on)}$ 是指放大器输出级中所用 MOSFET 的导通电阻。

静态控件/静态配置是指系统正常使用时不发生变化的控件。

过孔是指 PCB 中的镀铜通孔。

13.1.2 开发支持

有关 RDGUI 软件，请咨询当地的现场支持工程师。

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.

13.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.6 **Glossary**

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5806MDDCPR	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5806MD
TAS5806MDDCPR.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5806MD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
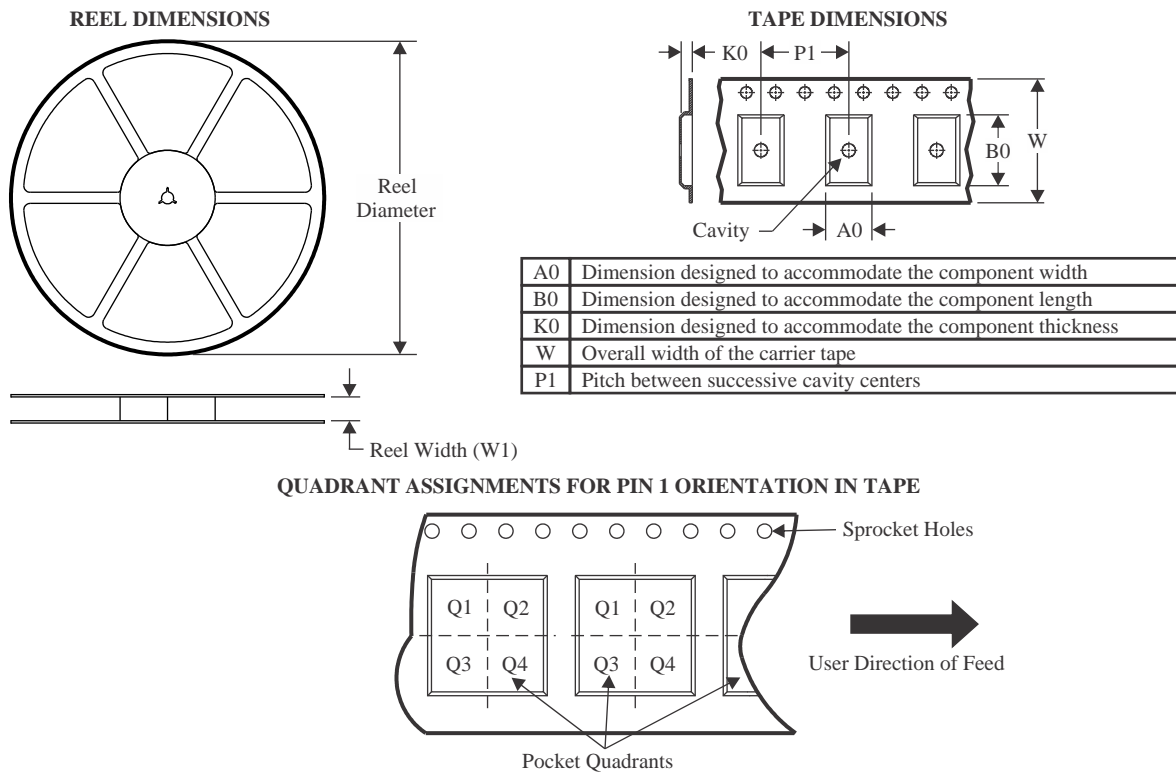
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5806MDDCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
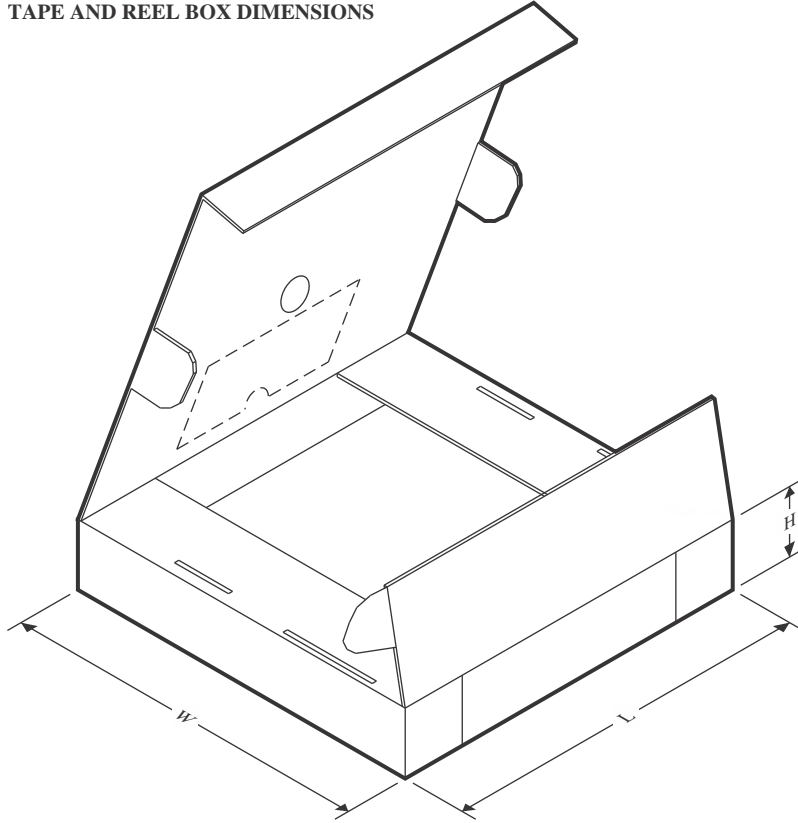
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5806MDDCPR	HTSSOP	DCP	38	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224560/B

6.6
6.2 TYP

A

PIN 1 INDEX
AREA

1

38

36X 0.5

9.8
9.6
NOTE 3

2X
9

19

20

B

4.5
4.3

38X 0.27
0.17

⊕ 0.08 Ⓜ C A B

C

◠ 0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

2X 0.95 MAX
NOTE 5

19

20

2X 0.95 MAX
NOTE 5

4.70
3.94

39

THERMAL
PAD

1

38

2.90
2.43

0.25

GAGE PLANE

0°-8°

0.75
0.50

1.2 MAX

0.15
0.05

DETAIL A
TYPICAL
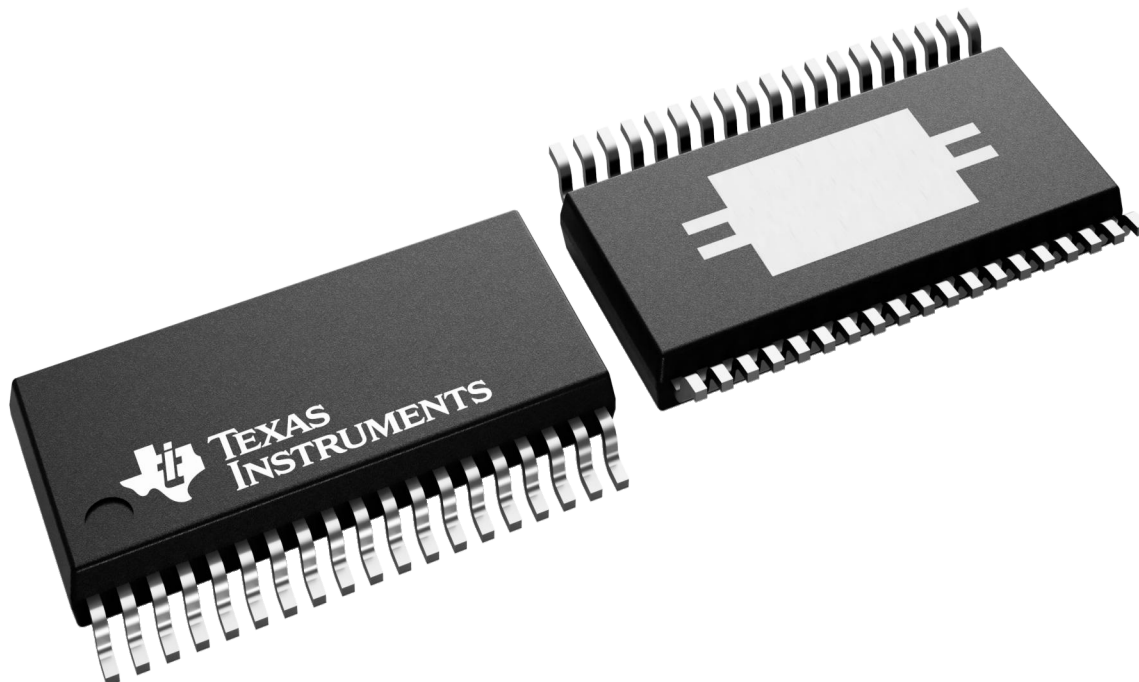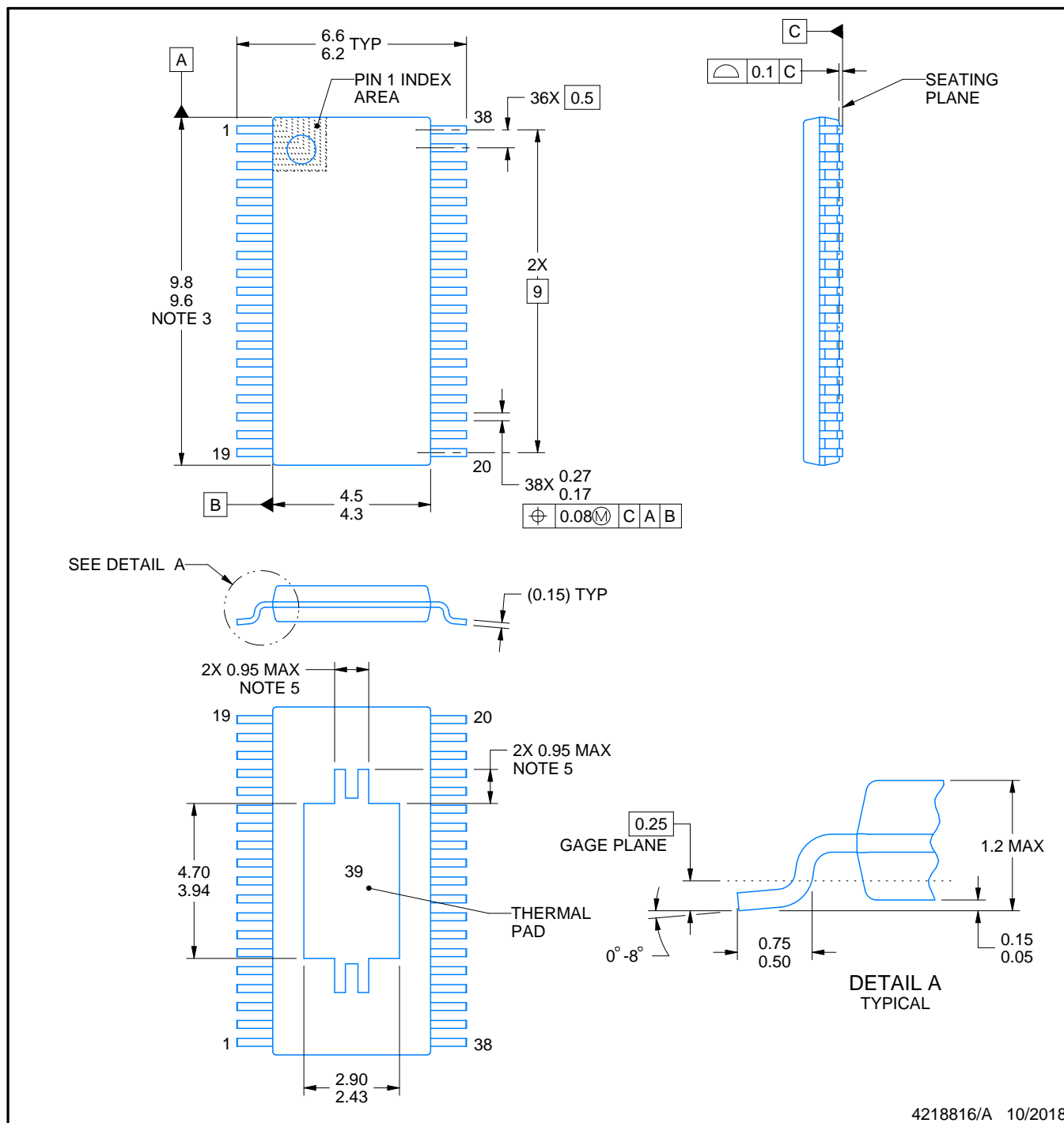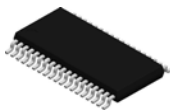
4218816/A   10/2018

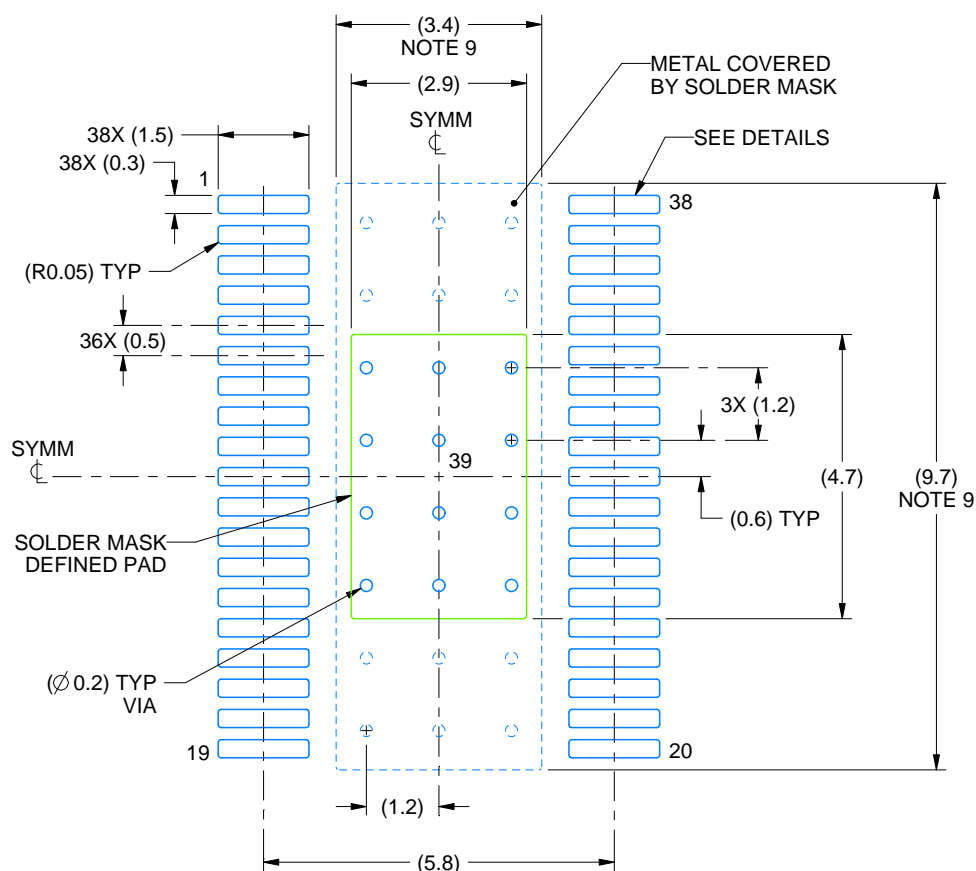PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
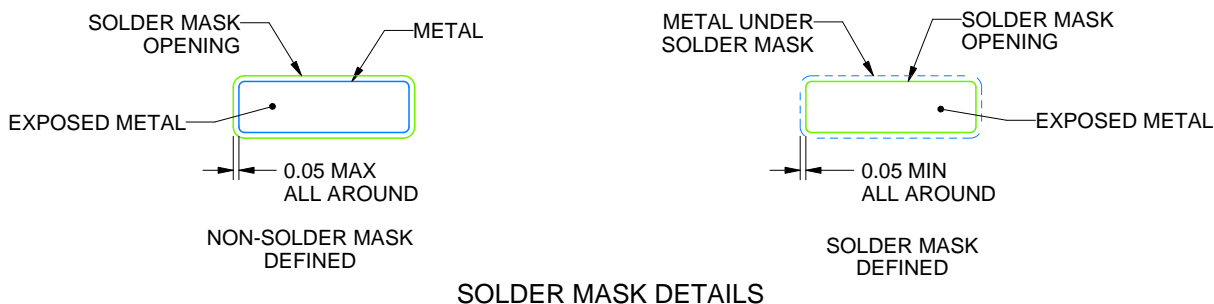5. Features may differ or may not be present.

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LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK DETAILS

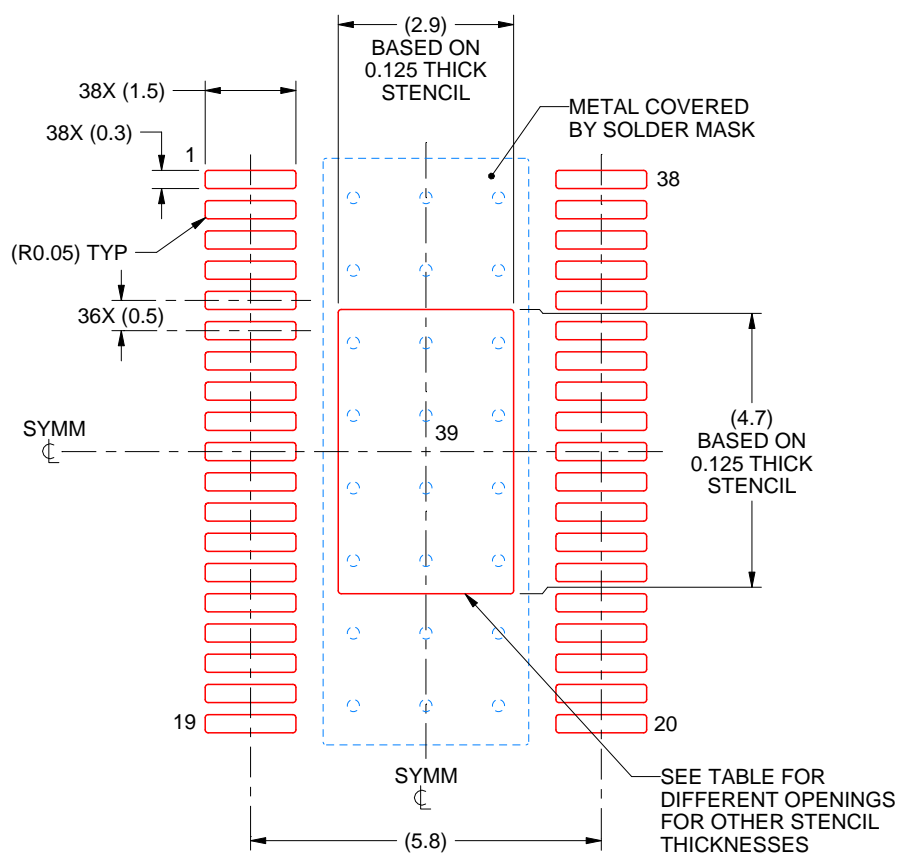4218816/A   10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

38X (1.5)

38X (0.3)

1

(R0.05) TYP

36X (0.5)

SYMM

(2.9)
BASED ON
0.125 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

38

39

(4.7)
BASED ON
0.125 THICK
STENCIL

19

20

SYMM

(5.8)

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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