TAS2560 具有 IV 感测功能的 5.6W D 类单声道音频放大器

1 特性

- 超低噪声单声道升压 D 类放大器
  - 在 4Ω 负载和 4.2V 电源电压条件下，总谐波失真 + 噪声 (THD+N) 为 1% 时的功率为 5.6W，THD+N 为 10% 时的功率为 6.9W
  - 在 8Ω 负载和 4.2V 电源电压条件下，THD+N 为 1% 时的功率为 3.7W，THD+N 为 10% 时的功率为 4.5W
- 数模转换器 (DAC) + D 类放大器的输出噪声 (ICN) 为 16.2μV
- 1% THD+N/8Ω 条件下的 DAC + D 类放大器的信噪比 (SNR) 为 111dB
- 1W/8Ω 条件下的 THD+N 为 –89dB（具有平坦频率响应）
- 后置滤波器反馈 (PFFB)
- 当频率为 217Hz 时，200 mVpp 纹波电压的电源抑制比 (PSRR) 为 110dB
- 输入采样速率范围为 8kHz 至 96kHz
- 高效 H 类升压转换器
  - 自动调节 D 类电源
  - 多级跟踪，可提升效率
- 内置扬声器感测
  - 测量扬声器电流和电压
  - 测量 VBAT 电压和芯片温度
- 内置自动增益控制 (AGC)
  - 限制电池电流消耗
- 可调节 D 类开关边缘速率控制
- 电源
  - 升压输入：2.9V 至 5.5V
  - 模拟/数字：1.65V 至 1.95V
  - 数字 I/O：1.62V 至 3.6V
- 热保护、短路保护和欠压保护
- I2S，左侧对齐，右侧对齐，数字信号处理器 (DSP)，时分复用 (TDM) 和脉宽调制 (PDM)
- 用于寄存器控制的 I2C 接口
- 可使用两个 TAS2560 器件实现立体声配置

2 应用

- 手机
- 平板电脑
- 个人电子产品
- 建筑/家庭自动化
- 蓝牙扬声器及配件

3 说明

TAS2560 是一款低功耗、高性能、数字输入升压 D 类音频放大器，可轻松实现单声道和立体声 (x2) 应用。该器件 具有 超低噪声音频 DAC 和 D 类功率放大器，其中整合的扬声器电压和电流感测反馈用于扬声器保护算法。

H 类升压转换器生成 D 类放大器电源轨。当音频信号只需要较低的 D 类输出功率时，可通过禁用升压并将 VBAT 直连 D 类放大器电源来提升系统效率。当需要较高的音频输出功率时，多级升压功能会重新激活信号跟踪，从而为负载提供额外的电压。

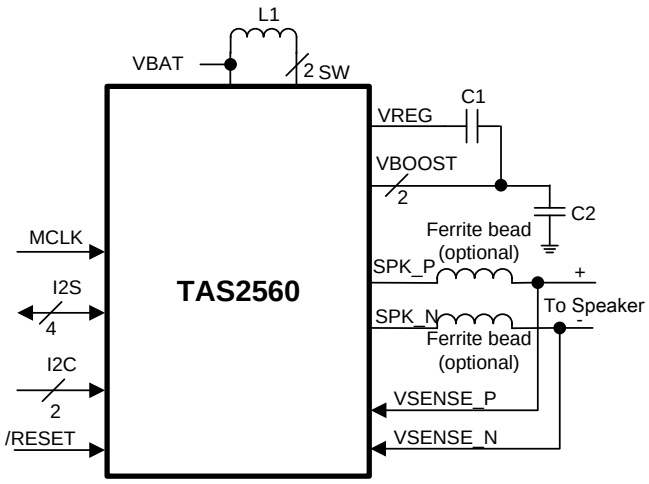
可配置的片上电池保护系统可降低电池电压过低期间的音频输出功率，从而尽量防止电池电压下降到系统欠压条件以下。此外，欠压、过流和过热等故障可使用 IRQ 引脚报告回主机处理器。通过读取寄存器可获得所有保护状态。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TAS2560	WCSP (30)	2.85mm x 2.63mm

(1) 如需了解所有可用封装，请参见产品说明书末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (November 2017) to Revision E — **Page**

- Changed MAX Switching value in the *Absolute Maximum Ratings* table to 1.8 5
- Changed *Absolute Maximum Ratings* table note 5
- 已更改 MIN value of C1 to 10 70
- 已更改 Capacitance at 8.5 V derating specification of C2 to 3.3 70
- 已添加 missing text to end of *Boost Converter Passive Devices* section 70

Changes from Revision C (July 2017) to Revision D — **Page**

- Changed the *Boost Converter Passive Devices* section 70

Changes from Revision B (August 2016) to Revision C — **Page**

- 已更改 将封装尺寸从“2.80mm × 2.60mm”改为“2.85mm × 2.63mm” 1

Changes from Revision A (June 2016) to Revision B — **Page**

- 已更改 封装图。 74

Changes from Original (June 2016) to Revision A — **Page**

- 已更改 “产品预览”至“量产数据” 1

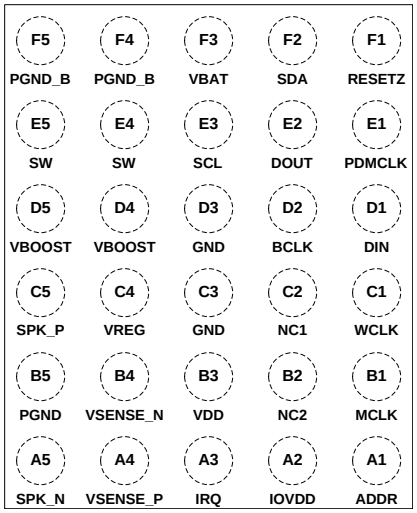
5 Device Comparison Table

PART NUMBER	CONTROL METHOD	Boost Voltage	SNR(1)	ICN(1)	THD+N	Boost Control	SmartAmp Digital Engine
TAS2552	I^2C	8.5 V	94 dB	130 µV	-64 dB	Class-G	NO (External Processing Required)
TAS2553	I^2C	7.5 V	94 dB	130 µV	-64 dB	Class-G	NO (External Processing Required)
TAS2555	I^2C or SPI	8.5 V	111 dB	15.9 µV	-90 dB	Class-H	YES (Processing on Chip)
TAS2560	I^2C	8.5 V	111 dB	16.2 µV	-88 dB	Class-H	NO (External Processing Required)

(1) A weighted data.

6 Pin Configuration and Functions

30-Ball WCSP
YFF Package
(Top View)



Pin Functions

PIN		I/O/POWER	DESCRIPTION
NAME	BALL NO.		
ADDR	A1	I	I^2C device ID setting
IOVDD	A2	P	1.8V or 3.3V Digital interface Power Supply for digital input and output levels
IRQ	A3	O	Active-high interrupt output
VSENSE_P	A4	I	Non-inverting voltage sense input
SPK_N	A5	O	Non-inverting Class D output
MCLK	B1	I	Master clock input
NC2	B2	-	Float Connection - Do not route any signal or supply to or through this pin
VDD	B3	P	1.8V power supply
VSENSE_N	B4	I	Inverting voltage sense input
PGND	B5	P	Power ground, connect to high current ground plane
WCLK	C1	I/O	Audio serial interface word clock
NC1	C2	-	Float Connection - Do not route any signal or supply to or through this pin
GND	C3,D3	P	Power ground, connect to high current ground plane
VREG	C4	P	Voltage regulator output
SPK_P	C5	O	Inverting Class D output
DIN	D1	I	Audio serial interface data input
BCLK	D2	I/O	Audio serial interface bit clock
VBOOST	D4,D5	P	Boost converter output
PDMCLK	E1	I/O	PDM bit stream clock
DOUT	E2	O	Audio serial interface data output
SCL	E3	I	I^2C interface serial clock
SW	E4,E5	P	Boost converter switch input
RESETZ	F1	I	Active-low hardware reset
SDA	F2	I/O	I^2C interface serial data
VBAT	F3	P	Battery power supply, connect to 2.9 V to 5.5 V battery supply
PGND_B	F4,F5	P	Power ground, connect to high current ground plane

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Battery voltage	VBAT	–0.3	6	V
Analog supply voltage	VDD	–0.3	2	V
I/O supply voltage	IOVDD	–0.3	3.9	V
Boost	VBST	–0.3	9.2	V
Switching	SW	–0.7	VBST + 1.8 (1)	V
Regulator voltage	VREG	–0.3	VBST + 5	V
Digital input voltage		–0.3	IOVDD + 0.3	V
Output continuous total power dissipation		See *Thermal Information*		
Storage temperature, T_{stg}		–65	150	°C

(1) Cannot exceed 11 V for greater than 10 nS or 10 V continuously.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Battery voltage	VBAT	2.9 (1)	3.6	5.5	V
	Analog supply voltage	VDD	1.65	1.8	1.95	V
	I/O supply voltage 1.8V	IOVDD	1.62	1.8	1.98	V
	I/O supply voltage 3.3V	IOVDD	3	3.3	3.6	V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		150	°C

(1) Device is functional down to 2.7 V. See *Battery Guard AGC*

7.4 Thermal Information

THERMAL METRIC (1)		TAS2560 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	8.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{BAT} = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, Gain = 16.4 dB, ERC = 14 ns, Boost Inductor = 2.2 µH, R_L = 8 Ω + 33 µH, 1-kHz input frequency, 48-kHz sample rate for digital input, Class-H Boost Enabled, T_A= 25°C, ILIM = 3 A (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER					
Boost output voltage	Average voltage (w/o including ripple).		8.5		V
Boost converter switching frequency			1.77		MHz
Boost converter current limit			3		A
Boost converter max in-rush current	High Efficiency Mode: Max inductor in-rush and startup current after enable		4		A
	Normal Efficiency Mode: Max inductor in-rush and startup current after enable		1.5		
CLASS-D CHANNEL					
Output voltage for full-scale digital input			6.67		V_{RMS}
Load resistance (Load spec resistance)		3.6	8		Ω
Class-D frequency	Avg frequency in spread-spectrum mode		384		kHz
	Fixed Frequency	44.1 × 8	48 × 8		
Class-D + boost efficiency	P_{OUT} = 3.5 W (sinewave) ROM Mode 1		81%		
	P_{OUT} = 0.44 W (sinewave) ROM Mode 1		87%		
Class-D output current limit (Short circuit protection)	VBOOST = 8.5 V, OUT– shorted to VBAT, VBOOST, GND		4		A
Class-D output offset voltage in digital input mode		–2.5		2.5	mV
Programmable channel gain accuracy			±0.5		dB
Mute attenuation	Device in shutdown or device in normal operation and MUTED		146		dB
VBAT Power Supply Rejection Ratio (PSRR)	Ripple of 200 mVpp at 217 Hz		110		dB
AVDD Power Supply Rejection Ratio (PSRR)	Ripple of 200 mVpp at 217 Hz		98		dB
THD+N	1 kHz, P_{OUT} = 0.1 W		0.0085 %		
	1 kHz, Po = 0.5 W		0.0046 %		
	1 kHz, Po = 1 W		0.0035 %		
	1 kHz, Po = 3 W		0.0043 %		
Output integrated noise (20 Hz to 20 kHz) - 8 Ω	A-wt Filter, DAC modulator switching		16.2		µV
Signal-to-noise ratio	Referenced to 1% THD+N at output, a-weighted		110.6		dB
Max output power, 3-A current limit	THD+N = 1%, 8-Ω Load		3.7		W
	THD+N = 1%, 6-Ω Load		4.5		
	THD+N = 1%, 4-Ω Load		5		
Startup pop	Digital input, a-weighted output		5		mV
Output impedance in shutdown	RESETZ = 0 V		10.4		kΩ
Startup time	Time taken from end of configuring device to speaker output signal in I^2C mode with 48ksps input		8		mS
Shutdown time	Measured from time when device is programmed in software shutdown mode		100		µS

Electrical Characteristics (continued)

V_{BAT} = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, Gain = 16.4 dB, ERC = 14 ns, Boost Inductor = 2.2 µH, R_L = 8 Ω + 33 µH, 1-kHz input frequency, 48-kHz sample rate for digital input, Class-H Boost Enabled, T_A= 25°C, ILIM = 3 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
	Current sense full scale	Peak current which will give full scale digital output 8-Ω load		1.25		A_{PEAK}
		Peak current which will give full scale digital output 8-Ω load PDM		4.022		
		Peak current which will give full scale digital output 6-Ω load		1.5		
		Peak current which will give full scale digital output 4-Ω load		1.75		
	Current sense accuracy	I_{OUT} = 354 mA_{RMS} (1 W)		1.7%		
	Current sense gain drift over temperature	–40°C to 85°C		4%		
	Current sense gain linearity	From 15 mW to 3.5 W for fin=1 kHz		1.5%		
THD+N	Distortion + Noise	P_{OUT} = 3 W (Load = 8 Ω + 33 µH)		0.196%		
		P_{OUT} = 3 W (Load = 4 Ω + 33 µH)		0.132%		
	SNR	20 Hz to 20 kHz, A-wt		–68		db
VOLTAGE SENSE						
	Voltage sense full scale	Peak voltage which will give full scale digital output(1)		9.353		V_{PEAK}
		Peak voltage which will give full scale digital output in PDM		16.65		
	Voltage sense accuracy	V_{OUT} = 2.83 Vrms (1 W)		1%		
	Voltage sense gain drift over temperature	–40°C to 85°C		1.2%		
	Voltage sense gain linearity	From 15 mW to 3.5 W for fin = 1 kHz		1%		
INTERFACE						
	Voltage and current sense data rate	TDM/I^2S		48		kHz
	Voltage and current sense ADC OSR	TDM/I^2S		64		OSR
F_{MCLK}	MCLK frequency		0.512		49.15	MHz
POWER CONSUMPTION						
	Power consumption with digital input and IV-sense disabled. Idle channel condition	From VBAT, no signal		3.2		mA
		From VDD, no signal		9.5		mA
	Power consumption with digital input and IV-sense enabled.	From VBAT, no signal		3.2		mA
		From VDD, no signal		10.6		mA
	Power consumption in hardware shutdown	From VBAT, RESETZ = 0		0.1		µA
		From VDD, RESETZ = 0		1.2		µA
	Power consumption in software shutdown. See *Low Power Sleep*	From VBAT		0.1		µA
		From VDD		9.8		µA
DIGITAL INPUT / OUTPUT						
V_{IH}	High-level digital input voltage	All digital pins except SDA and SCL, IOVDD = 1.8-V operation	0.65 × IOVDD			V
V_{IL}	Low-level digital input voltage				0.35 × IOVDD	V
V_{IH}	High-level digital input voltage	All digital pins except SDA and SCL, IOVDD = 3.3-V operation	2			V
V_{IL}	Low-level digital input voltage				0.45	V

(1) Voltage Sense Fullscale = 1.176 Vrms × $10^{(DAC\_GAIN/20)}$

Electrical Characteristics (continued)

V_{BAT} = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, Gain = 16.4 dB, ERC = 14 ns, Boost Inductor = 2.2 µH, R_L = 8 Ω + 33 µH, 1-kHz input frequency, 48-kHz sample rate for digital input, Class-H Boost Enabled, T_A= 25°C, ILIM = 3 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level digital output voltage	All digital pins except SDA and SCL, IOVDD = 1.8-V operation For I_{OL} = 2 mA and I_{OH} = –2 mA	IOVDD – 0.45			V
V_{OL}	Low-level digital output voltage				0.45	V
V_{OH}	High-level digital output voltage	All digital pins except SDA and SCL, IOVDD = 3.3-V operation For I_{OL} = 2 mA and I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level digital output voltage				0.4	V
I_{IH}	High-level digital input leakage current	Input = IOVDD	–5	0.1	5	µA
I_{IL}	Low-level digital input leakage current	Input = Ground	–5	0.1	5	µA
MISCELLANEOUS						
T_{TRIP}	Thermal Trip Point			135		°C

7.6 I²C Timing Requirements

For I²C interface signals over recommended operating conditions (unless otherwise noted).(1)

PARAMETER		TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4			0.6			µs
t_{LOW}	LOW period of the SCL clock		4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock		4			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			0.6			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices		0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
t_r	SDA and SCL Rise Time				1000	20 + 0.1 × Cb		300	ns
t_f	SDA and SCL Fall Time				300	20 + 0.1 × Cb		300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4			0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			1.3			µs
C_b	Capacitive load for each bus line				400			400	pF

(1) All timing specifications are specified by design but not tested at final test.

7.7 I²S/LJF/RJF Timing in Master Mode

All specifications at T_A = –40°C to 85°C, IOVDD data sheet limits, V_{IL} and V_{IH} applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted.(1)

SYMBOL	PARAMETER	CONDITIONS	IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_d(WS)	BCLK to WCLK delay	50% of BCLK to 50% of WCLK		35		25	ns
t_d(DO-WS)	WCLK to DOUT delay (For LJF Mode only)	50% of WCLK to 50% of DOUT		35		25	ns
t_d(DO-BCLK)	BCLK to DOUT delay	50% of BCLK to 50% of DOUT		35		25	ns
t_s(DI)	DIN setup		8		8		ns
t_h(DI)	DIN hold		8		8		ns
t_r	Rise time	10%-90% Rise Time		8		4	ns
t_f	Fall time	90%-10% Fall Time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

7.8 I²S/LJF/RJF Timing in Slave Mode

All specifications at T_A = –40°C to 85°C, IOVDD data sheet limits, V_{IL} and V_{IH} applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted.(1)

SYMBOL	PARAMETER	CONDITIONS	IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period		40		30		ns
t_L(BCLK)	BCLK low period		40		30		ns
t_s(WS)	(WS)		8		8		ns
t_h(WS)	WCLK hold		8		8		ns
t_d(DO-WS)	WCLK to DOUT delay (For LJF Mode only)	50% of WCLK to 50% of DOUT		35		25	ns
t_d(DO-BCLK)	BCLK to DOUT delay	50% of BCLK to 50% of DOUT		35		25	ns
t_s(DI)	DIN setup		8		8		ns
t_h(DI)	DIN hold		8		8		ns
t_r	Rise time	10%-90% Rise Time		8		4	ns
t_f	Fall time	90%-10% Fall Time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

7.9 DSP Timing in Master Mode

All specifications at T_A = –40°C to 85°C, IOVDD data sheet limits, V_{IL} and V$_I$H applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted.(1)

SYMBOL	PARAMETER	CONDITIONS	IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_d(WS)	BCLK to WCLK delay	50% of BCLK to 50% of WCLK		35		25	ns
t_d(DO-BCLK)	BCLK to DOUT delay	50% of BLCK to 50% of DOUT		35		25	ns
t_s(DI)	DIN setup		8		8		ns
t_h(DI)	DIN hold		8		8		ns
t_r	Rise time	10%-90% Rise Time		8		4	ns
t_f	Fall time	90%-10% Fall Time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

7.10 DSP Timing in Slave Mode

All specifications at T_A = –40°C to 85°C, IOVDD data sheet limits, V_{IL} and V_IH applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted.(1)

SYMBOL	PARAMETER	CONDITIONS	IOVDD=1.8V		IOVDD=3.3V		UNIT
			MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period		40		30		ns
t_L(BCLK)	BCLK low period		40		30		ns
t_s(WS)	WCLK seutp		8		8		ns
t_h(WS)	WCLK hold		8		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay (For LJF Mode only)	50% BCLK to 50% DOUT		35		25	ns
t_s(DI)	DIN setup		8		8		ns
t_h(DI)	DIN hold		8		8		ns
t_r	Rise time	10%-90% Rise Time		8		4	ns
t_f	Fall time	90%-10% Fall Time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

7.11 PDM Timing

All specifications at T_A = –40°C to 85°C, IOVDD data sheet limits, V_{IL} and V_IH applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted.(1)

PARAMETER		CONDITIONS	IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_s	DIN setup		20		20		ns
t_h	DIN hold		3		3		ns
t_r	Rise time	10%-90% Rise Time		8		4	ns
t_f	Fall time	90%-10% Fall Time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

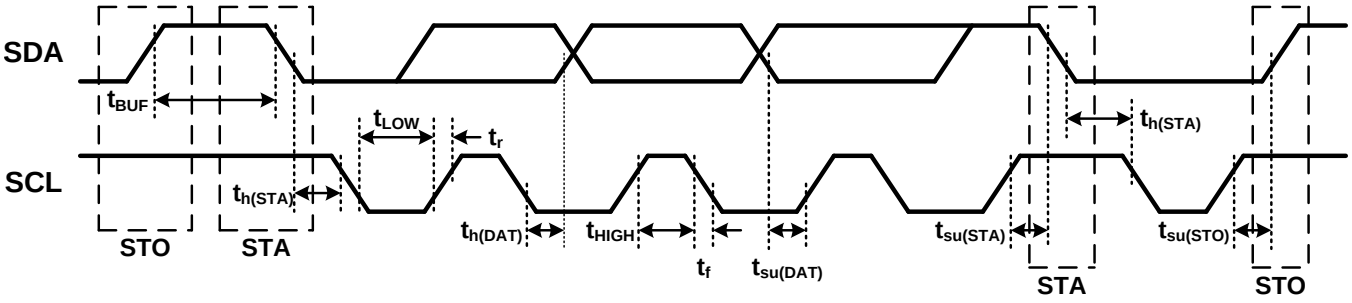


图 1. I²C Timing

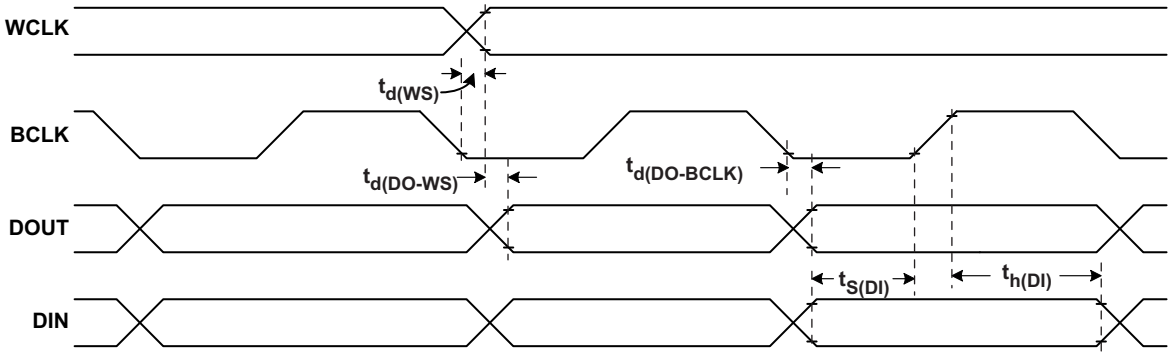


图 2. I²S/LJF/RJF Timing in Master Mode

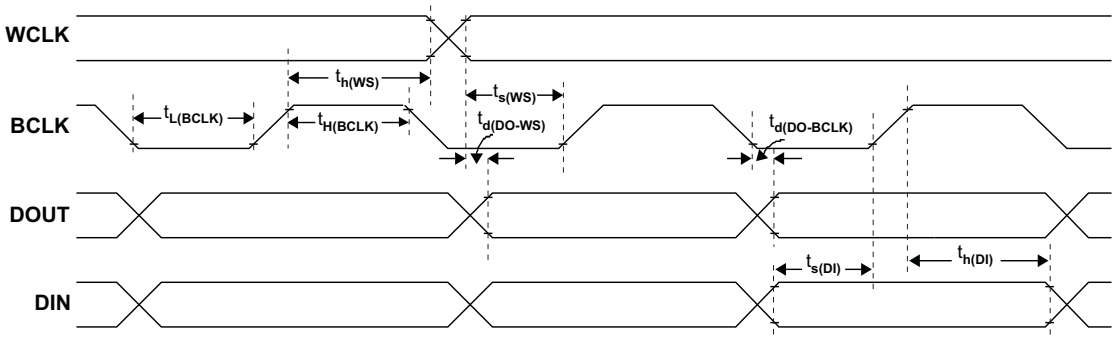


图 3. I²S/LJF/RJF Timing in Slave Mode

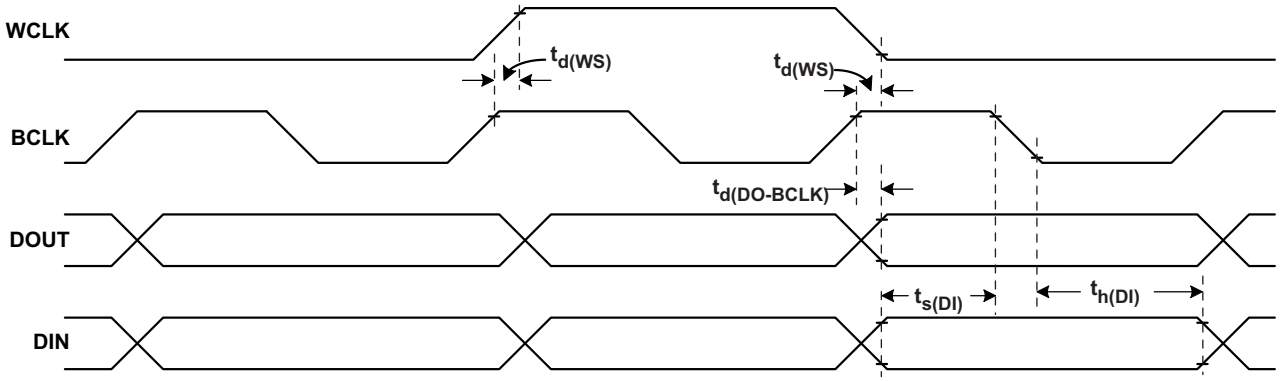


图 4. DSP Timing in Master Mode

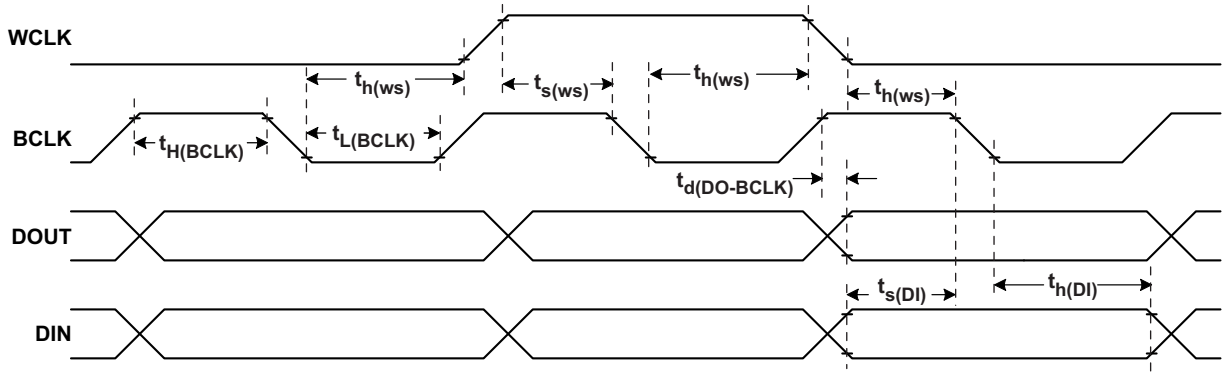


图 5. DSP Timing in Slave Mode

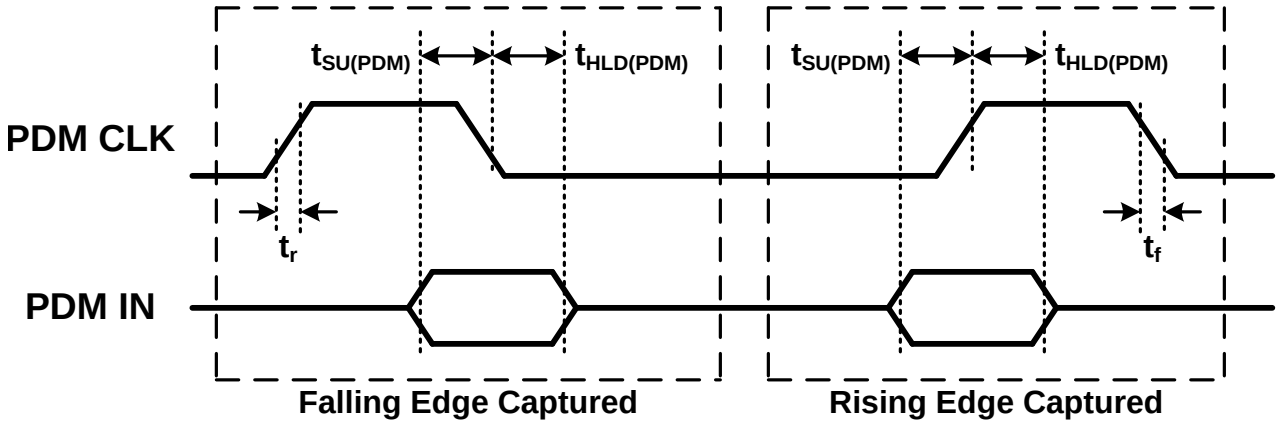
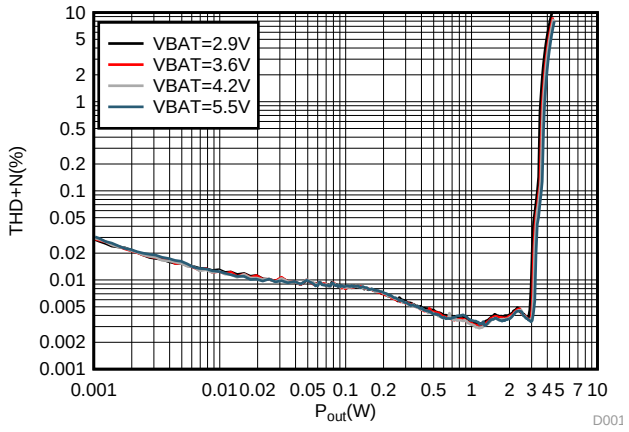


图 6. PDM Timing

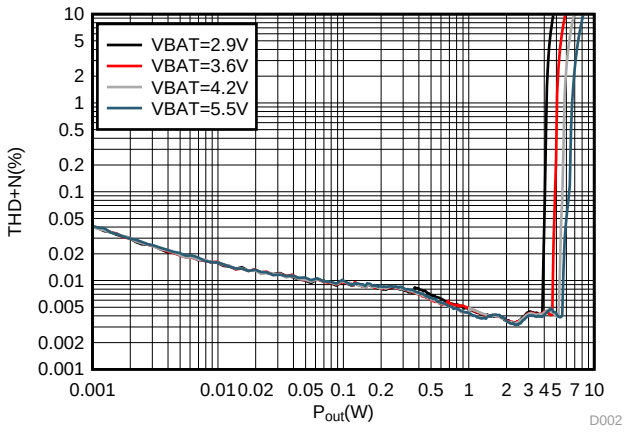
7.12 Typical Characteristics

VBAT = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, R_L = 8 Ω + 33 µH, I^2S digital input, Mode 2 (unless otherwise noted).



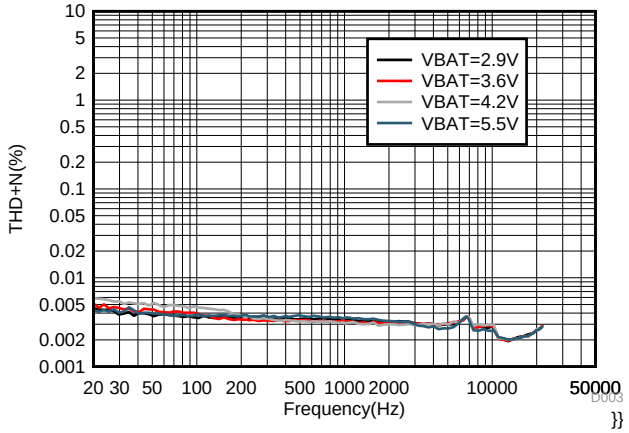
8 Ω + 33 µH Freq = 1 kHz

图 7. THD+N vs Output Power



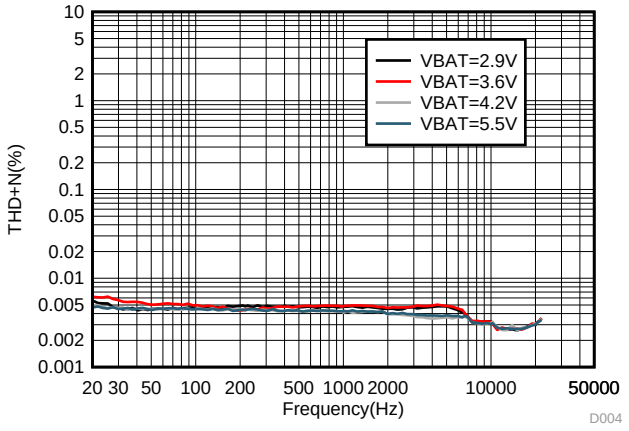
4 Ω + 16 µH Freq = 1 kHz

图 8. THD+N vs Output Power



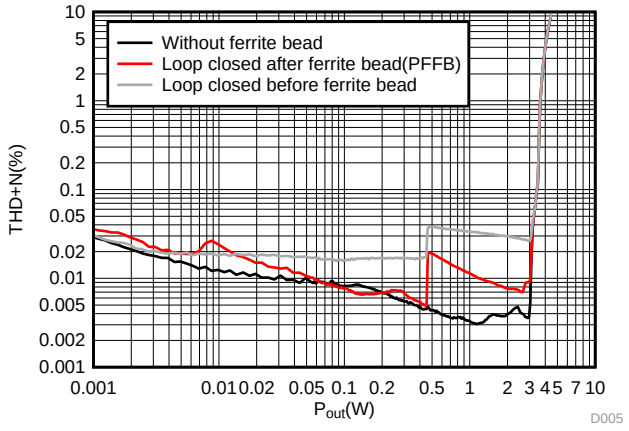
8 Ω + 33 µH P_{OUT} = 1 W

图 9. THD+N vs Frequency



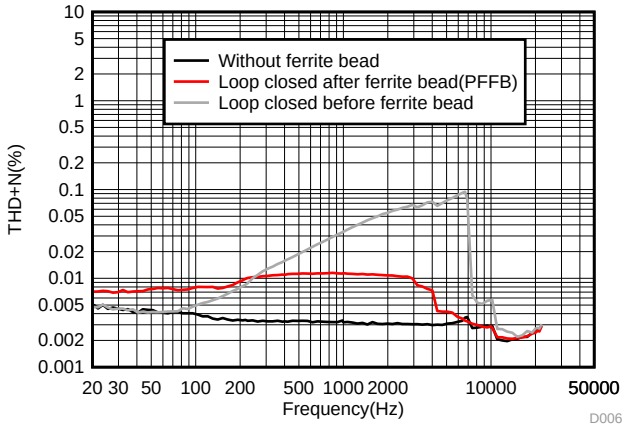
4 Ω + 16 µH P_{OUT} = 1 W

图 10. THD+N vs Frequency



8 Ω + 33 µH Freq = 1 kHz

图 11. THD+N vs Output Power



8 Ω + 33 µH P_{OUT} = 1 W

图 12. THD+N vs Frequency

Typical Characteristics (接下页)

VBAT = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, R_L = 8 Ω + 33 µH, I^2S digital input, Mode 2 (unless otherwise noted).

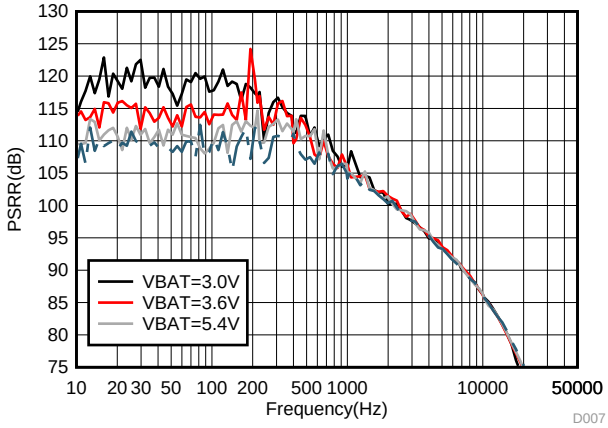


图 13. VBAT Supply Ripple Rejection vs Frequency

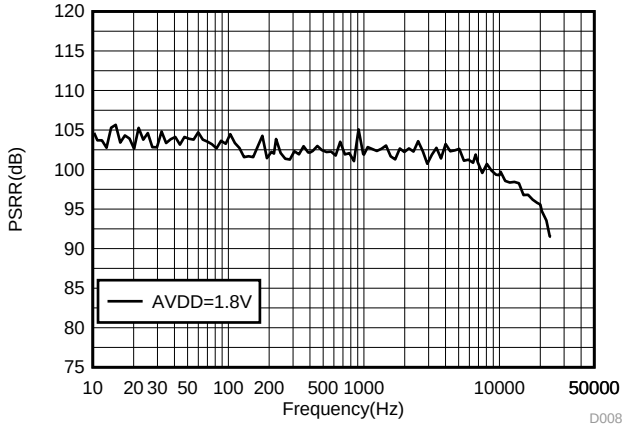
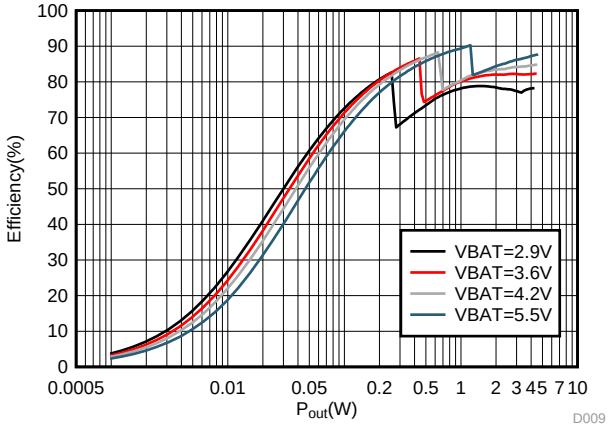
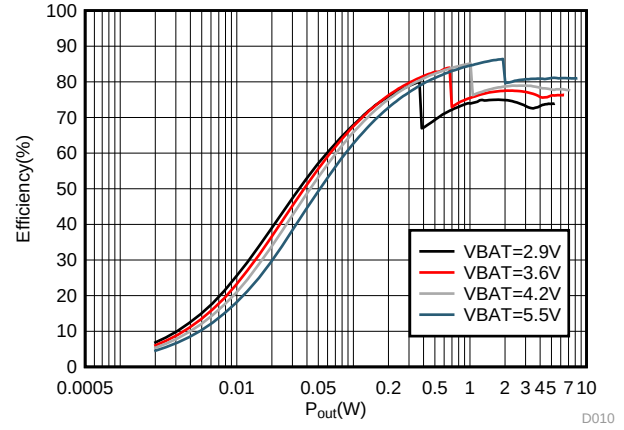


图 14. AVDD Supply Ripple Rejection vs Frequency



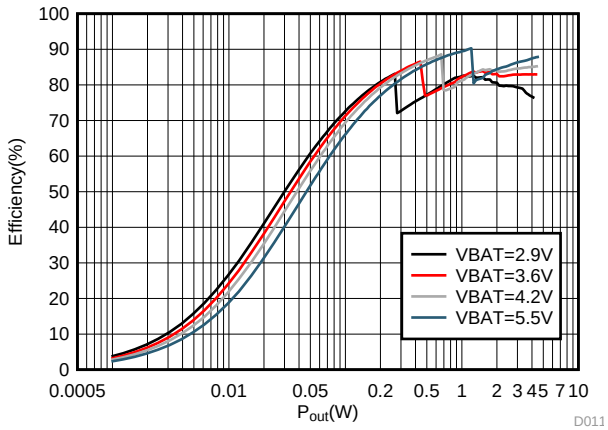
8 Ω + 33 µH SSM Mode

图 15. Efficiency vs Output Power Low Inrush



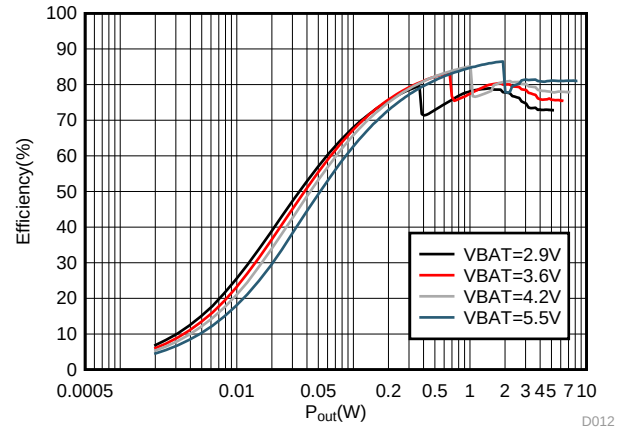
4 Ω + 16 µH SSM Mode

图 16. Efficiency vs Output Power Low Inrush



8 Ω + 33 µH SSM Mode

图 17. Efficiency vs Output Power High Efficiency

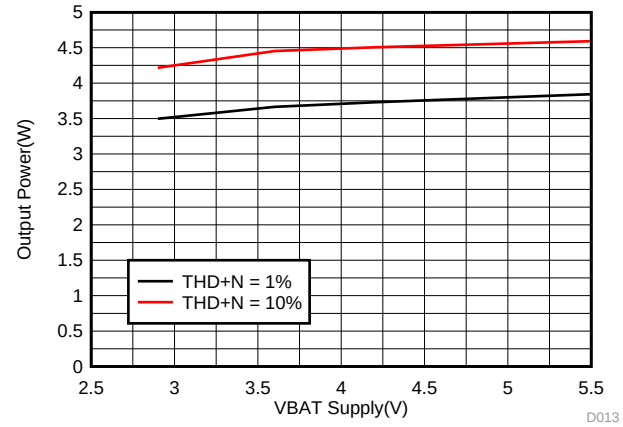


4 Ω + 16 µH SSM Mode

图 18. Efficiency vs Output Power High Efficiency

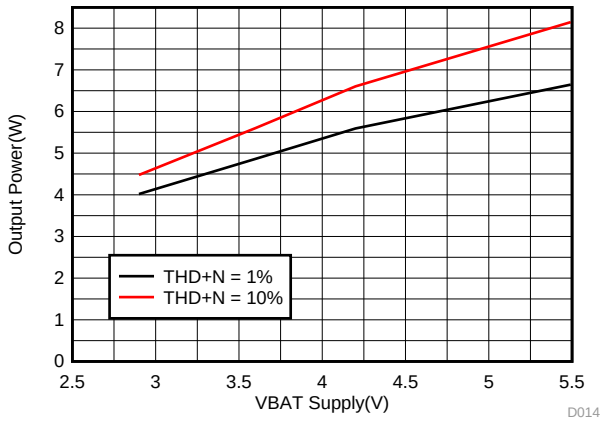
Typical Characteristics (接下页)

VBAT = 3.6 V, VDD = IOVDD = 1.8 V, RESETZ = IOVDD, R_L = 8 Ω + 33 µH, I^2S digital input, Mode 2 (unless otherwise noted).



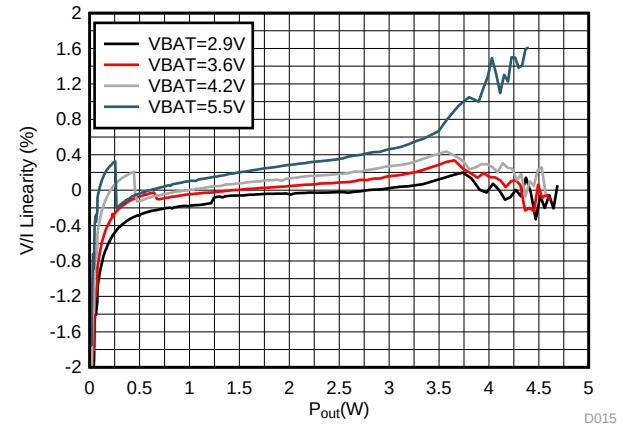
8 Ω+ 33 µH

图 19. Output Power for 1% and 10% THD+N vs VBAT



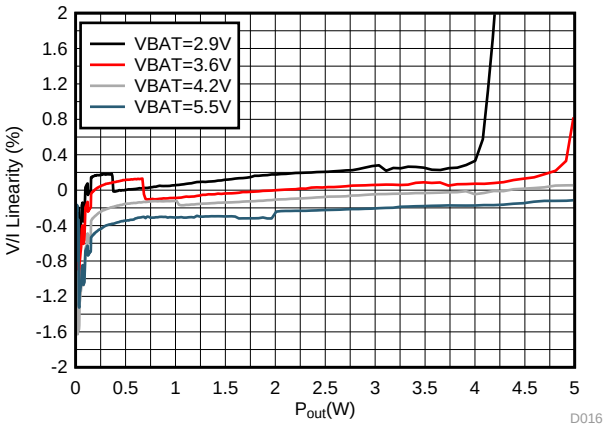
4 Ω+ 16 µH

图 20. Output Power for 1% and 10% THD+N vs VBAT



8 Ω + 33 µH

图 21. V/I Linearity vs Output Power



4 Ω+ 16µH

图 22. V/I Linearity vs Output Power

8 Parameter Measurement Information

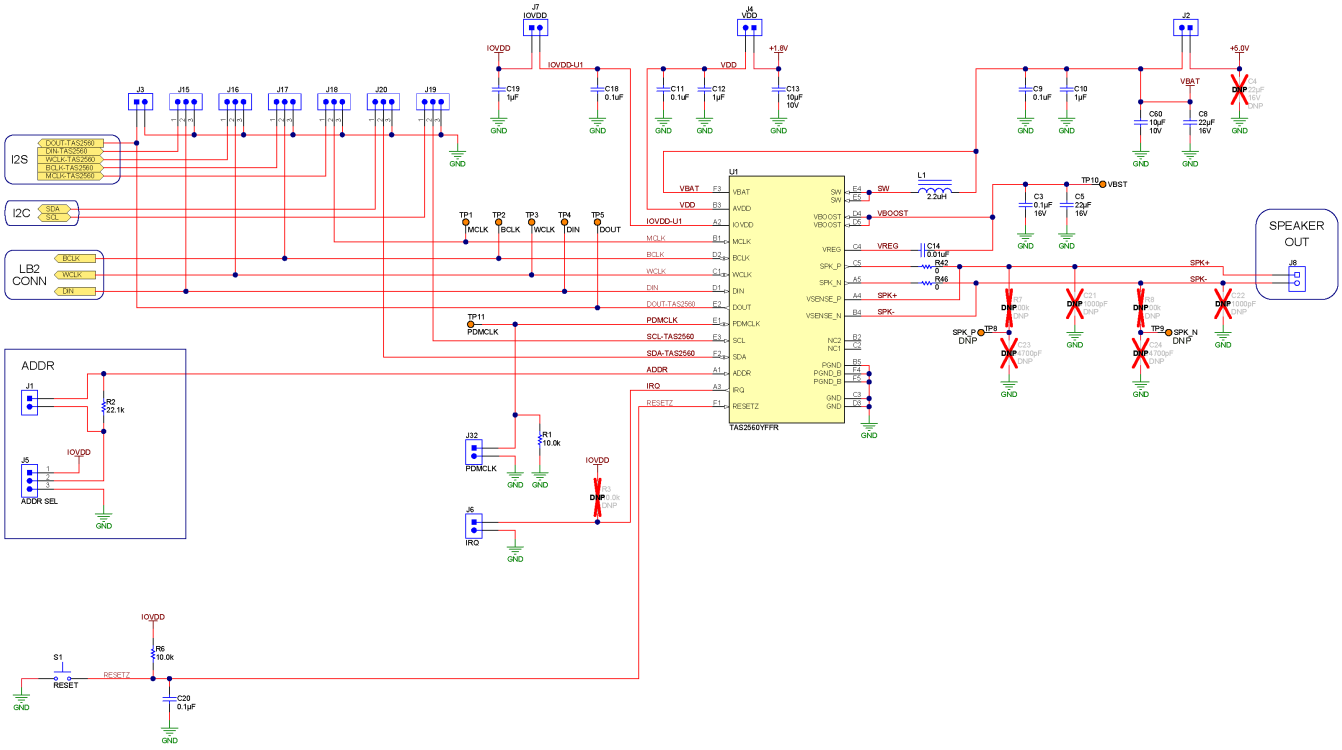


图 23. TAS2560 Test Circuit

All typical characteristics for the devices are measured using the bench EVM and an Audio Precision SYS-2722 audio analyzer. A Programable Serial Interface Adaptor (PSIA) is used to allow the I²S interface to be driven directly into the SYS-2722. SPEAKER OUT terminal is connected to Audio Precision analyzer inputs as shown below. There is a differential to single ended (D2S) filter, with 1st order Passive pole at 120 kHz is added. This is to ensure high performance Class-D amplifier sees a fully differential matched loading at its outputs and no degradation in performance measured due to loading effects of AUX filter on Class-D outputs.

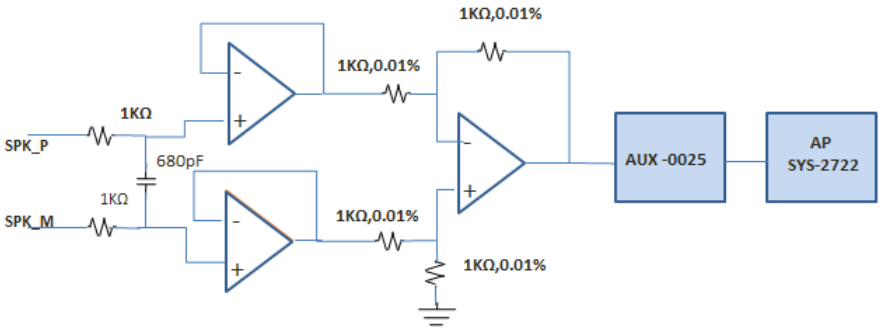


图 24. Differential To Single Ended (D2S) Filter

9 Detailed Description

9.1 Overview

The TAS2560 is a low-power, high-performance boosted Class-D Audio amplifier that can be used in numerous applications. The device features an ultra low-noise audio DAC and Class-D power amplifier which incorporates speaker voltage and current sensing feedback. The TAS2560, from a 4.2 V, supply drives up to 5.6 W into a 4-Ω speaker with 1% THDN or 3.7 W into an 8-Ω speaker with 1% THDN. The TAS2560 accepts input audio data rates from 8 kHz to 96 kHz to fully support both speaker-phone and music applications. The MCLK frequency range can be from 512 kHz to 49.15 Mhz. Also supported are crystal based MCLK frequencies of 6 Mhz, 12 Mhz, 13 Mhz, and 19.2 Mhz. Left + Right Input Mixing is available when used in a mono only application.

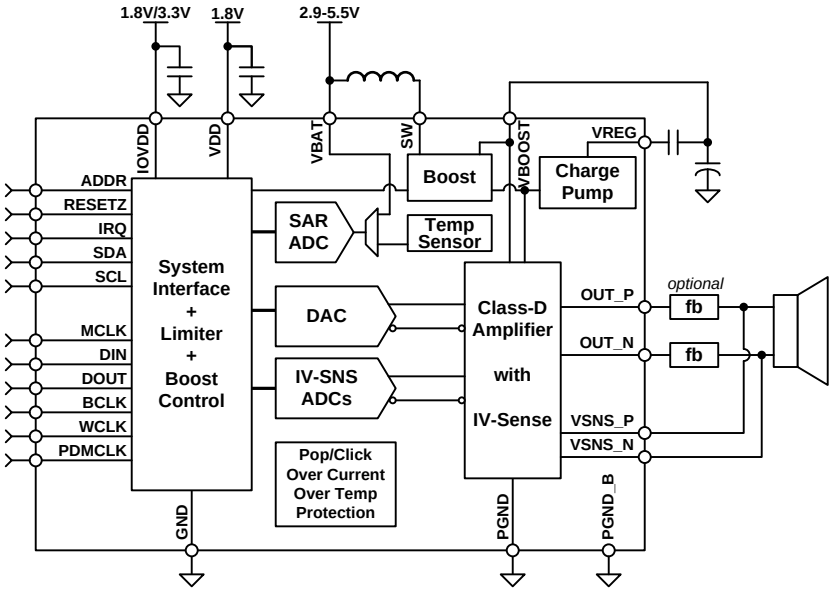
The multi-level Class-H boost converter generates the Class-D amplifier supply rail. When the audio signal requires a output power below VBAT, the boost improves system efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When higher audio output power is required, the boost quickly activates and provides a much louder and much clearer signal than can be achieved in any standard amplifier speaker system design approach. A boost inductor of 1uH can be used with a slight increase in boost ripple.

On-chip Battery Guard AGC system can limit audio power levels or even shutdown the TAS2560 to avoid an undesired system reset as the supply voltage decays. The Class-D output switching frequency is synchronous with the digital input audio sample rate to avoid left and right PWM frequency differences from beating in stereo applications. PWM Edge rate control and Spread Spectrum features are available if further EMI reduction is desired in the user's system.

The interrupt request pin, IRQ, indicates a device error condition. The interrupt flag conditions are selectable via I^2C and include: thermal overload, Class-D over-current, VBAT level low, brownout, and clock error. The IRQ signal is active-high for an interrupt request and high-Z during normal operation. This behavior can be changed by a register setting to tri-state the pin during normal operation to allow the IRQ pin to be tied in parallel with other active-low interrupt request pins on other devices in the system.

Stereo configuration can be achieved with two TAS2560 devices by using the ADDR pin to set different I^2C addresses in I^2C mode. Refer to the *General I^2C Operation* sections for more details.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 General I²C Operation

The TAS2560 operates as an I²C slave over the IOVDD voltage range. It is adjustable to one of four I²C addresses. This allows multiple TAS2560 devices in a system to connect to the same I²C bus. The I²C pins are fail-safe. Therefore, if the part is not powered or is in shutdown the I²C pins will not have an impact the I²C bus allowing it to remain useable.

The I²C address can then be set using the ADDR pin according to 表 1. The ADDR pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 10011xx. This permits the I²C address of TAS2560 to be 0x4C(7bit) through 0x4F(7-bit). For example, if the ADDR pin is shorted to ground the TAS2560 I²C address would be 0x4C(7bit). This is equivalent to 0x98 (8-bit) for writing and 0x99 (8-bit) for reading.

表 1. I²C Address Selection

ADDR Pin Conneciton	I²C Device Address
Short to GND	0x4C
Connection to GND using 22 kΩ Resistor	0x4D
Connection to IOVDD using 22 kΩ Resistor	0x4E
Short to IOVDD	0x4F

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The corresponding pins on the TAS2560 for the two signals are SDA and SCL. The bus transfers data serially, one bit at a time. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. 图 25 shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 660 Ω and 4.7 kΩ. Do not allow the SDA and SCL voltages to exceed the device digital interface supply voltage, IOVDD.

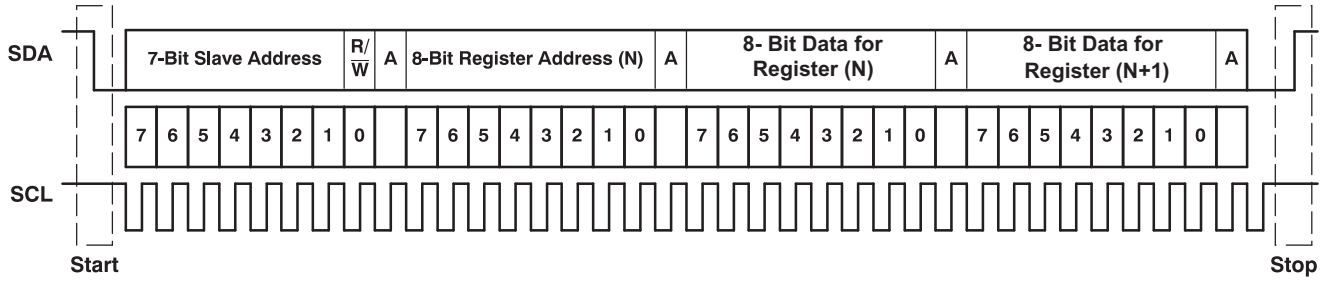


图 25. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. 图 25 shows a generic data transfer sequence.

9.3.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2560 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2560 supports sequential I^2C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I^2C write transaction has taken place. For I^2C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

9.3.3 Single-Byte Write

As shown in 图 26, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I^2C device address and the read/write bit, the TAS2560 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

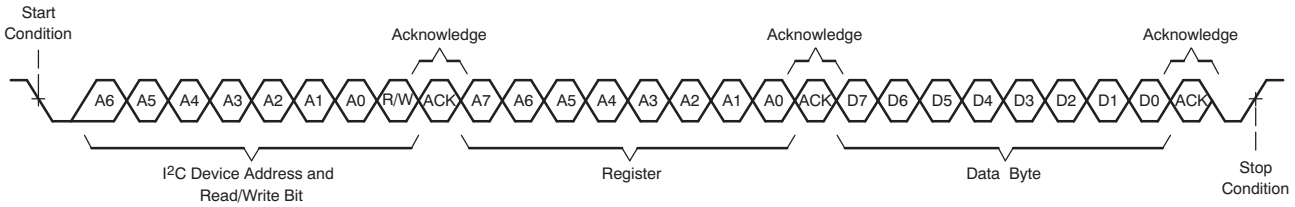


图 26. Single-Byte Write Transfer

9.3.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2560 as shown in 图 27. After receiving each data byte, the device responds with an acknowledge bit.

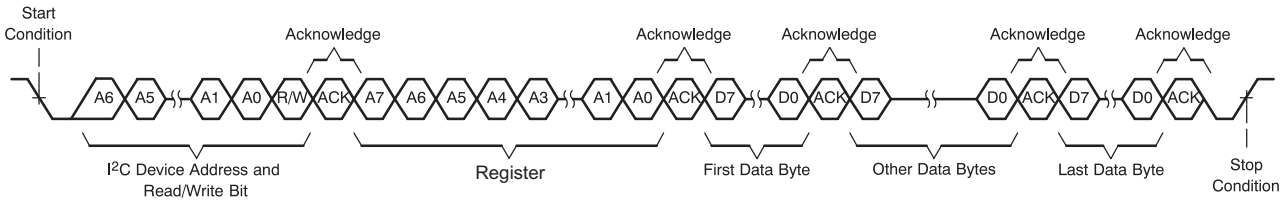


图 27. Multiple-Byte Write Transfer

9.3.5 Single-Byte Read

As shown in 图 28, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2560 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2560 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2560 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

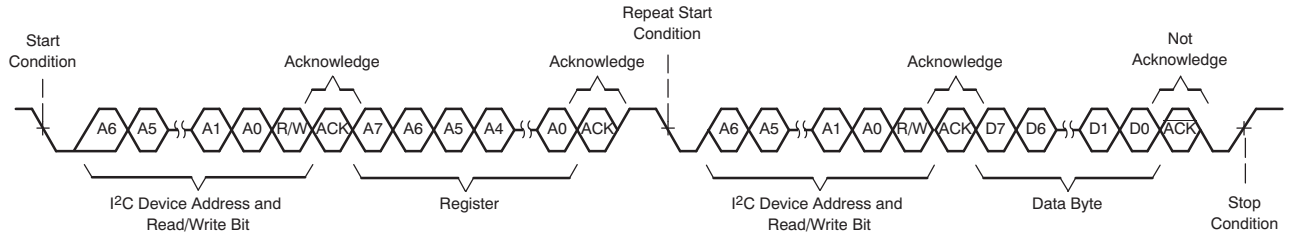


图 28. Single-Byte Read Transfer

9.3.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2560 to the master device as shown in 图 29. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

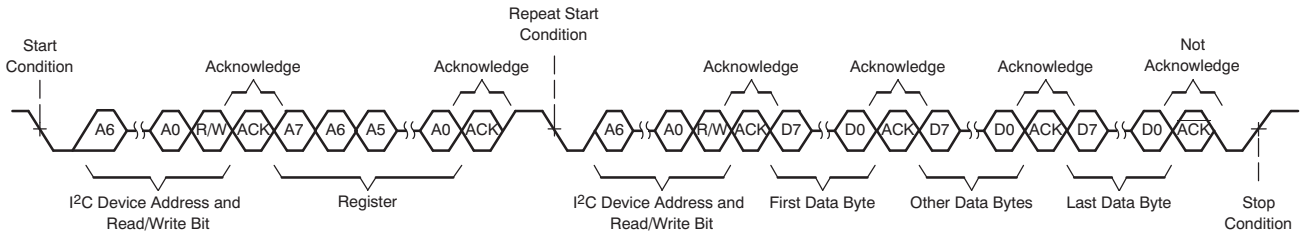


图 29. Multiple-Byte Read Transfer

9.3.7 PLL

The TAS2560 on-chip PLL generates the necessary internal clock frequency for the audio DAC, I-V sensing ADCs, and DSP. The programmability of the PLL allows TAS2560 operation from a wide variety of clocks that may be available in the system application. The configurable PLL clock path is shown in 图 30.

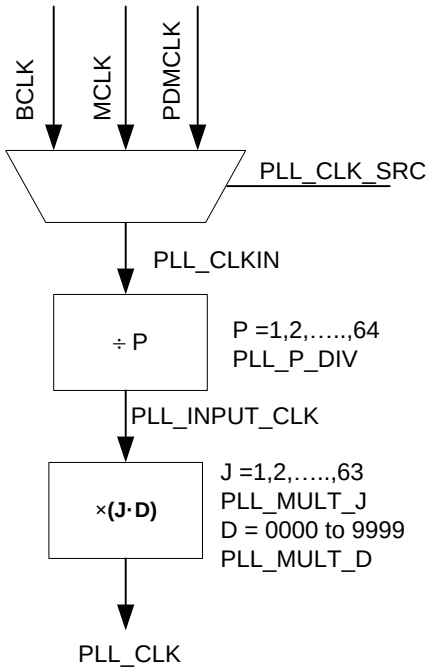


图 30. PLL_CLK Source and Generation

The PLL input supports clocks varying from 512 kHz to 20 MHz and is register programmable to enable generation of required PLL_CLK from various clocks with fine resolution. The PLL output clock PLL_CLK is determined from PLL_CLKIN using the following formula:

$$PLL\_CLK = \frac{PLL\_CLKIN * J.D}{P} \quad (1)$$

The PLL multipliers and dividers are program using the register in 表 2. The table includes also the range of values support and the default values. The D-divider value is 14-bits wide and is controlled by 2 registers. For proper update of the D-divider value, PLL_DVAL_1 must be programmed first followed immediately by PLL_DVAL_2. Unless the write to PLL_DVAL_2 is completed, the new value of D will not take effect.

表 2. PLL Scaling Registers

PLL Divider	Register Name	Field	Range	Default
J	PLL_JVAL[6:0]	PLL_MULT_J	1, 2, 3, … 63	4
D	PLL_DVAL_1[5:0] & PLL_DVAL_2[7:0]	PLL_MULT_D	0, 1, 2, ... 9999	0
P	PLL_CLKIN[5:0]	PLL_P_DIV	64,1,2,3, ... 63	1

Field PLL_CLK_SRC in register PLL_CLKIN configures the PLL clock input, PLL_CLKIN.

表 3. PLL Clock Input Source

PLL_CLKIN[7:6] (PLL_CLK_SRC)	PLL_CLKIN Source
00	Input from BCLK
01	Input from MCLK (default)
10	Input from PDMLK
11	Reserved

The following conditions must be satisfied in the PLL configuration:

- If D = 0 (Integer Mode), the PLL clock input (PLL_CLKIN) must satisfy:
  $512\ kHz \leq \frac{PLL\_CLKIN}{2^P} \leq 20MHz$
- If D > 0(Fractional Mode), the PLL clock input (PLL_CLKIN) must satisfy:
  $10\ MHz \leq \frac{PLL\_CLKIN}{2^P} \leq 20MHz$
- The PLL output needs to be configured between 100 MHz and 200 MHz

Finally, the PLL_LOWF field in register PLL_JVAL must be configured properly based on the PLL_INPUT_CLK intermediate clock frequency.

表 4. PLL Clock Input Source

PLL_JVAL[7] (PLL_LOWF)	PLL_INPUT_CLK Condition
0	>= 1MHz (default)
1	< 1MHz

9.3.8 Clock Distribution

TAS2560 clocking tree is driven by the PLL output. In order for this block to properly function, the output of the PLL (PLL_CLK) should be exactly 1024 times the sampling rate(Fs) or PLL_CLK=1204*Fs. For example, PLL_CLK should be 49.152 MHz for 48 kHz sampling rate or 45.1584 MHz for 44.1 kHz sampling rate. The following clocks that can be used for the audio interface clocking, see section Audio Digital I/O Interface for more information.

表 5. Clocking Block Rates

Internal Clocking Node	Clocking Rate
NDIV_CLK	CLK_IN / 2
DAC_MOD_CLK	CLK_IN / 16
ADC_MOD_CLK	CLK_IN / 16

9.3.9 Clock Error Detection

TAS2560 has two clock error detection blocks that soft-mute the playback path when errors in the clocking signals occur. Clock error detection 1 block is used for monitoring the audio interfaces. The clock error detection 2 block is used for monitoring the internal clocks for situations where the audio interface clocks are different from the PLL input clock.

表 6. Clock Error 1 Source

CLK_ERR_1[4] (CLK_E1_SRC)	Input Source
0	ASI_CLK (default)
1	PDM_CLK

表 7. Clock Error 2 Source

CLK_ERR_1[3:2] (CLK_E2_SRC)	Input Source
00	DAC Modulator Clock (default)
01	ADC Modulator Clock
10	PLL Clock
11	Reserved

The clock error detection blocks may be disabled using field CLK_ERR1_EN and CLK_ERR2_EN. It is recommend to disable these blocks. Both clock error blocks must be enable or disabled together to ensure correct operation. When clock error blocks are enabled the idle channel detection used to reduce power consumption must be disabled. It is recommended to use PurePath™ Console 3 Software TAS2560 Application software to generate the device configuration files. The following code should be written to disable the idle channel detection block.

```
#add in dsp memory write section after Device power up and a delay
#assuming B0_P0
w 98 00 32
w 98 6c 00 00 00 00 # disabling idle channel detect
w 98 00 00
```

表 8. Clock Error 1 Enable

CLK_ERR_1[1] (CLK_E1_EN)	Clock Error Detection
0	disabled
1	enabled (default)

表 9. Clock Error 2 Source

CLK_ERR_1[0] (CLK_E2_EN)	Clock Error Detection
0	disabled
1	enabled (default)

The detection block will trigger when the clock input to the specified detection block is not present within the respective specified time of field CLK_ERR1_TIME or CLK_ERR2_TIME

表 10. Clock Error 1 Timeout

CLK_ERR_2[5:3] (CLK_E1_TIME)	Timeout
000	11 ms
001	22 ms

表 10. Clock Error 1 Timeout (接下页)

CLK_ERR_2[5:3] (CLK_E1_TIME)	Timeout
010	44 ms
011	87 ms
100	174 ms
101	350 ms
110	700 ms
111	1.2 s (default)

表 11. Clock Error 2 Timeout

CLK_ERR_2[2:0] (CLK_E2_TIME)	Timeout
000	11 ms
001	22 ms
010	44 ms
011	87 ms
100	174 ms
101	350 ms
110	700 ms
111	1.2 s (default)

When a clocking error is detected the playback will be soft-mute at a rate set by field CLK_ERR_MR in register CLOCK_ERR_CFG_2. The error will be recorded in the sticky register INT_DET_1 and can be reported on the interrupt pin if mask in register INT_CFG_2

表 12. Clock Error Soft-mute Ramp Rate

CLK_ERR_CFG_2[7:6] (CLK_ERR_MR)	Ramp-down Rate
00	15 us per dB (default)
01	30 us per dB
10	60 us per dB
11	120 us per dB

When the clock is available the system will perform a pop-free un-mute and resume operation.

9.3.10 Class-D Edge Rate Control

The edge rate of the Class-D output is controllable via I^2C field EDGE_RATE in register EDGE_ISNS_BOOST. This allows users the ability to adjust the switching edge rate of the Class-D amplifier, trading off some efficiency for lower EMI. 表 13 lists the typical edge rates. The default edge rate of 14 ns passes EMI testing. The default value is recommended but may be changed if required.

表 13. Class-D Edge Rate Control

EDGE_ISNS_BOOST[7:5] (EDGE_RATE)	t_R AND t_F (TYPICAL)
000	Reserved
001	Reserved
010	29 ns
011	25 ns
100	14 ns (default)
101	13 ns
110	12 ns
111	11 ns

9.3.11 IV Sense

The TAS2560 provides speaker voltage and current sense for real-time monitoring of loudspeaker behavior. The VSNS_P and VSNS_N pins should be connected after any ferrite bead filter (or directly to the OUT_P and OUT_N connections if no EMI filter is used). The V-Sense connections eliminate IR drop error due to packaging, PCB interconnect or ferrite bead filter resistance. The V-sense connections are also used for post filter Class-D feedback to correct for any IR-drop induced gain error or non-linearities due to the ferrite bead. It should be noted that any interconnect resistance after the V-Sense terminals will not be corrected for. Therefore, it is advised to connect the sense connections as close to the load as possible. Additionally, the v-sense pins are used the close the feedback loop on the Class-D amplifier externally. This Post-Filter Feedback (PFFB) minimized the THD introduced from the filter-beads used in the system.

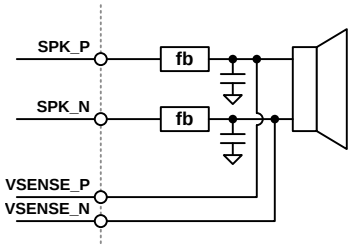


图 31. V-Sense Connections

The I-Sense can be configured for three ranges and shown in 表 14. This should be set appropriately based on the DC resistance of the speaker. I-Sense and V-Sense can additionally be powered down as shown in 表 15 and 表 16. When powered down, the device will return null samples for the powered down sense channels.

表 14. I-Sense Current Range

EDGE_ISNS_BOOST[4:3] (ISNS_SCALE)	Full Scale Current	Speaker Load Impedance
00	1.25 A (default)	8 Ω
01	1.5 A	6 Ω
10	1.75 A	4 Ω
11	Reserved	Reserved

表 15. I-Sense Power Down

PWR_CTRL_1[2] (MUTE_ISNS)	Setting
0	I-Sense is active (default)
1	I-Sense is powered down

表 16. V-Sense Power Down

PWR_CTRL_1[1] (MUTE_VSNS)	Setting
0	V-Sense is active (default)
1	V-Sense is powered down

9.3.12 Boost Control

The TAS2560 internal processing algorithm automatically enables the boost when need. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disable and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using 表 17.

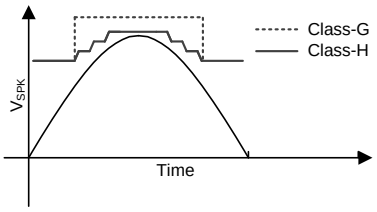


图 32. Boost Mode Signal Tracking Example

表 17. Boost Mode

SPK_CTRL[4] (BST_MODE)	Boost Mode
0	Class-H - High efficiency
1	Class-G - Low in-rush (default)

9.3.13 Thermal Fold-back

The TAS2560 monitors the die temperature and prevents if from going over a set limit. When enabled a internal controller will automatically adjust the signal path gain to prevent the die temperature from exceeding this limit. This allows instantaneous peak power to be delivered to the speaker while limiting the continuous power to prevent thermal shutdown. The configuration parameters for the thermal fold-back are part of the DSP core and can be set using the PurePath™ Console 3 Software TAS2560 Application software for the TAS2560 part under the Device Control Tab.

9.3.14 Battery Guard AGC

The TAS2560 monitors battery voltage and the audio signal to automatically decrease gain when the battery voltage is low and audio output power is high. This provides louder audio while preventing early shutdown at end-of-charge battery voltage levels. The battery tracking AGC starts to attenuate the signal once the voltage at the Class-D output exceeds V_{LIM} for a given battery voltage (VBAT). If the Class-D output voltage is below the V_{LIM} value, no attenuation occurs. If the Class-D output exceeds the V_{LIM} value the AGC starts to attack the signal and reduce the gain until the output is reduced to V_{LIM}. Once the signal returns below V_{LIM} plus some hysteresis the gain reduction decays. The V_{LIM} is constant above the user configurable inflection point. Below the inflection point the V_{LIM} is reduced by a user configurable slope in relation to the battery voltage. The attack time, decay time, hysteresis, inflection point and V_{LIM}/VBAT slope below the inflection point are user configurable. The parameters for the Battery Tracking AGC are part of the DSP core and can be set using the PurePath™ Console 3 Software TAS2560 Application software for the TAS2560 part under the Device Control Tab. Below a VBAT level of 2.9 V, the boost will turn on to ensure correct operation but results in increased current consumption. The device is functional until the set brownout level is reached and the device shuts down. The minimum brownout voltage is 2.7 V.

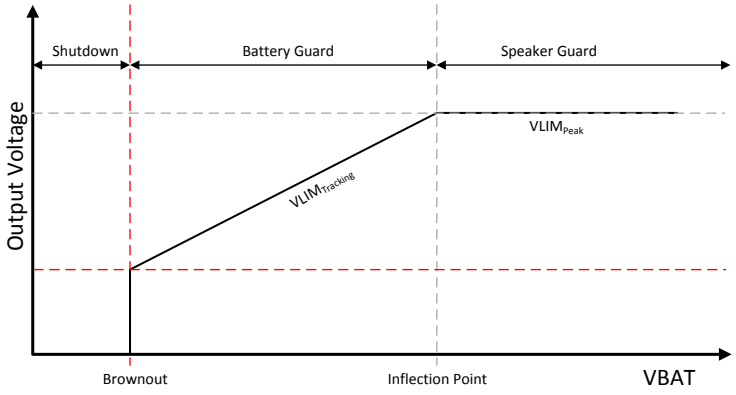


图 33. VLIM versus Supply Voltage (VBAT)

When the VBAT voltage drops below the brownout threshold the TAS2560 will power-down to prevent damage. The brownout can be reported on the interrupt pin. See section IRQs and Flags on how to enable this feature. Once the device voltage returns again above the brownout limit the device will need to be externally re-powered, see Brownout.

9.3.15 Configurable Boost Current Limit (ILIM)

The TAS2560 has a configurable boost current limit (ILIM). The default current limit is 3A but this limit may be set lower based on selection of passive components connected to the boost. The TAS2560 supports 4 different boost limits and can be set using 表 18.

表 18. Current Limit Settings

EDGE_ISNS_BOOST[1:0] (BOOST_ILIM)	BOOST CURRENT LIMIT (A)
00	1.5
01	2.0
10	2.5
11	3.0 (default)

9.3.16 Fault Protection

The TAS2560 has several protection blocks to prevent damage. Those blocks including how to resume from a fault are presented in this section.

9.3.16.1 Speaker Over-Current

The TAS2560 has an integrated over-current protection that is enabled once the Class-D is powered up. A fault on the Class-D output causing a large current in the range of 3 A to 5 A triggers the over-current fault. Once the fault is detected the TAS2560 disables the audio channel and powers down the Class-D amplifier. When an over-current event occurs, a status flag INT_OVRI is set. This register is sticky and the bit remains high for as long as it is not read, or the device is not reset. The over-current event can also be used to generate an interrupt if required. Refer to IRQs and Flags for more details. To re-enable the audio channel after a fault the Class-D the device must be powered back up using field PWR_DEV, see 表 53.

9.3.16.2 Analog Under-Voltage

The TAS2560 device has an integrated undervoltage protection on the analog power supply lines VDD and VBAT. The undervoltage limit fault is triggered when VDD is less than 1.5V or VBAT is less than 2.4 V. Once the fault is detected the TAS2560 device will disable the audio channel and power down the Class-D amplifier. When an under-voltage event occurs, a status flag INT_AUV is set. This register is sticky and the bit will remain high for as long as it is not read, or the device is not reset. The undervoltage event can also be used to generate an interrupt if required. Refer to IRQs and Flags for more details. To re-enable the audio channel after a fault the Class-D the device must be powered back up using field PWR_DEV, see 表 53.

9.3.16.3 Die Over-Temperature

The TAS2560 has an integrated over temperature protection that is enabled once the Class-D is powered up. If the device internal junction temperature exceeds the safe operating region it will trigger the over-temperature fault. Once the fault is detected the TAS2560 disables the audio channel and powers down the Class-D amplifier. By default the device is set to auto-retry and will attempt to power up the class-D every 100ms. If the over-termperature condition is still present it will shut-down again. The auto-retry can be disabled by setting the register field PROT_OT_AR high. When an over-temperature event occurs, a status flag at INT_ORVT is set. This register is sticky and the bit will remain high for as long as it is not read, or the device is not reset. The over temperature event can also be used to generate an interrupt if required. Refer to *IRQs and Flags* section for more details. To re-enable the audio channel after a fault the Class-D the device must be powered back up using field PWR_DEV, see 表 53.

表 19. Die Over-Temperature Auto-Retry

PROTECTION_CFG_1[2] (PROT_OT_AR)	Over Temperature Protection Auto-Retry
0	Enabled (default)
1	Disabled

9.3.16.4 Clocking Faults

The TAS2560 has two clock error detection blocks. The first is used to monitor the Audio Serial Interfaces (ASI). If a clock error is detected on the ASI interfaces audio artifacts can occur at the Class-D output. When enabled the ASI clock error detection can soft-mute the device, then shutdown the Class-D and DSP core. The second clock error detection block can monitor the internal DAC, ADC, and PLL clocks and used when the PLL clock may be from a different source than the ASI clocks. When a clock error is detected the output is soft-muted and the Class-D powered down. Information on configuring the error detection is in section Clock Error Detection

When a clocking error occurs the following sequence should be performed to restart the device.

- Clear the clock error interrupts by reading the sticky flags at register INT_DET_1 fields INT_CLK1 and INT_CLK2
- Clear the power error field PWR_ERR in register PWR_CTRL_2

9.3.16.5 Brownout

The TAS2560 has an integrated brownout system to shutdown the device when the battery voltage drops to an insufficient level. This user configurable level can be set under Device Control in the PurePath™ Console 3 Software TAS2560 Application. When brownout event occurs a status flag B0_P0_R38[3] is set. This register is sticky and the bit remains high for as long as it is not read, or the device is not reset. The brownout event can also be used to generate an interrupt if required. Refer to *IRQs and Flags* section for more details. Once the battery voltage drops below the defined threshold the following actions occur.

- The audio playback is muted in a graceful soft-stepping manner
- DSP, clock dividers, and analog blocks are powered down.
- The brownout is reported in field PWR_ERR.

Once the device voltage returns again above the brownout limit the device will need to be externally re-powered by

- Clear the brownout error interrupts by reading the sticky flags at register INT_DET_1 fields INT_BRNO
- Clear the field PWR_ERR in register PWR_CTRL_2.

表 20. Power Down Error

PWR_CTRL_2[0] (PWR_ERR)	Power Down
0	No error, device normal operation
1	Brownout detected, device powered down

9.3.17 Spread Spectrum vs Synchronized

The Class-D switching frequency can be selected to work in three different modes of operations selected by 表 21. This configuration needs to be done before powering up the audio channel. The first is a synchronized mode where the Class-D frequency is synchronized to audio input sample rate. This is the default mode of operation and can be used in stereo applications to avoid inter-modulation beating of the Class-D frequency from multiple chips. The Class-D switching frequency in this mode can be configured as 384 kHz or 352.8 kHz. The 384 kHz frequency is the default mode of operation, and can be used for input signals running on clock rates of 48 kHz or its sub-multiples. For input signals running on clock rate of 44.1 kHz and its sub-multiples, the switching frequency can be selected as 352.8 kHz using field RAMP_FREQ.

The second mode is fixed-frequency mode and the ramp is generated from the internal oscillator. The internal oscillators across chips will vary slightly and this can create an intermodulation beating in application where more than one TAS2560 is used.

The last mode is spread-spectrum mode and used to reduce wideband spectral content. This can improve EMI emissions radiated by the speaker by spreading out the noise in the spectrum. In this mode, the Class-D switching frequency varies +-5% or +-10% base on the 表 23 around the 表 22 around a 384 kHz center frequency. These registers should be written before powering up the audio channel.

表 21. Ramp Clock Mode

RAMP_CTRL[7:6] (RAMP_MODE)	Setting
00	Sync Mode - ramp generated from digital audio clock (default)

表 21. Ramp Clock Mode (接下页)

RAMP_CTRL[7:6] (RAMP_MODE)	Setting
01	Fixed Frequency Mode(FFM) - ramp generated from internal oscillator
10	Spread Spectrum Mode(SSM) - ramp generated from internal oscillator with spread spectrum
11	Reserved

表 22. Ramp Clock Frequency

RAMP_CTRL[5:4] (RAMP_FREQ)	Setting
00	384 kHz - Use for Fs multiples of 48 kHz (default)
01	352.8 kHz - Use fpr Fs multiples of 44.1 kHz
10	Reserved
11	Reserved

表 23. Ramp SSM Mode

RAMP_CTRL[1:0] (RAMP_FREQMOD)	Setting
00	Reserved
01	SSM mode enabled with ramp frequency modulated for ±5 % (default)
10	SSM mode enabled with ramp frequency modulated for ±10 %
11	Reserved

9.3.18 IRQs and Flags

Internal device flags such as over-current, under-voltage, etc can be routed to the interrupt. If more than one flag is asserted the interrupt output is the logical OR-ing of all flags. If multiple flags are asserted the host should then query the interrupts sticky register to determine which event triggered the interrupt. For example, to route the Brownout and Speaker Over Current flags to the IRQ pin the following register would be set INT_CFG_2=0x88.

表 24. Interrupt Registers

Flag Description	Sticky Register Bit	Register to Enable Interrupt Mask
Speaker Over Current	INT_DET1[7] (INT_OVRC)	INT_CFG_2[7] (INTM_OVRC)
Speaker Over Voltage	INT_DET1[6] (INT_OVRV)	INT_CFG_2[6] (INTM_ORV)
Clock Error Detection 1	INT_DET1[5] (INT_CLK1)	INT_CFG_2[5] (INTM_CLK2)
Over Temperature	INT_DET1[4] (INT_OVRT)	INT_CFG_2[4] (INTM_OVRT)
Brownout	INT_DET1[3] (INT_BRNO)	INT_CFG_2[3] (INTM_BRNO)
Clock Error Detection 2	INT_DET1[2] (INT_CLK2)	INT_CFG_2[2] (INTM_CLK1)
Clock Halt Word Clock	INT_DET2[7] (INT_WCHLT)	INT_CFG_2[1] (INTM_WCHLT)
Clock Halt Modulator Clock	INT_DET2[6] (INT_MCHLT)	INT_CFG_2[0] (INTM_MCHLT)

The IRQ pin will be low during normal operation and indicate an interrupt with a high signal output. The output drive options of the IRQ pin are shown in 表 25 and the output can be configured to support various use cases such as external HiZ for or-ing multiple parts are directly driving the high-low output. When an IRQ event occurs the IRQ can be set to toggle or pulse, see 表 28. Additionally the IRQ pin can be disabled, used as a register controlled general purpose output, or a clock pin in PDM mode of operation. The various modes are shown in 表 26. If using the IRQ pin as a general purpose output the value can be set per 表 27.

表 25. IRQ Pin Drive

IRQ_PIN_CFG[7:5] (IRQ_DRIVE)	Output Drive IRQ Pin
001	Drive both high and low values
010	Open Drain, low-actively driven, high-HiZ (default)
011	Open Drain, low-actively driven, high-HiZ w/ pull-up

表 25. IRQ Pin Drive (接下页)

IRQ_PIN_CFG[7:5] (IRQ_DRIVE)	Output Drive IRQ Pin
100	Open Drain, low-HiZ w/ pull-down, high-actively driven
101-111	Reserved

表 26. IRQ Pin Mode

IRQ_PIN_CFG[2:0] (IRQ_PIN_MODE)	IRQ Pin Mode
001	Disabled and IO buffers powered down
010	Interrupt controlled output (default)
011	Reserved
100	General purpose output
101	PDM_IN_DIV output
110-111	Reserved

表 27. IRQ GPO Value

IRQ_PIN_CFG[4] (IRQ_GPO_VAL)	IRQ Pin GPO Value
0	low (default)
1	high

表 28. IRQ Indicator Mode

INT_CFG_1[7:6] (IRQ_IND_CFG	IRQ Pin Indicator Mode
00	Interrupt will be only one pulse(active high) of duration 2 ms. (default)
01	Interrupt will be continuously pulsed with a duration 2ms and period 4ms until interrupt sticky flags are cleared by reading INT_DET_1 and INT_DET_2
01	Interrupt will remain high after interrupt is generated until interrupt sticky flags are cleared by reading INT_DET_1 and INT_DET_2
11	Reserved

9.3.19 CRC checksum for I^2C

The TAS2560 contain logic to verify that all write operations to the device were correctly received. This can be used to detect a configuration error of the device in the event of a problem or collision on the I^2C bus. On every register write other than to the book switch register(B0_P0_R127) or page switch register(B0_Px_R0) will update the 8-bit CRC checksum using the contents of the 8-bit register write data. Only register write operations will update the CRC, register read operations will not change the CRC value. The CRC checksum register CRC_CHECKSUM will return the current checksum from all previous write operations. The CRC checksum register can be write to initialize the starting value and is initially defaulted to 0x00 on a reset. The polynomial used for the CRC is 0x7 (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1+x^1+x^2+x^8)) Since we are using CRC, order of writes will also affect CRC.

```
global gChecksum # To keep track of the checksum in firmware

# Function to init the local checksum as well as that inside device
function initChecksum():
    gChecksum = 0
    i2c_write(regChecksum, 0) # regChecksum is the register number of the checksum R/W reg in device

# Function to update the local checksum
function addToChecksum(addr, data):
    if addr != regChecksum: # Checksum reg is ignored
        # Update gChecksum with data. Ignore book/page registers
        tempdata = gChecksum ^ inData
        for ( i = 0; i < 8; i++ ):
            if (( tempdata & 0x80 ) != 0 ):
                tempdata <<= 1
                tempdata ^= 0x07
```

```
            else:
                tempdata <<= 1;
            gChecksum = tempdata

# Function to compare checksums
function checkChecksum():
    return (i2c_read(regChecksum) == gChecksum)
    # Existing I2C write that does multibyte write to device

function i2c_write(addr, {data}):
    # Write the stuff to the device

function i2c_read(addr):
    # Read the data at device addr
    return result

# New function for verified writes
function i2c_write_checksum(addr, {data}):
    initChecksum()
    i2c_write(addr, {data})
    for word in data:
        addToChecksum(addr, word)
        addr++
    return checkChecksum()
```

9.3.20 PurePath™ Console 3 Software TAS2560 Application

The TAS2560 advanced features and a significant portion of the device configuration is performed using PurePath Console 3 (PPC3). The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2560 application can be download from with-in PPC3. The datasheet refers to options that can be configured using the PPC3 software tool.

9.4 Device Functional Modes

9.4.1 Audio Digital I/O Interface

Audio data is transferred between the host processor and the TAS2560 via the digital audio serial interface(ASI), or audio bus. The audio bus on this device is flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly. The audio bus of the TAS2560, when using PCM formatted input and/or output, can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits where the chip input can be left, right or L+R/2.

表 29. ASI PCM Mode

ASI_FORMAT[4:2] (ASI_MODE)	ASI Function Mode
000	I^2S Mode (default)
001	DSP Mode
010	Right-Justified Mode (RJF)
011	Left-Justified Mode (LJF)
100	Mono PCM Mode
101	DSP Time Slot Mode

表 30. ASI PCM Input Word Length

ASI_FORMAT[1:0] (ASI_LENGTH)	Word Length
00	16 bits
01	20 bits
10	24 bits (default)
11	32 bits

表 31. ASI PCM Channel Mode

ASI_CHANNEL[1:0] (ASI_CHAN_MODE)	Input Stereo Channel
00	Left (default)
01	Right
10	(Left + Right) / 2
11	monoPCM

In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse(DSP) or a 50% duty cycle signal(I^2S). The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies. Clock sources for Master mode are described in section Clock Distribution. When the audio serial data bus is powered down while configured in master mode, the terminals associated with the interface are put into a Hi-Z output state.

表 32. ASI WCLK Mode

ASI_CFG_1[5] (ASI_WCLKM)	WCLK Mode
0	Input - Slave Mode (default)
1	Output - Master Mode

表 33. ASI WCLK Edge

ASI_CFG_1[3] (ASI_WCLKE)	WCLK Edge
0	As per the timing spec (default)
1	Inverted with respect to timing spec

表 34. ASI Dividers Clock Source

ASI_DIV_SRC[1:0] (ASI_DIV_CLK_SRC)	Input Stereo Channel
00	DAC_MOD_CLK (default)
01	ADC_MOD_CLK
10	NDIV_CLK
11	Reserved

表 35. ASI WCLK Divider Power

ASI_WDIV[7] (ASI_WDIV_P)	WCLK Divider Power
0	Powered Down (default)
1	Powered Up

表 36. ASI WCLK Divider Ratio

ASI_WDIV[6:0] (ASI_WDIV_RATIO)	WCLK Divider Ratio
0x00	128
0x01-0x1F	Reserved
0x20	32
...	...
0x40	64 (default)
...	...
0x7F	127

The bit clock is used to clock-in and clock-out the digital audio data across the serial bus. This signal can be programmed to generate variable clock pulses by controlling the bit-clock multiply-divide factor. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TAS2560 devices may share the same audio bus.

表 37. ASI BCLK Mode

ASI_CFG_1[4] (ASI_BCLKM)	BCLK Mode
0	Input - Slave Mode (default)
1	Output - Master Mode

表 38. ASI BCLK Edge

ASI_CFG_1[2] (ASI_BCLKE)	BCLK Edge
0	As per the timing spec (default)
1	Inverted with respect to timing spec

表 39. ASI BCLK Divider Power

ASI_BDIV[7] (ASI_WDIV_P)	BCLK Divider Power
0	Powered Down (default)
1	Powered Up

表 40. ASI BCLK Divider Ratio

ASI_BDIV[6:0] (ASI_WDIV_RATIO)	BCLK Divider Ratio
0x00	128
0x01	1 (default)
0x02	2
...	...
0x7F	127

The TAS2560 also includes a feature to offset the position of start of data transfer with respect to the word-clock(WCLK). This offset is specified in number of bit-clocks. This can be used in cases where there is a non-zero bit-clock delay from WCLK edge or to support TDM modes of operation. The TAS2560 can place the DOUT line into a Hi-Z (tri-state) condition during all bit clocks when valid data is not being sent. TDM mode is useable with I^2S, LJF, RJF, and DSP interface modes and is required for stereo applications when more than one TAS2560 part is used, see Stereo Application Example - TDM Mode. The TAS2560 also has a bus keeper circuit that can be enabled in tri-sate mode. The bus-keeper is a weak internal latch that will hold the data line state without the need for external pull-up or pull-down resistors while signal lines are in the Hi-Z or non-driven state.

表 41. ASI OFFSET1

ASI_OFFSET_1 (ASI_OFFSET1)	BCLKs from WCLK edge for data channel
0x00	0 (default)
0x01	1
0x02	2
...	...
0xFF	255

表 42. ASI Tri-state

ASI_CFG_1[1] (ASI_TRISTATE)	Tri-state DOUT for extra BCLK cycles after frame is complete
0	disabled (default)
1	enabled

表 43. ASI Bus-keeper

ASI_CFG_1[0] (ASI_BUSKEEP)	Tri-state DOUT for extra BCLK cycles after frame is complete
0	disabled (default)
1	enabled

9.4.1.1 I^2S Mode

In I^2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

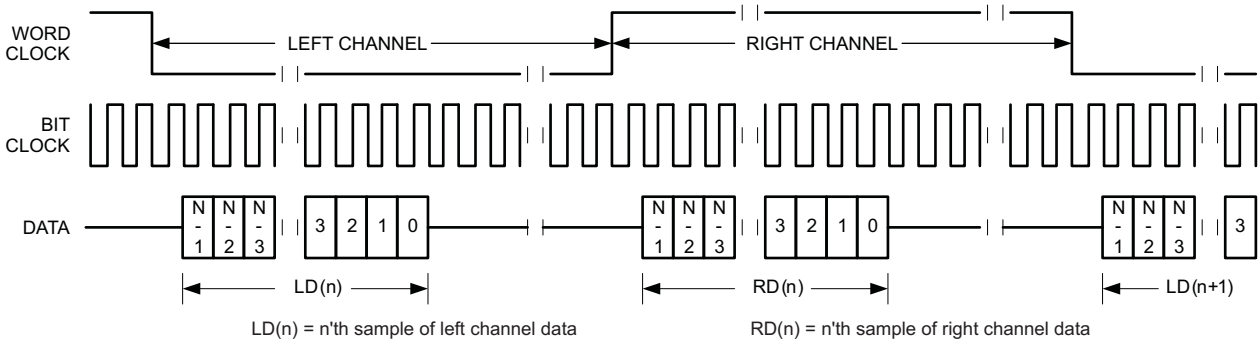


图 34. Timing Diagram for I^2S Mode

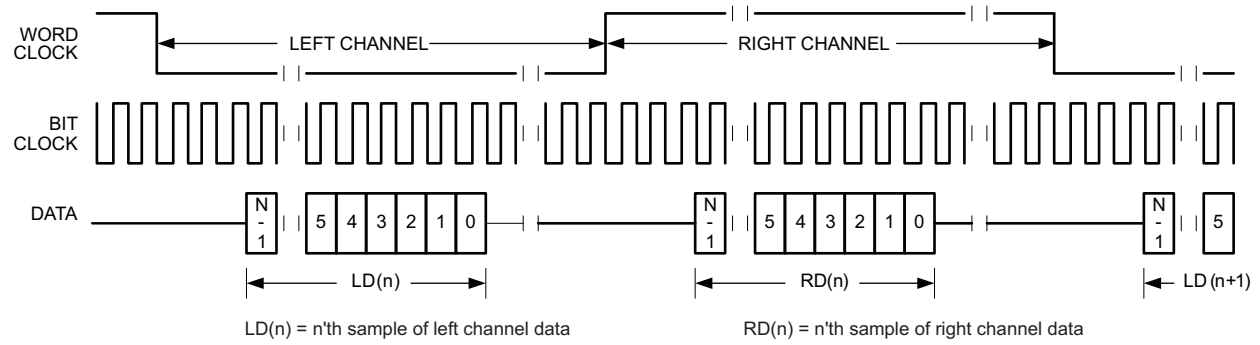


图 35. Timing Diagram for I^2S Mode with ASI_OFFSET1 = 2

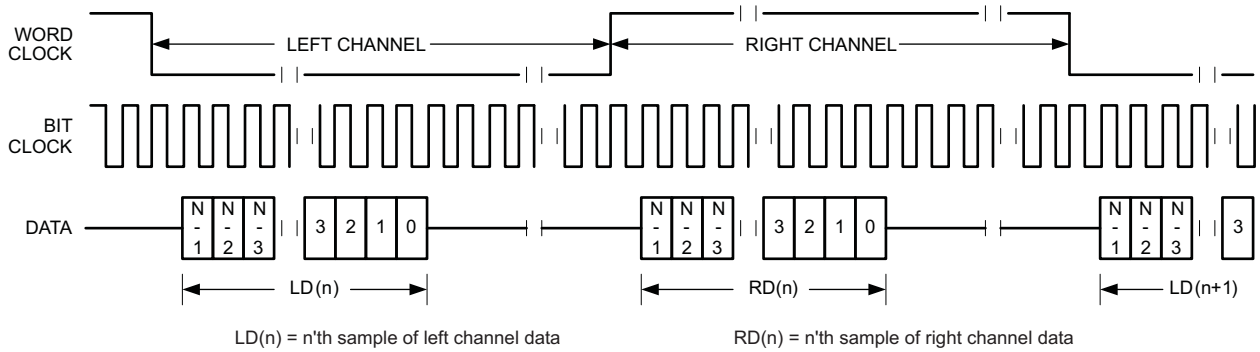


图 36. Timing Diagram for I^2S Mode with ASI_OFFSET1 = 0 and Inverted Bit Clock

For I^2S mode, the number of bit-clocks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

9.4.1.2 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

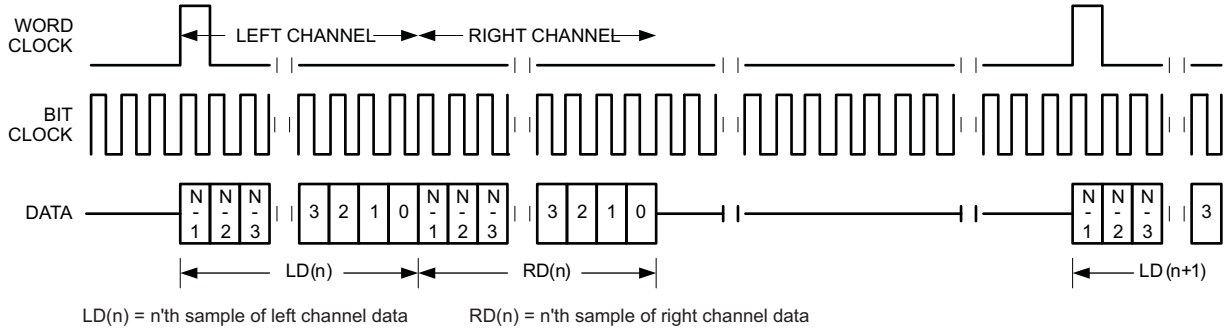


图 37. Timing Diagram for DSP Mode

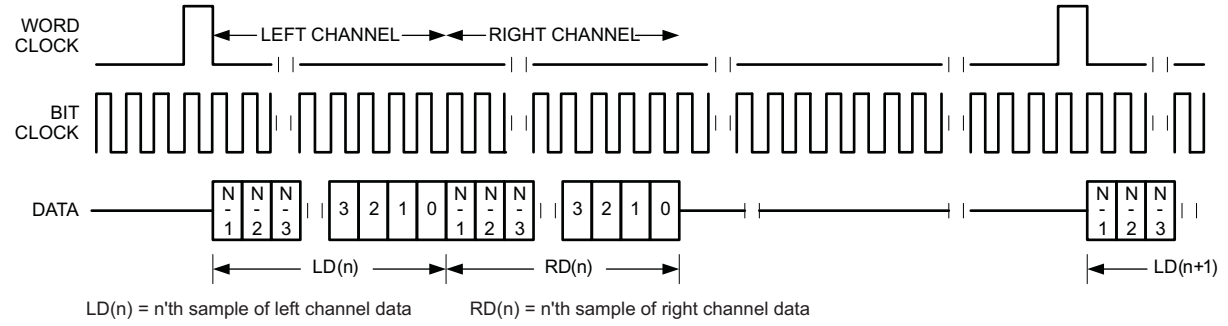


图 38. Timing Diagram for DSP Mode with ASI_OFFSET1=1

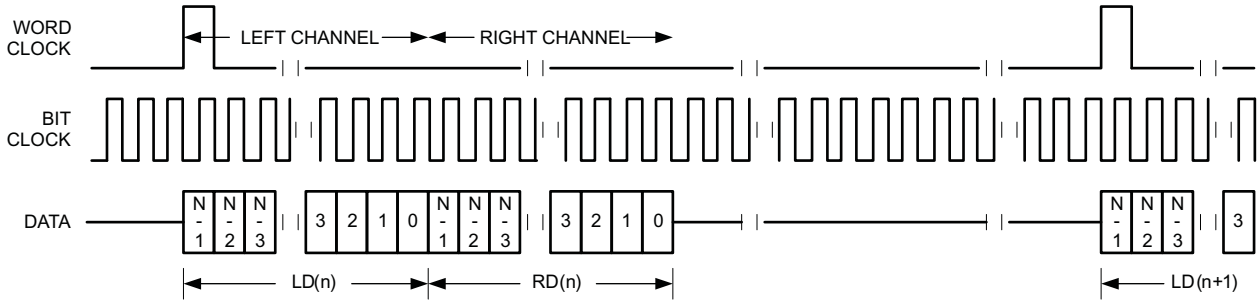


图 39. Timing Diagram for DSP Mode with ASI_OFFSET1=0 and Inverted Bit Clock

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

9.4.1.3 DSP Time Slot Mode

In addition the TAS2560 support DSP Time slot mode. The ASI_OFFSET_2 register allows us to place the right channel anywhere in the frame after the left channel. By utilizing Time Slot Mode, the individual left and right channels can be grouped together, as shown in 图 40. Assuming each channel contains N bits in this example to capture the left and right of channel 1 set a value off ASI_OFFSET_1=0 and ASI_OFFSET2=M*N.

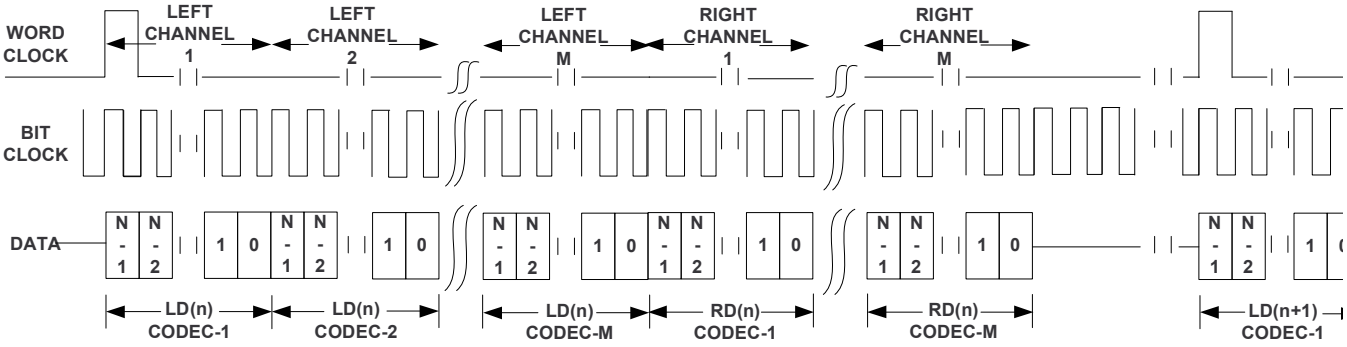


图 40. DSP Timing for Multiple Devices Interfaced Together, Grouped Left Channels and Right Channels

表 44. ASI OFFSET1

ASI_OFFSET_2 (ASI_OFFSET2)	BCLKs from end of left channel data channel
0x00	0 (default)
0x01	1
0x02	2
...	...
0xFF	255

9.4.1.4 Right-Justified Mode (RJF)

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

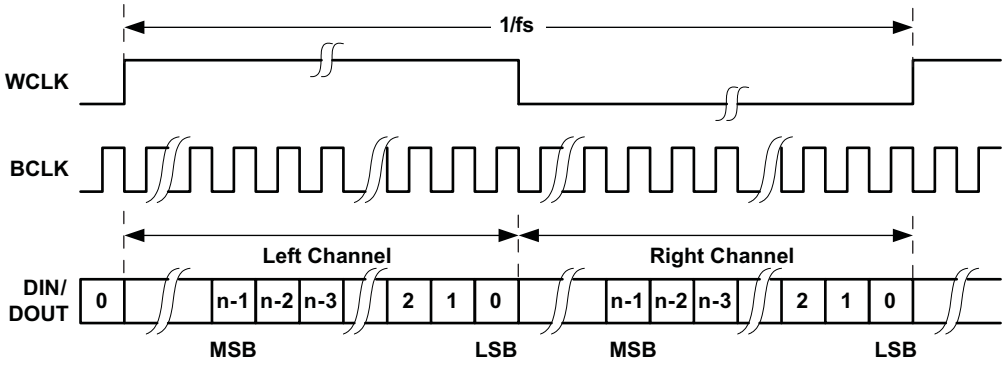


图 41. Timing Diagram for Right-Justified Mode

For right-justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

9.4.1.5 Left-Justified Mode (LJF)

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

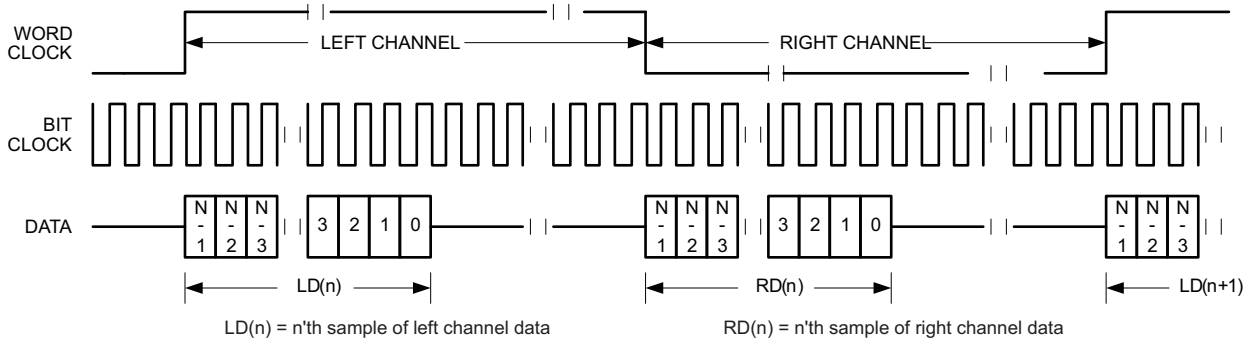


图 42. Timing Diagram for Left-Justified Mode

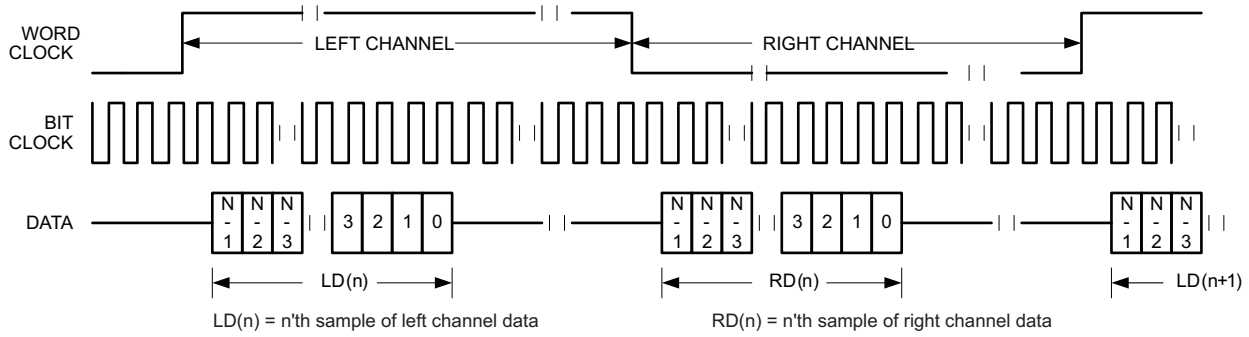


图 43. Timing Diagram for Light-Left Mode with ASI_OFFSET1 = 1

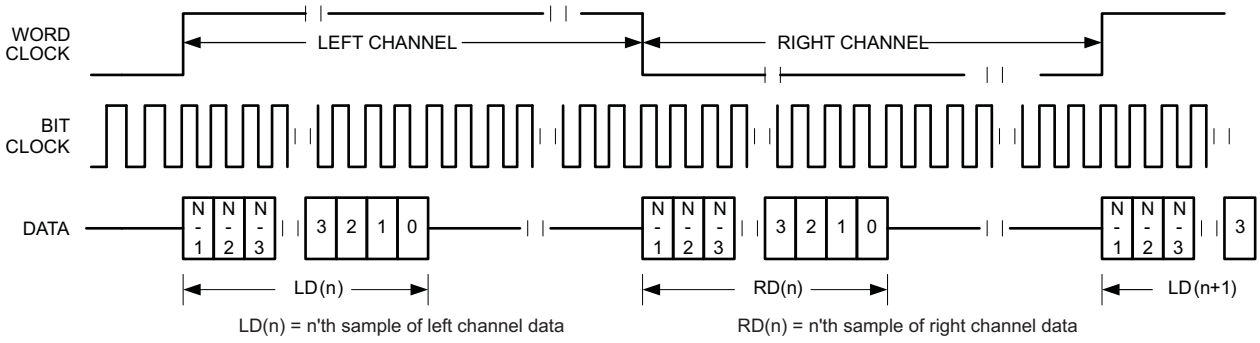


图 44. Timing Diagram for Left-Justified Mode with ASI_OFFSET1 = 0 and Inverted Bit Clock

For left-justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

9.4.1.6 Mono PCM Mode

In mono PCM mode, the rising edge of the word clock starts the data transfer of the single channel of data. Each data bit is valid on the falling edge of the bit clock.

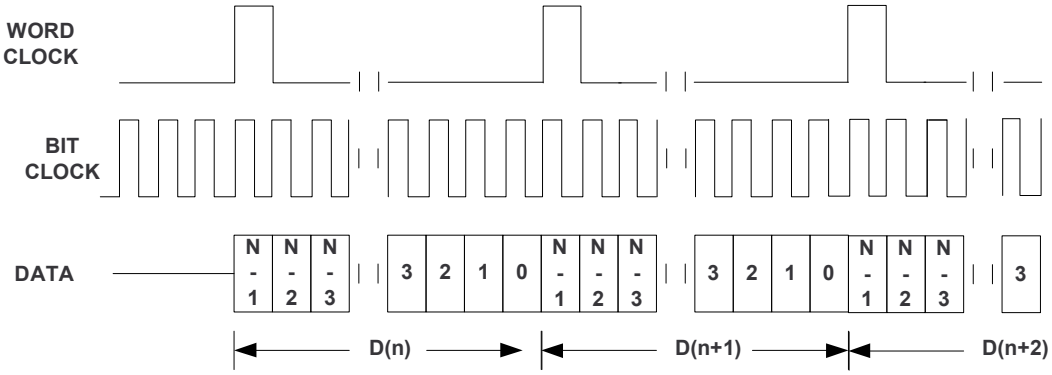


图 45. Timing Diagram for Mono PCM Mode

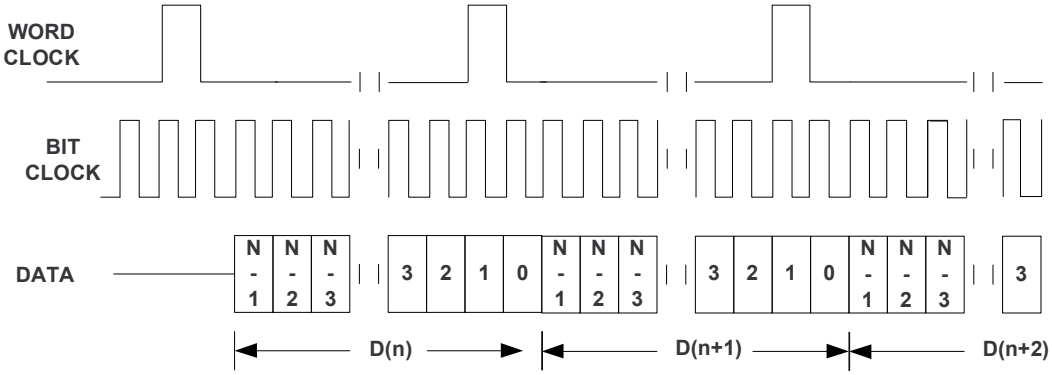


图 46. Timing Diagram for Mono PCM Mode with ASI_OFFSET1=2

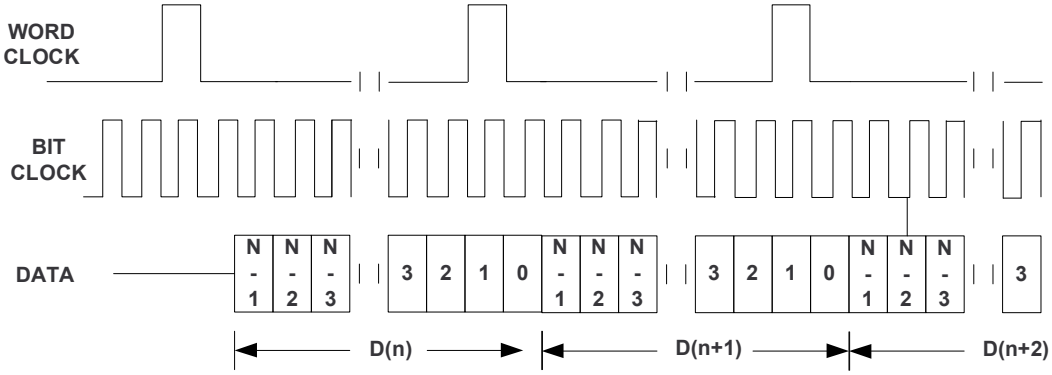


图 47. Timing Diagram for Mono PCM Mode with ASI_OFFSET1=2 and Bit Clock Inverted

For mono PCM mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

9.4.1.7 Stereo Application Example - TDM Mode

Time-division multiplexing (TDM) is required for two or more devices to share a common DIN connection and a common DOUT connection. Using TDM mode, all devices transmit their DOUT data in user-specified sub-frames within one WCLK period. When one device transmits its DOUT information, the other devices place their DOUT terminals in a high impedance tri-state mode. The host processor can operate in I^2S mode while the TAS2560 is running in I^2S TDM mode to support sharing of the same DOUT line.

TDM mode is useable with I^2S, LJF, RJF, and DSP interface modes. Refer to the respective sections for a description of how to set the TAS2560 into those modes.

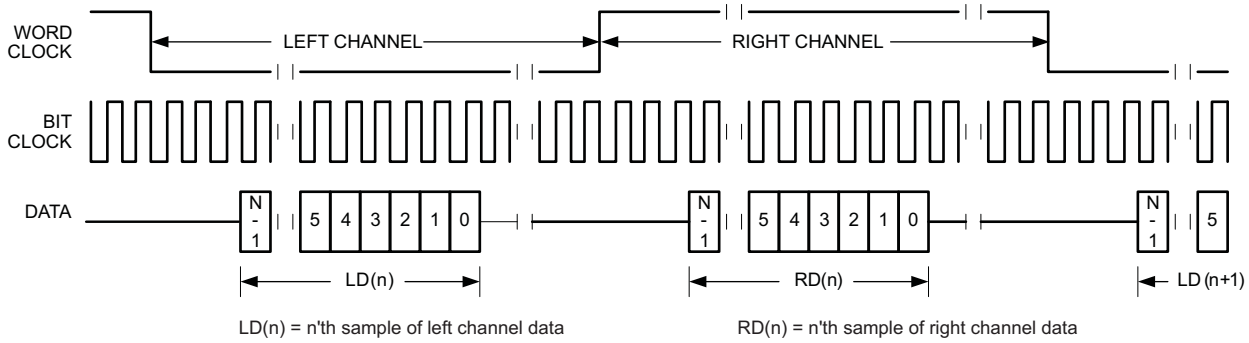


图 48. Timing Diagram for I^2S in TDM Mode with ASI_OFFSET1=2

For TDM mode, the number of bit-clocks per frame should be less than the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

图 49 shows how to connect two TAS2560 for a stereo application.

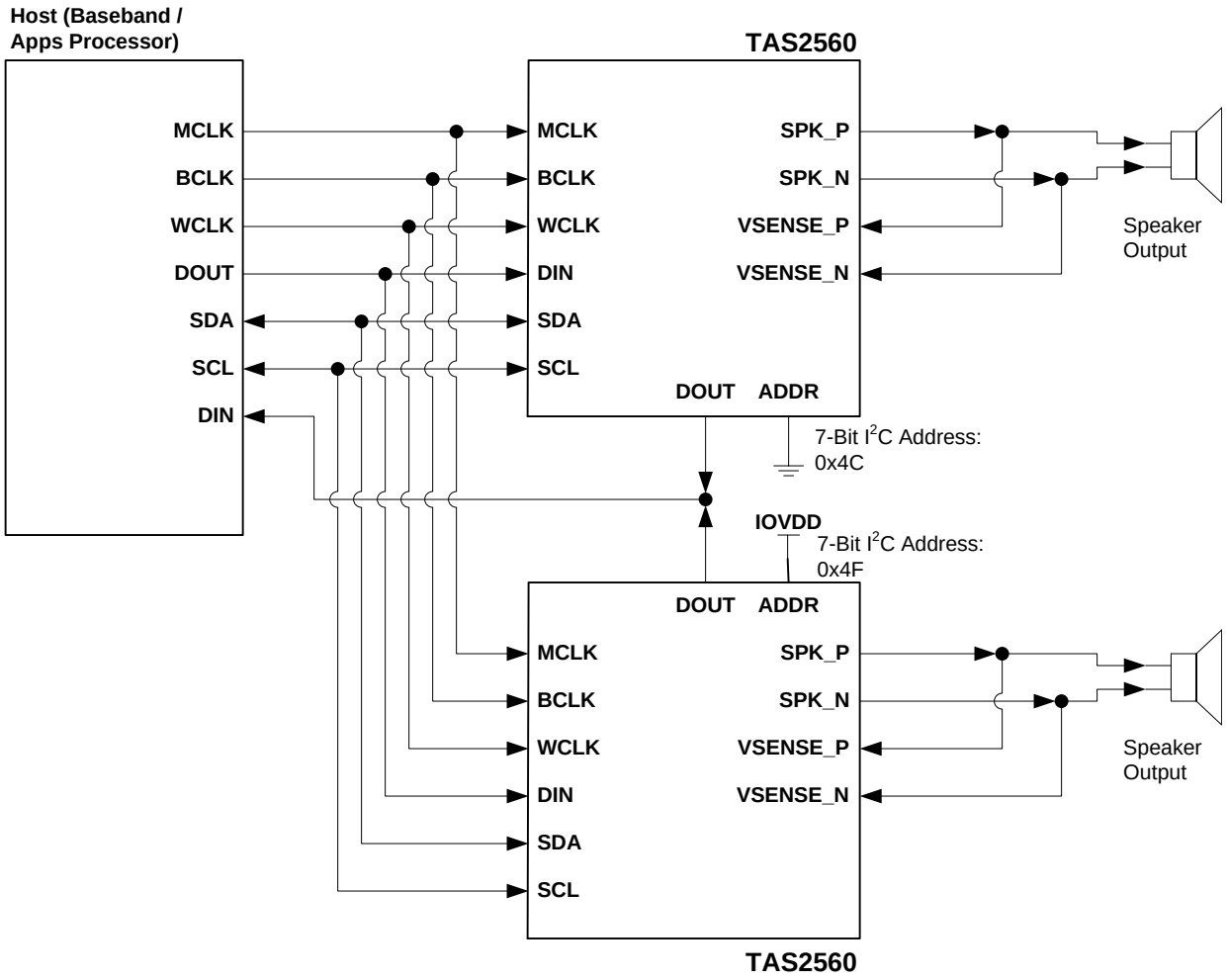


图 49. Stereo Configuration with Two TAS2560 DOUT Muxed in TDM Mode

9.4.2 PDM MODE

When the TAS2560 is running in operating Mode 3 - PCM input playback + PDM IVsense output,Mode 4 - PDM input playback only, or Mode 5 - PDM input playback + PDM IVsense output the Pulse Density Modulation (PDM) interface is used and accepts Double-Date Rate (DDR) PDM stream. In PDM mode a modulated signal is applied to DIN pin. The TAS2560 PDM can be configured in a master or slave mode of operation. In master mode operation the BCLK pin will supply a clock generated from the internal clocking block at 8 times the sampling rate(see 表 5). In master mode another clock must be supplied to drive the TAS2560 internal PLL for generation of all internal clocks. In slave mode the input clock should be supplied. The PDM clock should be 8 times the audio sampling rate (PDMCLK=8*Fs) for proper operation. When PDM input clock mode (表 46) is set to slave mode, PDM slave mode intput clock divider power (表 48) needs to be set to be powered up. Similarly, when PDM output clock mode (表 47) is set to slave mode, PDM slave mode output clock divider power (表 49) needs to be set to powered up.

The Isense and Vsense data is returned on pin DOUT as a DDR PDM stream when operating in Mode 3 - PCM input playback + PDM IVsense output or Mode 5 - PDM input playback + PDM IVsense output. In these modes the Isense data is clocked out during the rising channel and the Vsense data during the falling channel of the PDM clock. Only mono PDM input data is accepted and PDM intput data edge (表 45) is used to select the clock edge or audio channel.

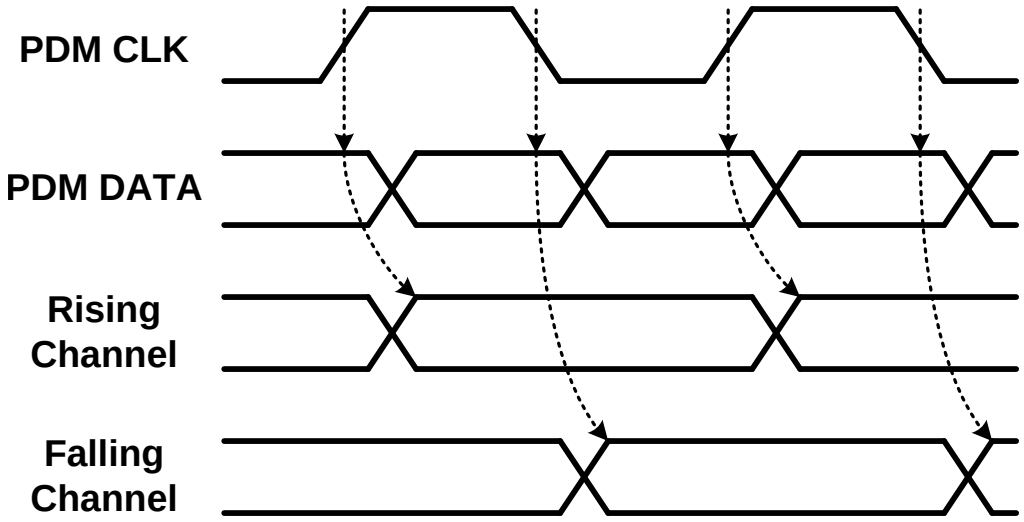


图 50. PDM DDR Waveform

表 45. PDM Input Data Edge

PDM_CFG[2] (PDM_CLK_E)	PDM Data Channel
0	Rising edge (default)
1	Falling edge

表 46. PDM Input Clock Mode

PDM_CFG[1] (PDM_CI_M)	PDM Input Clock
0	Slave - input (default)
1	Master - output

表 47. PDM Output Clock Mode

PDM_CFG[0] (PDM_CO_M)	PDM Output Clock
0	Slave - input (default)
1	Master - output

表 48. PDM Slave Mode Input Clock Divider Power

PDM_DIV[7] (PDM_DIV_P)	PDM Slave Mode Input Clock Divider Power
0	Powered Down (default)
1	Powered Up

表 49. PDM Slave Mode Output Clock Divider Power

DSD_DIV[7] (PDM_DSD_P)	PDM Slave Mode Output Clock Divider Power
0	Powered Down (default)
1	Powered Up

9.5 Operational Modes

9.5.1 Hardware Shutdown

The device enters hardware shutdown mode if the RESETZ pin is asserted low. In hardware shutdown mode, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers loose state in this mode and I^2C communication is disabled.

If RESETZ is asserted low while audio is playing, the device immediately stop operation and enter hardware shutdown mode. This may result in pops or clicks. It is recommend to first enter software shutdown before entering hardware shutdown.

When RESETZ is released, the device will enter software shutdown. A power up sequence such as Device Power Up and Un-mute Sequence 8Ω load with the appropriate mode selected should be executed to exist shutdown in the desired mode of operation.

9.5.2 Software Shutdown

Software shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to loose register state. Software shutdown is enabled by following Mute and Device Power Down Sequence sequence.

9.5.3 Low Power Sleep

The device has a low power sleep (表 50) mode option to reduce the power consumption on analog supply VBAT. In order to use this operating mode the VBAT supply should remain powered up when in this mode. This mode disables the Power-on Reset connected to the VBAT supply reducing current consumption.

表 50. Low Power Sleep

LOW_PWR_MODE[7] (VBAT_POR)	Low Power Sleep Mode
0	Disabled (default)
1	Enabled - VBAT POR shutdown

9.5.4 Software Reset

The TAS2560 internal logic must be initialized to a known condition for proper device function by doing a software reset. Performing software reset after a hardware reset is mandatory for reliable device boot up. A software reset can be accomplished by asserting 表 51 bit, which is self clearing. This will restore all registers to their default values. After software reset is performed, no register read/write should be performed within 100us while initialization sequence occurs.

表 51. Software Reset

RESET[0] (RESET)	Action
0	Don't reset (default)
1	Reset(Self clearing)

9.5.5 Device Processing Modes

The TAS2560 can be initialized into one of five modes after a. These modes have should be correctly selected based on audio input and output formats and the need for IV-sense at the speaker terminals. The advanced processing features such as Battery Guard, thermal fold-back, brownout, and boost mode can be configured using PurePath™ Console 3 Software TAS2560 Application.

表 52. Device Power Mode

BOOT_MODE[3:0] (DSP_MODE)	Operating Mode
0000	Reserved
0001	Mode 1 - PCM input playback only(default)
0010	Mode 2 - PCM input playback + PCM IVsense output
0011	Mode 3 - PCM input playback + PDM IVsense output

表 52. Device Power Mode (接下页)

BOOT_MODE[3:0] (DSP_MODE)	Operating Mode
0100	Mode 4 - PDM input playback only
0101	Mode 5 - PDM input playback + PDM IVsense output

Once the mode is selected the system is powered up using field PWR_DEV. The mode should only be selected when the device is powered down PWR_DEV = 00b. Additionally, if a system fault occurs, see Fault Protection, and the system is configured to shutdown instead of auto-retry the device will enter power state powered down (PWR_DEV=00b).

表 53. Device Power Mode

PWR_CTRL_1[7:6] (PWR_DEV)	Device Power State
00	Powered down (default)
01	Powered up with boost
10	Powered up without boost
11	Reserved

9.5.5.1 Mode 1 - PCM input playback only

Mode 1 configures the part as a digital input only amplifier and is the lowest power mode. This mode can be used to play a known power up audio sequence before the rest of the audio system software is loaded. The mode provides fault protection, brownout protection volume control, and Class-H controller. With minimal additional configuration the Battery Guard can be enabled. The I/V sense ADC are powered down to minimize power consumption.

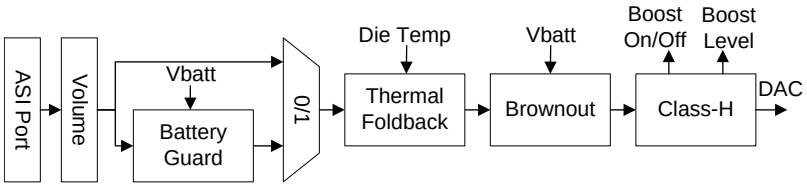


图 51. Mode 1 Processing Block Diagram

A MCLK is needed in this mode if the BCLK is less than 1MHz. If BCLK and WCLK are configured for output then MCLK is taken as the input root clock.

表 54. Pin Use Matrix Mode 1

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
BCLK	WCLK	DIN	NA	MCLK	NA	IRQ

9.5.5.2 Mode 2 - PCM input playback + PCM IVsense output

Mode 2 is similar to Mode 1 except the I/V sense ADCs are powered up and the data is routed back on the L/R return channels of the ASI port. This mode can be used to return the I/V data to the host to perform computations on the speaker I/V measurements such as speaker protection.

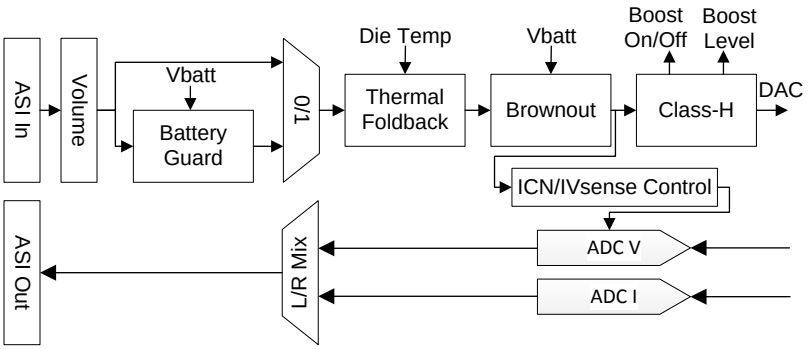


图 52. Mode 2 Processing Block Diagram

A MCLK is needed in this mode if the BCLK is less than 1MHz. If BCLK and WCLK are configured for output then MCLK is also required for proper internal clocking.

表 55. Pin Use Matrix Mode 2

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
BCLK	WCLK	DIN	DOUT	MCLK	NA	IRQ

9.5.5.3 Mode 2 96k

Mode 2 96k is similar to Mode 2 except battery guard, brownout, and class-H is not supported at this sampling rate.

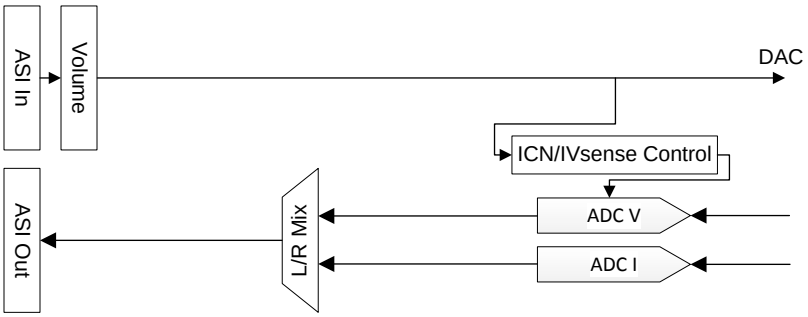


图 53. Mode 2 96k Processing Block Diagram

A MCLK is needed in this mode if the BCLK is less than 1MHz. If BCLK and WCLK are configured for output then MCLK is also required for proper internal clocking.

表 56. Pin Use Matrix Mode 2 96k

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
BCLK	WCLK	DIN	DOUT	MCLK	NA	IRQ

9.5.5.4 Mode 3 - PCM input playback + PDM IVsense output

Mode 3 supports I^2S/TDM in playback and returns IV sense on PDM output.

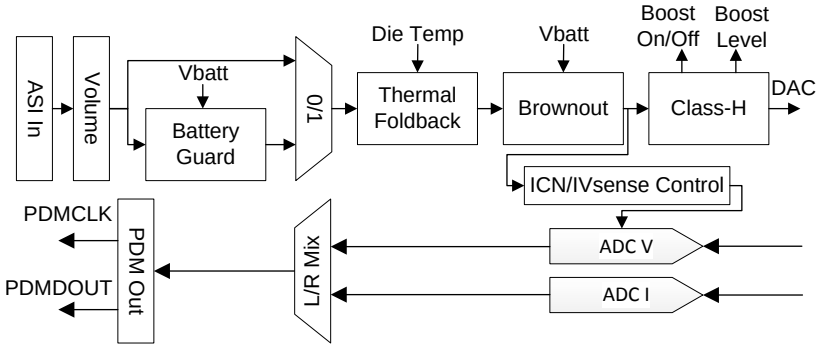


图 54. Mode 3 Processing Block Diagram

A MCLK is needed in this mode if the BCLK or PDMCLK operating in input mode is less than 1MHz. If BCLK and PDMCLK are configured for output then MCLK is also required for proper internal clocking.

表 57. Pin Use Matrix Mode 3

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
BCLK	WCLK	DIN	PDMDOUT	MCLK	PDMCLK	IRQ

9.5.5.5 Mode 4 - PDM input playback only

Mode 4 supports PDM in playback only.

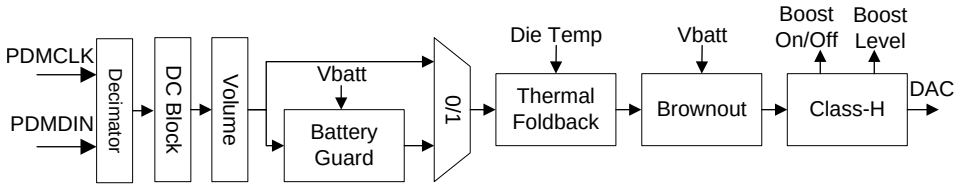


图 55. Mode 4 Processing Block Diagram

If PDMCLK is an output or and input at a clock frequency of less than 1MHz then a separate MCLK is required to provide proper internal clocking.

表 58. Pin Use Matrix Mode 4

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
PDMCLK	NA	PDMDIN	NA	MCLK	NA	IRQ

9.5.5.6 Mode 5 - PDM input playback + PDM IVsense output

Mode 5 supports PDM playback with IV sense on PDM output.

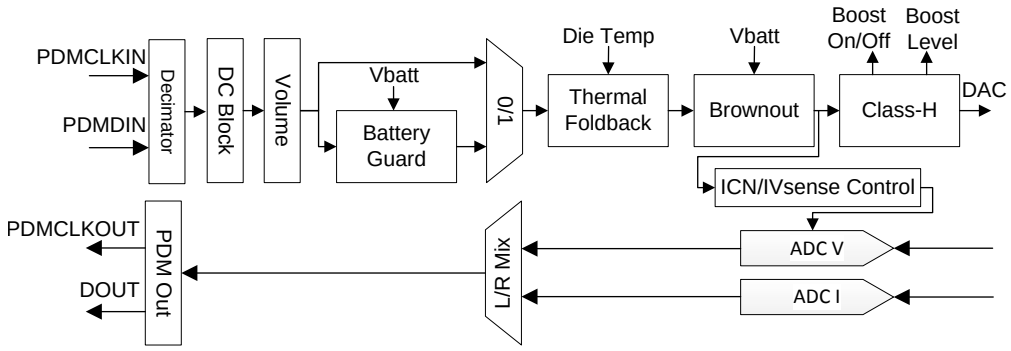


图 56. Mode 5 Processing Block Diagram

If either PDMCLKIN or PDMCLKOUT is an input and greater than 1MHz MCLK is not require. If both are output or less that 1MHz clock rate then a separate MCLK needs to be provided for proper internal clocking.

表 59. Pin Use Matrix Mode 5

BCLK	WCLK	DIN	DOUT	MCLK	PDMCLK	IRQ
PDMCLKIN	NA	PDMDIN	PDMDOUT	MCLK	PDMCLKOUT	IRQ

9.6 Programming

While the below scripts are provided as configuration examples, it is recommended to use PurePath™ Console 3 Software TAS2560 Application software to generate the device configuration files. This software contains configuration checks to ensure proper settings are used in the device for various cases and loaded the needed fixed-function DSP patches.

9.6.1 Device Power Up and Un-mute Sequence 8Ω load

The following code example provide the correct sequence including patch to power up the device, unmute and mute, and provide a clean power-down. The PurePath™ Console 3 Software TAS2560 Application software will create output files with the most updated patch commands. The following is a example of powering up the part in DSP Mode 2 with proper sequencing.

```
Example script (Power up Mode 2 and Unmute):
#############################################################################################
i i2cstd
#mclk expected is 12.288 MHz
#configuring device registers for 8 ohm speaker load
############################   DEVICE INIT SEQ START#################################################
w 98 00 00  #Page-0
w 98 7f 00  #Book-0
w 98 01 01  #Software reset (PAGE0_REG1)

d 1        #Required=50e-6  #wait time for OTP-
One Time Programmable memory values to be transferred to device

##### INIT SECTION START
w 98 49 0c
w 98 3c 33
##### INIT SECTION END

##### DSP PROG SETTING START
w 98 02 02  # operate device in dev mode 2
w 98 21 00 #disable clock error detection
w 98 08 81 # SSM enabled
##### DSP PROG SETTING END

############################   DEVICE INIT SEQ END ##################################################
```

Programming (接下页)

```
###################    CHANNEL POWER UP    ######################################################
w 98 07 41 #power up device mute class d
#############################################################################################

##### DSP patch
d 10
w 98 00 32
w 98 28 7F FB B5 00
w 98 2c 80 04 4c 00
w 98 30 7F F7 6A 00
w 98 1c 7F Ff ff ff
w 98 20 00 00 00 00
w 98 24 00 00 00 00
w 98 00 3
w 98 18 04 cc cc cc
w 98 00 00
##### DSP patch update END

w 98 07 40 #power up device unmute class d

## optional(ending the script in B0_P0)
w 98 00 00 # page 0
w 98 7f 00 # book 0
########################################
```

Programming (接下页)

9.6.2 Device Power Up and Un-mute Sequence 4Ω or 6Ω load

The following code examples provide the correct sequence including patch to power up the device, unmute and mute, and provide a clean power-down. The PurePath™ Console 3 Software TAS2560 Application software will create output files with the most updated patch commands. The following sequence is a example of powering up the part in DSP Mode 2 with proper sequencing.

```
Example script (Power up Mode 2 and Unmute):
#################################################################################################
i i2cstd
#mclk expected is 12.288 MHz
#configuring device registers for 8 ohm speaker load
############################   DEVICE INIT SEQ START#################################################
w 98 00 00  #Page-0
w 98 7f 00  #Book-0
w 98 01 01  #Software reset (PAGE0_REG1)

d 1        #Required=50e-6  #wait time for OTP-
One Time Programmable memory values to be transferred to device

##### INIT SECTION START
w 98 49 0c
w 98 3c 33
w 98 09 93 # 4-ohm load setting
#w 98 09 8B # 6-ohm load setting
##### INIT SECTION END

##### DSP PROG SETTING START
w 98 02 02  # operate device in dev mode 2
w 98 21 00 #disable clock error detection
w 98 08 81 # SSM enabled
##### DSP PROG SETTING END

############################   DEVICE INIT SEQ END ##################################################

###################    CHANNEL POWER UP    ###################################################
w 98 07 41 #power up device mute class d
#################################################################################################

##### DSP patch
d 10
w 98 00 32
w 98 28 7F FB B5 00
w 98 2c 80 04 4c 00
w 98 30 7F F7 6A 00
w 98 1c 7F Ff ff ff
w 98 20 00 00 00 00
w 98 24 00 00 00 00
w 98 00 33
w 98 10 6f 5c 28 f5
w 98 14 67 ae 14 7a
w 98 20 1c 00 00 00
w 98 24 1f 0a 3d 70
w 98 28 22 14 7a e1
w 98 2c 25 1e b8 51
w 98 30 28 28 f5 c2
w 98 34 2b 33 33 33
w 98 38 2e 3d 70 a3
w 98 3c 31 47 ae 14
w 98 00 33
w 98 18 06 66 66 66
w 98 00 34
w 98 34 3a 46 74 00
w 98 38 22 f3 07 00
w 98 3c 80 77 61 00
w 98 40 22 a7 cc 00
w 98 44 3a 0c 93 00
w 98 00 00
##### DSP patch update END

w 98 07 40 #power up device unmute class d
```

Programming (接下页)

```
## optional(ending the script in B0_P0)
w 98 00 00 # page 0
w 98 7f 00 # book 0
########################################
```

9.6.3 Mute and Device Power Down Sequence

The following code example provide the correct sequence to power down the device into software shutdown. The PurePath™ Console 3 Software TAS2560 Application software will create output files with these commands.

```
Example script (Mute / Software Shutdown):
#################################################################################################
i i2cstd

###################    CHANNEL POWER DOWN ########################################################
w 98 00 00  #Page-0
w 98 7f 00  #Book-0
###################    CHANNEL POWER UP    ########################################################
w 98 07 41 #power up device mute class d
#################################################################################################
w 98 01 01 # software reset
```

9.7 Register Map

See the General I²C Operation section for more details on addressing. Register settings should be set based on the files generated from the PPC3 GUI. Because the TAS2560 is a complex system including the internal software, changes made in the TAS2560 registers not known in the PPC3 generated configurations can result in the speaker protection not operating correctly. Changes should be made from within *PurePath™ Console 3 Software TAS2560 Application* instead of manually changing registers when possible. New configuration files can be generated from PPC3 to prevent invalid configurations.

9.7.1 Register Map Summary

9.7.1.1 Register Summary Table

Addr	Register	Description	Section
0x00	PAGE	Page Select	PAGE (book=0x00 page=0x00 address=0x00) [reset=0h]
0x01	RESET	Software Reset	RESET (book=0x00 page=0x00 address=0x01) [reset=0h]
0x02	MODE	Mode Control	MODE (book=0x00 page=0x00 address=0x02) [reset=1h]
0x04	SPK_CTRL	Speaker Control	SPK_CTRL (book=0x00 page=0x00 address=0x04) [reset=5Fh]
0x05	PWR_CTRL_2	Power Up Control 2	PWR_CTRL_2 (book=0x00 page=0x00 address=0x05) [reset=0h]
0x07	PWR_CTRL_1	Power Up Control 1	PWR_CTRL_1 (book=0x00 page=0x00 address=0x07) [reset=0h]
0x08	RAMP_CTRL	Class	RAMP_CTRL (book=0x00 page=0x00 address=0x08) [reset=1h]
0x09	EDGE_ISNS_BOOST	Edge Rate, Isense Scale, Boost limit	EDGE_ISNS_BOOST (book=0x00 page=0x00 address=0x09) [reset=83h]
0x0F	PLL_CLKIN	PLL Clock Input Control	PLL_CLKIN (book=0x00 page=0x00 address=0x0F) [reset=41h]
0x10	PLL_JVAL	PLL J Multiplier Control	PLL_JVAL (book=0x00 page=0x00 address=0x10) [reset=4h]
0x11	PLL_DVAL_1	PLL Fractional Multiplier D Val MSB	PLL_DVAL_1 (book=0x00 page=0x00 address=0x11) [reset=0h]
0x12	PLL_DVAL_2	PLL Fractional Multiplier D Val LSB	PLL_DVAL_2 (book=0x00 page=0x00 address=0x12) [reset=0h]
0x14	ASI_FORMAT	ASI Mode Control	ASI_FORMAT (book=0x00 page=0x00 address=0x14) [reset=2h]
0x15	ASI_CHANNEL	ASI Channel Control	ASI_CHANNEL (book=0x00 page=0x00 address=0x15) [reset=0h]
0x16	ASI_OFFSET_1	ASI Offset	ASI_OFFSET_1 (book=0x00 page=0x00 address=0x16) [reset=0h]
0x17	ASI_OFFSET_2	ASI Offset Second Slot	ASI_OFFSET_2 (book=0x00 page=0x00 address=0x17) [reset=0h]
0x18	ASI_CFG_1	ASI Configuration	ASI_CFG_1 (book=0x00 page=0x00 address=0x18) [reset=0h]
0x19	ASI_DIV_SRC	ASI BDIV Clock Input	ASI_DIV_SRC (book=0x00 page=0x00 address=0x19) [reset=0h]
0x1A	ASI_BDIV	ASI BDIV Configuration	ASI_BDIV (book=0x00 page=0x00 address=0x1A) [reset=1h]
0x1B	ASI_WDIV	ASI WDIV Configuration	ASI_WDIV (book=0x00 page=0x00 address=0x1B) [reset=40h]
0x1C	PDM_CFG	PDM Configuration	PDM_CFG (book=0x00 page=0x00 address=0x1C) [reset=0h]
0x1D	PDM_DIV	PDM Divider Configuration	PDM_DIV (book=0x00 page=0x00 address=0x1D) [reset=8h]
0x1E	DSD_DIV	DSD Divider Configuration	DSD_DIV (book=0x00 page=0x00 address=0x1E) [reset=8h]
0x21	CLK_ERR_1	Clock Error and DSP memory Reload	CLK_ERR_1 (book=0x00 page=0x00 address=0x21) [reset=3h]
0x22	CLK_ERR_2	Clock Error Configuration	CLK_ERR_2 (book=0x00 page=0x00 address=0x22) [reset=3Fh]
0x23	IRQ_PIN_CFG	Interrupt Pin Configuration	IRQ_PIN_CFG (book=0x00 page=0x00 address=0x23) [reset=21h]
0x24	INT_CFG_1	Interrupt Configuration 1	INT_CFG_1 (book=0x00 page=0x00 address=0x24) [reset=0h]
0x25	INT_CFG_2	Interrupt Configuration 2	INT_CFG_2 (book=0x00 page=0x00 address=0x25) [reset=0h]
0x26	INT_DET_1	Interrupt Detected 1	INT_DET_1 (book=0x00 page=0x00 address=0x26) [reset=0h]
0x27	INT_DET_2	Interrupt Detected 2	INT_DET_2 (book=0x00 page=0x00 address=0x27) [reset=0h]

Register Map (continued)

0x2A	STATUS_POWER	Status Block Power	STATUS_POWER (book=0x00 page=0x00 address=0x2A) [reset=0h]
0x2D	SAR_VBAT_MSB	SAR VBAT Measurement MSB	SAR_VBAT_MSB (book=0x00 page=0x00 address=0x2D) [reset=C0h]
0x2E	SAR_VBAT_LSB	SAR VBAT Measurement LSB	SAR_VBAT_LSB (book=0x00 page=0x00 address=0x2E) [reset=0h]
0x31	DIE_TEMP_SENSOR	Die Temperature Sensor	DIE_TEMP_SENSOR (book=0x00 page=0x00 address=0x31) [reset=0h]
0x35	LOW_PWR_MODE	Low Power Configuration	LOW_PWR_MODE (book=0x00 page=0x00 address=0x35) [reset=0h]
0x36	PCM_RATE	PCM Sample Rate	PCM_RATE (book=0x00 page=0x00 address=0x36) [reset=32h]
0x4F	CLOCK_ERR_CFG_1	Clock Error Configuration 1	CLOCK_ERR_CFG_1 (book=0x00 page=0x00 address=0x4F) [reset=0h]
0x50	CLOCK_ERR_CFG_2	Clock Error Configuration 2	CLOCK_ERR_CFG_2 (book=0x00 page=0x00 address=0x50) [reset=11h]
0x58	PROTECTION_CFG_1	Class	PROTECTION_CFG_1 (book=0x00 page=0x00 address=0x58) [reset=3h]
0x7E	CRC_CHECKSUM	Checksum	CRC_CHECKSUM (book=0x00 page=0x00 address=0x7E) [reset=0h]
0x7F	BOOK	Book Selection	BOOK (book=0x00 page=0x00 address=0x7F) [reset=0h]

9.7.2 PAGE (book=0x00 page=0x00 address=0x00) [reset=0h]

Selects the page for the next read or write.

Figure 57. PAGE Register Address: 0x00

7	6	5	4	3	2	1	0
PAGE[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. Page Select Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Selects the Register Page for the next read or write command

9.7.3 RESET (book=0x00 page=0x00 address=0x01) [reset=0h]

Controls the software reset

Figure 58. RESET Register Address: 0x01

7	6	5	4	3	2	1	0
Reserved							RESET
R-0h							RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. Software Reset Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0h	Reserved
0	RESET	RW	0h	0 = Don't care 1 = Self clearing software reset

9.7.4 MODE (book=0x00 page=0x00 address=0x02) [reset=1h]

Controls the mode of the part

Figure 59. MODE Register Address: 0x02

7	6	5	4	3	2	1	0
AUTOPAGE	Reserved				DSP_MODE[2:0]		
RW-0h	RW-0h				RW-1h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. Mode Control Field Descriptions

Bit	Field	Type	Reset	Description
7	AUTOPAGE	RW	0h	0 Enable page auto increment for memory mapped registers 1 Self clearing software reset
6-3	Reserved	RW	0h	Reserved
2-0	DSP_MODE[2:0]	RW	1h	0 = Reserved 1 = PCM input playback only 2 = PCM input playback + PCM IV out 3 = PCM input playback + PDM IV out 4 = PDM input playback only 5 = PDM input playback + PDM IV out 6 = Reserved

9.7.5 SPK_CTRL (book=0x00 page=0x00 address=0x04) [reset=5Fh]

Configure the boost mode and DAC gain

Figure 60. SPK_CTRL Register Address: 0x04

7	6	5	4	3	2	1	0
BST_OFFDLY[1:0]		BST_PRE	BST_MODE	DAC_GAIN[3:0]			
RW-1h		RW-0h	RW-1h	RW-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. Speaker Control Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_OFFDLY[1:0]	RW	1h	0 = Reserved 1 = Reserved 2 = Reserved
5	BST_PRE	RW	0h	0 = Reserved
4	BST_MODE	RW	1h	0 = Class H - multi-level boost mode. In this mode the boost voltage will track the signal. It will result in higher inrush current from VBATT. 1 = Class -G boost mode. When the boost is needed it will turn on to the maximum boost voltage.
3-0	DAC_GAIN[3:0]	RW	Fh	DAC gain is 0 = 0db 1 = 1db 2 = 2db ... 14 = 14db 15 = 15db

9.7.6 PWR_CTRL_2 (book=0x00 page=0x00 address=0x05) [reset=0h]

This register controls device power up

Figure 61. PWR_CTRL_2 Register Address: 0x05

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		PWR_ERR
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h		RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. Power Up Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	Reserved	RW	0h	Reserved
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3	Reserved	RW	0h	Reserved
2-1	Reserved	RW	0h	Reserved
0	PWR_ERR	RW	0h	Reserved 0 = No error condition 1 = Error condition detected

9.7.7 PWR_CTRL_1 (book=0x00 page=0x00 address=0x07) [reset=0h]

This register controls device power up

Figure 62. PWR_CTRL_1 Register Address: 0x07

7	6	5	4	3	2	1	0
PWR_DEV[1:0]		Reserved	Reserved	Reserved	MUTE_ISNS	MUTE_VSNS	MUTE_AUDIO
RW-0h		RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. Power Up Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PWR_DEV[1:0]	RW	0h	Controls the device power state. If a fault is detected that powers the device down the state will be reflected in this register. 0 = Device is powered down 1 = Power up device with boost 2 = Power up device without boost 3 = Reserved
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3	Reserved	RW	0h	Reserved
2	MUTE_ISNS	RW	0h	Isense is 0 = Unmuted 1 = Muted
1	MUTE_VSNS	RW	0h	Vsense D is 0 = Unmuted 1 = Muted
0	MUTE_AUDIO	RW	0h	Audio playback (pop-free) is 0 = Unmuted 1 = Muted

9.7.8 RAMP_CTRL (book=0x00 page=0x00 address=0x08) [reset=1h]

D Ramp Control

Figure 63. RAMP_CTRL Register Address: 0x08

7	6	5	4	3	2	1	0
RAMP_MODE[1:0]		RAMP_FREQ[1:0]		Reserved		RAMP_FREQMOD[1:0]	
RW-0h		RW-0h		RW-0h		RW-1h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. Class Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RAMP_MODE[1:0]	RW	0h	The Class-D ramp clock mode 0 = SYNC, generated from digital audio stream 1 = FFM, generated from internal oscillator 2 = SSM, generated from internal oscillator with spread-spectrum 3 = Reserved
5-4	RAMP_FREQ[1:0]	RW	0h	The ramp frequency is 0 = 348kHz (Use for Fs=48ksps and multiples) 1 = 352.8kHz (Use for Fs=44.1ksps and multiples) 2 = Reserved
3-2	Reserved	RW	0h	Reserved
1-0	RAMP_FREQMOD[1:0]	RW	0h	Sets the ramp frequency modulation rate or to a fixed offset. 0 = Reserved 1 = Set the SSM to 5% frequency modulation 2 = Set the SSM to 10% frequency modulation 3 = Reserved

9.7.9 EDGE_ISNS_BOOST (book=0x00 page=0x00 address=0x09) [reset=83h]

Controls edge rate, sense, and boost limits

Figure 64. EDGE_ISNS_BOOST Register Address: 0x09

7	6	5	4	3	2	1	0
EDGE_RATE[2:0]			ISNS_SCALE[1:0]		Reserved	BOOST_ILIM[1:0]	
RW-4h			RW-0h		RW-0h	RW-3h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. Edge Rate, Isense Scale, Boost limit Field Descriptions

Bit	Field	Type	Reset	Description
7-5	EDGE_RATE[2:0]	RW	4h	Set the Class-D output edge rate control to 0 = Reserved 1 = Reserved 2 = 29ns 3 = 25ns 4 = 14ns 5 = 13ns 6 = 12ns 7 = 11ns
4-3	ISNS_SCALE[1:0]	RW	0h	Sets the full-scale value of Isense channel. Should be changed based on the speaker DC impedance R0. 0 = 8ohm, Isense full-scale = 1.25A 1 = 6ohm, Isense full-scale = 1.5A 2 = 4ohm, Isense full-scale = 1.75A 3 = Reserved
2	Reserved	RW	0h	Reserved
1-0	BOOST_ILIM[1:0]	RW	3h	Sets the boost current limit to 0 = 1.5A 1 = 2A 2 = 2.5A 3 = 3A

9.7.10 PLL_CLKIN (book=0x00 page=0x00 address=0x0F) [reset=41h]

PLL Clock Input Control

Figure 65. PLL_CLKIN Register Address: 0x0F

7	6	5	4	3	2	1	0
PLL_CLK_SRC[1:0]		PLL_P_DIV[5:0]					
RW-1h		RW-1h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 68. PLL Clock Input Control Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PLL_CLK_SRC[1:0]	RW	1h	PLL Clock Input Source. PLL CLKIN is from 0 = BCLK 1 = MCLK 2 = PDMCLK
5-0	PLL_P_DIV[5:0]	RW	1h	The PLL_CLKIN divider ration that generated the input clock for the PLL P-divider is 0 = 64 1 = 1 2 = 2 ... 62 = 62 63 = 63

9.7.11 PLL_JVAL (book=0x00 page=0x00 address=0x10) [reset=4h]

PLL J Multiplier Control

Figure 66. PLL_JVAL Register Address: 0x10

7	6	5	4	3	2	1	0
PLL_LOWF	PLL_MULT_J[6:0]						
RW-0h	RW-4h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 69. PLL J Multiplier Control Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL_LOWF	RW	0h	This value should be set based on the output frequency of the PLL CLK_DIV register. It should be set based on this frequency being equal to and greater than 1MHz or less than 1 MHz 0 = If the PLL_CLKIN is equal to or greater than 1MHz 1 = If the PLL_CLKIN is less than 1MHz
6-0	PLL_MULT_J[6:0]	RW	4h	The PLL Multiplier J is 0 = Reserved 1 = 1 2 = 2 ... 62 = 62 63 = 63

9.7.12 PLL_DVAL_1 (book=0x00 page=0x00 address=0x11) [reset=0h]

PLL Fractional Multiplier D Val MSB

Figure 67. PLL_DVAL_1 Register Address: 0x11

7	6	5	4	3	2	1	0
Reserved		PLL_MULT_D[13:8]					
RW-0h		RW-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. PLL Fractional Multiplier D Val MSB Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5--8	PLL_MULT_D[13:0]	RW	0h	PLL Fractional Multiplier D[13:8] value bits

9.7.13 PLL_DVAL_2 (book=0x00 page=0x00 address=0x12) [reset=0h]

PLL Fractional Multiplier D Val LSB

Figure 68. PLL_DVAL_2 Register Address: 0x12

7	6	5	4	3	2	1	0
PLL_MULT_D[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. PLL Fractional Multiplier D Val LSB Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL_MULT_D[7:0]	RW	0h	PLL Fractional Multiplier D[7:0] value bits

9.7.14 ASI_FORMAT (book=0x00 page=0x00 address=0x14) [reset=2h]

Configures the Audio Serial Interface mode and word length

Figure 69. ASI_FORMAT Register Address: 0x14

7	6	5	4	3	2	1	0
Reserved			ASI_MODE[2:0]			ASI_LENGTH[1:0]	
RW-0h			RW-0h			RW-2h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. ASI Mode Control Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	RW	0h	Reserved
4-2	ASI_MODE[2:0]	RW	0h	The ASI Input mode format is set to 0 = I2S 1 = DSP 2 = RJF , For non-zero values of ASI_OFFSET1, LJF is preferred 3 = LJF 4 = MonoPCM 5 = TDM (DSP timeslot) 6-15 = Reserved
1-0	ASI_LENGTH[1:0]	RW	2h	Sets the ASI input word-length to 0 = 16bits 1 = 20bits 2 = 24bits 3 = 32bits

9.7.15 ASI_CHANNEL (book=0x00 page=0x00 address=0x15) [reset=0h]

Configures the Audio Serial Interface channel modes

Figure 70. ASI_CHANNEL Register Address: 0x15

7	6	5	4	3	2	1	0
Reserved				Reserved		ASI_CHAN_MODE[1:0]	
RW-0h				RW-0h		RW-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. ASI Channel Control Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	0h	Reserved
3-2	Reserved	RW	0h	Reserved
1-0	ASI_CHAN_MODE[1:0]	RW	0h	Configures the ASI input stereo channel mode. Do no change this register for PDM input modes. ASI input playback is 0 = Left Channel 1 = Right Channel 2 = (Left + Right) / 2 3 = monoPCM

9.7.16 ASI_OFFSET_1 (book=0x00 page=0x00 address=0x16) [reset=0h]

Configures the ASI input offset. Offset is measured with respect to WCLK

Figure 71. ASI_OFFSET_1 Register Address: 0x16

7	6	5	4	3	2	1	0
ASI_OFFSET1[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. ASI Offset Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ASI_OFFSET1[7:0]	RW	0h	ASI_OFFSET1[7:0]

9.7.17 ASI_OFFSET_2 (book=0x00 page=0x00 address=0x17) [reset=0h]

Configures the right channel offset from the left channel slot in DSP Timeslot mode

Figure 72. ASI_OFFSET_2 Register Address: 0x17

7	6	5	4	3	2	1	0
ASI_OFFSET2[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. ASI Offset Second Slot Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ASI_OFFSET2[7:0]	RW	0h	ASI_OFFSET2[7:0]

9.7.18 ASI_CFG_1 (book=0x00 page=0x00 address=0x18) [reset=0h]

Configure various ASI options

Figure 73. ASI_CFG_1 Register Address: 0x18

7	6	5	4	3	2	1	0
Reserved	Reserved	ASI_WCLKM	ASI_BCLKM	ASI_WCLKE	ASI_BCLKE	ASI_TRISTATE	ASI_BUSKEEP
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. ASI Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	Reserved	RW	0h	Reserved

Table 76. ASI Configuration Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ASI_WCLKM	RW	0h	Configure the ASI WCLK direction 0 = Input 1 = Output
4	ASI_BCLKM	RW	0h	Configure the ASI BCLK direction 0 = Input 1 = Output
3	ASI_WCLKE	RW	0h	Configure the WCLK to be 0 = As per the timing Protocol 1 = Inverted with respect to the timing protocol
2	ASI_BCLKE	RW	0h	Configure the BCLK to be 0 = As per the timing Protocol 1 = Inverted with respect to the timing protocol
1	ASI_TRISTATE	RW	0h	Tri-stating of DOUT for the extra ASI_BCLK cycles after Data Transfer is over for a frame is 0 = Disabled 1 = Enabled
0	ASI_BUSKEEP	RW	0h	DOUT Bus-keeper is 0 = Disabled 1 = Enabled

9.7.19 ASI_DIV_SRC (book=0x00 page=0x00 address=0x19) [reset=0h]

ASI BDIV Clock Input

Figure 74. ASI_DIV_SRC Register Address: 0x19

7	6	5	4	3	2	1	0
Reserved						ASI_DIV_CLK_SRC[1:0]	
RW-0h						RW-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. ASI BDIV Clock Input Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	RW	0h	Reserved
1-0	ASI_DIV_CLK_SRC[1:0]	RW	0h	Selects the ASI_CLKIN source for BDIV and WDIV is 0 = DAC_MOD_CLK 1 = ADC_MOD_CLK 2 = NDIV_CLK 3 = Reserved

9.7.20 ASI_BDIV (book=0x00 page=0x00 address=0x1A) [reset=1h]

ASI BDIV Configuration

Figure 75. ASI_BDIV Register Address: 0x1A

7	6	5	4	3	2	1	0
ASI_BDIV_P	ASI_BDIV_RATIO[6:0]						
RW-0h	RW-1h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. ASI BDIV Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_BDIV_P	RW	0h	ASI BDIV divider is 0 = Powered down 1 = Powered up

Table 78. ASI BDIV Configuration Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	ASI_BDIV_RATIO[6:0]	RW	1h	The ASI_BDIV ration is 0 = 128 1-31 = Reserved 32 = 32 33 = 33 ... 126 = 126 127 = 127

9.7.21 ASI_WDIV (book=0x00 page=0x00 address=0x1B) [reset=40h]

ASI WDIV Configuration

Figure 76. ASI_WDIV Register Address: 0x1B

7	6	5	4	3	2	1	0
ASI_WDIV_P	ASI_WDIV_RATIO[6:0]						
RW-0h	RW-40h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. ASI WDIV Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_WDIV_P	RW	0h	ASI WDIV divider is 0 = Powered down 1 = Powered up
6-0	ASI_WDIV_RATIO[6:0]	RW	40h	The ASI_WDIV ration is 0 = 128 1-31 = Reserved 32 = 32 33 = 33 ... 126 = 126 127 = 127

9.7.22 PDM_CFG (book=0x00 page=0x00 address=0x1C) [reset=0h]

PDM Configuration

Figure 77. PDM_CFG Register Address: 0x1C

7	6	5	4	3	2	1	0
Reserved			Reserved		PDM_CLK_E	PDM_CI_M	PDM_CIO_M
RW-0h			RW-0h		RW-0h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. PDM Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	RW	0h	Reserved
4-3	Reserved	RW	0h	Reserved
2	PDM_CLK_E	RW	0h	Data is latch on the following edge of the PDM clock 0 = Rising 1 = Falling
1	PDM_CI_M	RW	0h	PDM_IN_CLK direction is 0 = input 1 = output
0	PDM_CIO_M	RW	0h	PDM_OUT_CLK direction is 0 = input 1 = output

9.7.23 PDM_DIV (book=0x00 page=0x00 address=0x1D) [reset=8h]

PDM Divider Configuration

Figure 78. PDM_DIV Register Address: 0x1D

7	6	5	4	3	2	1	0
PDM_DIV_P	Reserved						
RW-0h	RW-8h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. PDM Divider Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	PDM_DIV_P	RW	0h	PDM_IN_DIV divider is 0 = Powered down 1 = Powered up
6-0	Reserved	RW	8h	Reserved

9.7.24 DSD_DIV (book=0x00 page=0x00 address=0x1E) [reset=8h]

DSD Divider Configuration

Figure 79. DSD_DIV Register Address: 0x1E

7	6	5	4	3	2	1	0
DSD_DIV_P	Reserved	Reserved					
RW-0h	RW-0h	RW-8h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. DSD Divider Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	DSD_DIV_P	RW	0h	DSD_DIV divider is 0 = Powered down 1 = Powered up
6	Reserved	RW	0h	Reserved
5-0	Reserved	RW	8h	Reserved

9.7.25 CLK_ERR_1 (book=0x00 page=0x00 address=0x21) [reset=3h]

Clock Error and DSP memory Reload

Figure 80. CLK_ERR_1 Register Address: 0x21

7	6	5	4	3	2	1	0
DSP_MEMRST	Reserved	Reserved	CLK_E1_SRC	CLK_E2_SRC[1:0]		CLK_E1_EN	CLK_E2_EN
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h		RW-1h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 83. Clock Error and DSP memory Reload Field Descriptions

Bit	Field	Type	Reset	Description
7	DSP_MEMRST	RW	0h	Determine if the DSP memory locations will be reloaded for reasons other than user power down such as clock-halt, brownout, over current, over temp, and over voltage. 0 = Do not reload on restart 1 = Reload defaults on restart
6	Reserved	RW	0h	Reserved
5	Reserved	RW	0h	Reserved
4	CLK_E1_SRC	RW	0h	Clock error detection 1 block input is from 0 = ASI_CLK 1 = PDM_CLK

Table 83. Clock Error and DSP memory Reload Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CLK_E2_SRC[1:0]	RW	0h	Clock error detection 2 block input is from 0 = DAC Modulator Clock 1 = ADC Modulator Clock 2 = PLL Clock 3 = Reserved
1	CLK_E1_EN	RW	0h	Clock error detection block 1 is 0 = Disabled 1 = Enabled
0	CLK_E2_EN	RW	0h	Clock error detection block 2 is 0 = Disabled 1 = Enabled

9.7.26 CLK_ERR_2 (book=0x00 page=0x00 address=0x22) [reset=3Fh]

Sets the clock error timeouts for detecting missing clocks

Figure 81. CLK_ERR_2 Register Address: 0x22

7	6	5	4	3	2	1	0
Reserved	Reserved	CLK_E1_TIME[2:0]			CLK_E2_TIME[2:0]		
RW-0h	RW-0h	RW-7h			RW-7h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. Clock Error Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	Reserved	RW	0h	Reserved
5-3	CLK_E1_TIME[2:0]	RW	0h	The chip will shutdown with a clock error 1 is the clock input to the error 1 detection block is not present for the specified time. B0_P0_R5[0] will be set to high and must be cleared before repowering the device. The clock missing time is 0 = 11ms 1 = 22ms 2 = 44ms 3 = 87ms 4 = 174ms 5 = 350ms 6 = 700ms 7 = 1.2s
2-0	CLK_E2_TIME[2:0]	RW	7h	The chip will shutdown with a clock error 1 is the clock input to the error 1 detection block is not present for the specified time. B0_P0_R5[0] will be set to high and must be cleared before repowering the device. The clock missing time is 0 = 11ms 1 = 22ms 2 = 44ms 3 = 87ms 4 = 174ms 5 = 350ms 6 = 700ms 7 = 1.2s

9.7.27 IRQ_PIN_CFG (book=0x00 page=0x00 address=0x23) [reset=21h]

Sets the interrupt pin mode of operation

Figure 82. IRQ_PIN_CFG Register Address: 0x23

7	6	5	4	3	2	1	0
IRQ_DRIVE[2:0]			IRQ_GPO_VAL	Reserved	IRQ_PIN_MODE[2:0]		
RW-1h			RW-0h	RW-0h	RW-1h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. Interrupt Pin Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7-5	IRQ_DRIVE[2:0]	RW	1h	Sets the output drive mode of the IRQ interrupt pin to 0 = Drive both high and low values 1 = Open Drain, low-actively driven, high-HiZ 2 = Open Drain, low-HiZ, high-actively drive 3 = Open Drain, low-actively driven, high-HiZ w/ pull-up 4 = Open Drain, low-HiZ w/ pull-down, high-actively driven 5 = Reserved Others = Reserved
4	IRQ_GPO_VAL	RW	0h	When B0_P0_R35[2:0]=b011 this is used set the value of the IRQ pin 0 = low 1 = high
3	Reserved	RW	0h	Reserved
2-0	IRQ_PIN_MODE[2:0]	RW	1h	Configures the IRQ pin mode of operation. IRQ pin is 0 = Disabled and IO buffers powered down 1 = Interrupt controlled output 2 = Reserved 3 = General purpose output 4 = PDM_IN_DIV output 5 = Reserved Others = Reserved

9.7.28 INT_CFG_1 (book=0x00 page=0x00 address=0x24) [reset=0h]

Sets the interrupt pin toggle behavior and the interrupt mask flags

Figure 83. INT_CFG_1 Register Address: 0x24

7	6	5	4	3	2	1	0
IRQ_IND_CFG[1:0]		Reserved				Reserved	Reserved
RW-0h		RW-0h				RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. Interrupt Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IRQ_IND_CFG[1:0]	RW	0h	Configures the interrupt indication mode and determines how the IRQ pin will indicate the interrupt. 0 = Interrupt will be only one pulse(active high) of duration 2ms. 1 = Interrupt will be multiple pulses(active high) of duration 2ms and period 4ms until interrupt sticky flags are cleared by reading INT_DET_1 and INT_DET_2 2 = Interrupt will remain high after interrupt is generated until interrupt sticky flags are cleared by reading INT_DET_1 and INT_DET_2
5-2	Reserved	RW	0h	Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

9.7.29 INT_CFG_2 (book=0x00 page=0x00 address=0x25) [reset=0h]

Sets the interrupt mask flags.

Figure 84. INT_CFG_2 Register Address: 0x25

7	6	5	4	3	2	1	0
INTM_OVRI	INTM_AUV	INTM_CLK2	INTM_OVRT	INTM_BRNO	INTM_CLK1	INTM_MCHLT	INT_WCHLT
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. Interrupt Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	INTM_OVRI	RW	0h	Sets the interrupt mask flag for the speaker over current detected to 0 = Clear (not used) 1 = Set (used)
6	INTM_AUV	RW	0h	Sets the interrupt mask flag for the analog under voltage detected to 0 = Clear (not used) 1 = Set (used)
5	INTM_CLK2	RW	0h	Sets the interrupt mask flag for the clock error 2 detected to 0 = Clear (not used) 1 = Set (used)
4	INTM_OVRT	RW	0h	Sets the interrupt mask flag for the die over-temperature detected to 0 = Clear (not used) 1 = Set (used)
3	INTM_BRNO	RW	0h	Sets the interrupt mask flag for the brownout detected to 0 = Clear (not used) 1 = Set (used)
2	INTM_CLK1	RW	0h	Sets the interrupt mask flag for the clock error 1 detected to 0 = Clear (not used) 1 = Set (used)
1	INTM_MCHLT	RW	0h	Sets the interrupt mask flag for the modulator clock halt detected to 0 = Clear (not used) 1 = Set (used)
0	INT_WCHLT	RW	0h	Sets the interrupt mask flag for the WCLK clock halt detected to 0 = Clear (not used) 1 = Set (used)

9.7.30 INT_DET_1 (book=0x00 page=0x00 address=0x26) [reset=0h]

Sticky register used to indicate the source of an interrupt trigger. Register is cleared once read.

Figure 85. INT_DET_1 Register Address: 0x26

7	6	5	4	3	2	1	0
INT_OVRI	INT_AUV	INT_CLK1	INT_OVRT	INT_BRNO	INT_CLK2	INT_SAR	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. Interrupt Detected 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_OVRI	R	0h	Sticky bit indicating that speaker over current condition 0 = did not occurred since last read 1 = occurred since last read
6	INT_AUV	R	0h	Sticky bit indicating that analog under voltage condition 0 = did not occurred since last read 1 = occurred since last read
5	INT_CLK1	R	0h	Sticky bit indicating that clock error 1 condition 0 = did not occurred since last read 1 = occurred since last read

Table 88. Interrupt Detected 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_OVRT	R	0h	Sticky bit indicating that die over-temperature condition 0 = did not occurred since last read 1 = occurred since last read
3	INT_BRNO	R	0h	Sticky bit indicating that brownout condition 0 = did not occurred since last read 1 = occurred since last read
2	INT_CLK2	R	0h	Sticky bit indicating that the clock error 2 condition 0 = did not occurred since last read 1 = occurred since last read
1	INT_SAR	R	0h	Sticky bit indicating that the SAR complete condition 0 = did not occurred since last read 1 = occurred since last read
0	Reserved	R	0h	Reserved

9.7.31 INT_DET_2 (book=0x00 page=0x00 address=0x27) [reset=0h]

Sticky register used to indicate the source of an interrupt trigger

Figure 86. INT_DET_2 Register Address: 0x27

7	6	5	4	3	2	1	0
INT_WCHLT	INT_MCHLT	Reserved				Reserved	Reserved
R-0h	R-0h	R-0h				R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. Interrupt Detected 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_WCHLT	R	0h	Sticky bit indicating that WCLK clock halt condition 0 = did not occurred since last read 1 = occurred since last read
6	INT_MCHLT	R	0h	Sticky bit indicating that the modulator clock halt condition 0 = did not occurred since last read 1 = occurred since last read
5-2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

9.7.32 STATUS_POWER (book=0x00 page=0x00 address=0x2A) [reset=0h]

This register indicated the operational status of various internal blocks

Figure 87. STATUS_POWER Register Address: 0x2A

7	6	5	4	3	2	1	0
SPWR_DAC	SPWR_CD	SPWR_BST	SPWR_BSTPT	SPWR_ISNS	SPWR_VSNS	Reserved	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. Status Block Power Field Descriptions

Bit	Field	Type	Reset	Description
7	SPWR_DAC	R	0h	The DAC block is 0 = powered down 1 = powered up
6	SPWR_CD	R	0h	The Class-D block is 0 = powered down 1 = powered up

Table 90. Status Block Power Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SPWR_BST	R	0h	The boost block is 0 = powered down 1 = powered up
4	SPWR_BSTPT	R	0h	The boost pass-thru is 0 = disabled 1 = enabled
3	SPWR_ISNS	R	0h	The i-sense block is 0 = powered down 1 = powered up
2	SPWR_VSNS	R	0h	The v-sense block is 0 = powered down 1 = powered up
1-0	Reserved	R	0h	Reserved

9.7.33 SAR_VBAT_MSB (book=0x00 page=0x00 address=0x2D) [reset=C0h]

SAR VBAT Measurement MSB

Figure 88. SAR_VBAT_MSB Register Address: 0x2D

7	6	5	4	3	2	1	0
SAR_VBAT[9:2]							
R-C0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. SAR VBAT Measurement MSB Field Descriptions

Bit	Field	Type	Reset	Description
7--2	SAR_VBAT[9:0]	R	C0h	The VBAT measurement from the SAR ADC when enabled

9.7.34 SAR_VBAT_LSB (book=0x00 page=0x00 address=0x2E) [reset=0h]

SAR VBAT Measurement LSB

Figure 89. SAR_VBAT_LSB Register Address: 0x2E

7	6	5	4	3	2	1	0
SAR_VBAT[1:0]		Reserved					
R-0h		R-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. SAR VBAT Measurement LSB Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SAR_VBAT[1:0]	R	0h	The VBAT measurement from the SAR ADC when enabled
5-0	Reserved	R	0h	Reserved

9.7.35 DIE_TEMP_SENSOR (book=0x00 page=0x00 address=0x31) [reset=0h]

Request a die temperature reading and register to read back the die temperature range.

Figure 90. DIE_TEMP_SENSOR Register Address: 0x31

7	6	5	4	3	2	1	0
Reserved		DTMP_INIT	DTMP_VALID	DTMP_VAL[3:0]			
RW-0h		RW-0h	R-0h	R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. Die Temperature Sensor Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5	DTMP_INIT	RW	0h	Request a reading of the die temperature be performed. The die temp measurement acquisition is 0 = idle 1 = Initiated (self cleared when completed)
4	DTMP_VALID	R	0h	Indicated the validity of the die temperature registers. This will be invalid when the acquisition is in progress. Die temperature reading is 0 = invalid 1 = valid
3-0	DTMP_VAL[3:0]	R	0h	The last die temperature measurement was 0 = less than 30 C 1 = in the range 30 C to 50 C 2 = in the range 50 C to 65 C 3 = in the range 65 C to 80 C 4 = in the range 80 C to 85 C 5 = in the range 85 C to 90 C 6 = in the range 90 C to 95 C 7 = in the range 95 C to 100 C 8 = in the range 100 C to 105 C 9 = in the range 105 C to 110 C 10 = in the range 110 C to 115 C 11 = in the range 115 C to 120 C 12 = in the range 120 C to 125 C 13 = in the range 125 C to 130 C 14 = in the range 130 C to 140 C 15 = is greater than 140 C

9.7.36 LOW_PWR_MODE (book=0x00 page=0x00 address=0x35) [reset=0h]

Sets the VBAT POR status to save idle current consumption in shutdown.

Figure 91. LOW_PWR_MODE Register Address: 0x35

7	6	5	4	3	2	1	0
VBAT_POR	Reserved						
RW-0h	RW-0h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. Low Power Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	VBAT_POR	RW	0h	Set the VBAT POR block state. When the VBAT POR is disabled the lowest shutdown current can be obtained. The VBAT should remain powered up when the POR is disabled. The VBAT POR is 0 = powered up 1 = powered down
6-0	Reserved	RW	0h	Reserved

9.7.37 PCM_RATE (book=0x00 page=0x00 address=0x36) [reset=32h]

Sets the PCM input sampling rate

Figure 92. PCM_RATE Register Address: 0x36

7	6	5	4	3	2	1	0
Reserved		Reserved		Reserved		PCM_RATE[1:0]	
RW-0h		RW-3h		RW-0h		RW-2h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. PCM Sample Rate Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5-4	Reserved	RW	3h	Reserved
3-2	Reserved	RW	3h	Reserved
1-0	PCM_RATE[1:0]	RW	0h	Configure the ASI PCM rate used to 0 = 8 kHz 1 = 16 kHz 2 = 48 kHz 3 = 96 kHz

9.7.38 CLOCK_ERR_CFG_1 (book=0x00 page=0x00 address=0x4F) [reset=0h]

Sets if the device will try to auto

Figure 93. CLOCK_ERR_CFG_1 Register Address: 0x4F

7	6	5	4	3	2	1	0
Reserved				CLK_ERR2_AR	CLK_ERR1_AR	Reserved	
RW-0h				RW-0h	RW-0h	RW-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Clock Error Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	0h	Reserved
3	CLK_ERR2_AR	RW	0h	When an error occurs on clock error 2 block the device will 0 = perform a recovery when condition clears 1 = will shutdown and require user recovery
2	CLK_ERR1_AR	RW	0h	When an error occurs on clock error 1 block the device will 0 = perform a recovery when condition clears 1 = will shutdown and require user recovery
1-0	Reserved	RW	0h	Reserved

9.7.39 CLOCK_ERR_CFG_2 (book=0x00 page=0x00 address=0x50) [reset=11h]

Sets if the device will try to auto

Figure 94. CLOCK_ERR_CFG_2 Register Address: 0x50

7	6	5	4	3	2	1	0
CLK_ERR_MR[1:0]		CLK_ERR1_TO[2:0]			CLK_ERR2_TO[2:0]		
RW-0h		RW-2h			RW-1h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. Clock Error Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CLK_ERR_MR[1:0]	RW	0h	On clock error detection the channel gain will ramp-down at the rate 0 = 15us per dB 1 = 30us per dB 3 = 60us per dB 4 = 120us per dB

Table 97. Clock Error Configuration 2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	CLK_ERR1_TO[2:0]	RW	2h	Playback path is muted if clock input doesn't come to clock error detection1 block for 0 = 10.6 us 1 = 21.3 us 2 = 42.6 us 3 = 85.3 us 4 = 0.34 ms 5 = 0.68 ms 6 = 1.36 ms 7 = 2.73 ms
2-0	CLK_ERR2_TO[2:0]	RW	1h	Playback path is muted if clock input doesn't come to clock error detection2 block for 0 = 10.6 us 1 = 21.3 us 2 = 42.6 us 3 = 85.3 us 4 = 0.34 ms 5 = 0.68 ms 6 = 1.36 ms 7 = 2.73 ms

9.7.40 PROTECTION_CFG_1 (book=0x00 page=0x00 address=0x58) [reset=3h]

D Proteciton Configuration 1

Figure 95. PROTECTION_CFG_1 Register Address: 0x58

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	PROT_OT_AR	Reserved	Reserved
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-1h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. Class Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	Reserved	RW	0h	Reserved
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3	Reserved	RW	0h	Reserved
2	PROT_OT_AR	RW	0h	Die over temperature auto retry is 0 = enabled 1 = disabled
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

9.7.41 CRC_CHECKSUM (book=0x00 page=0x00 address=0x7E) [reset=0h]

Hold the running CRC8 checksum of I2C transactions

Figure 96. CRC_CHECKSUM Register Address: 0x7E

7	6	5	4	3	2	1	0
CRC_VAL[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. Checksum Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CRC_VAL[7:0]	RW	0h	Current CRC value. Writing to this register will reset the checksum

9.7.42 BOOK (book=0x00 page=0x00 address=0x7F) [reset=0h]

Book Selection

Figure 97. BOOK Register Address: 0x7F

7	6	5	4	3	2	1	0
BOOK[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. Book Selection Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	RW	0h	Set the device book 0 = Book 0 1 = Book 1 ... 255 = Book 255

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TAS2560 is a digital or analog input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-H boost converter. In auto passthrough mode, the Class-H boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. To enable load monitoring, the TAS2560 constantly measures the current and voltage across the load and provides a digital stream of this information back to a processor.

10.2 Typical Applications

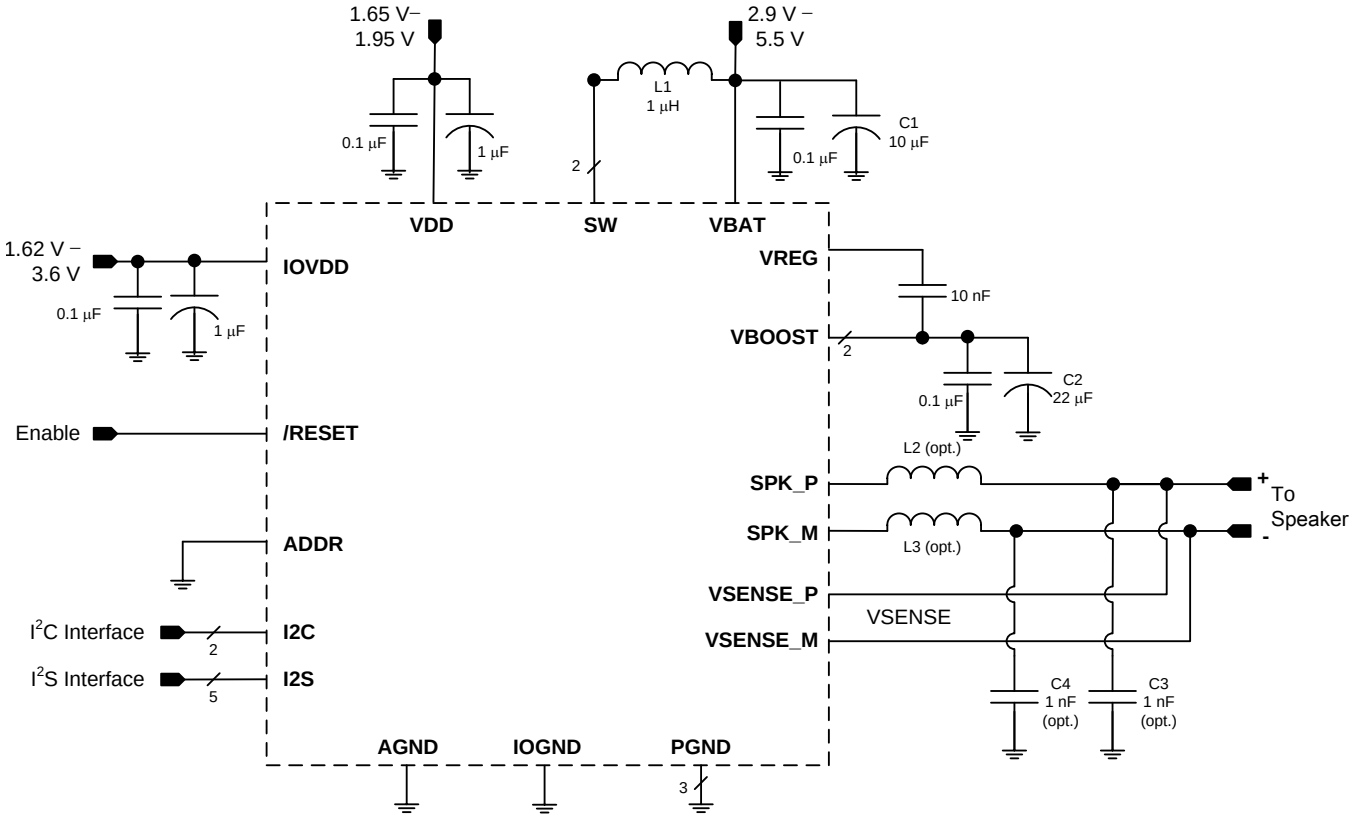


图 98. Typical Application - Digital Audio Input

Typical Applications (接下页)

表 101. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
L1	Boost Converter Inductor(1)	Inductance, 20% Tolerance	1	1		µH
		Saturation Current		3.1		A
L2, L3	EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. TAS2560 is a filter-less Class-D and does not require these bead inductors.	Impedance at 100 MHz		120		O
		DC Resistance			0.095	O
		DC Current			2	A
		Size		0402		EIA
C1	Boost Converter Input Capacitor(1)	Capacitance, 20% Tolerance	10			µF
C2	Boost Converter Output Capacitor	Type	X5R			
		Capacitance, 20% Tolerance	22		47	µF
		Rated Voltage	16			V
		Capacitance at 8.5 V derating	3.3			µF
C3, C4	EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used)	Capacitance		1		nF

(1) See sectionBoost Converter Passive Devices for additional requirements on derating, stability, and inductor value trade-offs.

10.2.1 Design Requirements

For this design example, use the parameters shown in 表 102.

表 102. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	Digital Audio, I^2S
Current and Voltage Data Stream	Digital Audio, I^2S
Mono or Stereo Configuration	Mono
Max Output Power at 1% THD+N	3.8 W

10.2.1.1 Detailed Design Procedure

10.2.1.1.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See *General I^2C Operation* for information on changing the I^2C address of the TAS2560 to support stereo operation. Mono or stereo configuration does not impact the device performance.

10.2.1.1.2 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in 图 98 and whose specifications are provided in 表 101. These specifications are based on the design of the TAS2560 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

Additionally, the ratio of L1/C2 (the derated value of C2 at 8.5 V should be used in this ratio) has to be lesser than 1/3 for boost stability. This 1/3 ratio should be maintained including the worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be ≥ 1 µH at the boost switching frequency (approximately 1.7 MHz). Using a 1 µH will have more boost ripple than a 2.2 µH but the PSRR should minimize the effect from the additional ripple. Finally, the minimum C2 (derated value at 8.5 V) should be > 3.3 µF for Class-D power delivery specification.

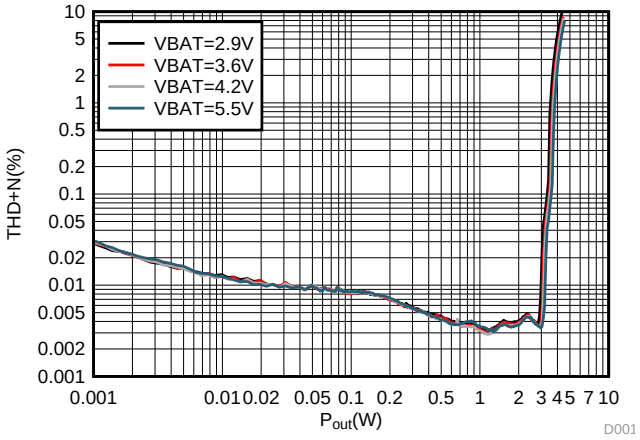
10.2.1.1.3 EMI Passive Devices

The TAS2560 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output devices. These passive devices that are labeled L2, L3, C3 and C4 in 图 98 and their recommended specifications are provided in 表 101. If C3 and C4 are used, they must be placed after L2 and L3 respectively to maintain the stability of the output stage.

10.2.1.1.4 Miscellaneous Passive Devices

- VREG Capacitor: Needs to be 10 nF to meet boost and Class-D power delivery and efficiency specs.

10.2.2 Application Performance Plots



Freq = 1kHz VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, RESETZ = IOVDD, R_L = 8 Ω + 33 µH, I^2S digital input, Mode 1

图 99. THD+N vs Output Power (8 Ω) for Digital Input

10.3 Initialization Set Up

To configure the TAS2560, follow these steps.

1. Bring-up the power supplies as in *Power Supply Sequencing*.
2. Set the RESETZ terminal to HIGH.
3. Follow the software sequence in the *Programming* section.

11 Power Supply Recommendations

11.1 Power Supplies

The TAS2560 requires four power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 2.9 V to 5.5 V
  - Max Current: 5 A for ILIM = 3.0 A (default)
- Analog Supply (terminal: VDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- Digital I/O Supply (terminal: IOVDD)
  - Voltage: 1.62 V to 3.6 V
  - Max Current: 5 mA

The decoupling capacitors for the power supplies should be placed close to the device terminals. For VBAT, IOVDD, and VDD, a small decoupling capacitor of 0.1 µF should be placed as close as possible to the device terminals. Refer to *图 100* for the schematic.

11.2 Power Supply Sequencing

The following power sequence should be followed for power up and power down. If the recommended sequence is not followed there can be large current in device due to faults in level shifters and diodes becoming forward biased. The T_{delay} between power supplies should be large enough for the power rails to settle.

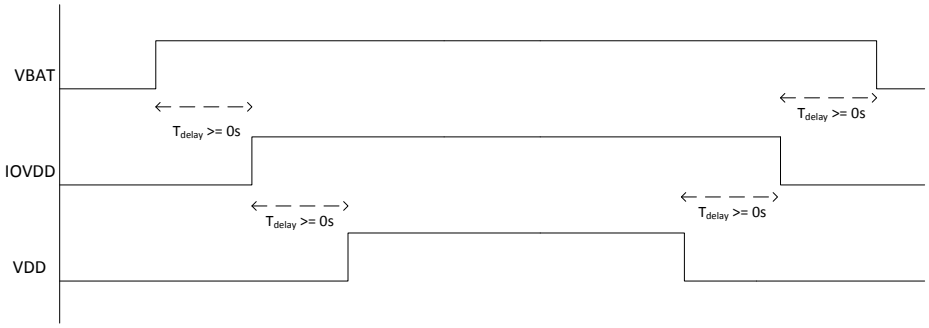


图 100. Power Supply Sequence for Power-Up and Power-Down

When the supplies have settled, the RESETZ terminal can be set HIGH to operate the device. Additionally the RESETZ pin can be tied to IOVDD and the internal DVDD POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100uS to allow the OTP to load. The above sequence should be completed before any I^2C operation.

11.2.1 Boost Supply Details

The boost supply (VBAT) and associated passives need to be able to support the current requirements of the device. By default, the peak current limit of the boost is set to 3 A. Refer to *Configurable Boost Current Limit (ILIM)* for information on changing the current limit. A minimum of a 10 µF capacitor is recommended on the boost supply to quickly support changes in required current. Refer to for the schematic.

The current requirements can also be reduced by lowering the gain of the amplifier, or in response to decreasing battery through the use of the battery-tracking AGC feature of the TAS2560 described in *Battery Guard AGC*.

12 Layout

12.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VBOOST close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBOOST/VBAT and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Do not use VIAS for traces that carry high current. These include the traces for VBOOST, SW, VBAT, PGND and the speaker SPK_P, SPK_M.
- Use epoxy filled vias for the interior pads.
- Connect VSENSE_P, VSENSE_N as close as possible to the speaker.
  - VSENSE_P, VSENSE_N should be connected between the EMI ferrite and the speaker if EMI ferrites are used on SPK_P, SPK_M.
  - EMI ferrites must be used if EMI capacitors are used on SPK_P, SPK_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in *图 98* and described in *Power Supplies*.
- Place EMI ferrites, if used, close to the device.

12.2 Layout Example

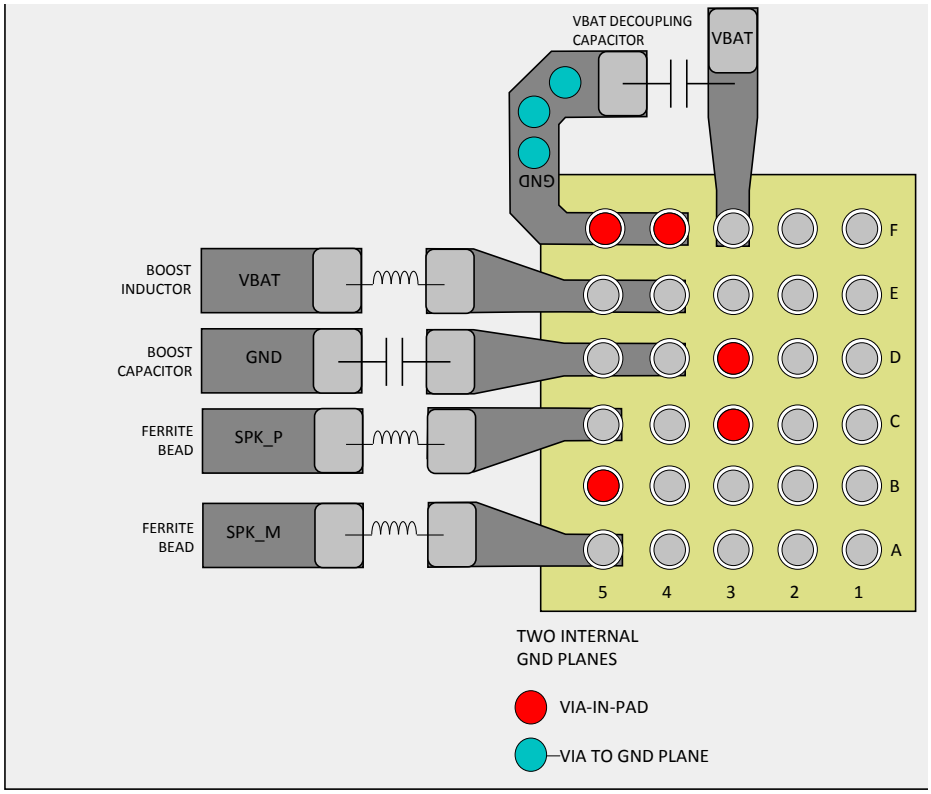


图 101. TAS2560 Board Layout

13 器件和文档支持

13.1 文档支持

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.3 商标

PurePath, E2E are trademarks of Texas Instruments.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

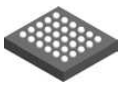
14.1 封装尺寸

TAS2560 采用 30 焊球、间距为 0.4mm 的晶圆级芯片封装 (WCSP)。

封装尺寸 **(**接下页**)**

TAS2560YFF

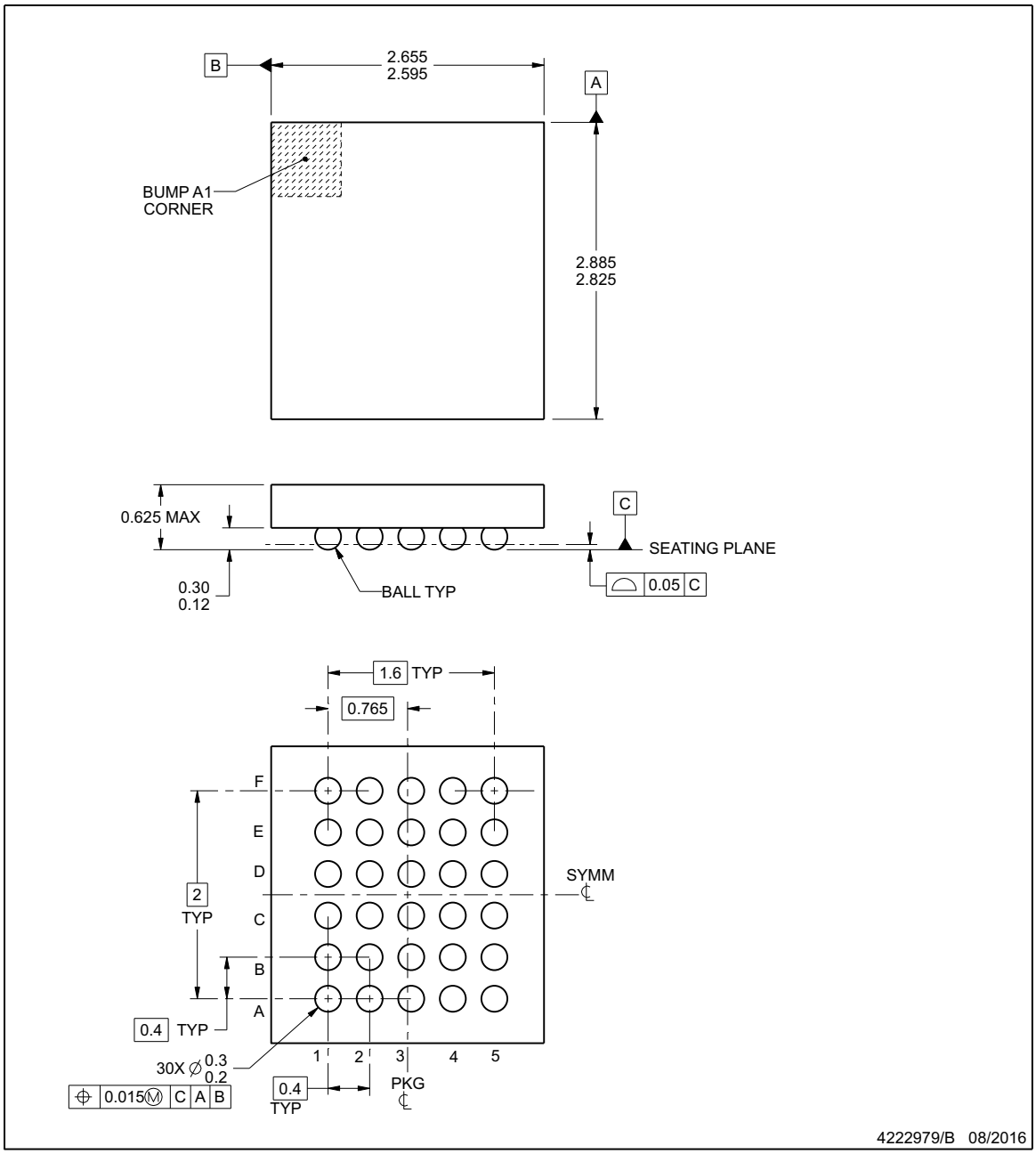
YFF0030-C01



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

封装尺寸 **(**接下页**)**

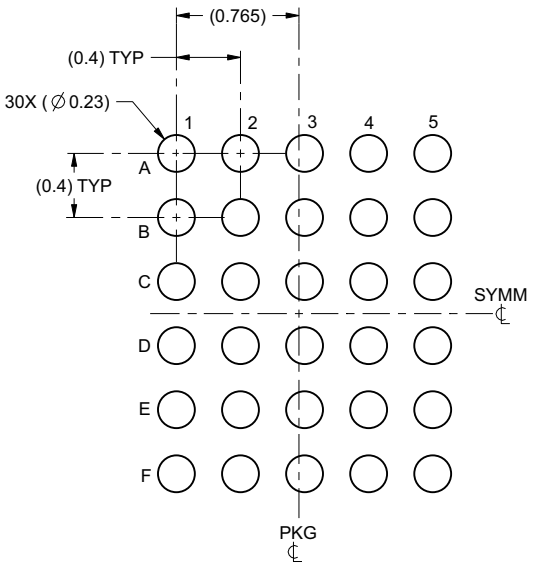
TAS2560YFF

YFF0030-C01

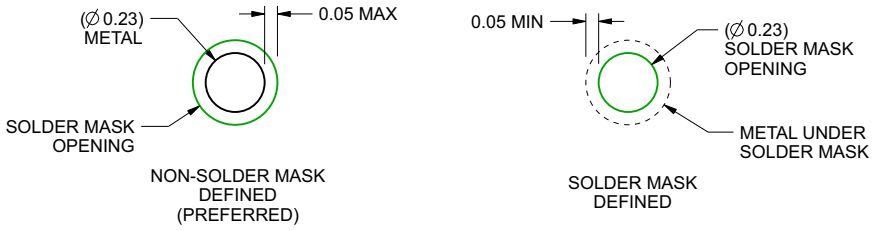
EXAMPLE BOARD LAYOUT

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222979/B 08/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

封装尺寸 **(**接下页**)**

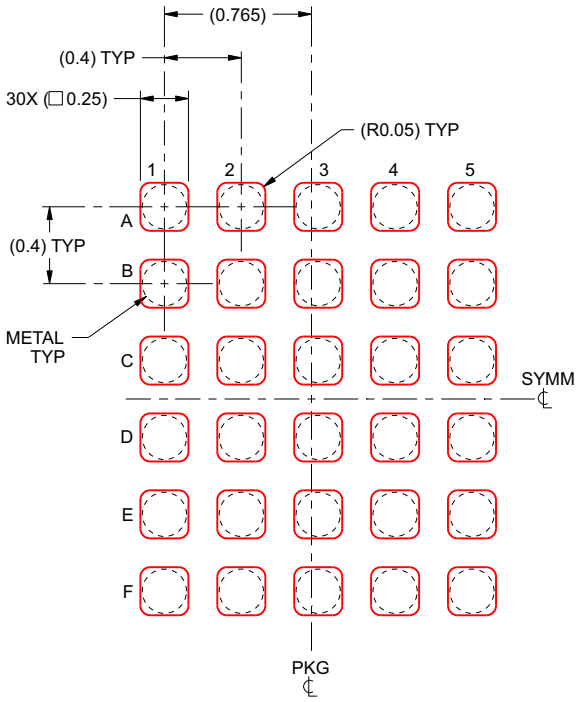
TAS2560YFF

YFF0030-C01

EXAMPLE STENCIL DESIGN

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222979/B 08/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS2560YFFR	ACTIVE	DSBGA	YFF	30	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2560	Samples
TAS2560YFFT	ACTIVE	DSBGA	YFF	30	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2560	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

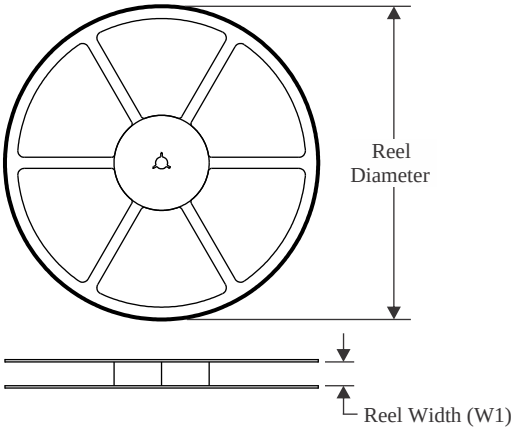
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

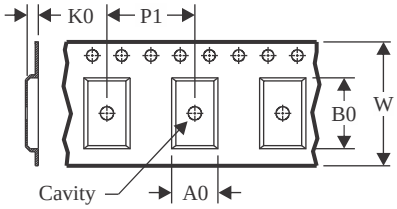
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

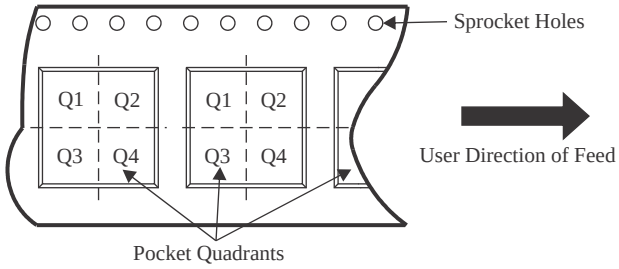


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

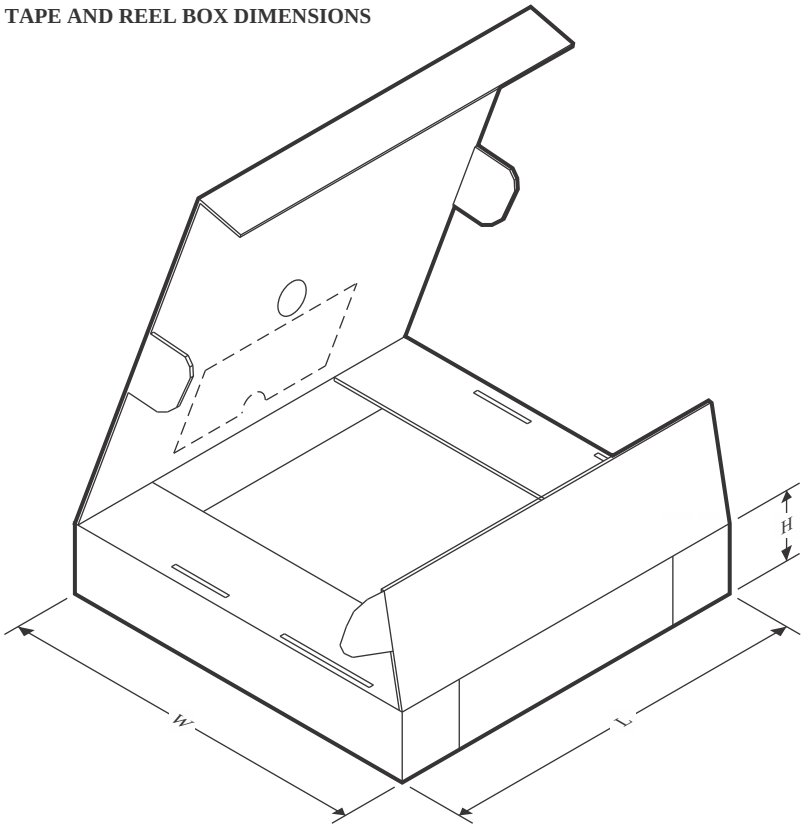
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2560YFFR	DSBGA	YFF	30	3000	178.0	9.2	2.76	3.02	0.83	4.0	8.0	Q1
TAS2560YFFR	DSBGA	YFF	30	3000	180.0	8.4	2.76	3.02	0.83	4.0	8.0	Q1
TAS2560YFFT	DSBGA	YFF	30	250	180.0	8.4	2.76	3.02	0.83	4.0	8.0	Q1
TAS2560YFFT	DSBGA	YFF	30	250	178.0	9.2	2.76	3.02	0.83	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2560YFFR	DSBGA	YFF	30	3000	220.0	220.0	35.0
TAS2560YFFR	DSBGA	YFF	30	3000	182.0	182.0	20.0
TAS2560YFFT	DSBGA	YFF	30	250	182.0	182.0	20.0
TAS2560YFFT	DSBGA	YFF	30	250	220.0	220.0	35.0

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