TEXAS INSTRUMENTS
SRC4190
SBFS023C – JUNE 2003 – REVISED DECEMBER 2016

SRC4190 192-kHz Stereo Asynchronous Sample-Rate Converters

1 Features

- Automatic Sensing of the Input-to-Output Sampling Ratio
- Wide Input-to-Output Sampling Range: 16:1 to 1:16
- Supports Input and Output Sampling Rates up to 212 kHz
- Dynamic Range: 128 dB (–60-dB f_S Input, BW = 20 Hz to f_S / 2, A-Weighted)
- THD+N: –125 dB (0-dB f_S Input, BW = 20 Hz to f_S / 2)
- Attenuates Sampling and Reference Clock Jitter
- High-Performance, Linear Phase Digital Filtering
- Flexible Audio Serial Ports:
  - Master or Slave Mode Operation Supports I^2S, Left Justified, Right Justified, and TDM Data Formats
  - Supports 16-, 18-, 20-, or 24-Bit Audio Data, TDM Mode Allows Daisy Chaining of up to Eight Devices
- Supports 24-, 20-, 18-, or 16-Bit Input and Output
  - All Output Data is Dithered from the Internal 28-Bit Data Path
- Low Group Delay Option for Interpolation Filter
- Soft Mute Function
- Bypass Mode
- Power-Down Mode
- Operates from a Single 3.3-V Power Supply
- Small 28-Pin SSOP Package
- Pin Compatible With the SRC4192, AD1895, and AD1896

NOTE: U.S. Patent No. 7,262,716

NOTE: See *Application and Implementation* for details.

2 Applications

- Digital Mixing Consoles
- Digital Audio Workstations
- Audio Distribution Systems
- Broadcast Studio Equipment
- High-End A/V Receivers
- General Digital Audio Processing

3 Description

The SRC4190 device is an asynchronous sample rate converter designed for professional and broadcast audio applications. The SRC4190 combines a wide input-to-output sampling ratio with outstanding dynamic range and low distortion. Input and output serial ports support standard audio formats, as well as a Time Division Multiplexed (TDM) mode. Flexible audio interfaces allow the SRC4190 to connect to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4190 is a standalone pin-programmed device, with control pins for mode, data format, mute, bypass, and low group delay functions.

The SRC4190 may be operated from a single 3.3-V power supply. A separate digital I/O supply (VIO) operates with a 1.65-V to 3.6-V supply, allowing greater flexibility when interfacing to current and future generation signal processors and logic devices. The SRC4190 is available in a 28-pin SSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SRC4190	SSOP (28)	10.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

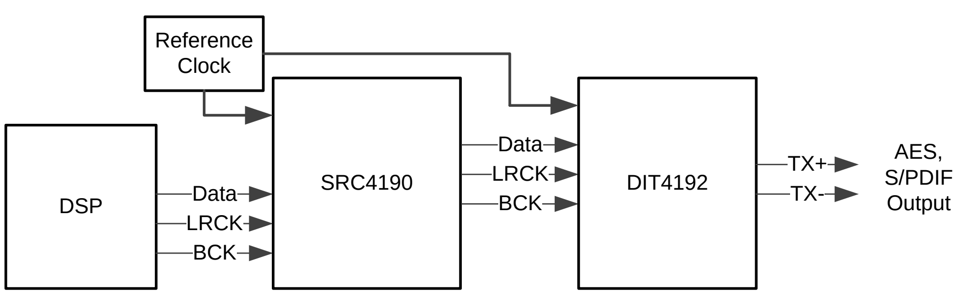


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2007) to Revision C — **Page**

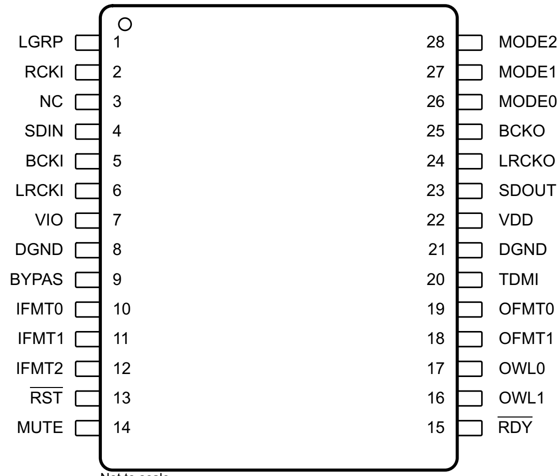
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet 1
- Added *Thermal Information* table 4

Changes from Revision A (July 2003) to Revision B — **Page**

- Added U.S. patent number to note (1) 1

5 Pin Configuration and Functions

DB Package
28-Pin SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BCKI	5	Input and Output	Input port bit clock I/O
BCKO	25	Input and Output	Output port bit clock I/O
BYPAS	9	Input	ASRC bypass control input (active high)
DGND	8, 21	Ground	Digital ground
IFMT0	10	Input	Input port data format control input
IFMT1	11	Input	Input port data format control input
IFMT2	12	Input	Input port data format control input
LGRP	1	Input	Low group delay control input (active high)
LRCKI	6	Input and Output	Input port left and right word clock I/O
LRCKO	24	Input and Output	Output port left and right word clock I/O
MODE0	26	Input	Serial port mode control input
MODE1	27	Input	Serial port mode control input
MODE2	28	Input	Serial port mode control input
MUTE	14	Input	Output mute control input (active high)
NC	3	—	No connection
OFMT0	19	Input	Output port data format control input
OFMT1	18	Input	Output port data format control input
OWL0	17	Input	Output port data word length control input
OWL1	16	Input	Output port data word length control input
RCKI	2	Input	Reference clock input
$\overline{\text{RDY}}$	15	Output	ASRC ready status output (active low)
$\overline{\text{RST}}$	13	Input	Reset input (active low)
SDIN	4	Input	Audio serial data input
SDOUT	23	Output	Audio serial data output
TDMI	20	Input	TDM data input. Connect to DGND when not in use.
VDD	22	Power	Digital core supply, 3.3 V
VIO	7	Power	Digital I/O supply, 1.65 V to V_{DD}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.3	4	V
Supply voltage, V_{IO}	–0.3	4	V
Digital input voltage	–0.3	4	V
Operating temperature	–45	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	VDD supply voltage	3	3.3	3.6	V
	VIO 1.8-V supply voltage	1.65	1.8	1.95	V
	VIO 3.3-V supply voltage	3	3.3	3.6	V
	Operating temperature	–45		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SRC4190 DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V = V_{IO} = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE (1)							
	Resolution				24		Bits
f_{SIN}	Input sampling frequency			4		212	kHz
f_{SOUT}	Output sampling frequency			4		212	kHz
	Input:Output sampling ratio	Upsampling				1:16	
		Downsampling				16:1	
	Dynamic range	BW = 20 Hz to f_{SOUT} / 2, –60-dBFS input, f_{IN} = 1 kHz, Unweighted (add 3 dB for A-weighted result)	44.1 kHz:48 kHz		125		dB
			48 kHz:44.1 kHz		125		
			48 kHz:96 kHz		125		
			44.1 kHz:192 kHz		125		
			96 kHz:48 kHz		125		
			192 kHz:12 kHz		125		
			192 kHz:32 kHz		125		
			192 kHz:48 kHz		125		
			32 kHz:48 kHz		125		
			12 kHz:192 kHz		125		
	Total harmonic distortion + noise	BW = 20 Hz to f_{SOUT} / 2, 0-dBFS input, f_{IN} = 1 kHz, Unweighted	44.1 kHz:48 kHz		–125		dB
			48 kHz:44.1 kHz		–125		
			48 kHz:96 kHz		–125		
			44.1 kHz:192 kHz		–125		
			96 kHz:48 kHz		–125		
			192 kHz:12 kHz		–125		
			192 kHz:32 kHz		–125		
			192 kHz:48 kHz		–125		
			32 kHz:48 kHz		–125		
			12 kHz:192 kHz		–125		
	Interchannel gain mismatch				0		dB
	Interchannel phase deviation				0		°
	Mute attenuation	24-bit word length, A-weighted			–128		dB
DIGITAL INTERPOLATION FILTER							
	Passband					0.4535 × f_{SIN}	Hz
	Passband ripple					±0.007	dB
	Transition band			0.4535 × f_{SIN}		0.5465 × f_{SIN}	Hz
	Stop band			0.5465 × f_{SIN}			Hz
	Stop band attenuation			–125			dB
	Normal group delay (LGRP = 0)				102.53125 / f_{SIN}		s
	Low group delay (LGRP = 1)				70.53125 / f_{SIN}		s
DIGITAL DECIMATION FILTER							
	Passband					0.4535 × f_{SOUT}	Hz
	Passband ripple					±0.008	dB
	Transition band			0.4535 × f_{SOUT}		0.5465 × f_{SOUT}	Hz
	Stop band			0.5465 × f_{SOUT}			Hz
	Stop band attenuation			–125			dB
	Group delay				36.46875 / f_{SOUT}		s
DIGITAL I/O							
V_{IH}	High-level input voltage			0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage			0		0.3 × V_{IO}	V
I_{IH}	High-level input current				0.5	10	µA
I_{IL}	Low-level input current				0.5	10	µA

(1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.

Electrical Characteristics (continued)

T_A = 25°C, V_{DD} = 3.3 V = V_{IO} = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_O = –4 mA		0.8 × V_{IO}		V_{IO}	V
V_{OL}	Low-level output voltage	I_O = 4 mA		0		0.2 × V_{IO}	V
C_{IN}	Input capacitance				3		pF
POWER SUPPLY							
V_{DD}	VDD operating voltage			3	3.3	3.6	V
V_{IO}	VIO operating voltage			1.65	3.3	3.6	V
I_{DD}	VDD supply current	V_{DD} = V_{IO} = 3.3 V, $\overline{RST}$ = 0, No clocks, f_{SIN} = 192 kHz, f_{SOUT} = 192 kHz	Power down			100	µA
			Dynamic		66		mA
I_{IO}	VIO supply current	V_{DD} = V_{IO} = 3.3 V, $\overline{RST}$ = 0, No clocks, f_{SIN} = 192 kHz, f_{SOUT} = 192 kHz	Power down			100	µA
			Dynamic		2		mA
P_D	Power dissipation	V_{DD} = V_{IO} = 3.3 V, $\overline{RST}$ = 0, No clocks, f_{SIN} = 192 kHz, f_{SOUT} = 192 kHz	Power down			660	µW
			Dynamic		225		mW

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
REFERENCE CLOCK TIMING					
	RCKI frequency(1)(2)		128 × f_{SMIN}	50	MHz
t_{RCKIP}	RCKI period		20	1 / (128 × f_{SMIN})	ns
t_{RCKIH}	RCKI pulse width HIGH		0.4 × t_{RCKIP}		ns
t_{RCKIL}	RCKI pulse width LOW		0.4 × t_{RCKIP}		ns
RESET TIMING					
t_{RSTL}	$\overline{RST}$ pulse width LOW		500		ns
INPUT SERIAL PORT TIMING					
t_{LRIS}	LRCKI to BCKI setup time		10		ns
t_{SIH}	BCKI pulse width HIGH		10		ns
t_{SIL}	BCKI pulse width LOW		10		ns
t_{LDIS}	SDIN data setup time		10		ns
t_{LDIH}	SDIN data hold time		10		ns
OUTPUT SERIAL PORT TIMING					
t_{DOPD}	SDOUT data delay time			10	ns
t_{DOH}	SDOUT data hold time		2		ns
t_{SOH}	BCKO pulsewidth HIGH		10		ns
t_{SOL}	BCKO pulse width LOW		5		ns
TDM MODE TIMING					
t_{LROS}	LRCKO setup time		10		ns
t_{LROH}	LRCKO hold time		10		ns
t_{TDMS}	TDMI data setup time		10		ns
t_{TDMH}	TDMI data hold time		10		ns

(1) f_{SMIN} = minimum (f_{SIN}, f_{SOUT}).
(2) f_{SMAX} = maximum (f_{SIN}, f_{SOUT}).

6.7 Typical Characteristics

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

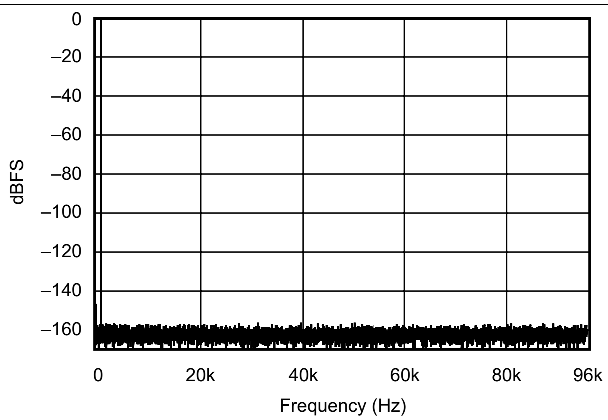


Figure 1. FFT With 1 kHz Input Tone at 0 dBFS (12 kHz:192 kHz)

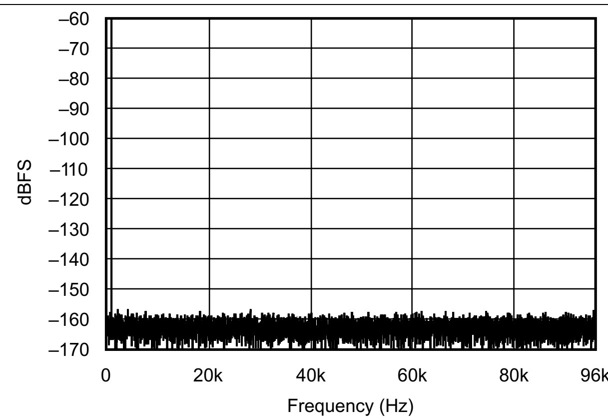


Figure 2. FFT With 1 kHz Input Tone at –60 dBFS (12 kHz:192 kHz)

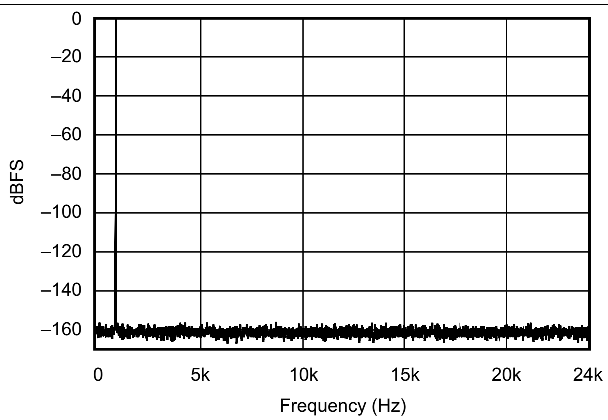


Figure 3. FFT With 1 kHz Input Tone at 0 dBFS (32 kHz:48 kHz)

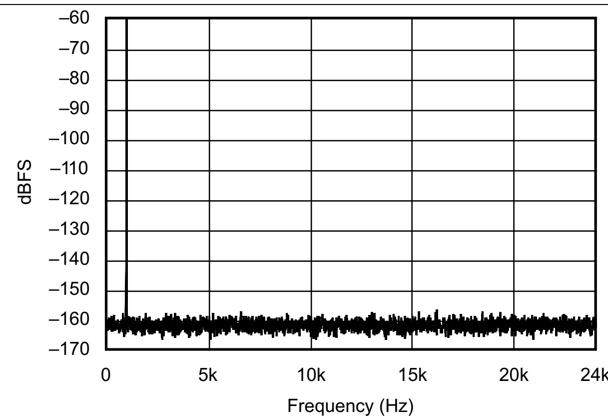


Figure 4. FFT With 1 kHz Input Tone at –60 dBFS (32 kHz:48 kHz)

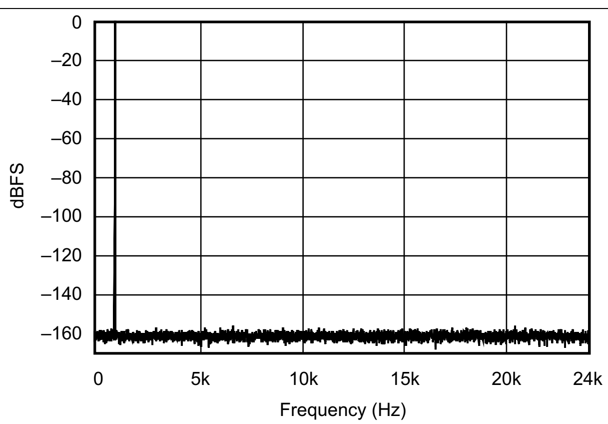


Figure 5. FFT With 1 kHz Input Tone at 0 dBFS (44.1 kHz:48 kHz)

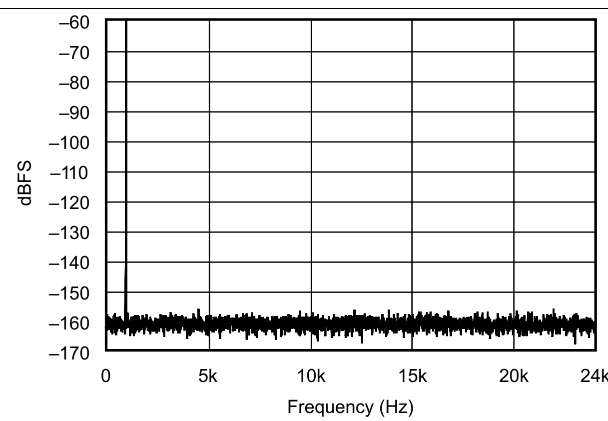


Figure 6. FFT With 1 kHz Input Tone at –60 dBFS (44.1 kHz:48 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

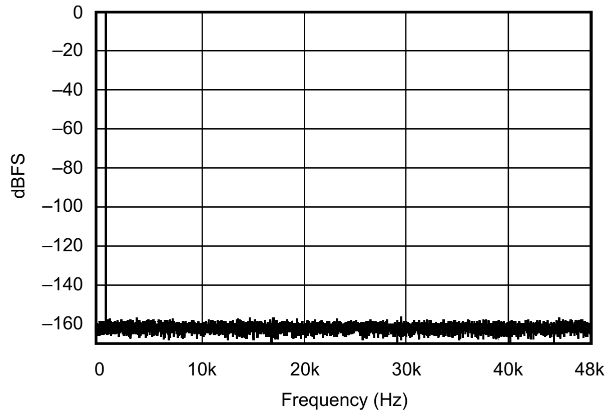


Figure 7. FFT With 1 kHz Input Tone at 0 dBFS (44.1 kHz:96 kHz)

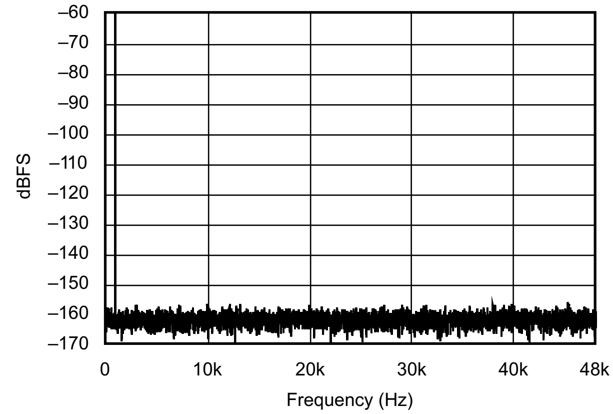


Figure 8. FFT With 1 kHz Input Tone at –60 dBFS (44.1 kHz:96 kHz)

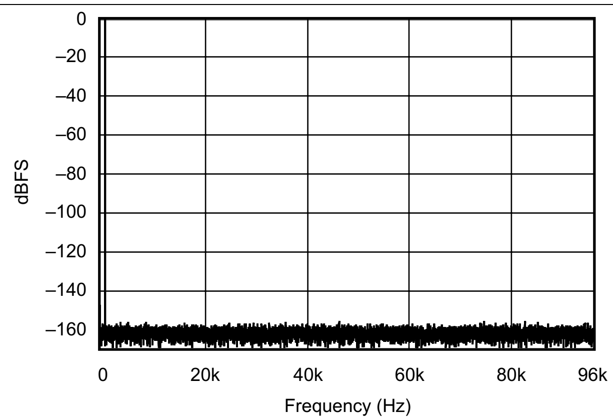


Figure 9. FFT With 1 kHz Input Tone at 0d BFS (44.1 kHz:192 kHz)

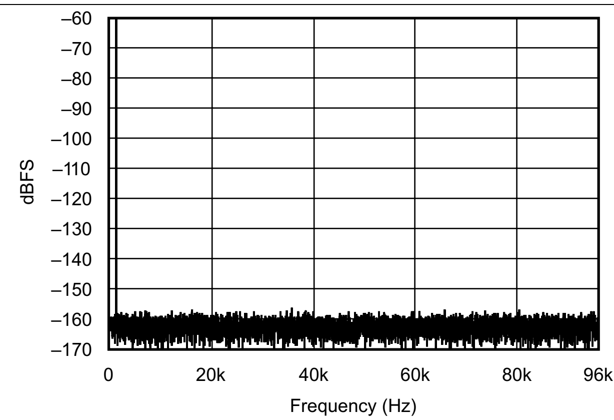


Figure 10. FFT With 1 kHz Input Tone at –60 dBFS (44.1 kHz:192 kHz)

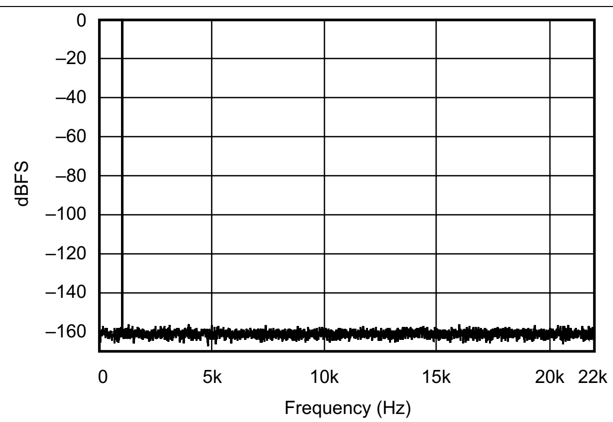


Figure 11. FFT With 1 kHz Input Tone at 0 dBFS (48 kHz:44.1 kHz)

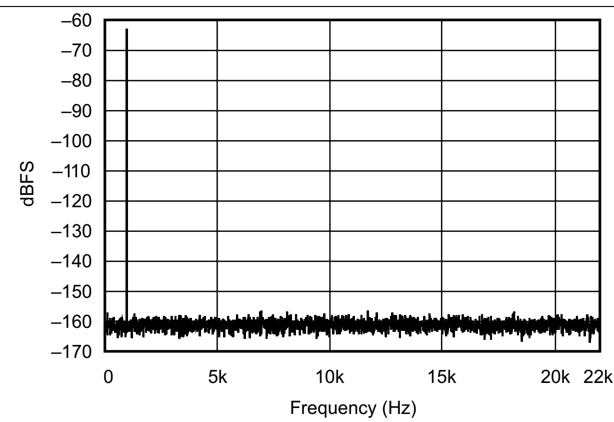


Figure 12. FFT With 1 kHz Input Tone at –60 dBFS (48 kHz:44.1 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

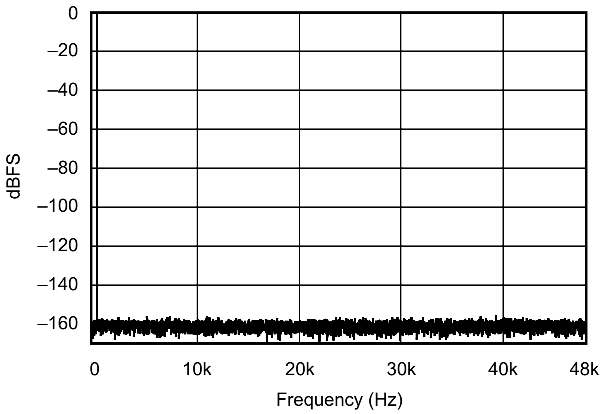


Figure 13. FFT With 1 kHz Input Tone at 0 dBFS (48 kHz:96 kHz)

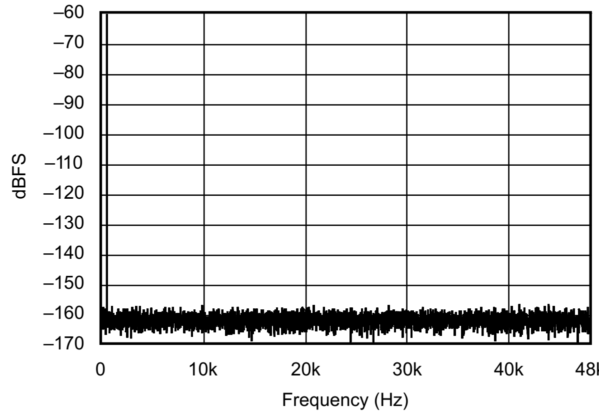


Figure 14. FFT With 1 kHz Input Tone at –60 dBFS (48 kHz:96 kHz)

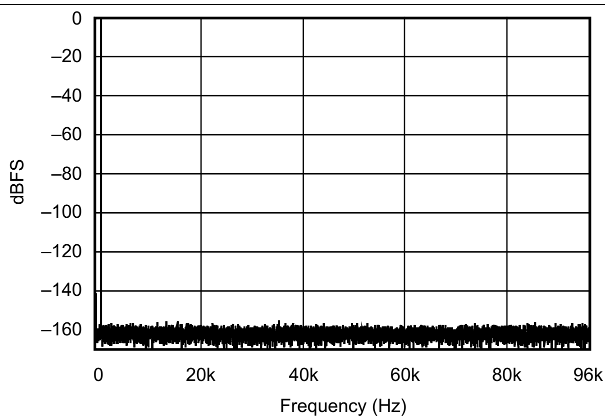


Figure 15. FFT With 1 kHz Input Tone at 0 dBFS (48 kHz:192 kHz)

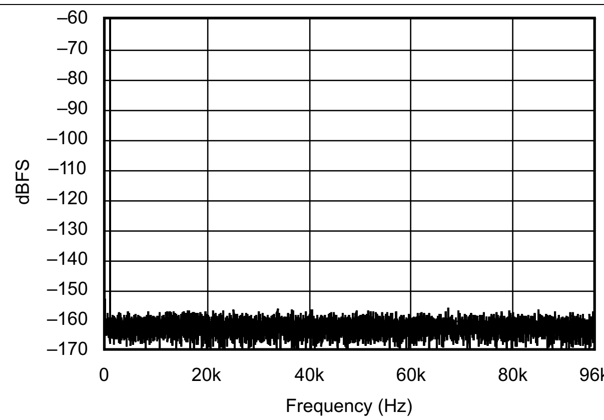


Figure 16. FFT With 1 kHz Input Tone at –60 dBFS (48 kHz:192 kHz)

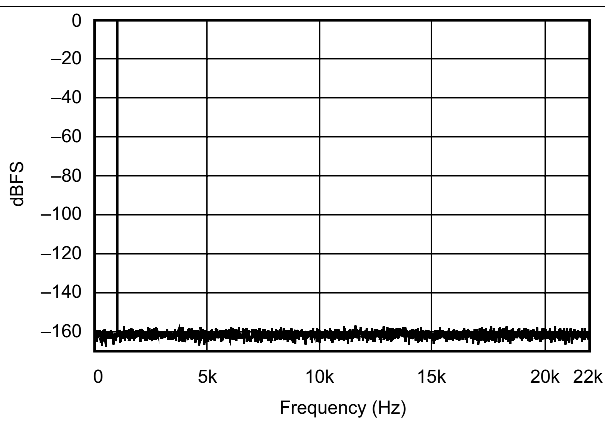


Figure 17. FFT With 1 kHz Input Tone at 0 dBFS (96 kHz:44.1 kHz)

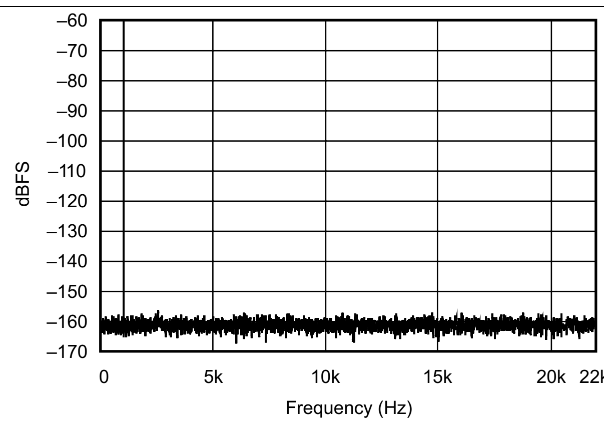


Figure 18. FFT With 1 kHz Input Tone at –60 dBFS (96 kHz:44.1 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

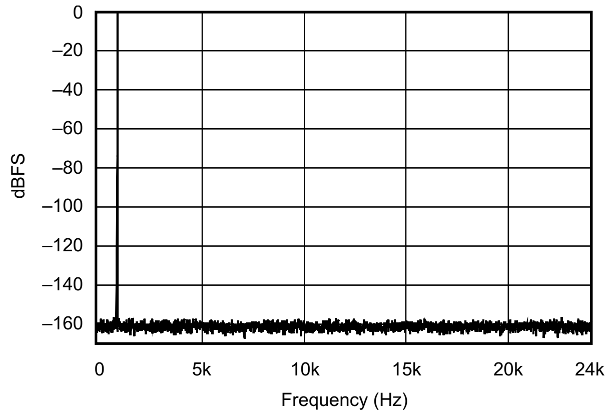


Figure 19. FFT With 1 kHz Input Tone at 0 dBFS (96 kHz:48 kHz)

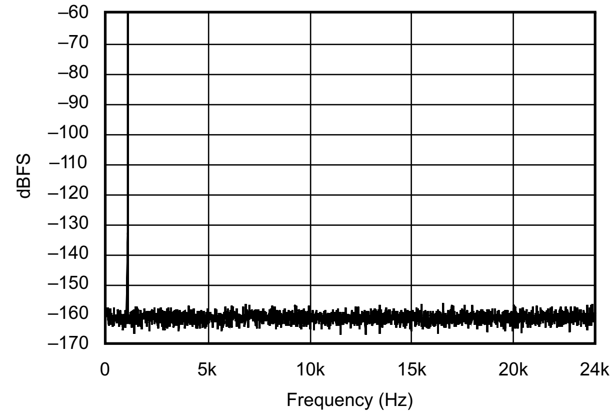


Figure 20. FFT With 1 kHz Input Tone at –60 dBFS (96 kHz:48 kHz)

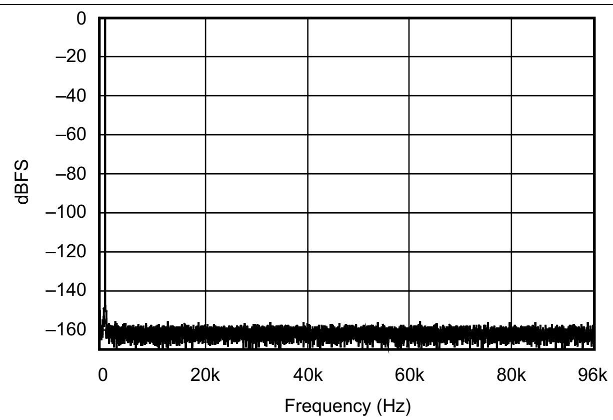


Figure 21. FFT With 1 kHz Input Tone at 0 dBFS (96 kHz:192 kHz)

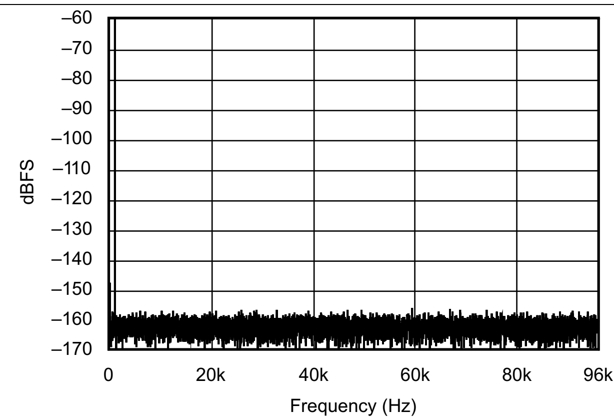


Figure 22. FFT With 1 kHz Input Tone at –60 dBFS (96 kHz:192 kHz)

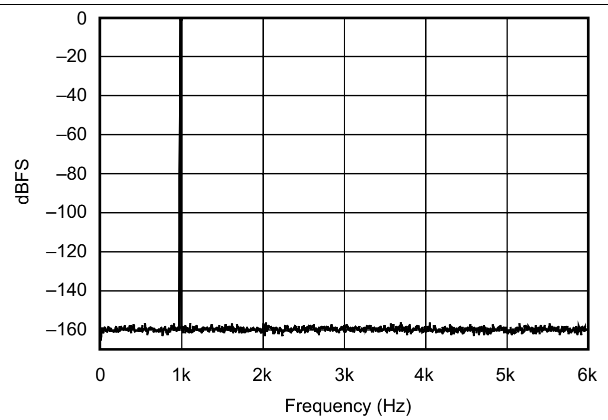


Figure 23. FFT With 1 kHz Input Tone at 0 dBFS (192 kHz:12 kHz)

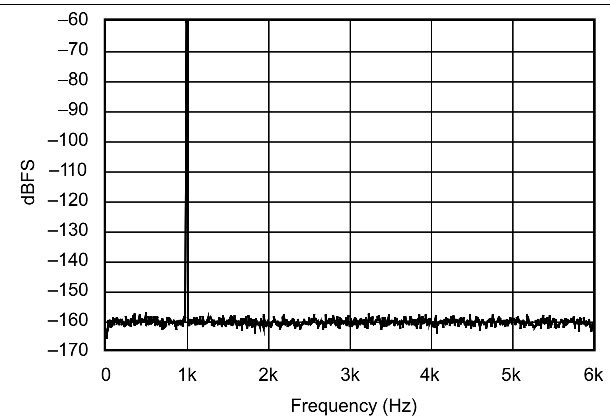


Figure 24. FFT With 1 kHz Input Tone at –60 dBFS (192 kHz:12 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

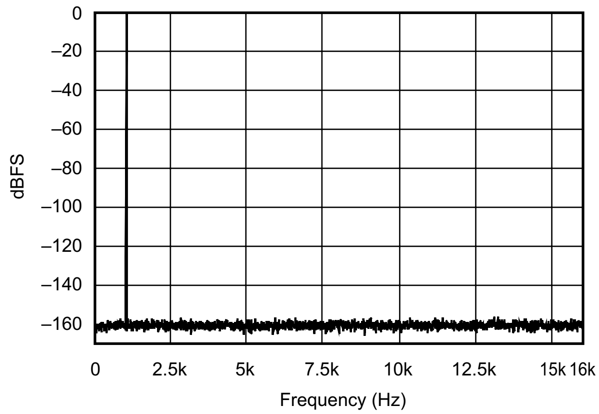


Figure 25. FFT With 1 kHz Input Tone at 0 dBFS (192 kHz:32 kHz)

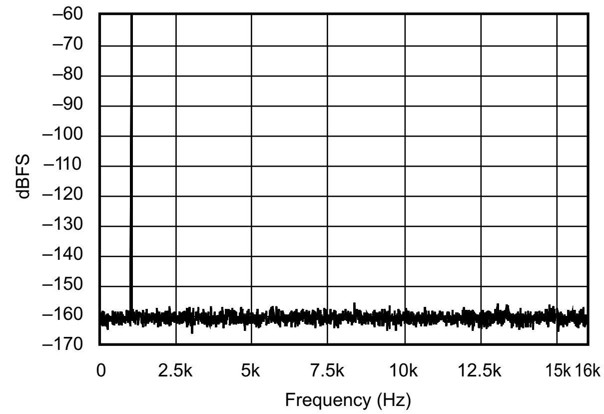


Figure 26. FFT With 1 kHz Input Tone at –60 dBFS (192 kHz:12 kHz)

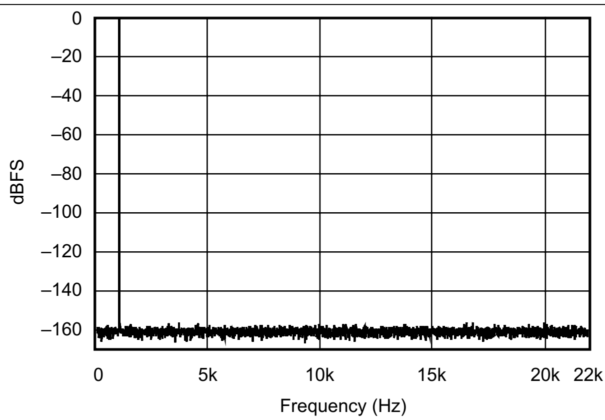


Figure 27. FFT With 1 kHz Input Tone at 0 dBFS (192 kHz:44.1 kHz)

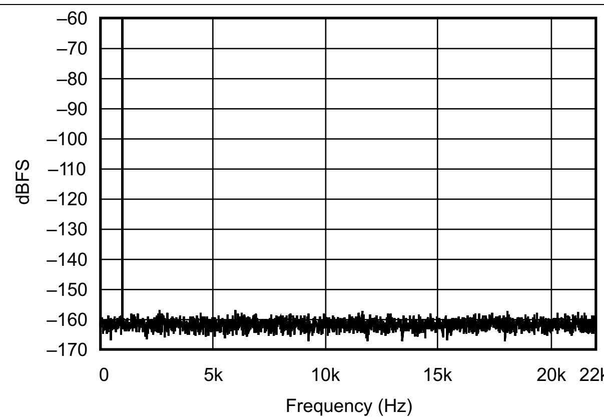


Figure 28. FFT With 1 kHz Input Tone at –60 dBFS (192 kHz:44.1 kHz)

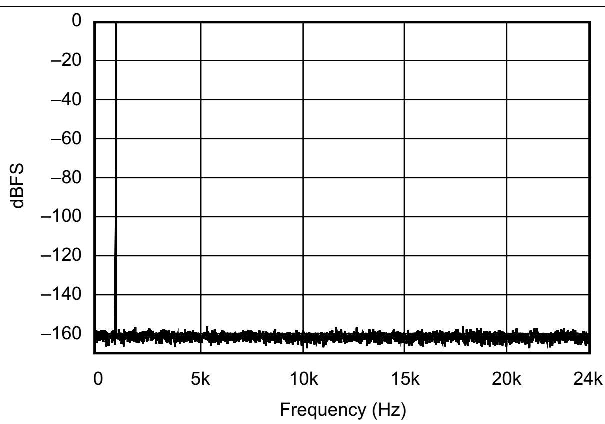


Figure 29. FFT With 1 kHz Input Tone at 0 dBFS (192 kHz:48 kHz)

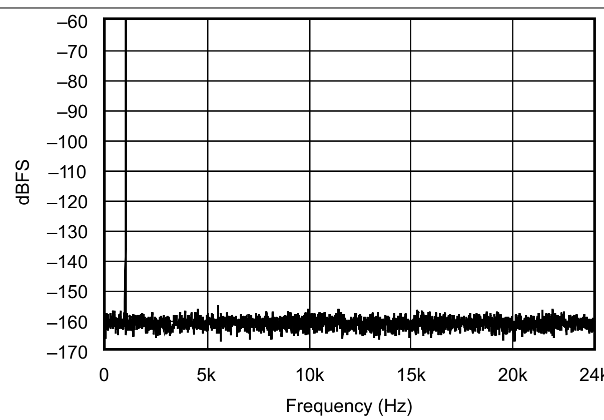


Figure 30. FFT With 1 kHz Input Tone at –60 dBFS (192 kHz:48 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

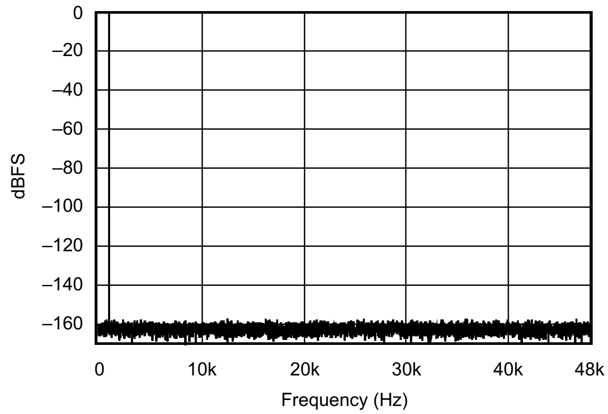


Figure 31. FFT With 1 kHz Input Tone at 0 dBFS (192 kHz:96 kHz)

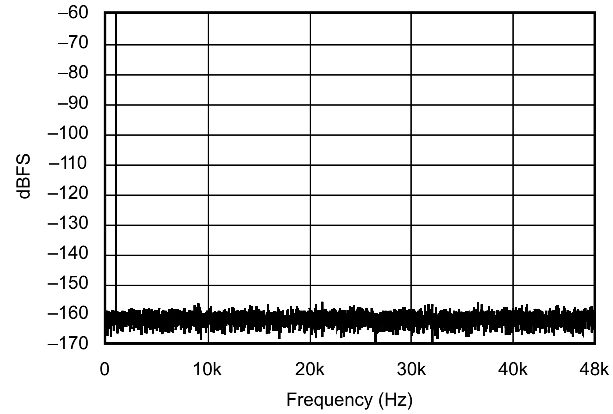


Figure 32. FFT With 1 kHz Input Tone at –60 dBFS (192kHz:96 kHz)

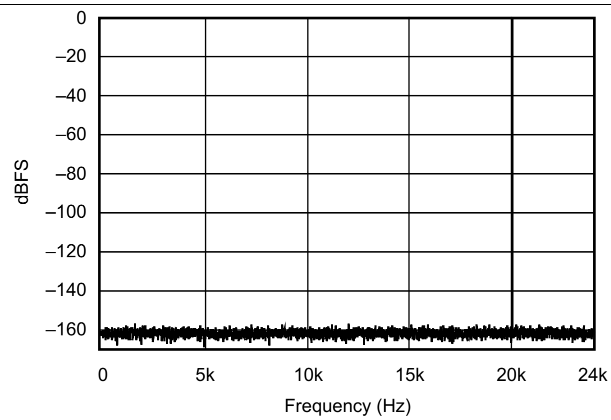


Figure 33. FFT With 20 kHz Input Tone at 0 dBFS (44.1 kHz:48 kHz)

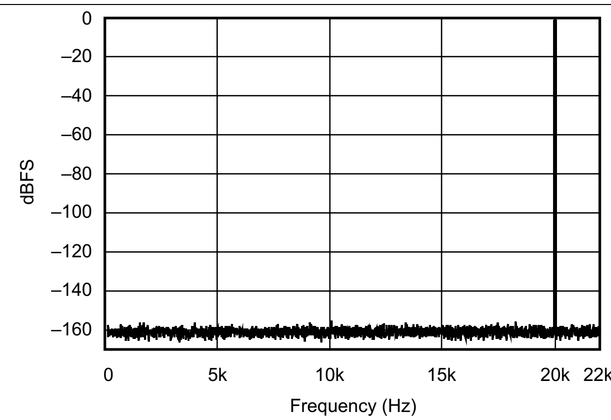


Figure 34. FFT With 20 kHz Input Tone at 0 dBFS (48 kHz:44.1 kHz)

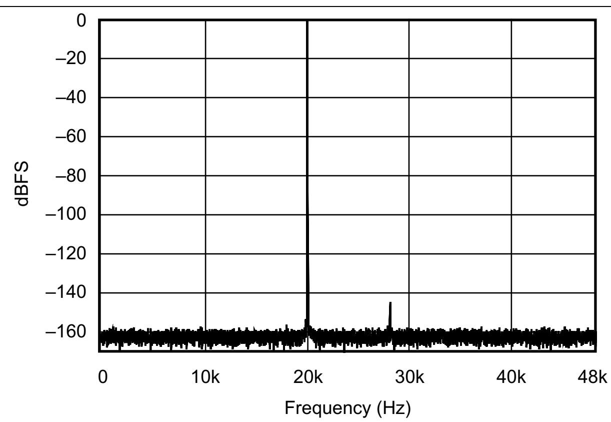


Figure 35. FFT With 20 kHz Input Tone at 0 dBFS (48 kHz:96 kHz)

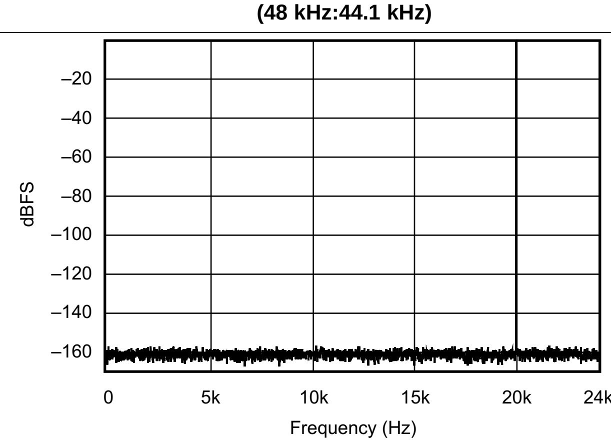


Figure 36. FFT With 20 kHz Input Tone at 0 dBFS (96 kHz:48 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

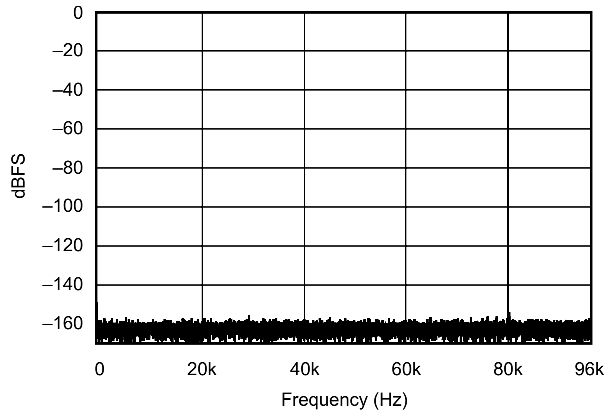


Figure 37. FFT With 80 kHz Input Tone at 0 dBFS (192 kHz:192 kHz)

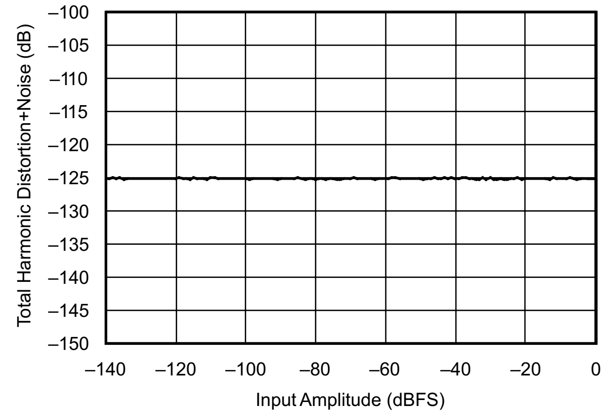


Figure 38. THD+N vs Input Amplitude f_{IN} = 1 kHz (44.1 kHz:48 kHz)

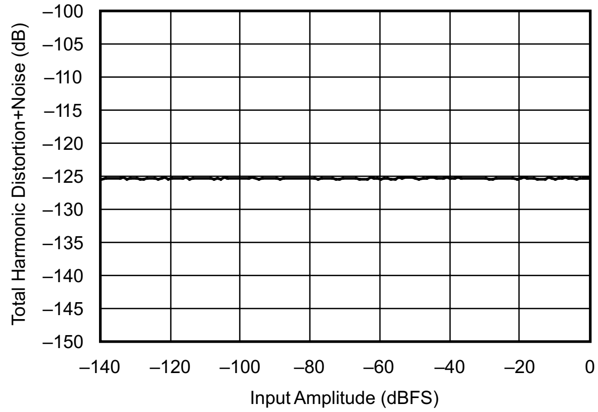


Figure 39. THD+N vs Input Amplitude f_{IN} = 1 kHz (48 kHz:44.1 kHz)

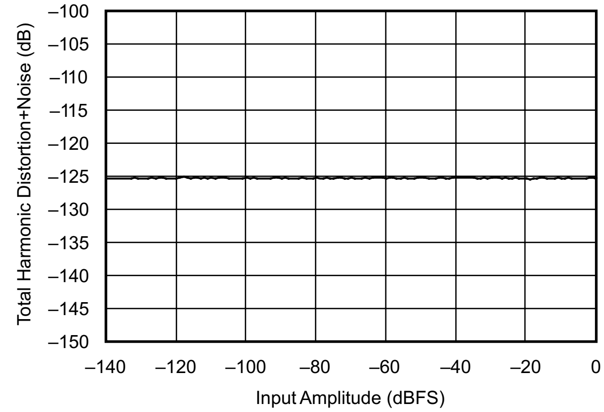


Figure 40. THD+N vs Input Amplitude f_{IN} = 1 kHz (48 kHz:96 kHz)

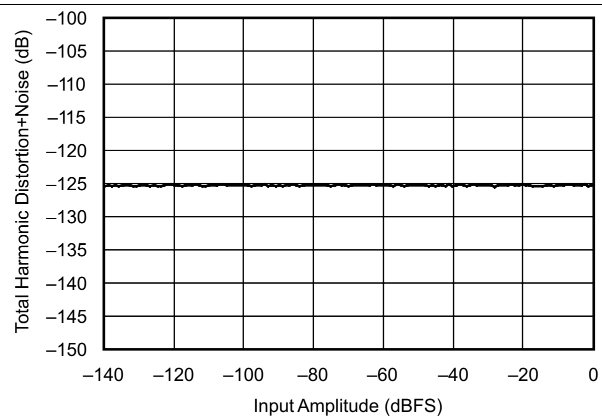


Figure 41. THD+N vs Input Amplitude f_{IN} = 1 kHz (96 kHz:48 kHz)

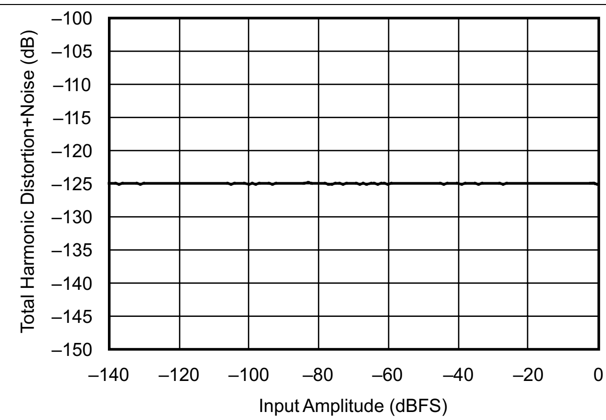


Figure 42. THD+N vs Input Amplitude f_{IN} = 1 kHz (44.1 kHz:192 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

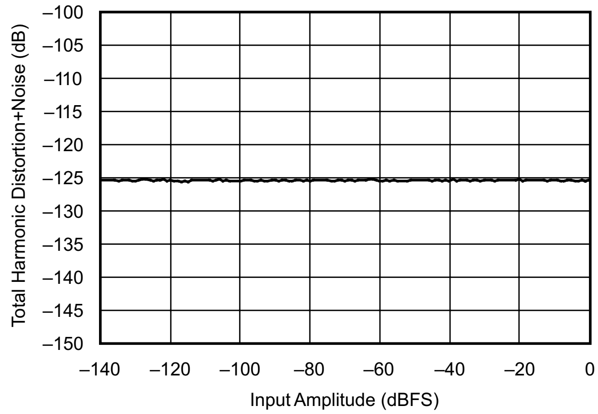


Figure 43. THD+N vs Input Amplitude f_{IN} = 1 kHz (192 kHz:44.1 kHz)

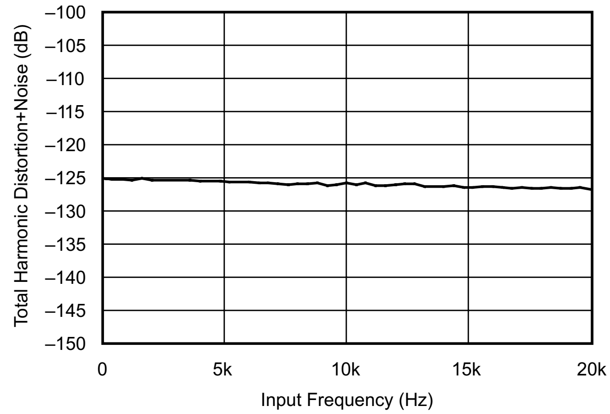


Figure 44. THD+N vs Input Frequency With 0 dBFS Input (44.1 kHz:48 kHz)

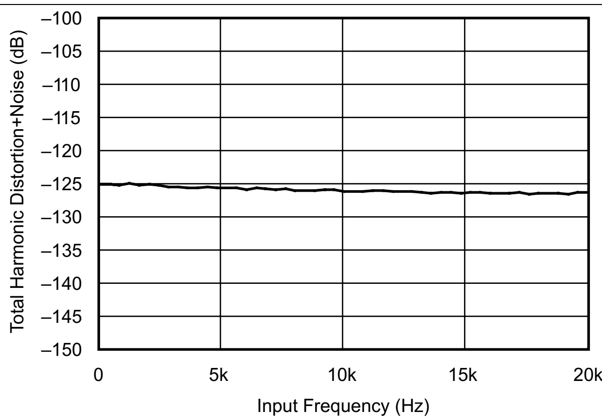


Figure 45. THD+N vs Input Frequency With 0 dBFS Input = 1 kHz (48 kHz:44.1 kHz)

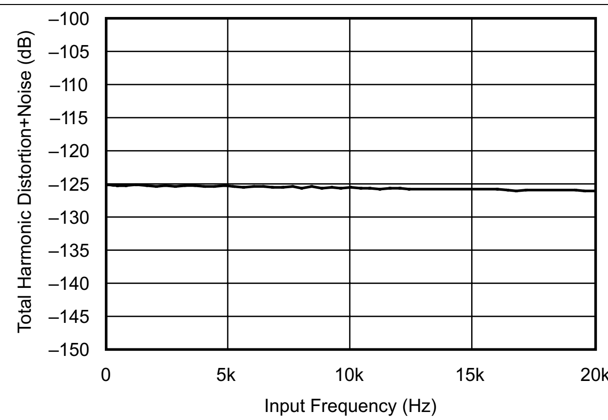


Figure 46. THD+N vs Input Frequency With 0 dBFS (48 kHz:96 kHz)

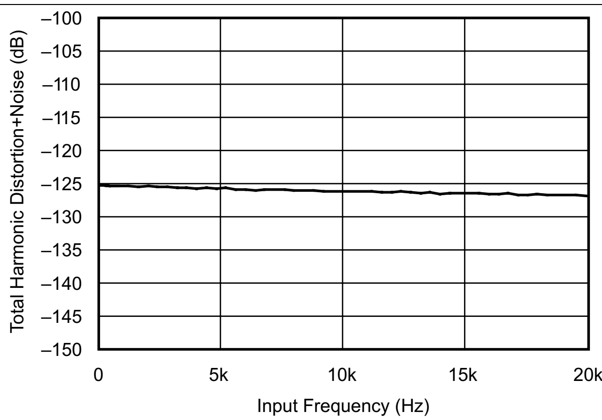


Figure 47. THD+N vs Input Frequency With 0 dBFS (96 kHz:48 kHz)

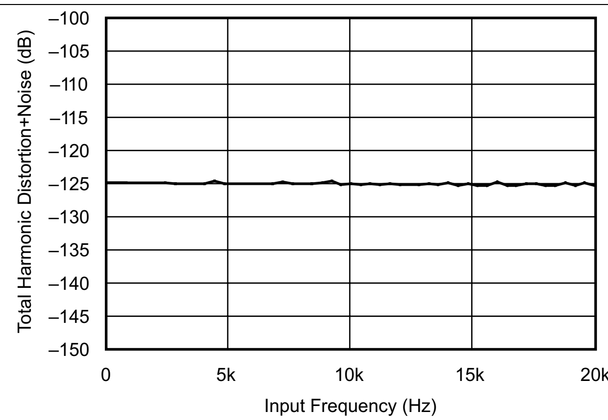


Figure 48. THD+N vs Input Frequency With 0 dBFS (44.1 kHz:192 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

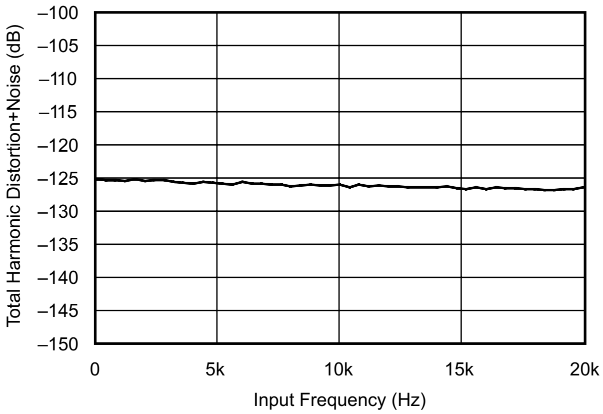


Figure 49. THD+N vs Input Frequency With 0 dBFS (192 kHz:44.1 kHz)

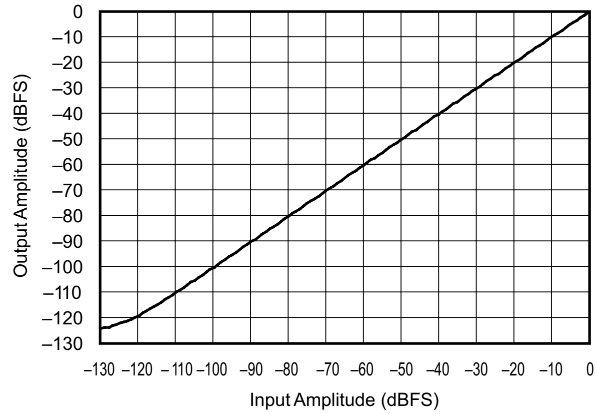


Figure 50. Linearity With f_{IN} = 200 Hz (44.1 kHz:48 kHz)

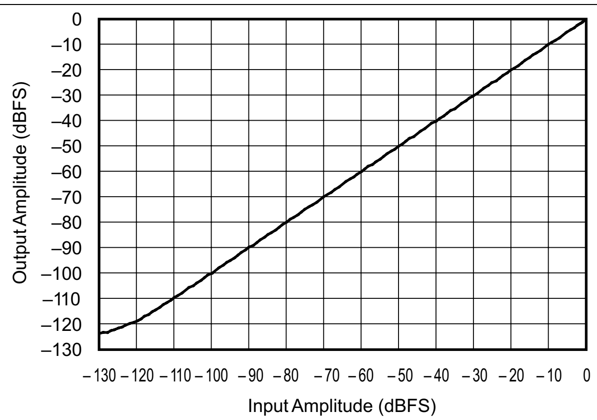


Figure 51. Linearity With f_{IN} = 200 Hz (48 kHz:44.1 kHz)

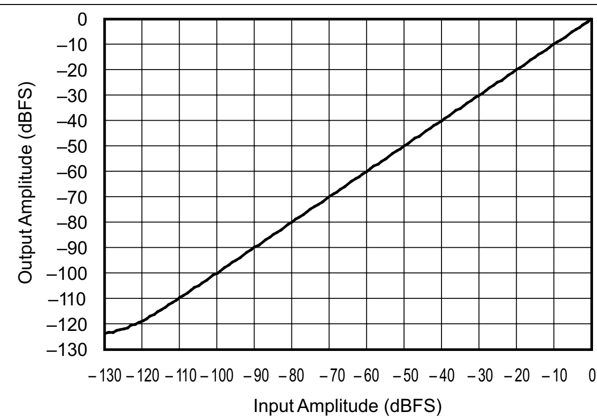


Figure 52. Linearity With f_{IN} = 200 Hz (48 kHz:96 kHz)

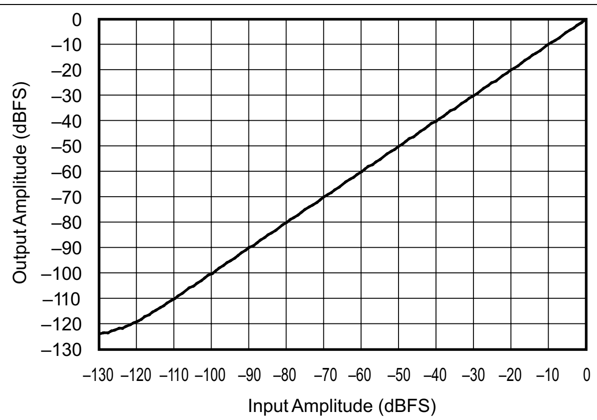


Figure 53. Linearity With f_{IN} = 200 Hz (96 kHz:48 kHz)

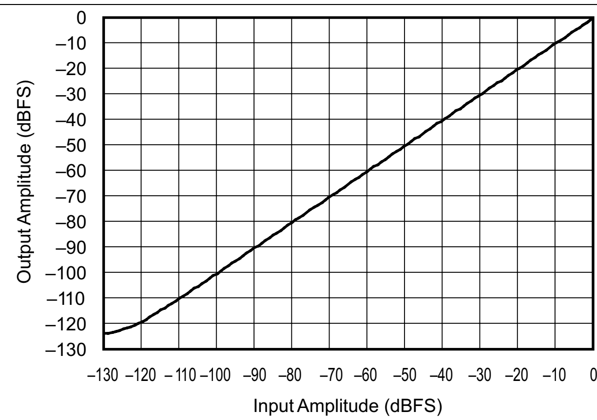


Figure 54. Linearity With f_{IN} = 200 Hz (44.1 kHz:192 kHz)

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = V_{IO} = 3.3 V (unless otherwise noted).

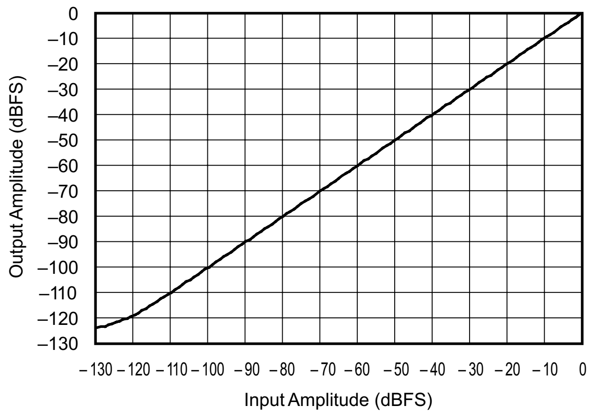


Figure 55. Linearity With f_{IN} = 200 Hz (192 kHz:44.1 kHz)

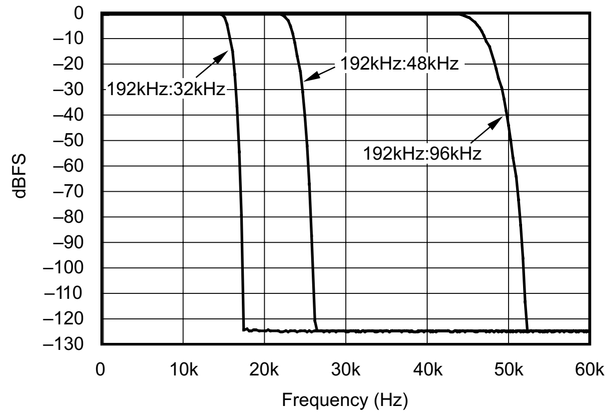


Figure 56. Frequency Response With 0 dBFS Input

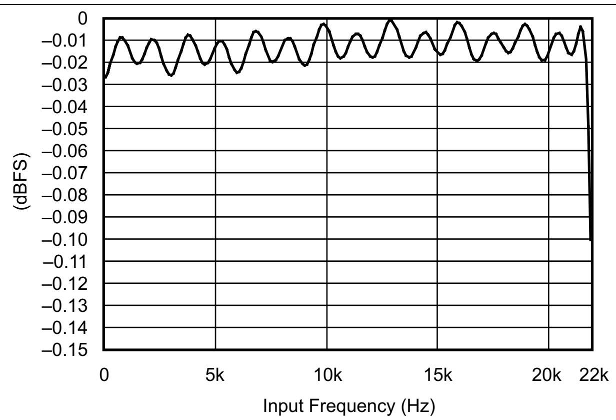


Figure 57. Passband Ripple (48 kHz:48 kHz)

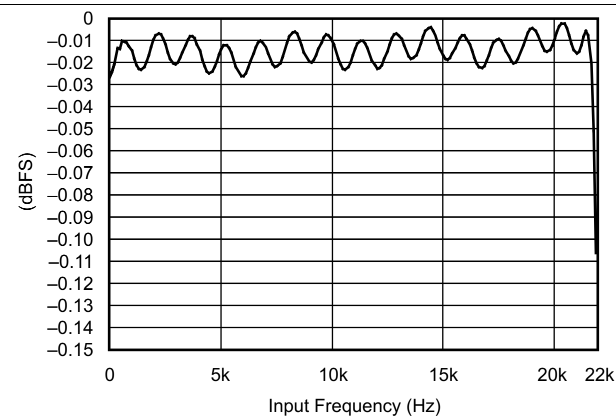


Figure 58. Passband Ripple (192 kHz:48 kHz)

7 Detailed Description

7.1 Overview

The SRC4190 device is an asynchronous sample rate converter (ASRC) designed for professional audio applications. Operation at input and output sampling frequencies up to 212 kHz is supported, with an input-to-output sampling ratio from 16:1 to 1:16. Excellent dynamic range and total harmonic distortion plus noise (THD+N) are achieved by employing high performance and linear phase digital filtering. Digital filtering options allow for lower group delay processing.

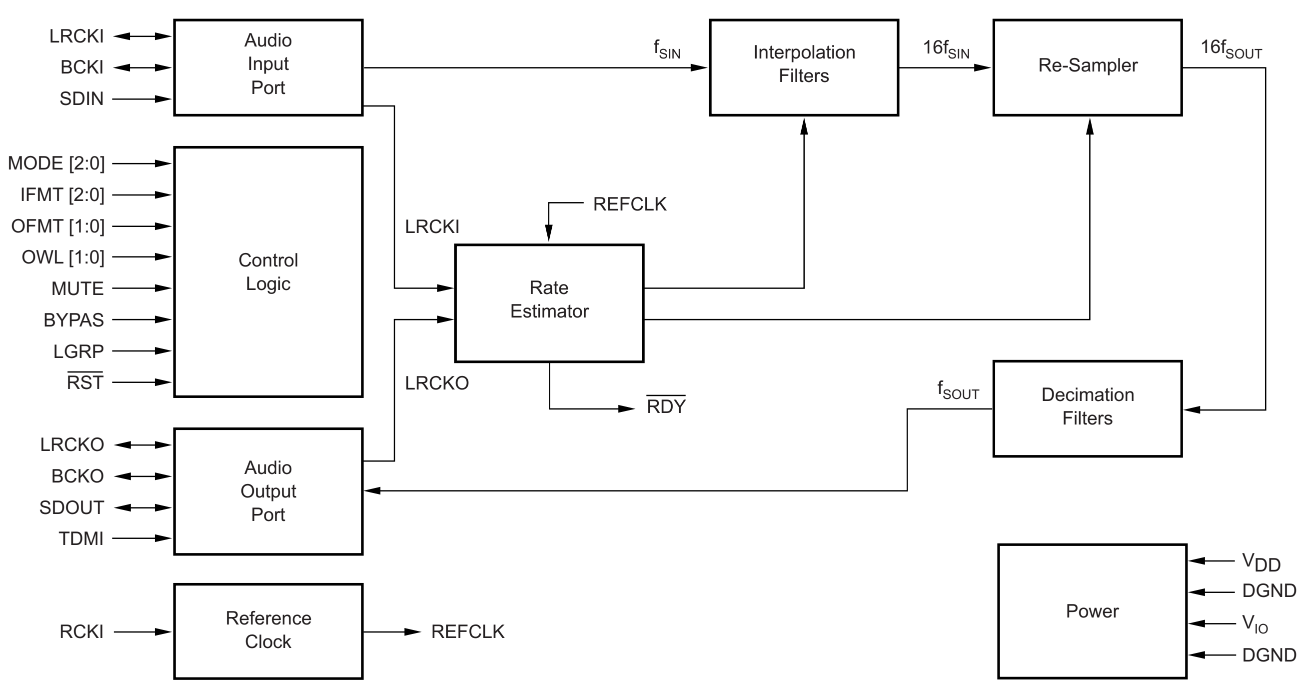
The audio input and output ports support standard audio data formats, as well as a TDM interface mode. 24-, 20-, 18-, and 16-bit word lengths are supported. Both ports may operate in slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in master mode while the other remains in slave mode. In master mode, the LRCK and BCK clocks are derived from the reference clock input (RCKI). The flexible configuration of the input and output ports allows connection to a wide variety of audio data converters, interface devices, digital signal processors, and programmable logic.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through encoded or compressed audio data, or nonaudio control or status data.

A soft mute function is available providing artifact-free operation while muting the audio output signal. The mute attenuation is typically –128 dB.

The output port data is clocked by either the audio data source in slave mode, or by the SRC4190 in master mode. The input data is passed through interpolation filters which up-sample the data, which is then passed on to the re-sampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results include an offset for the FIFO pointer and the coefficients needed for re-sampling function. The output of the re-sampler is then passed on to the decimation filter. The decimation filter performs down-sampling and anti-alias filtering functions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Mute Function

The soft mute function of the SRC4190 may be invoked by forcing the MUTE pin high. The soft mute function slowly attenuates the output signal level down to all zeroes plus ±4 LSB of dither. This provides an artifact-free muting of the audio output port.

7.3.2 Ready Output

The SRC4190 includes an active low ready output (RDY). This is an output from the rate estimator block, which indicates that the input-to-output sampling frequency ratio has been determined. The ready signal can be used as a flag or indicator output. The ready signal can also be connected to the active high MUTE pin to provide an auto-mute function, so that the output port is muted when the rate estimator is in transition.

7.4 Device Functional Modes

7.4.1 Bypass Mode

The SRC4190 includes a bypass function, which routes the input port data directly to the output port, bypassing the ASRC function. Bypass mode may be invoked by forcing the BYPAS pin high. For normal ASRC operation, the BYPAS pin must be set to 0.

No dithering is applied to the output data in bypass mode; digital attenuation and mute functions are also unavailable in this mode.

7.4.2 Audio Port Modes

The SRC4190 supports seven serial port modes, shown in Table 1. The audio port mode is selected using the MODE0, MODE1, and MODE2 pins.

In slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input (RCKI). Only one port can be set to master mode at any given time, as indicated in Table 1.

Table 1. Setting the Serial Port Modes

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	0	0	Both input and output ports are slave mode
0	0	1	Output port is master mode with RCKI = 128 f_S
0	1	0	Output port is master mode with RCKI = 512 f_S
0	1	1	Output port is master mode with RCKI = 256 f_S
1	0	0	Both input and output ports are slave mode
1	0	1	Input port is master mode with RCKI = 128 f_S
1	1	0	Input port is master mode with RCKI = 512 f_S
1	1	1	Input port is master mode with RCKI = 256 f_S

7.4.3 Input Port Operation

The audio input port is a three-wire synchronous serial interface that may operate in either slave or master mode. The SDIN pin 4 is the serial audio data input. Audio data is input at this pin in one of three standard audio data formats: Philips I^2S, Left Justified, or Right Justified. The audio data word length may be up to 24 bits for I^2S and Left Justified formats, while the Right Justified format supports 16, 18, 20, or 24-bit data. The data formats are shown in Figure 59, while critical timing parameters are shown in Figure 60 and listed in *Switching Characteristics*.

The bit clock is either an input or output at BCKI. In slave mode, BCKI is configured as an input pin, and may operate at rates from 32 f_S to 128 f_S, with a minimum of one clock cycle per data bit. In master mode, BCKI operates at a fixed rate of 64 f_S.

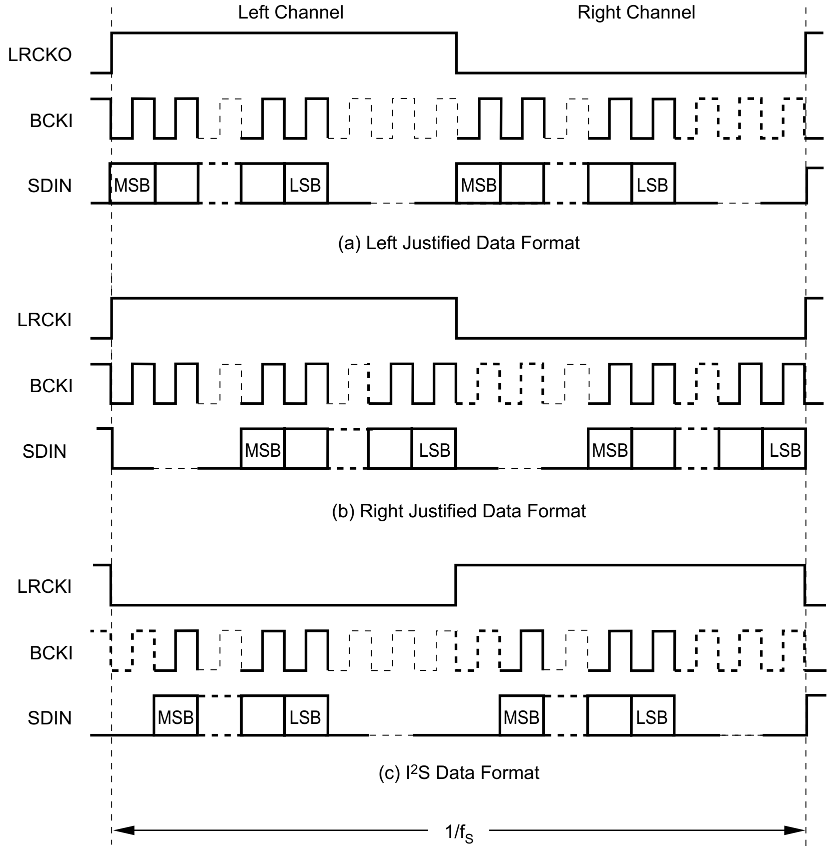


Figure 59. Input Data Formats

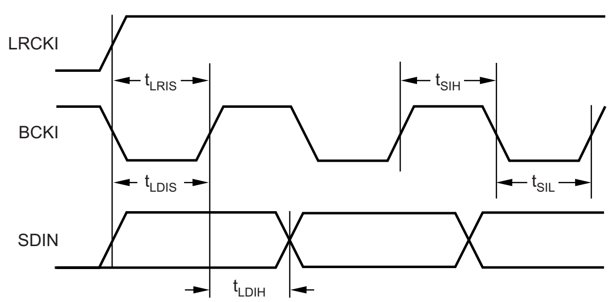


Figure 60. Input Port Timing

The left and right word clock (LRCKI), may be configured as an input or output pin. In slave mode, LRCKI is an input pin, while in master mode LRCKI is an output pin. In either case, the clock rate is equal to the input sampling frequency (f_S). The LRCKI duty cycle is fixed to 50% for master mode operation. Table 2 illustrates data format selection for the input port. The IFMT0, IFMT1, and IFMT2 pins are utilized to set the input port data format.

Table 2. Input Port Data Format Selection

IFMT2	IMFT1	IMFT0	INPUT PORT DATA FORMAT
0	0	0	24-Bit Left Justified
0	0	1	24-Bit I2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right Justified
1	0	1	18-Bit Right Justified
1	1	0	20-Bit Right Justified
1	1	1	24-Bit Right Justified

7.4.4 Output Port Operation

The audio output port is a four-wire synchronous serial interface that may operate in either slave or master mode. The SDOUTpin is the serial audio data output. Audio data is output at this pin in one of four data formats: Philips I^2S, Left Justified, Right Justified, or TDM. The audio data word length may be 16, 18, 20, or 24 bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 61, while critical timing parameters are shown in Figure 62 and listed in *Switching Characteristics*. The TDM format and timing are shown in Figure 66 and Figure 66, respectively, while examples of standard TDM configurations are shown in Figure 69 and Figure 70. The bit clock is either input or output at BCKO. In slave mode, BCKO is configured as an input pin, and may operate at rates from 32 f_S to 128 f_S, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at N × 64fS, where N is equal to the number of SRC4190 devices included on the TDM interface. In master mode, BCKO operates at a fixed rate of 64 f_S for all data formats except TDM, where BCKO operates at the reference clock (RCKI) frequency. Additional information regarding TDM mode operation is included in *Application and Implementation*.

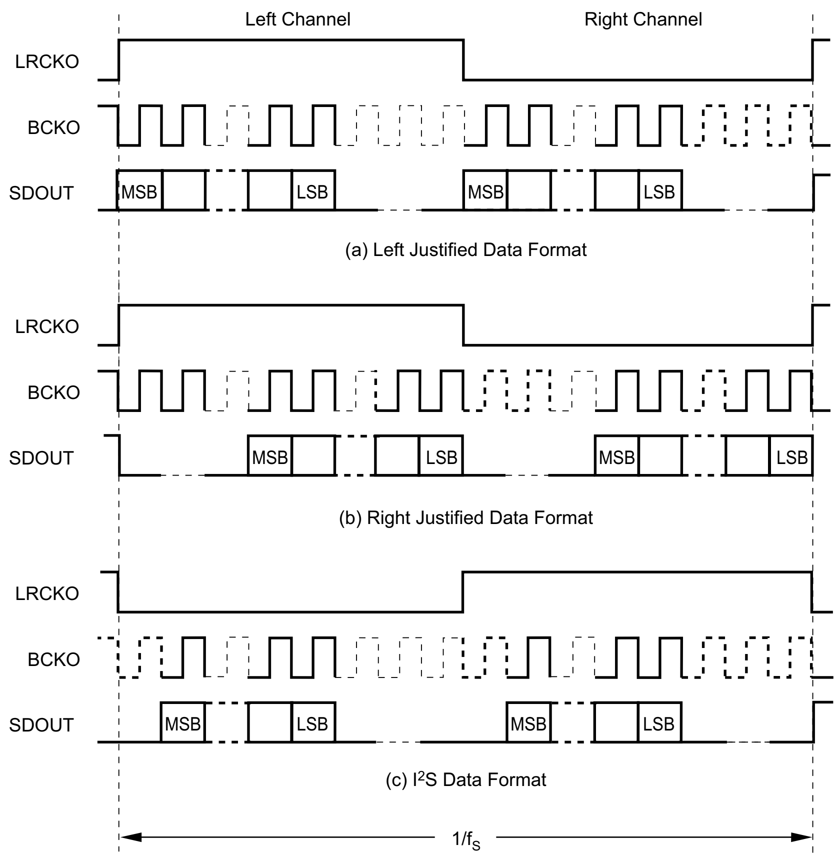


Figure 61. Output Data Formats

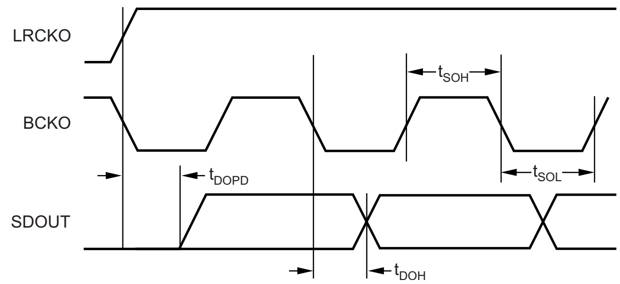


Figure 62. Output Port Timing

The left and right word clock (LRCKO), may be configured as an input or output pin. In slave mode, LRCKO is an input pin, while in master mode it is an output pin. In either case, the clock rate is equal to the output sampling frequency (f_S). The clock duty cycle is fixed to 50% for I^2S, Left Justified, and Right Justified formats in master mode. The LRCKO pulse width is fixed to 32 BCKO cycles for the TDM format in master mode.

Table 3 shows data format selection for the output port. The OFMT0, OFMT1, OWL0, and OWL1 inputs are utilized to set the output port data format and word length.

Table 3. Output Port Data Format Selection

OFMT1	OFMT0	OUTPUT PORT DATA FORMAT
0	0	Left Justified
0	1	I^2S
1	0	TDM
1	1	Right Justified
OWL1	**OWL2**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24 bits
0	1	20 bits
1	0	18 bits
1	1	16 bits

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The audio input and output ports can handle 16-, 18-, 20-, or 24-bit right-justified PCM serial data, as well as 24-bit I^2S or left-justified PCM serial data at up to 212-kHz sampling rate. A TDM format is also available. Both input and output can operate in slave mode, or one can operate as a master while the other operates as a slave. A 16:1 or 1:16 ratio is the maximum supported between the input and output audio sampling rates.

8.2 Typical Application

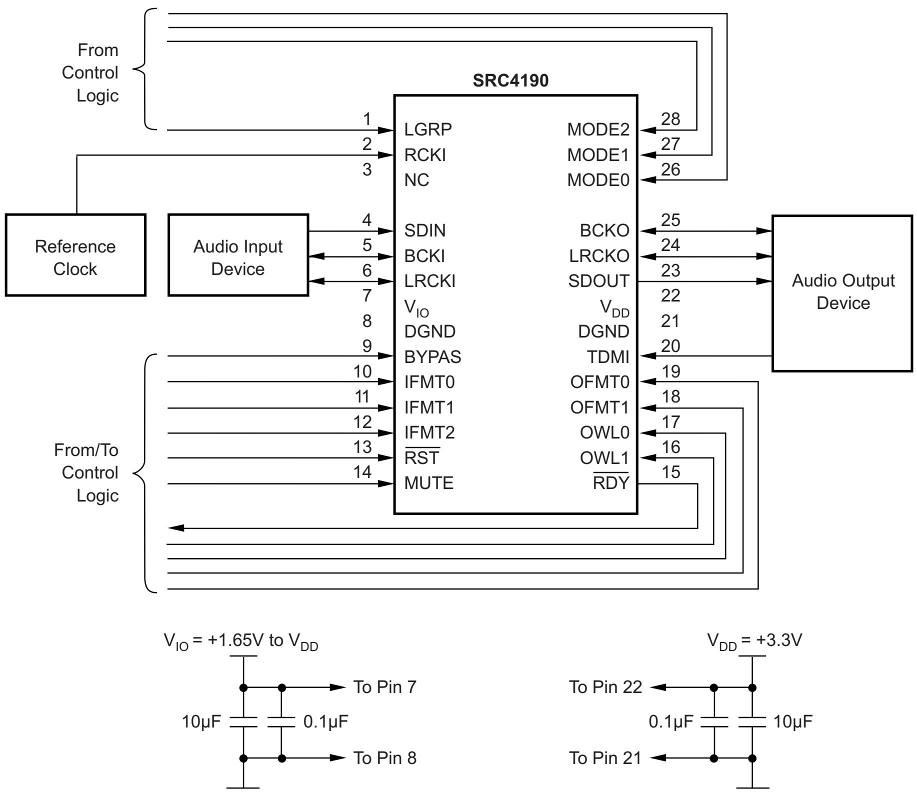


Figure 63. Typical Connection Diagram for the SRC4190

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

PARAMETER	VALUE
VDD supply voltage, V_{DD}	3.3 V
VIO supply voltage, V_{IO}	1.65 V to V_{DD}
Bypass capacitors	0.1 µF and 10 µF

8.2.2 Detailed Design Procedure

The typical connection diagram for the SRC4190 is shown in Figure 63. Recommended values for power supply bypass capacitors are included. These capacitors must be placed as close to the IC package as possible.

8.2.2.1 Reference Clock

The SRC4190 requires a reference clock for operation. The reference clock is applied at the RCKI input. Figure 64 shows the reference clock connections and requirements for the SRC4190. The reference clock may operate at 128 f_S, 256 f_S, or 512 f_S, where f_S is the input or output sampling frequency. The maximum external reference clock input frequency is 50 MHz.

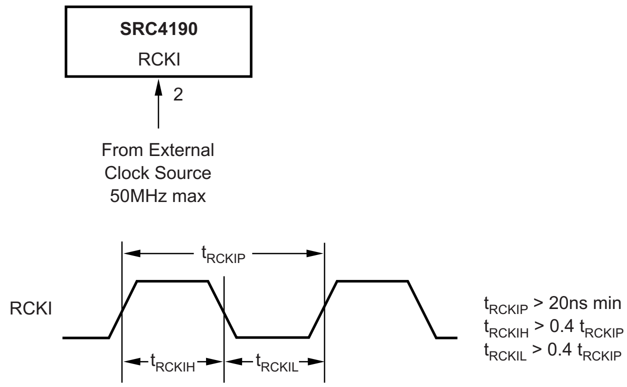
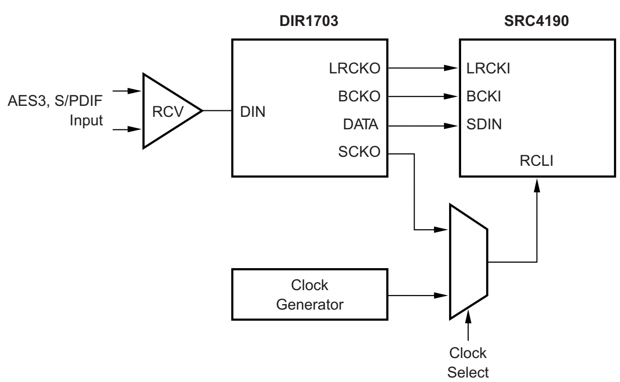


Figure 64. Reference Clock Input Connections and Timing Requirements

8.2.2.2 Interfacing to Digital Audio Receivers and Transmitters

The SRC4190 input and output ports are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications. Texas Instruments manufactures the DIR1703 digital audio interface receiver and the DIT4096 and DIT4192 digital audio transmitters to address these applications.

Figure 65 illustrates interfacing the DIR1703 to the SRC4190 input port. The DIR1703 operates from a single 3.3-V supply, which requires the VIO supply for the SRC4190 to be set to 3.3-V for interface compatibility.



Copyright © 2016, Texas Instruments Incorporated

Figure 65. Interfacing the SRC4190 to the DIR1703 Digital Audio Interface Receiver

Figure 66 shows the interface between the SRC4190 output port and the DIT4096 or DIT4192 audio serial port. Once again, the VIO supplies for both the SRC4190, DIT4096, and DIT4192 are set to 3.3 V for compatibility.

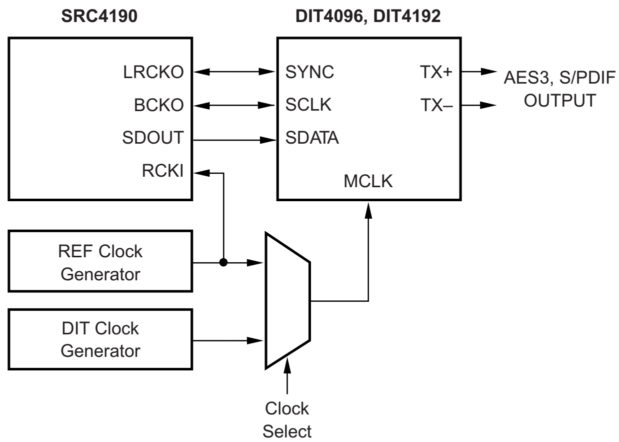
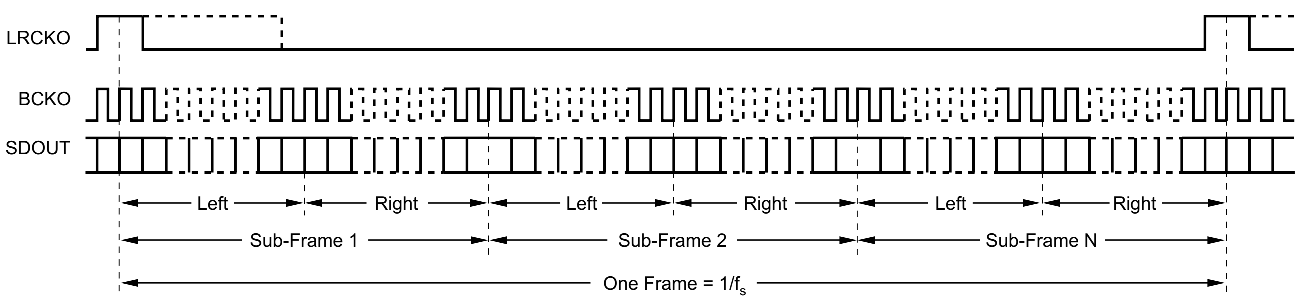


Figure 66. Interfacing the SRC4190 to the DIT4096 and DIT4192 Digital Audio Interface Transmitter

Like the SRC4190 output port, the DIT4096 and DIT4192 audio serial port may be configured as a master or slave. In cases where the SRC4190 output port is set to master mode, TI recommends using the reference clock source (RCKI) as the master clock source (MCLK) for the DIT4096 and DIT4192, to ensure that the transmitter is synchronized to the SRC4190 output port data.

8.2.2.3 TDM Applications

The SRC4190 supports a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one sub-frame within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is Left Justified within the allotted 32 bits. Figure 66 illustrates the TDM frame format, while Figure 68 shows the TDM input timing parameters, which are listed in *Switching Characteristics*.



N = Number of Daisy-Chained Devices

One Sub-Frame contains 64 bits, with 32 bits per channel.

For each channel, the audio data is Left Justified, MSB first format, with the word length determined by OWL[1:0].

Figure 67. TDM Frame Format

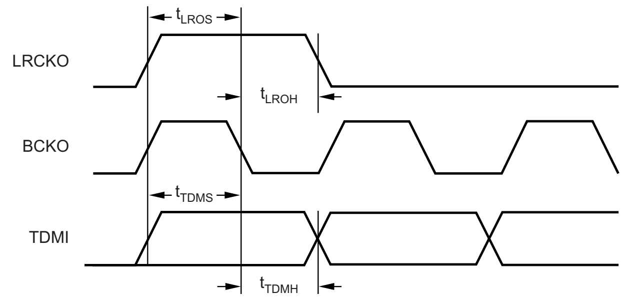


Figure 68. Input Timing for TDM Mode

The frame rate is equal to the output sampling frequency. The BCKO frequency for the TDM interface is N × 64 f_S, where N is the number of devices included in the daisy chain. For master mode, the output BCKO frequency is fixed to the reference clock (RCKI) input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the BCKO frequency, leading to the numerical relationship in Equation 1

Number of daisy-chained devices = $(f_{BCKO} / f_S) / 64$

where

- f_{BCKO} = Output port bit clock (BCKO) (27.136-MHz maximum)
- f_S = Output port sampling (LRCKO) frequency (212-kHz maximum) (1)

This relationship holds true for both slave and master modes. Figure 69 and Figure 70 show typical connection schemes for the TDM mode. Although the TMS320C671x DSP family is shown as the audio processing engine in these figures, other TI digital signal processors with a multi-channel buffered serial port (McBSPTM) may also function with this arrangement. Interfacing to processors from other manufacturers is also possible. See Figure 62, along with the equivalent serial port timing diagrams shown in the DSP data sheet, to determine compatibility.

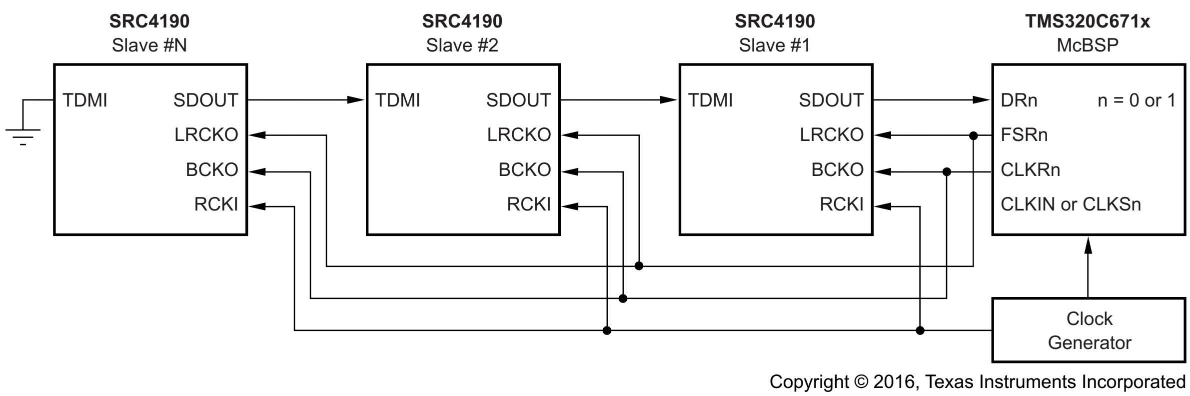


Figure 69. TDM Interface With All Devices as Slaves

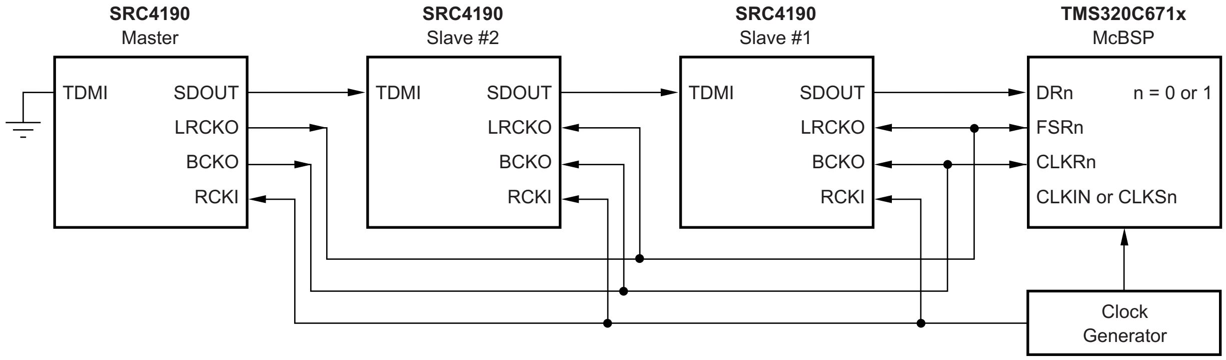


Figure 70. TDM Interface With One Device as Master to Multiple Slaves

8.2.2.4 Pin Compatibility With the Analog Devices AD1895 and AD1896

The SRC4190 is pin and function-compatible with the AD1895 and AD1896 when observing the guidelines indicated in the following paragraphs.

8.2.2.4.1 Power Supplies

To ensure compatibility, the VDD_IO and VDD_CORE supplies of the AD1895 and AD1896 must be set to 3.3 V, while the VIO and VDD supplies of the SRC4190 must be set to 3.3 V.

8.2.2.4.2 Pin 1 Connection

For the AD1895, pin 1 is not connected. For the SRC4190, pin 1 (LGRP) functions as the low group delay selection input, and must not be left unconnected. LGRP must be connected to either digital ground or the VIO supply, dependent upon the desired group delay.

8.2.2.4.3 Crystal Oscillator

The SRC4190 does not have an on-chip crystal oscillator. An external reference clock is required at the RCKI pin.

8.2.2.4.4 Reference Clock Frequency

The reference clock input frequency for the SRC4190 must be no higher than 30 MHz, in order to match the master clock frequency specification of the AD1895 and AD1896. In addition, the SRC4190 does not support the 768-f_S reference clock rate.

8.2.2.4.5 Master Mode Maximum Sampling Frequency

When the input or output ports are set to master mode, the maximum sampling frequency must be limited to 96 kHz in order to support the AD1895 and AD1896 specification. This is despite the fact that the SRC4190 supports a maximum sampling frequency of 212 kHz in master mode. The user must consider building an option into his or her design to support the higher sampling frequency of the SRC4190.

8.2.2.4.6 Matched Phase Mode

Due to the internal architecture of the SRC4190, it does not require or support the matched phase mode of the AD1896. Given multiple SRC4190 devices, if all reference clock (RCKI) inputs are driven from the same clock source, the devices is phase matched.

8.2.3 Application Curves

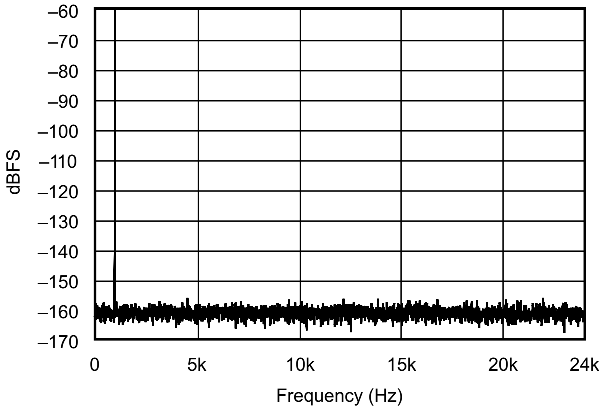


Figure 71. FFT With 1 kHz Input Tone at –60 dBFS (44.1 kHz:48 kHz)

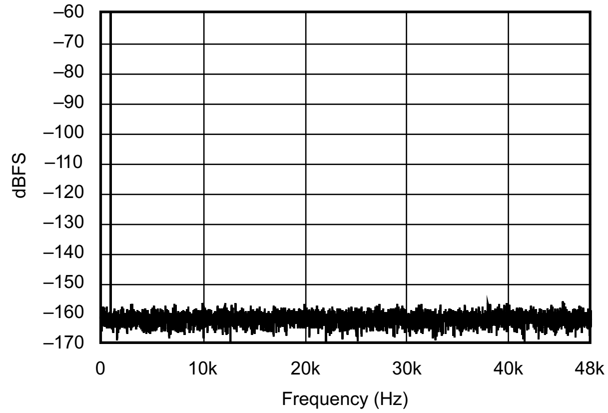


Figure 72. FFT With 1 kHz Input Tone at –60 dBFS (44.1 kHz:96 kHz)

9 Power Supply Recommendations

The SRC4190 has two supply inputs (VDD and VIO). VDD operates at 3.3 V, while VIO can operate at either 1.8 V or 3.3 V to allow interaction with a range of digital devices. TI recommends using a decoupling capacitor for each supply pin placed as close to the pin as possible.

10 Layout

10.1 Layout Guidelines

10.1.1 Power Supply Pins

Place power supply decoupling capacitors as close to the supply pins as possible to minimize noise on device supplies. TI recommends values of 10 µF and 0.1 µF for these capacitors.

10.1.2 Digital Interface

With high frequency clocks being input or produced on the digital interface pins, reflections can become an issue, causing system noise. A series resistor in the tens of ohms can be placed on each trace to minimize reflections.

10.2 Layout Example

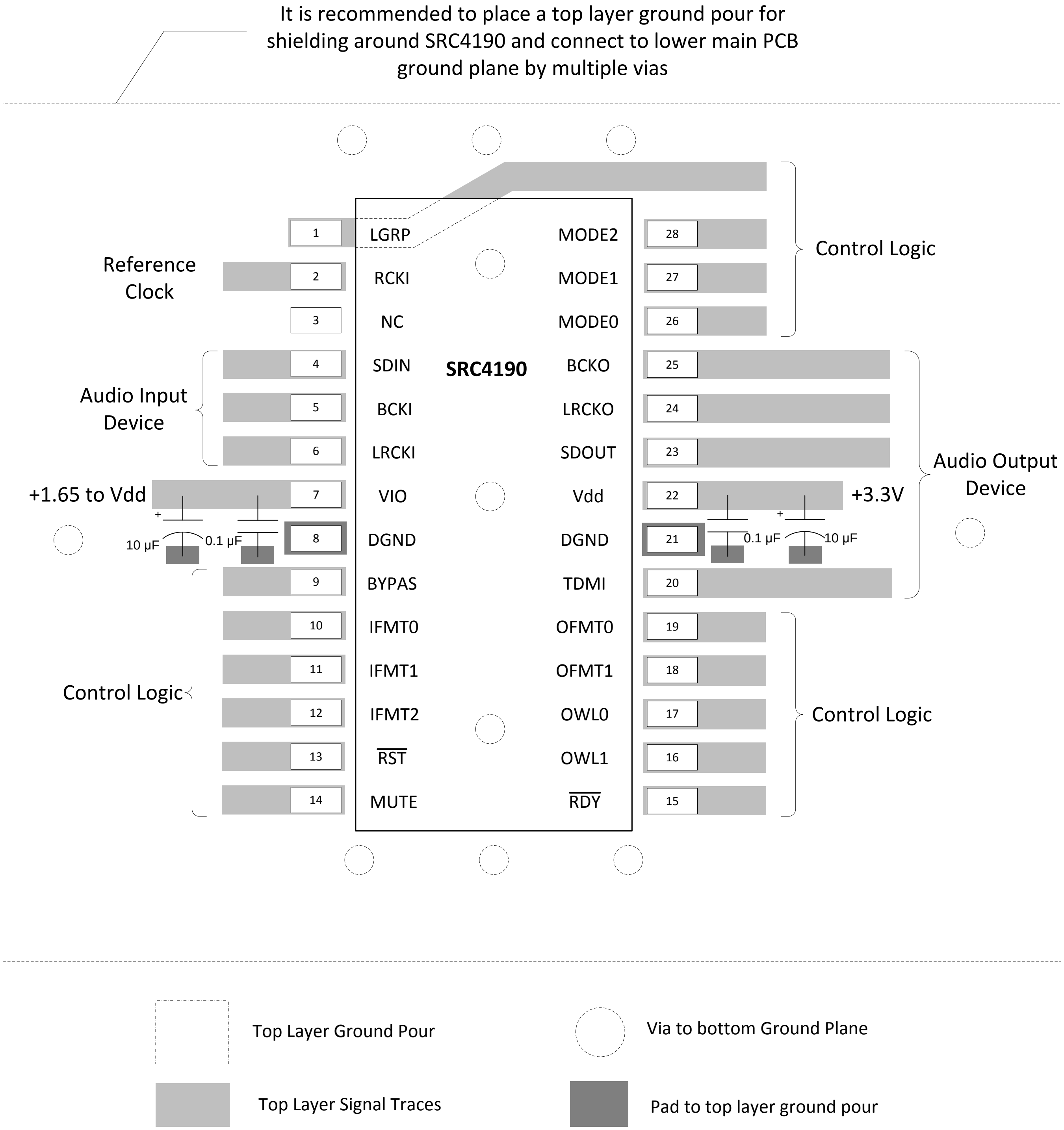


Figure 73. Diagram of an Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *DIT4096 96-kHz Digital Audio Transmitter* (SBOS225)
- *DIT4192 192-kHz Digital Audio Transmitter* (SBOS229)
- *SRC4190/92/93EVM, User's Guide* (SBAU088)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SRC4190IDB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I
SRC4190IDB.A	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I
SRC4190IDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I
SRC4190IDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I
SRC4190IDBR1G4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I
SRC4190IDBR1G4.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4190I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

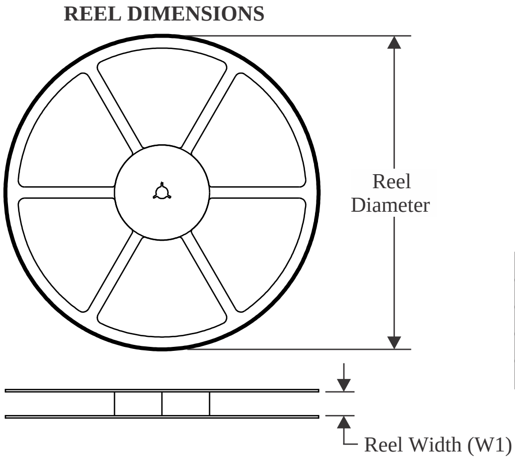
OTHER QUALIFIED VERSIONS OF SRC4190 :

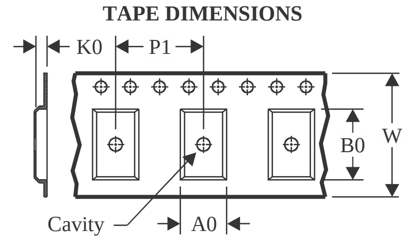
- Automotive : SRC4190-Q1

NOTE: Qualified Version Definitions:

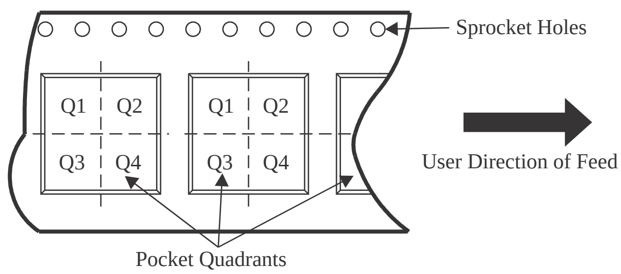
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





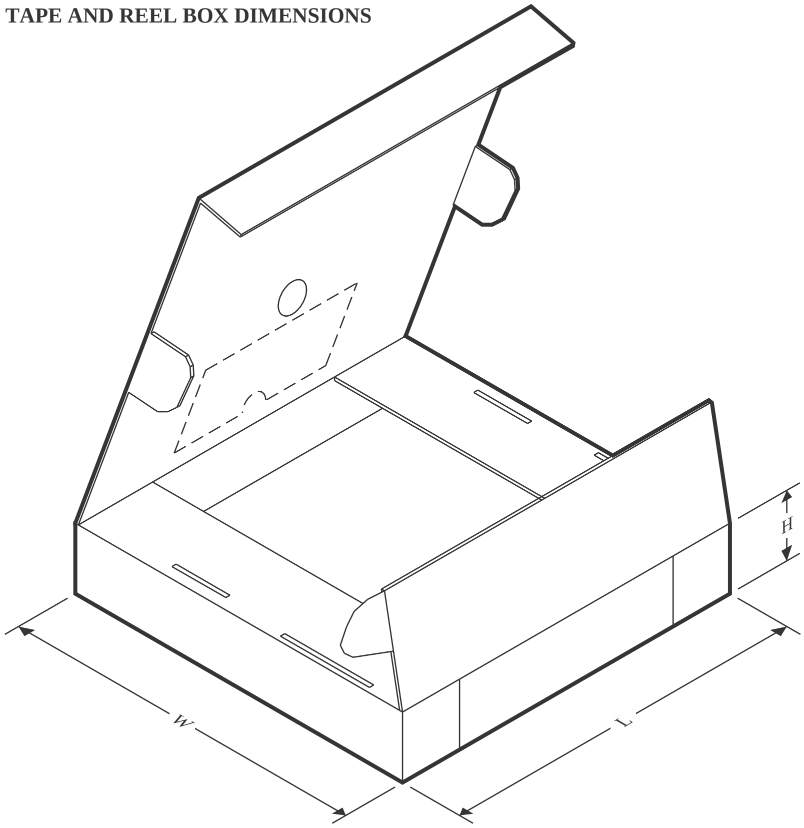
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SRC4190IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SRC4190IDBR1G4	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

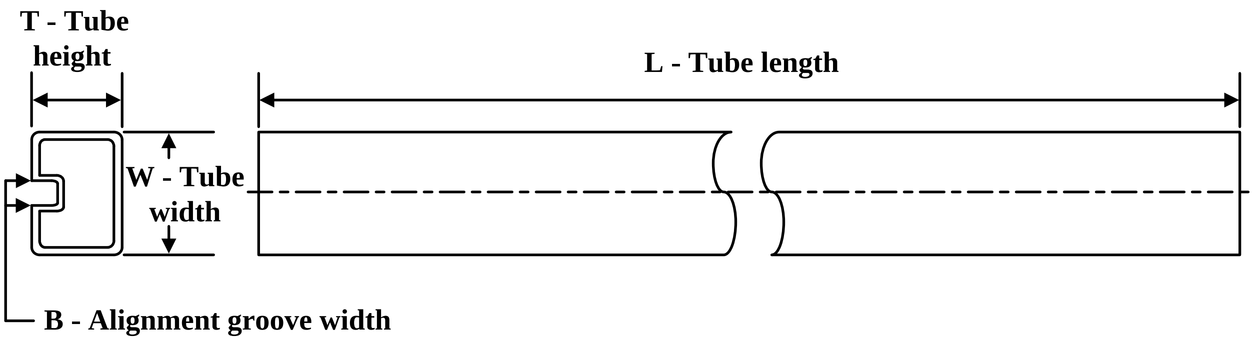
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SRC4190IDBR	SSOP	DB	28	2000	350.0	350.0	43.0
SRC4190IDBR1G4	SSOP	DB	28	2000	350.0	350.0	43.0

TUBE



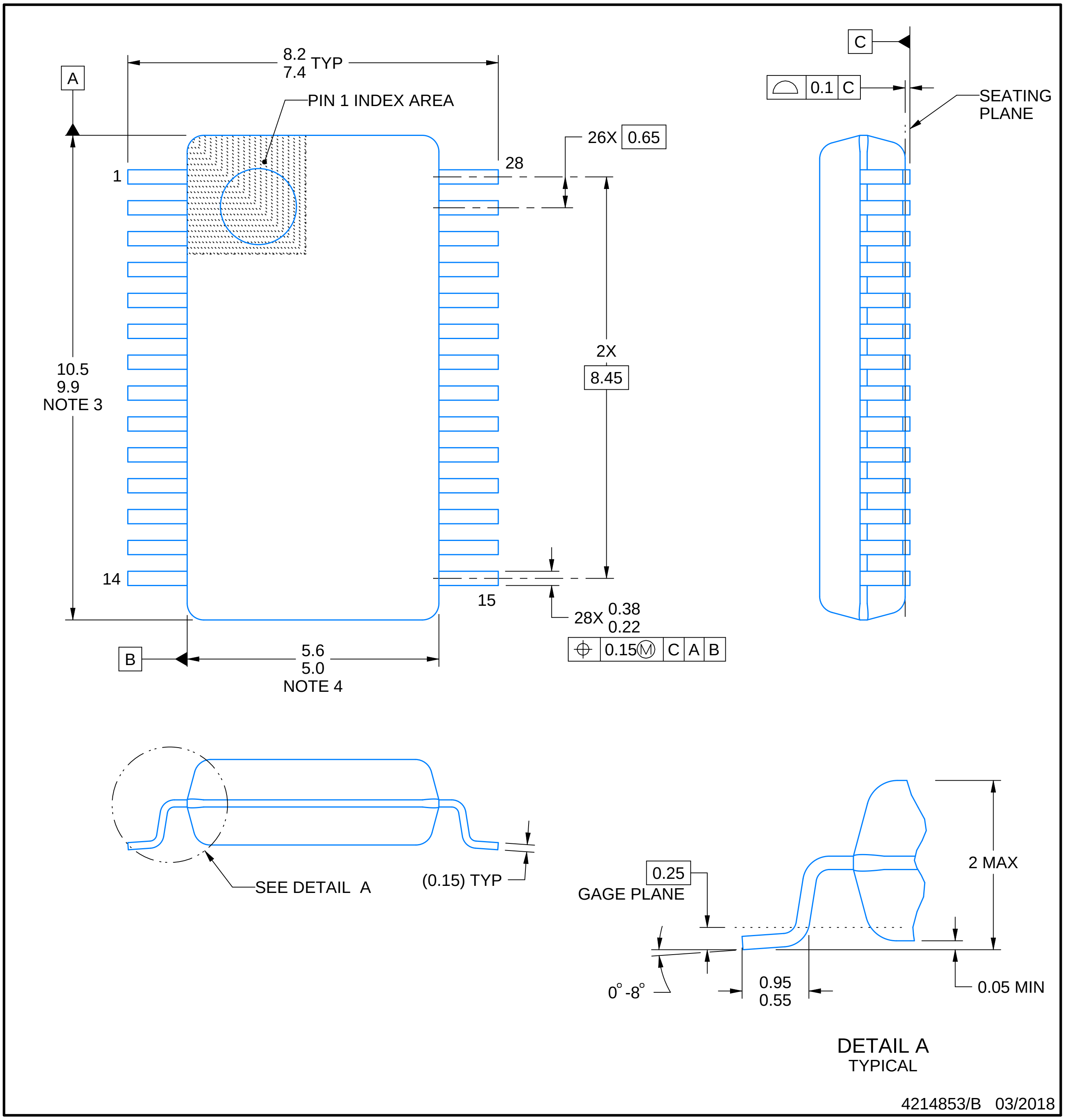
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SRC4190IDB	DB	SSOP	28	50	530	10.5	4000	4.1
SRC4190IDB	DB	SSOP	28	50	530	10.5	4000	4.1
SRC4190IDB.A	DB	SSOP	28	50	530	10.5	4000	4.1
SRC4190IDB.A	DB	SSOP	28	50	530	10.5	4000	4.1
SRC4190IDBR	DB	SSOP	28	2000	530	10.5	4000	4.1
SRC4190IDBR.A	DB	SSOP	28	2000	530	10.5	4000	4.1

DB0028A

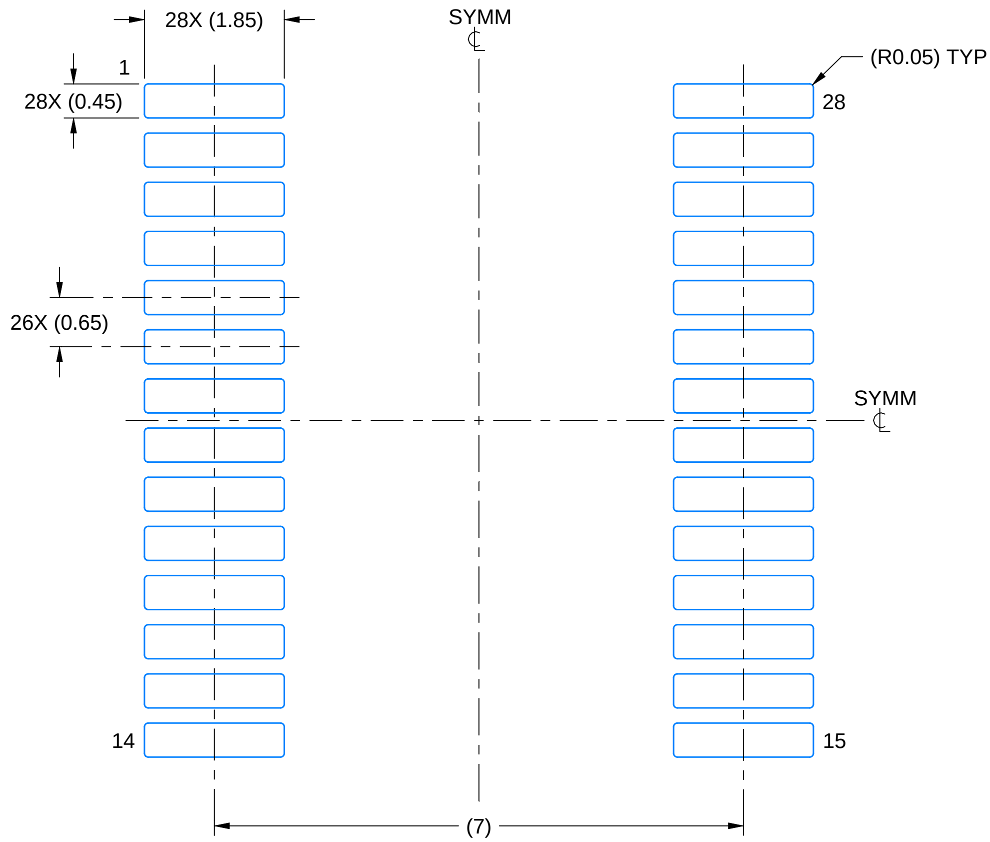
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

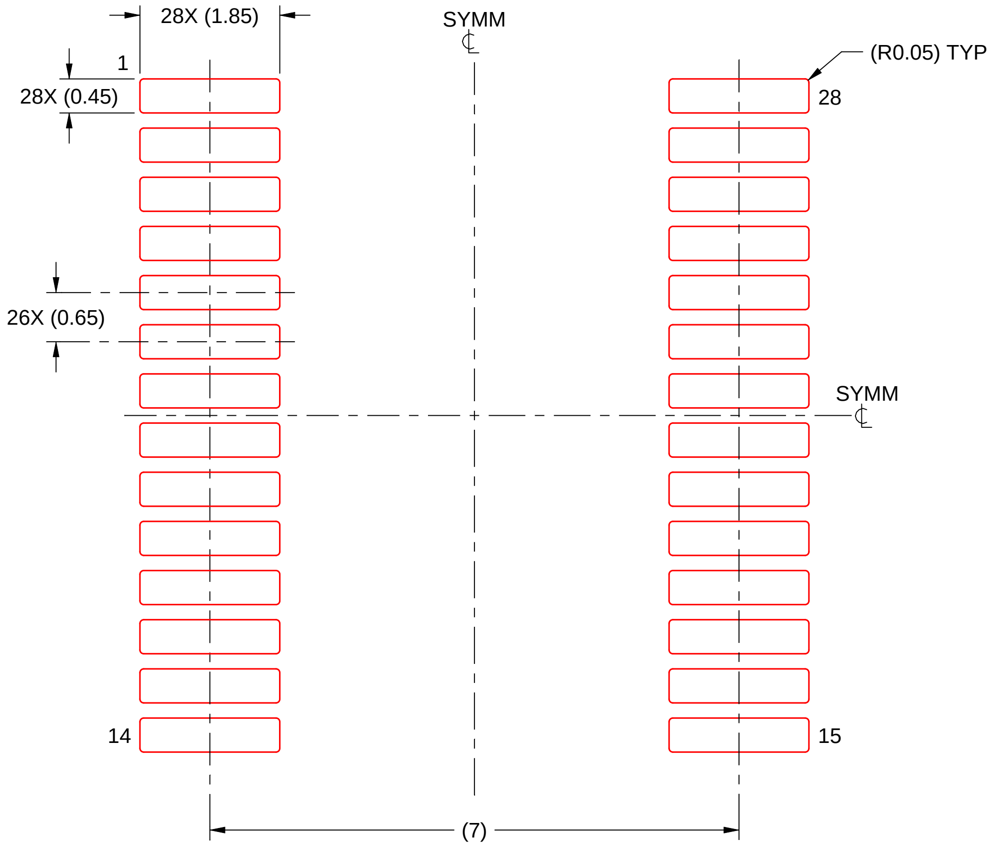
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.