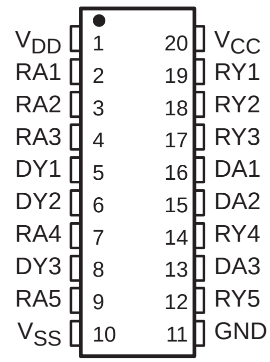
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Single Chip With Easy Interface Between UART and Serial-Port Connector**
- **Less Than 9-mW Power Consumption**
- **Wide Driver Supply Voltage . . . 4.5 V to 13.2 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1100 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Texas Instruments SN75185**
- **Operates Up to 120 kbit/s Over a 3-Meter Cable (See *Application Information* for Conditions)**

DW OR N PACKAGE
(TOP VIEW)



description

The SN75C185 is a low-power BiMOS device containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). Typically, the SN75C185 replaces one SN75188 and two SN75189 devices. This device conforms to TIA/EIA-232-F. The drivers and receivers of the SN75C185 are similar to those of the SN75C188 and SN75C189A, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs, and the receivers have filters that reject input noise pulses that are shorter than 1 μs. Both these features eliminate the need for external components.

The SN75C185 uses the low-power BiMOS technology. In most applications, the receivers contained in this device interface to single inputs of peripheral devices such as ACEs, UARTS, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C185 is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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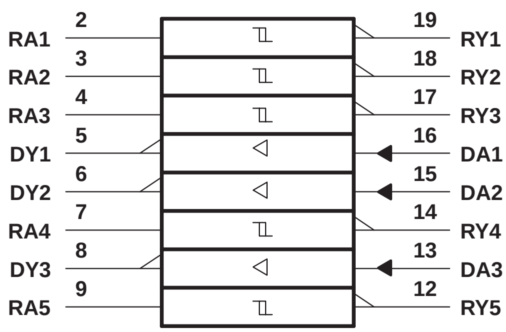
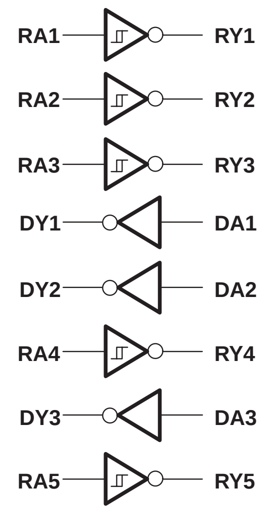
logic symbol†

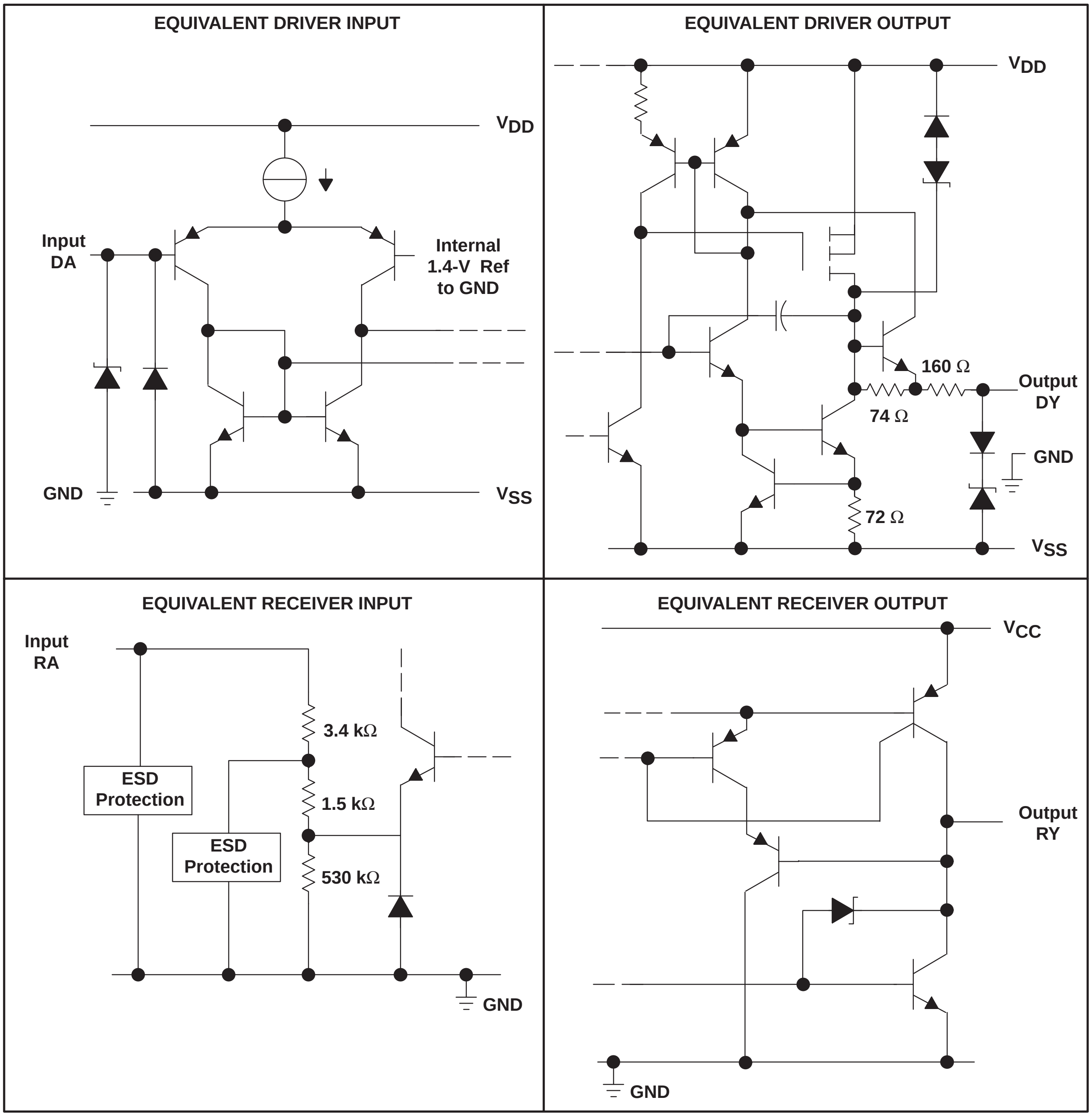


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



equivalent schematics of inputs and outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 13.5 V
Supply voltage, V_{SS} . . . . –13.5 V
Supply voltage, V_{CC} . . . . 7 V
Input voltage range, V_I: Driver . . . . V_{SS} to V_{DD}
Receiver . . . . –30 V to 30 V
Output voltage range, V_O: Driver . . . . V_{SS} – 6 V to V_{DD} + 6 V
Receiver . . . . –0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . 58°C/W
N package . . . . 69°C/W
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	NOM	MAX	UNIT
	Supply voltage	V_{DD}	4.5	12	13.2	V
		V_{SS}	–4.5	–12	–13.2	V
		V_{CC}	4.5	5	6	V
V_I	Input voltage (see Note 3)	Drivers	V_{SS}+2		V_{DD}	V
		Receivers	–25		25	
V_{IH}	High-level input voltage	Drivers	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Receivers			–1	mA
I_{OL}	High-level output current				3.2	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 3: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = –5 V		115	200	µA
			V_{DD} = 12 V,	V_{SS} = –12 V		115	200	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = –5 V		–115	–200	µA
			V_{DD} = 12 V,	V_{SS} = –12 V		–115	–200	
I_{CC}	Supply current from V_{CC}	No load All inputs at 0 or 5 V	V_{DD} = 5 V,	V_{SS} = –5 V			750	µA
			V_{DD} = 12 V,	V_{SS} = –12 V			750	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = –5 V	4	4.5		V
			V_{DD} = 12 V V_{SS} = –12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 3)	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = –5 V		–4.4	–4	V
			V_{DD} = 12 V V_{SS} = –12 V		–10.7	–10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2				–1	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 4)	V_I = 0.8 V, V_O = 0 or V_O = V_{SS}, See FIgure 1		–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 4)	V_I = 2 V, V_O = 0 or V_O = V_{DD}, See Figure 1		4.5	12	19.5	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = – 2 V to 2 V, See Note 5		300	400		Ω

† All typical values are at T_A = 25°C.

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.
4. Not more than one output should be shorted at one time.
5. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output (see Note 6)			2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output		0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output		0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output (see Note 7)	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		1		µs
t_{THL}	Transition time, high- to low-level output (see Note 7)			1		µs
S_R	Output slew rate (see Note 7)	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	4	10	30	V/µs

NOTES: 6. t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
7. Measured between 3-V and –3-V points of output waveform TIA/EIA-232-F conditions), and all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	See Figure 5		1.6	2.1	2.55	V
V_{IT-}	Negative-going input threshhold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			600	1100		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = –20 μA, See Figure 5 and Note 8		3.5			V
		V_I = 0.75 V, I_{OH} = –1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 3 V		0.43	0.55	1	mA
		V_I = 25 V		3.6	4.6	8.3	
I_{IL}	Low-level input current	V_I = –3 V		–0.43	–0.55	–1	mA
		V_I = –25 V		–3.6	–5.0	–8.3	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4			–8	–15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4			13	25	mA

† All typical values are at T_A = 25°C.

NOTE 8: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 5 kΩ, C_L = 50 pF		3	4	μs
t_{PHL}	Propagation delay time, high- to low-level output			3	4	μs
t_{TLH}	Transition time, low- to high-level output			300	450	ns
t_{THL}	Transition time, high- to low-level output			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise (see Note 9)	R_L = 5 kΩ, C_L = 50 pF	1		4	μs

NOTE 9: The receiver ignores any postive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

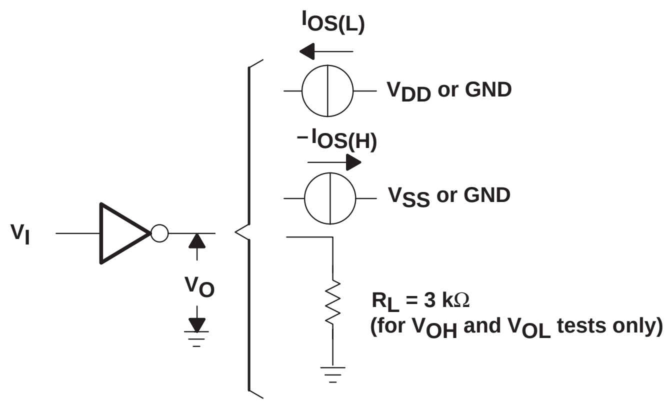


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

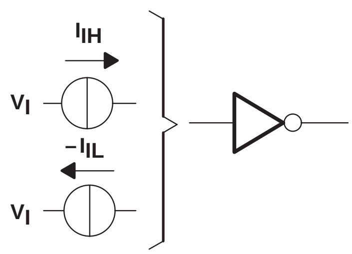
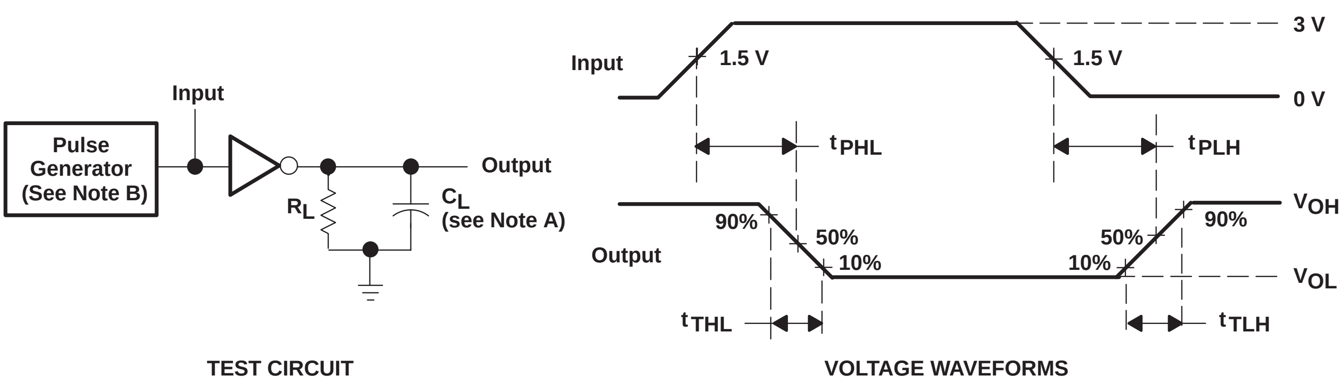


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

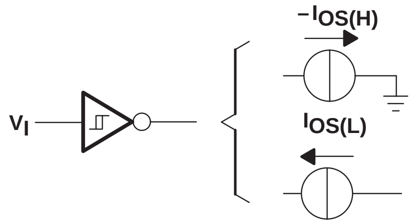


Figure 4. Receiver Test Circuit for $I_{OS(H)}$ and $I_{OS(L)}$

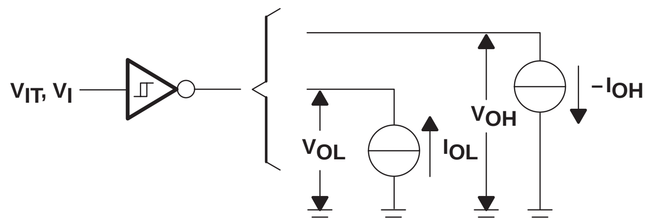
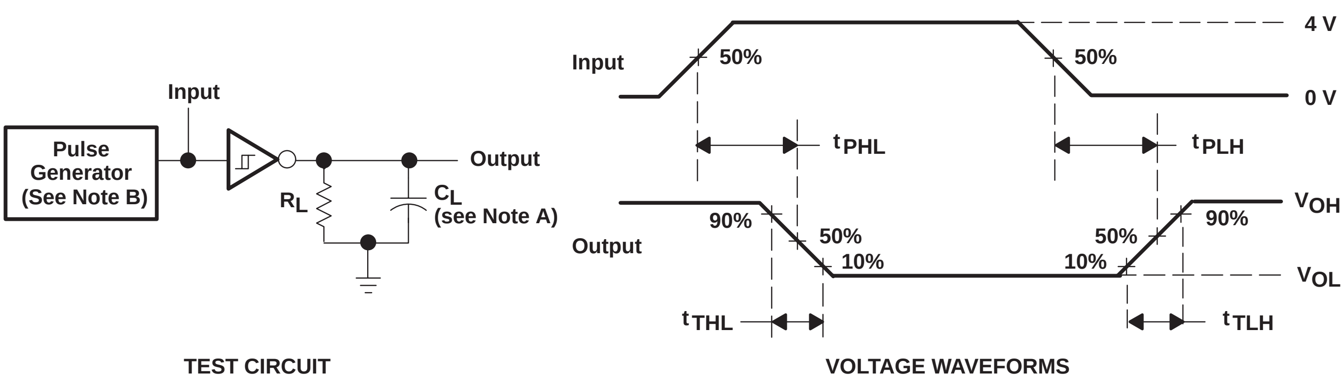


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

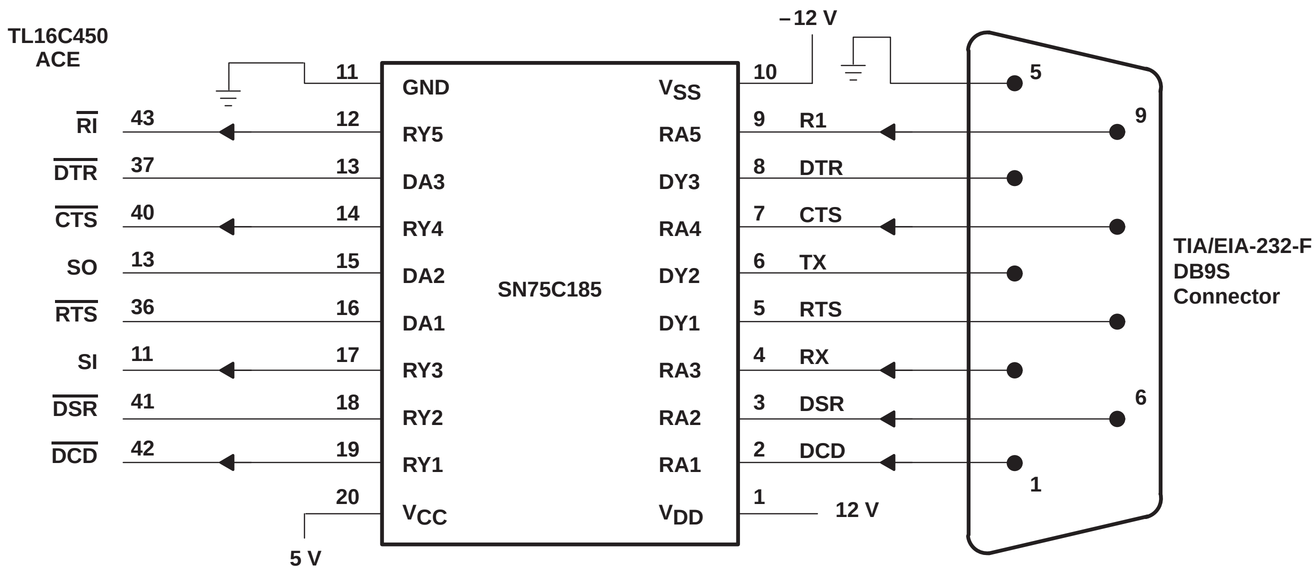
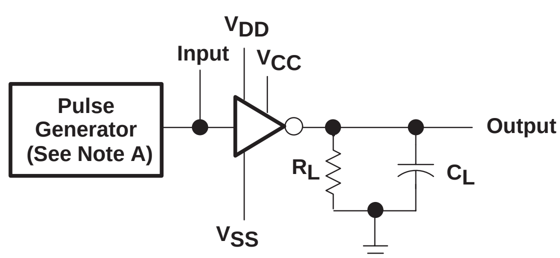


Figure 7. Typical Connection

The SN75C185 supports data rates up to 120 kbit/s over a 3-meter cable. Laboratory experiments show that, with C_L= 500 pF and R_L = 3 kΩ (minimum RS-232 input resistance load), the device can support this data rate. The 500-pF load approximates a typical 3-meter cable because the maximum RS-232 specification is 2500 pF (or about 15 meters). Figure 8 shows the test circuit used. Temperature was varied from 0°C to 70°C for the experiment.



NOTES: A. The pulse generator has the following characteristics: PRR = 60 kHz (120 kbit/s), Z_O = 50 Ω.
B. V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V.

Figure 8. Data-Rate Test Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75C185DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	SN75C185
SN75C185DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C185
SN75C185DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C185
SN75C185N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C185N
SN75C185N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C185N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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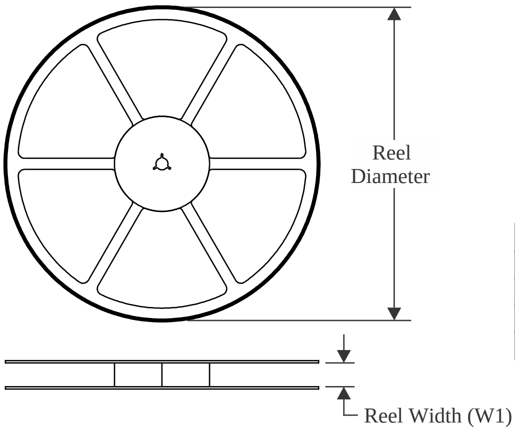
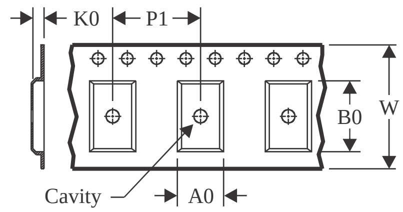
TAPE AND REEL INFORMATION

REEL DIMENSIONS

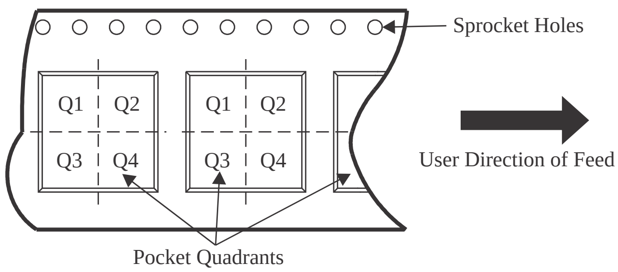


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

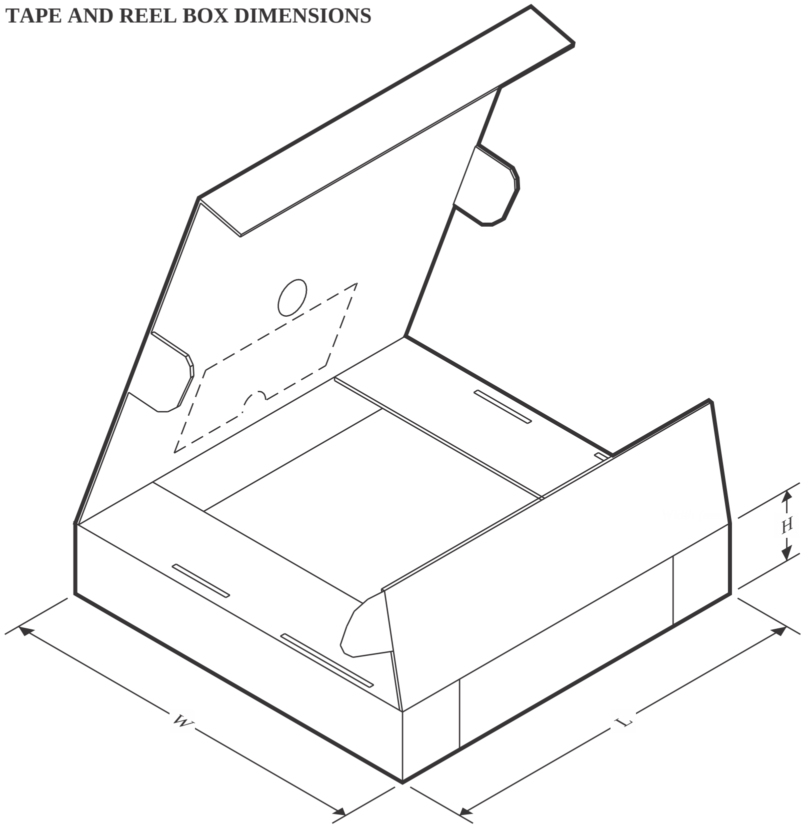
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

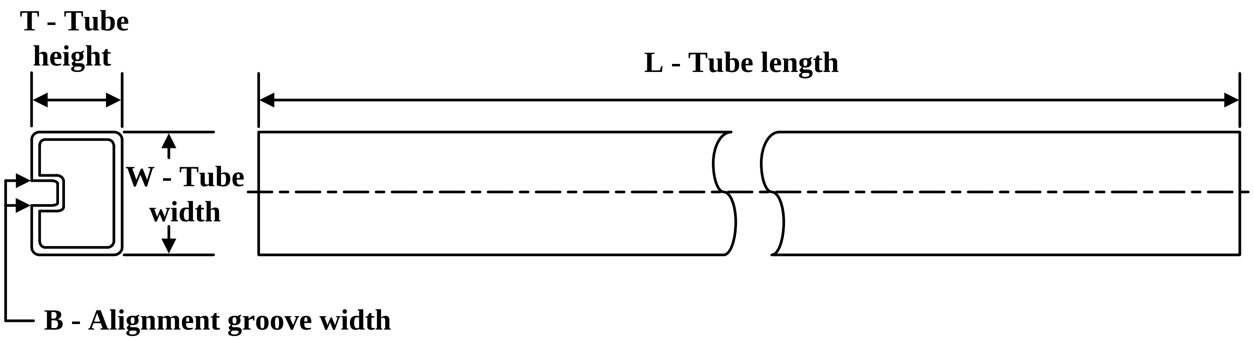
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C185DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE

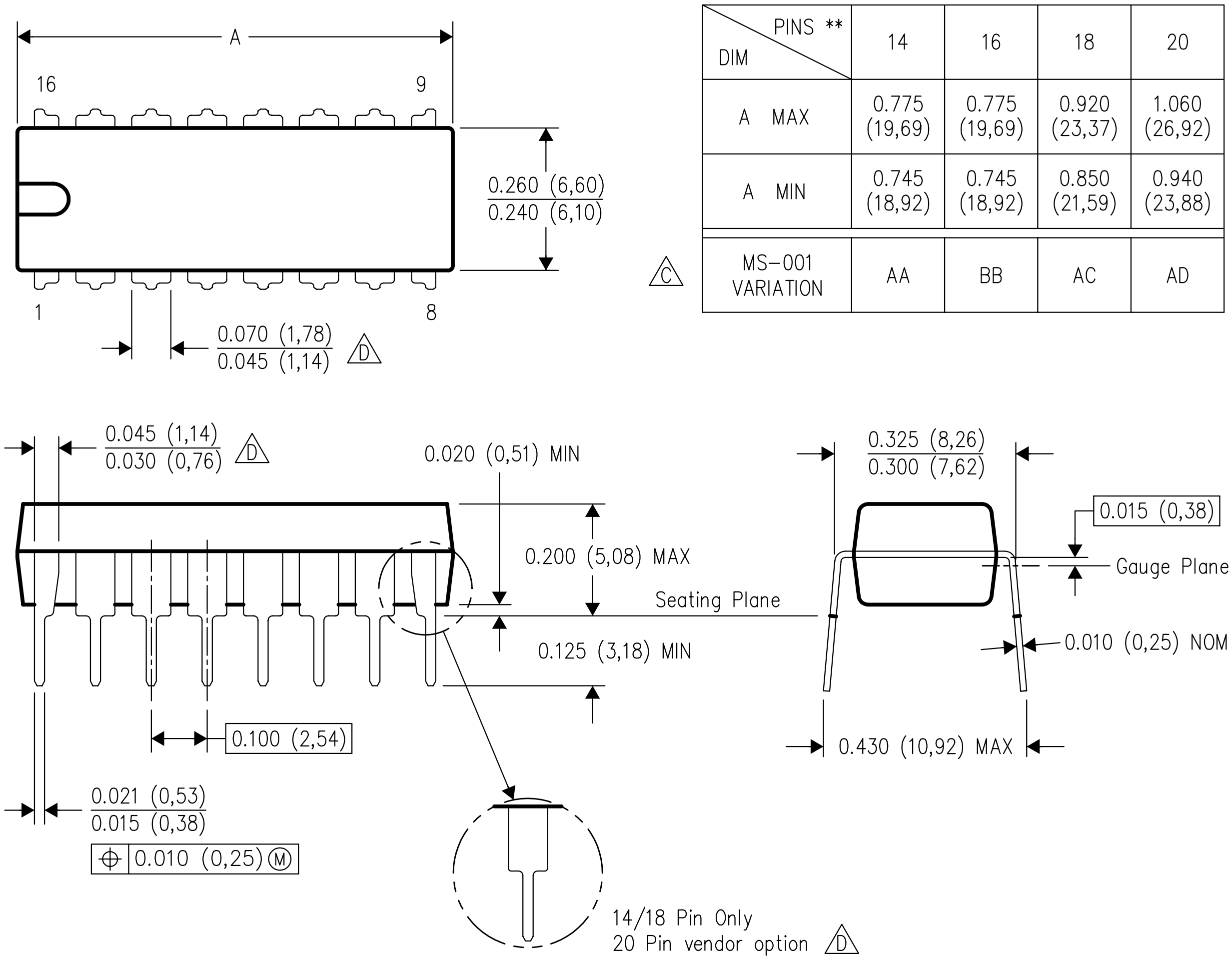


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75C185N	N	PDIP	20	20	506	13.97	11230	4.32
SN75C185N.A	N	PDIP	20	20	506	13.97	11230	4.32

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

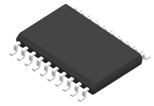
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

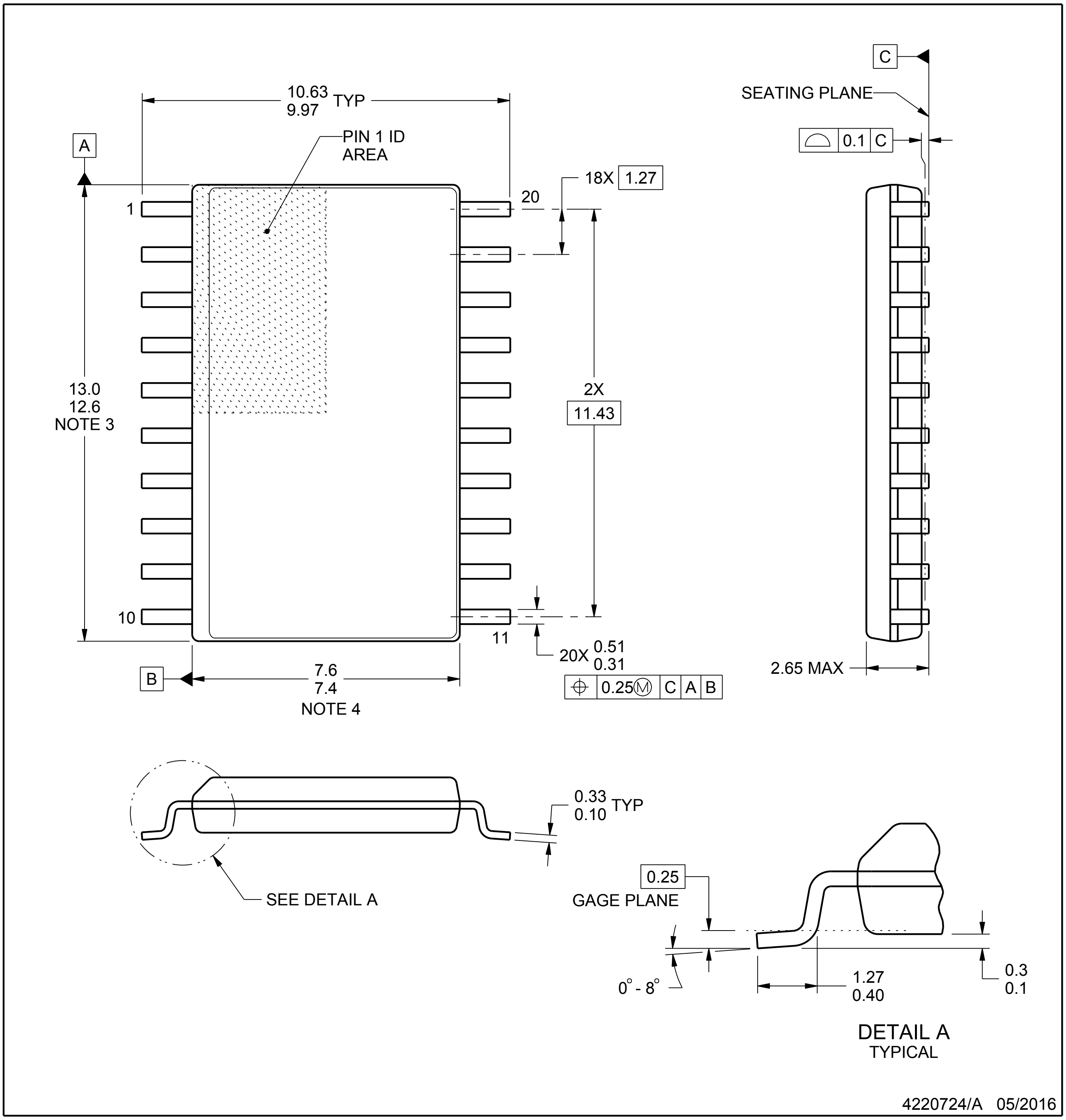
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

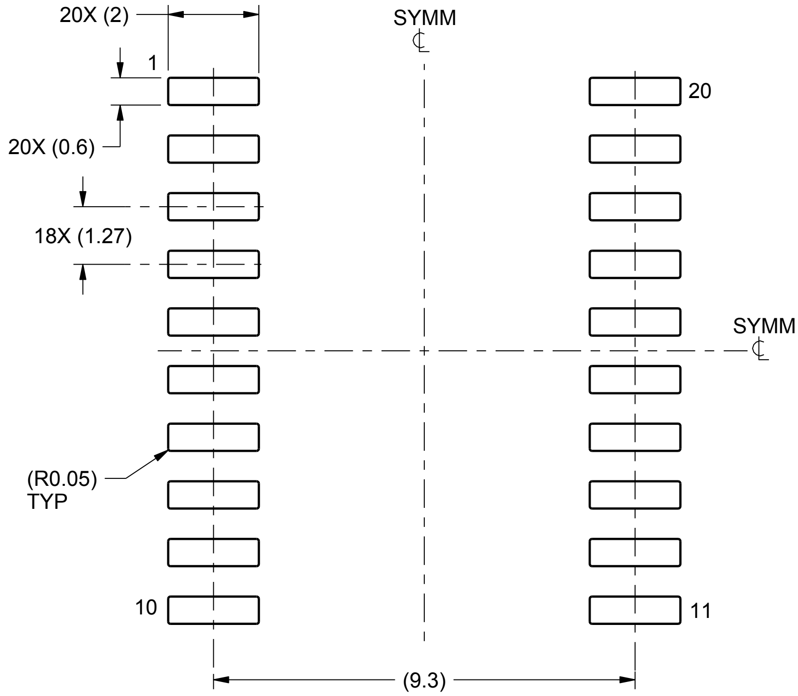
SOIC - 2.65 mm max height

SOIC

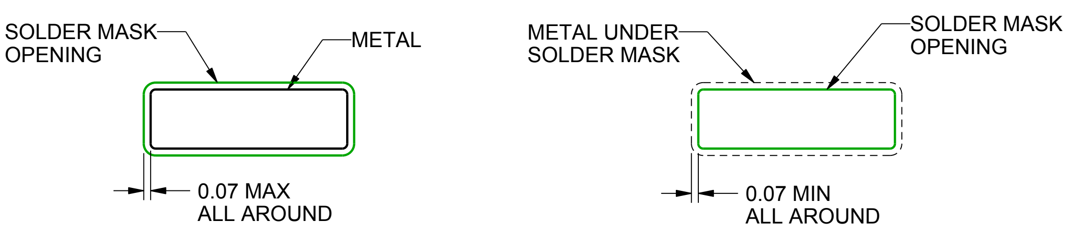


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

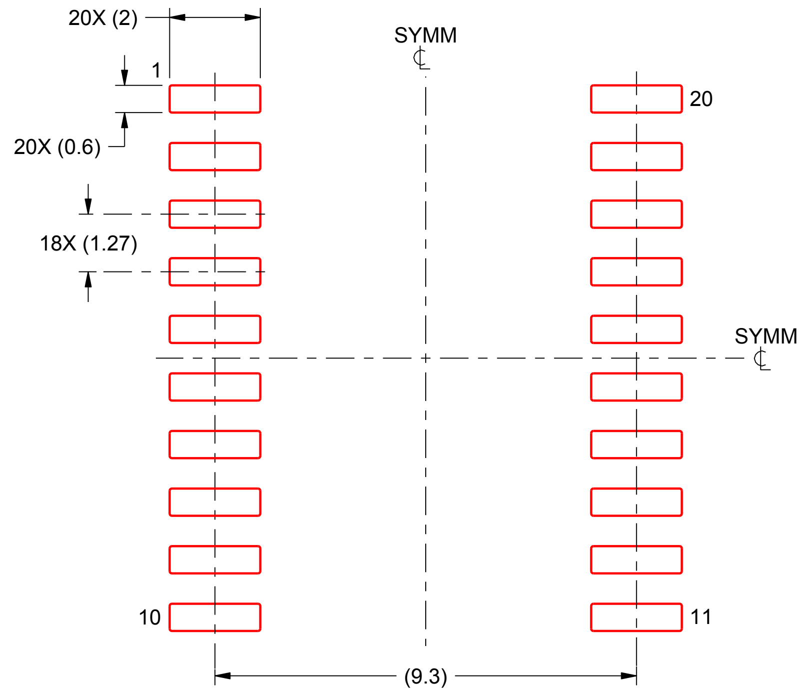
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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