

## FEATURES

- Controlled Baseline
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- Designed to Operate at up to 20 Million Data Transfers per Second (Fast-20 SCSI)
- Nine Differential Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI)
- SN75976A Packaged in Thin Shrink Small-Outline Package with 20-Mil Terminal Pitch (DGG)
- Two Skew Limits Available
- ESD Protection on Bus Terminals Exceeds 12 kV
- Low Disabled Supply Current 8 mA Typical
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Power-Up/Down Glitch Protection

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**DGG PACKAGE  
(TOP VIEW)**

GND	1	56	CDE2
BSR	2	55	CDE1
$\overline{\text{CRE}}$	3	54	CDE0
1A	4	53	9B+
1DE/ $\overline{\text{RE}}$	5	52	9B-
2A	6	51	8B+
2DE/ $\overline{\text{RE}}$	7	50	8B-
3A	8	49	7B+
3DE/ $\overline{\text{RE}}$	9	48	7B-
4A	10	47	6B+
4DE/ $\overline{\text{RE}}$	11	46	6B-
V <sub>CC</sub>	12	45	V <sub>CC</sub>
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V <sub>CC</sub>	18	39	V <sub>CC</sub>
5A	19	38	5B+
5DE/ $\overline{\text{RE}}$	20	37	5B-
6A	21	36	4B+
6DE/ $\overline{\text{RE}}$	22	35	4B-
7A	23	34	3B+
7DE/ $\overline{\text{RE}}$	24	33	3B-
8A	25	32	2B+
8DE/ $\overline{\text{RE}}$	26	31	2B-
9A	27	30	1B+
9DE/ $\overline{\text{RE}}$	28	29	1B-

Terminals 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

## DESCRIPTION/ORDERING INFORMATION

The SN75976A is an improved replacement for the industry's first 9-channel 485 transceiver – the SN75LBC976. The A version offers improved switching performance, a smaller package, and higher ESD protection. The SN75976A is offered in two versions. The '976A2 skew limits of 4 ns for the differential drivers and 5 ns for the differential receivers complies with the recommended skew budget of the Fast-20 SCSI standard for data transfer rates up to 20 million transfers per second. The '976A1 supports the Fast SCSI skew budget for 10 million transfers per second. The skew limit ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN75976A-EP

## 9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS878A–JANUARY 2008–REVISED FEBRUARY 2008

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The patented thermal enhancements made to the 56-pin shrink small-outline package (SSOP) of the SN75976 have been applied to the new, thin shrink, small-outline package (TSSOP). The TSSOP package offers even less board area requirements than the SSOP while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

In addition to speed improvements, the '976A can withstand electrostatic discharges exceeding 12 kV using the human-body model, and 600 V using the machine model of MIL-PRF-38535, Method 3015.7 on the RS-485 I/O terminals. This is six times the industry standard and provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

Each of the nine channels of the '976A typically meet or exceed the requirements of 485 (1983) and ISO 8482-1987/ TIA TR30.2 referenced by American National Standard of Information (ANSI) Systems, X3.131-1994 (SCSI-2) standard, X2.277-1996 (Fast-20 Parallel Interface), and the Intelligent Peripheral Interface Physical Layer-ANSI X3.129-1986 standard.

The SN75976A is characterized for operation over an ambient air temperature range of –55°C to 125°C.

### AVAILABLE OPTIONS<sup>(1)</sup>

T <sub>A</sub>	SKEW LIMIT (ns)		PACKAGE <sup>(2)(3)</sup>
	DRIVER	RECEIVER	TSSOP (DGG)
–55°C to 125°C	8	9	SN75976A1MDGGREP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) The R suffix indicates taped and reeled packages.

### TERMINAL FUNCTIONS

TERMINAL		LOGIC LEVEL	I/O	TERMINATION	DESCRIPTION
NAME	NO.				
1A to 9A	4, 6, 8, 10, 19, 21, 23, 25, 27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29, 31, 33, 35, 37, 46, 48, 50, 52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30, 32, 34, 36, 38, 47, 49, 51, 53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/RE and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/RE – 9DE/RE are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
CRE	3	TTL	Input	Pullup	CRE is the common receiver enable. When high, CRE disables receiver channels 5 to 9.
1DE/RE to 9DE/RE	5, 7, 9, 11, 20, 22, 24, 26, 28	TTL	Input	Pullup	1DE/RE–9DE/RE are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/RE–9DE/RE and CRE and BSR are low and CDE1 and CDE2 are low.
GND	1, 13, 14, 15, 16, 17, 40, 41, 42, 43, 44	NA	Power	NA	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity. <sup>(1)</sup>
VCC	12, 18, 39, 45	NA	Power	NA	Supply voltage

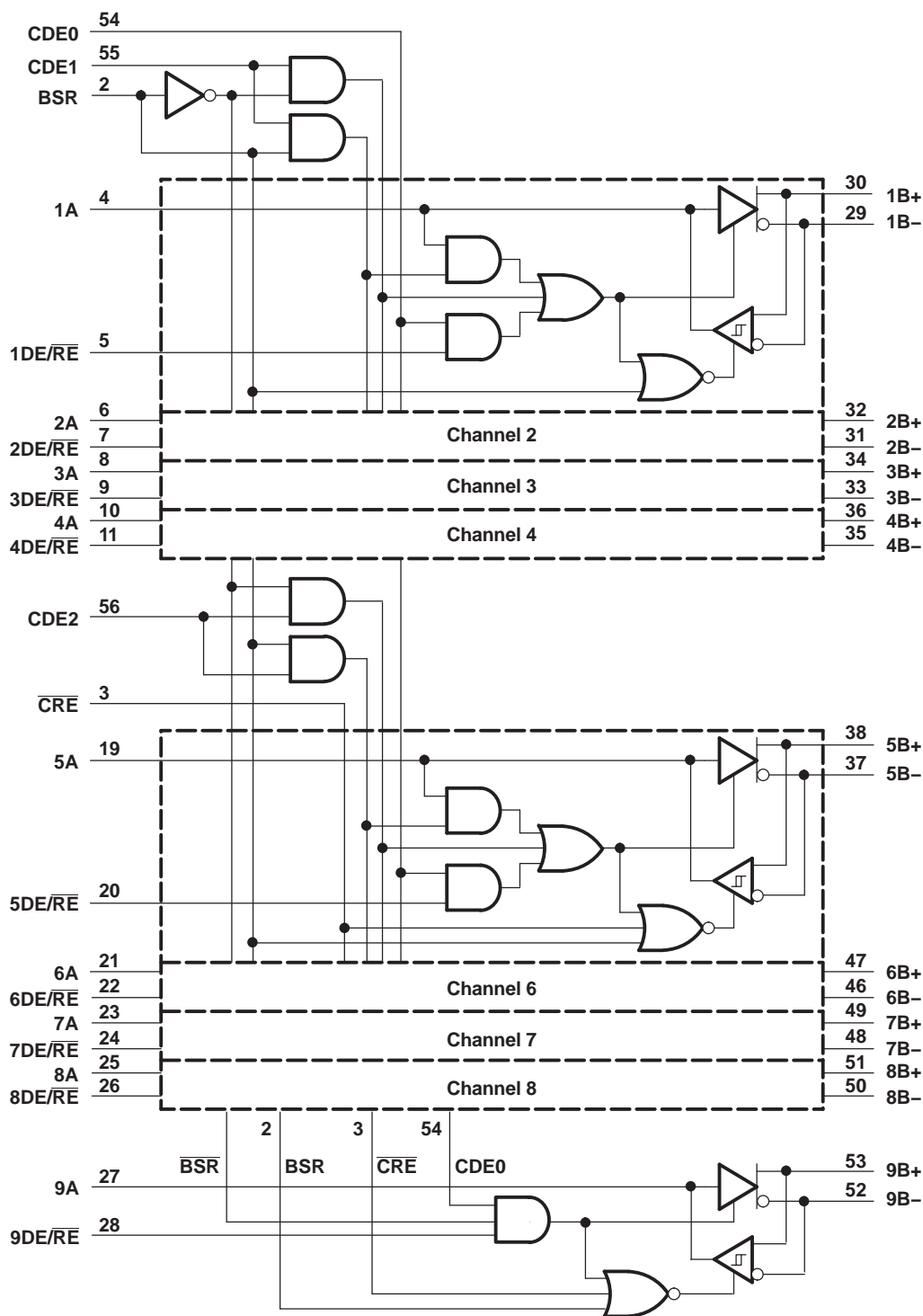
(1) Terminal 1 must be connected to signal ground for proper operation.

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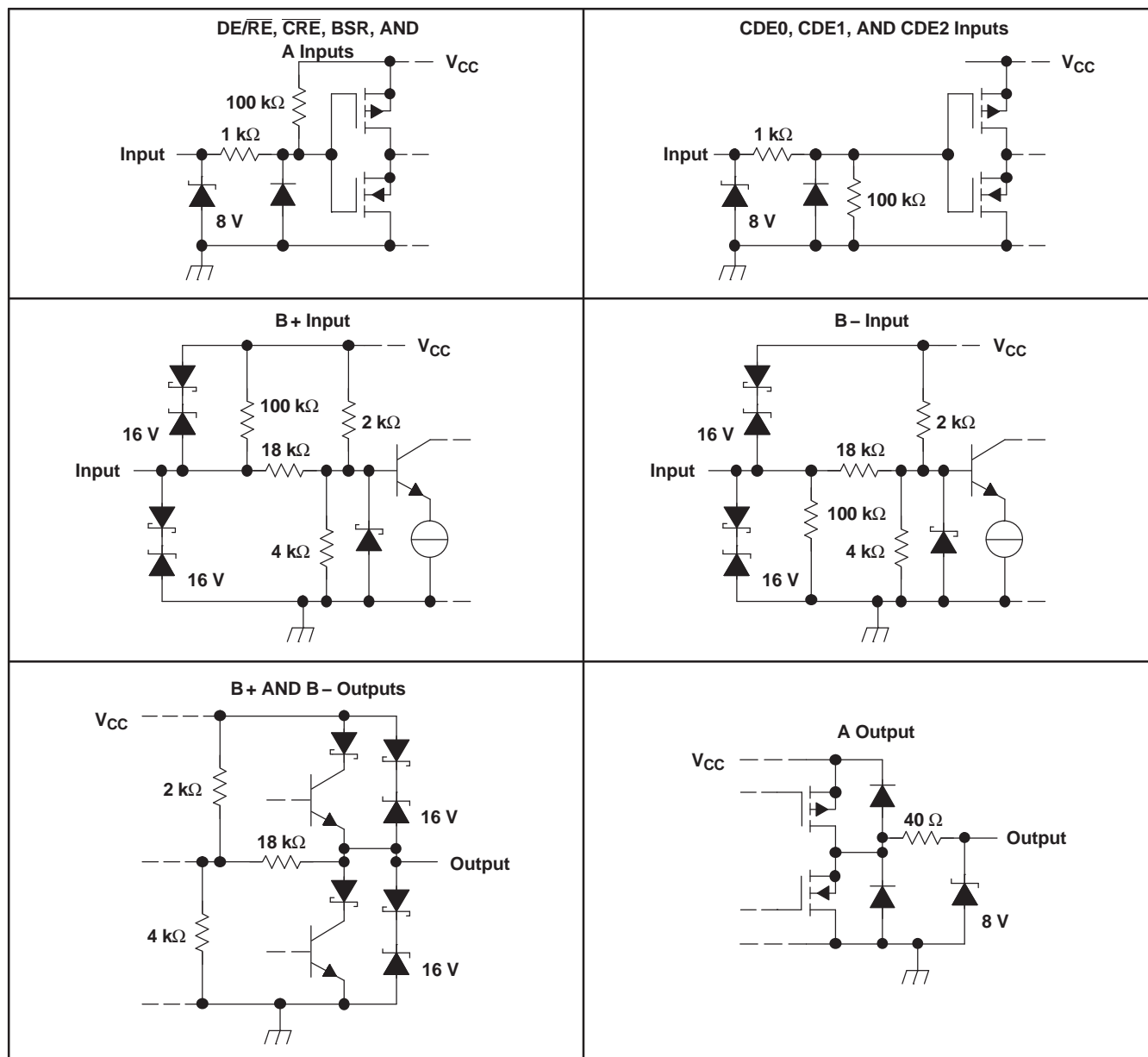
## 9-CHANNEL DIFFERENTIAL TRANSCIEVER

SLLS878A—JANUARY 2008—REVISED FEBRUARY 2008

LOGIC DIAGRAM (POSITIVE LOGIC)



## SCHEMATICS OF INPUTS AND OUTPUTS



# SN75976A-EP

## 9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS878A–JANUARY 2008–REVISED FEBRUARY 2008

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	–0.3	6	V
	Bus voltage range	–10	15	V
	Data I/O and control (A side) voltage range	–0.3	$V_{CC} + 0.5$	V
$I_O$	Receiver output current		±40	mA
Electrostatic discharge	B side and GND, Class 3, A: <sup>(3)</sup>		12	kV
	B side and GND, Class 3, B: <sup>(3)</sup>		400	V
	All terminals, Class 3, A:		4	kV
	All terminals, Class 3, B:		400	V
$T_{stg}$	Storage temperature	–65	150	°C
	Continuous total power dissipation <sup>(4)</sup>	Internally Limited		

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.
- (3) This absolute maximum rating is tested in accordance with MIL-STD-883, Method 3015.7.
- (4) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

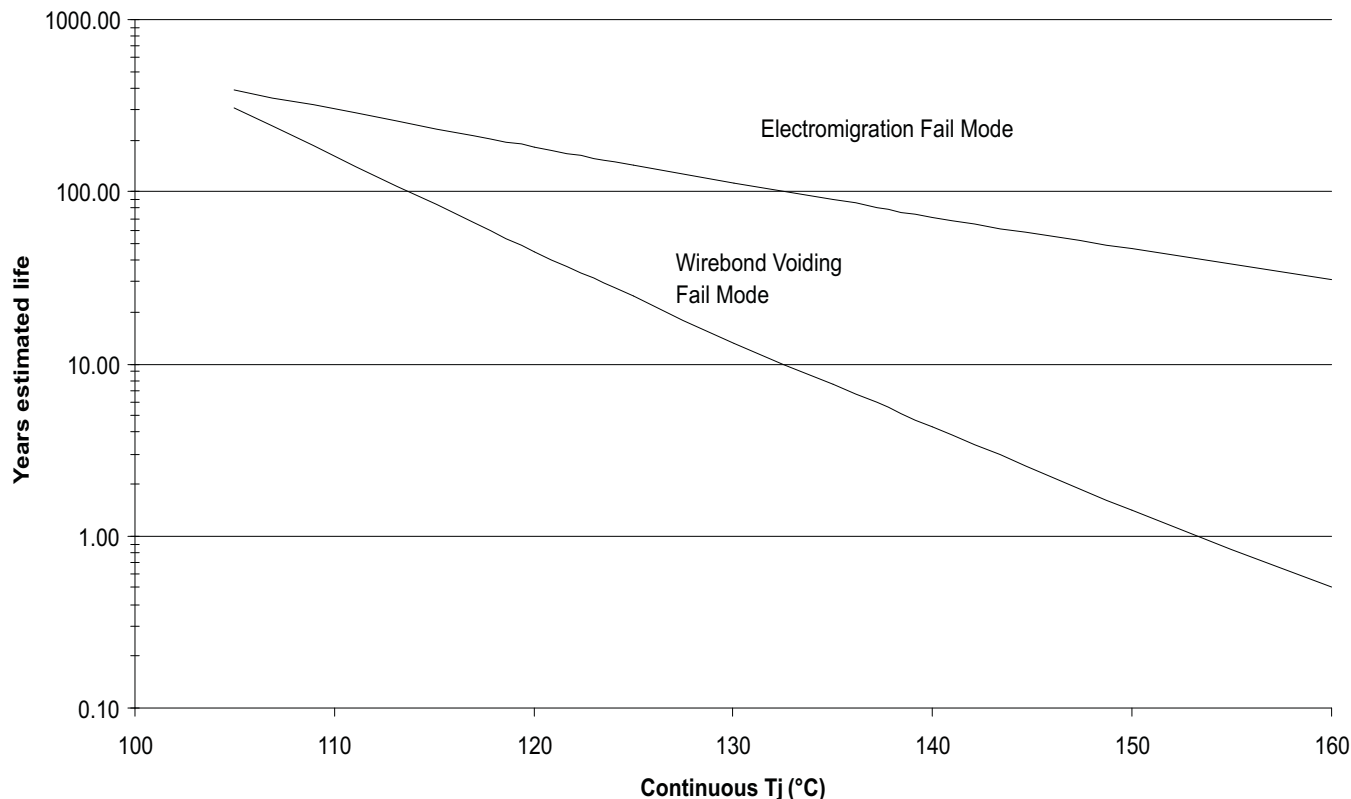
### Dissipation Ratings

PACKAGE	$T_A \leq 25^\circ\text{C}$	OPERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW	–

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

### Package Thermal Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		27		°C/W
$T_{JS}$	Thermal-shutdown junction temperature		165		°C



- A. See Datasheet for Absolute Maximum and Minimum Recommended Operating Conditions.
- B. Silicon Operating life Design Goal is 10 years @105°C Junction Temperature (does not include package interconnect life).
- C. Enhanced Plastic Product Disclaimer Applies.
- D. Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Chart for additional information on thermal derating. Electromigration failure mode applies to powered part, Kirkendall voiding failure mode is a function of temperature only.

Figure 1. SN75976A-EP Operating Life Derating Chart

## Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	Except nB+, nB– <sup>(1)</sup>	2			V
V <sub>IL</sub>	Low-level input voltage	Except nB+, nB– <sup>(1)</sup>			0.8	V
V <sub>O</sub> , V <sub>I</sub> , or V <sub>IC</sub>	Voltage at any bus terminal (separately or common-mode)	nB+ or nB–			12 –7	V
I <sub>OH</sub>	High-level output current	Driver			–60	mA
		Receiver			–8	
I <sub>OL</sub>	Low-level output current	Driver			60	mA
		Receiver			8	
T <sub>A</sub>	Operating free-air temperature	SN75976A	–55		125	°C

(1) n = 1 – 9

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## 9-CHANNEL DIFFERENTIAL TRANSCEIVER

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### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>ODH</sub>	Driver differential high-level output voltage	S1 to A,	V <sub>T</sub> = 5 V,	See Figure 2	0.7			V
		S1 to B, See Figure 1	V <sub>T</sub> = 5 V,		0.7			
V <sub>ODL</sub>	Driver differential low-level output voltage	S1 to A, T <sub>C</sub> ≥ 25°C	V <sub>T</sub> = 5 V, See Figure 2		0.7	–1.4		V
		S1 to B,	V <sub>T</sub> = 5 V,	See Figure 2	0.7	–1.8		
		S1 to A, See Figure 1	V <sub>T</sub> = 5 V,		–0.8	–1.4		
V <sub>OH</sub>	High-level output voltage	A side, I <sub>OH</sub> = –8 mA	V <sub>ID</sub> = 200 mV, See Figure 4		4	4.5		V
		B side,	V <sub>T</sub> = 5 V,	See Figure 2		3		
V <sub>OL</sub>	Low-level output voltage	A side, I <sub>OH</sub> = 8 mA	V <sub>ID</sub> = –200 mV, See Figure 4			0.6	0.8	V
		A side,	V <sub>T</sub> = 5 V,	See Figure 2		1		
V <sub>IT+</sub>	Receiver positive-going differential input threshold voltage	I <sub>OH</sub> = –8 mA,	See Figure 4				0.2	V
V <sub>IT–</sub>	Receiver negative-going differential input threshold voltage	I <sub>OL</sub> = 8 mA,	See Figure 4				–0.2	V
V <sub>hys</sub>	Receiver input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )	V <sub>CC</sub> = 5 V,	T <sub>A</sub> = 25°C		24	45		mV
I <sub>I</sub>	Bus input current	V <sub>IH</sub> = 12 V,	V <sub>CC</sub> = 5 V,	Other input at 0 V		0.4	1	mA
		V <sub>IH</sub> = 12 V,	V <sub>CC</sub> = 0,	Other input at 0 V		0.5	1	
		V <sub>IH</sub> = –7 V,	V <sub>CC</sub> = 5 V,	Other input at 0 V		–0.4	–0.8	
		V <sub>IH</sub> = –7 V,	V <sub>CC</sub> = 0,	Other input at 0 V		–0.3	–0.8	
I <sub>IH</sub>	High-level input current	A, BSR, DE/ $\overline{RE}$ , and $\overline{CRE}$ ,	V <sub>IH</sub> = 2 V				–100	μA
		CDE0, CDE1, and CDE2,	V <sub>IH</sub> = 2 V				100	
I <sub>IL</sub>	Low-level input current	A, BSR, DE/ $\overline{RE}$ , and $\overline{CRE}$ ,	V <sub>IL</sub> = 0.8 V				–100	μA
		CDE1, CDE1, and CDE2,	V <sub>IL</sub> = 0.8 V				100	
I <sub>OS</sub>	Short circuit output current	nB+ or nB–					±260	mA
I <sub>OZ</sub>	High-impedance-state output current	A			See I <sub>IH</sub> and I <sub>IL</sub>			
		nB+ or nB–			See I <sub>I</sub>			
I <sub>CC</sub>	Supply current	Disabled					10	mA
		All drivers enabled, no load					60	
		All receivers enabled, no load					45	
C <sub>O</sub>	Output capacitance	nB+ or nB– to GND				18		pF
C <sub>pd</sub>	Power dissipation capacitance <sup>(2)</sup>	Receiver				40		pF
		Driver				100		

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) C<sub>pd</sub> determines the no-load dynamic supply current consumption, I<sub>S</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f + I<sub>CC</sub>.

### Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>pd</sub>	Propagation delay time, t <sub>PHL</sub> or t <sub>PLH</sub> (see Figures 2 and 3)	'976A1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			15	ns
t <sub>sk(lim)</sub>	Skew limit, maximum t <sub>pd</sub> – minimum t <sub>pd</sub> <sup>(2)</sup>	'976A1				8	ns
t <sub>sk(p)</sub>	Pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>					4	ns

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) This parameter is applicable at one V<sub>CC</sub> and operating temperature within the recommended operating conditions and to any two devices.



## Driver Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_f$	Fall time	S1 to B, See Figure 3		4		ns
$t_r$	Rise time	See Figure 3		8		ns
$t_{en}$	Enable time, control inputs to active output				60	ns
$t_{dis}$	Disable time, control inputs to high-impedance output				140	ns
$t_{PHZ}$	Propagation delay time, high-level to high-impedance output	See Figures 6 and 7			120	ns
$t_{PLZ}$	Propagation delay time, low-level to high-impedance output				120	ns
$t_{PZH}$	Propagation delay time, high-impedance to high-level output				60	ns
$t_{PZL}$	Propagation delay time, high-impedance to low-level output				60	ns

## Receiver Switching Characteristics

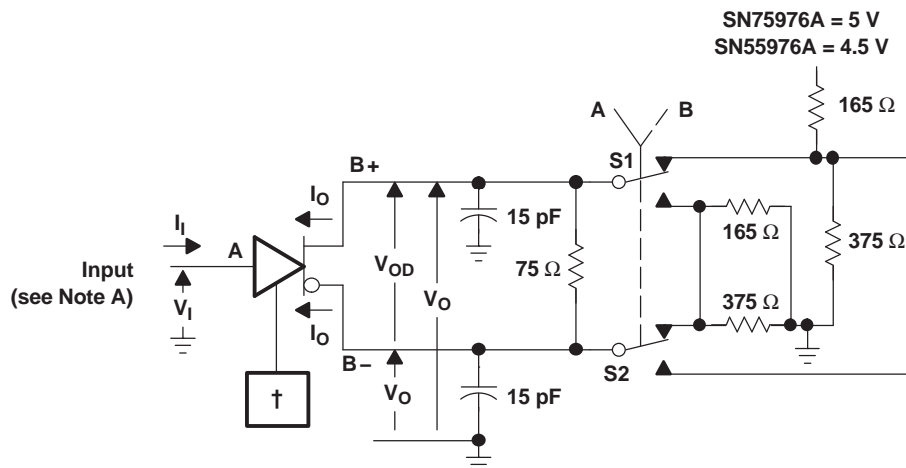
over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}$	Propagation delay time, $t_{PHL}$ or $t_{PLH}$ (see Figures 4 and 5)	'976A1	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			19	ns
$t_{sk(lim)}$	Skew limit, maximum $t_{pd}$ – minimum $t_{pd}$ <sup>(2)</sup>	'976A1				9	ns
$t_{sk(p)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				0.6	4	ns
$t_t$	Transition time ( $t_r$ or $t_f$ )		See Figure 5		2		ns
$t_{en}$	Enable time, control inputs to active output					70	ns
$t_{dis}$	Disable time, control inputs to high-impedance output					80	ns
$t_{PHZ}$	Propagation delay time, high-level to high-impedance output	See Figures 8 and 9				80	ns
$t_{PLZ}$	Propagation delay time, low-level to high-impedance output					70	ns
$t_{PZH}$	Propagation delay time, high-impedance to high-level output					70	ns
$t_{PZL}$	Propagation delay time, high-impedance to low-level output					70	ns

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions and to any two devices.

## PARAMETER MEASUREMENT INFORMATION

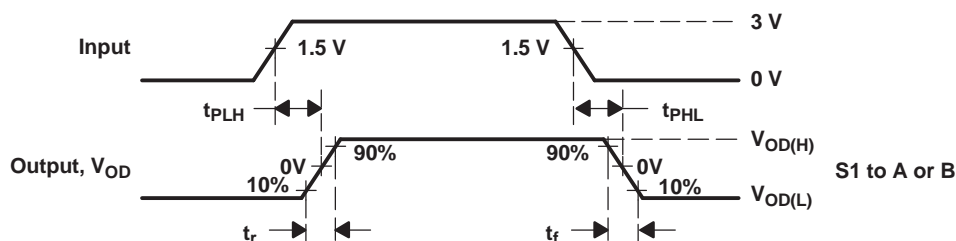


† CDE0 and DE/RE are at 2 V, BSR is at 0.8 V and, for the SN75976A only, all others are open.

‡ For the SN75976A only, all nine drivers are enabled, similarly loaded, and switching.

- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50$  Ω.
- B. All resistances are in Ω and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

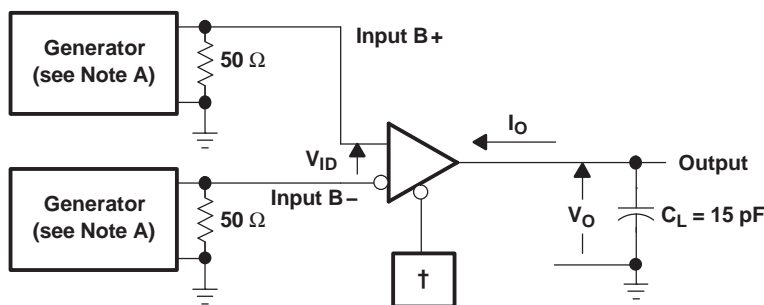
**Figure 2. Driver Test Circuit, Currents, and Voltages**



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50$  Ω.
- B. All resistances are in Ω and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

**Figure 3. Driver Delay and Transition Time Test Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)

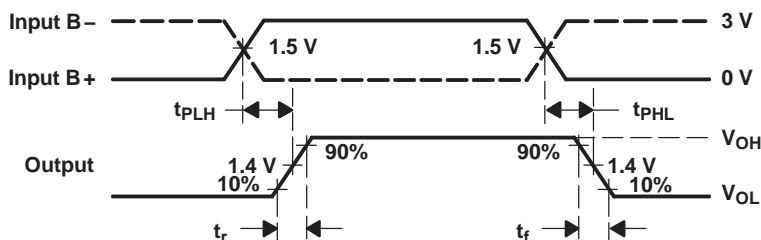


† CDE0, CDE1, CDE2, BSR, CRE, and DE/ $\overline{RE}$  at 0.8 V

‡ For the SN75976A only, all nine receivers are enabled and switching.

- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50$   $\Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

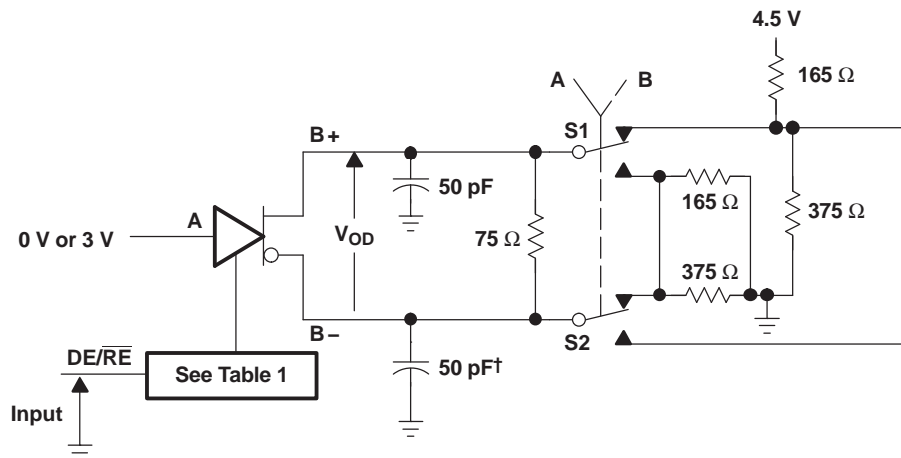
**Figure 4. Receiver Propagation Delay and Transition Time Test Circuit**



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50$   $\Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

**Figure 5. Receiver Delay and Transition Time Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)



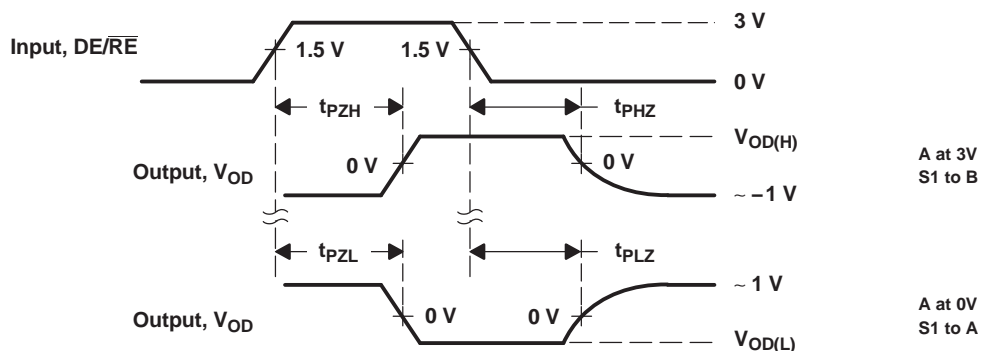
† Includes probe and jig capacitance in two places.

- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

Figure 6. Driver Enable and Disable Time Test Circuit

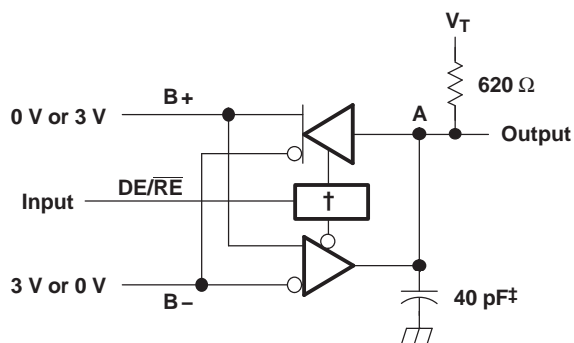
Table 1. Enabling For Driver Enable and Disable Time

DRIVER	BSR	CDE0	CDE1	CDE2	CRE
1 – 8	H	H	L	L	X
9	L	H	H	H	H



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

Figure 7. Driver Enable Time Waveforms

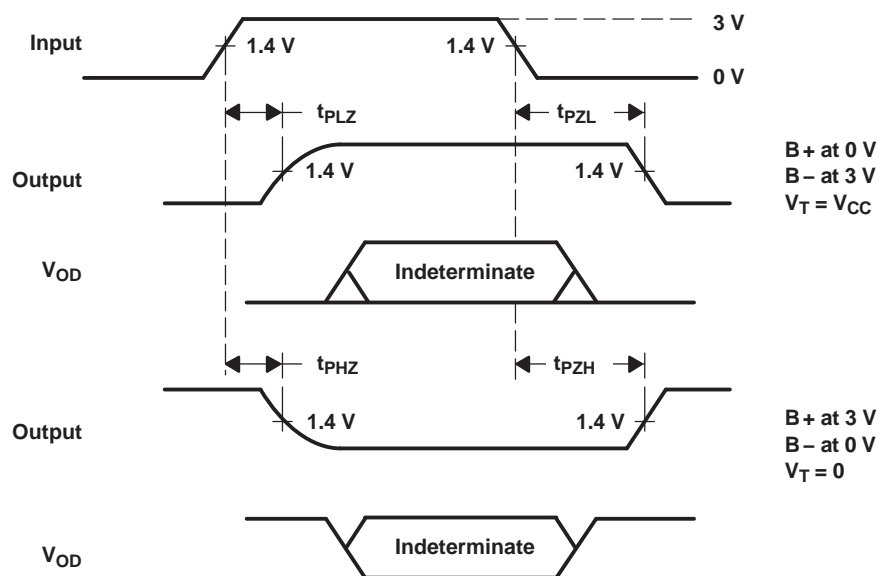


† CDE0 is high, CDE1, CDE2, BSR, and  $\overline{\text{CRE}}$  are low and, for the SN75976A only, all others are open.

‡ Includes probe and jig capacitance.

- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

Figure 8. Receiver Enable and Disable Time Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

Figure 9. Receiver Enable and Disable Time Waveforms

## TYPICAL CHARACTERISTICS

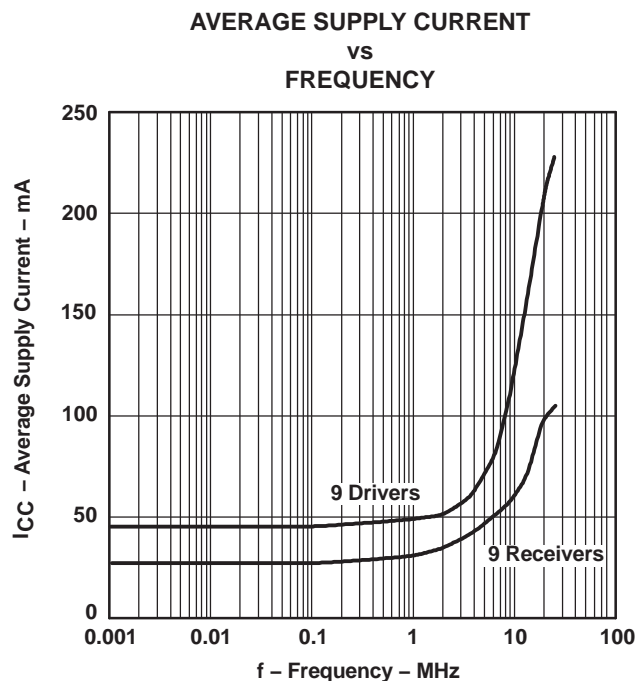


Figure 10.

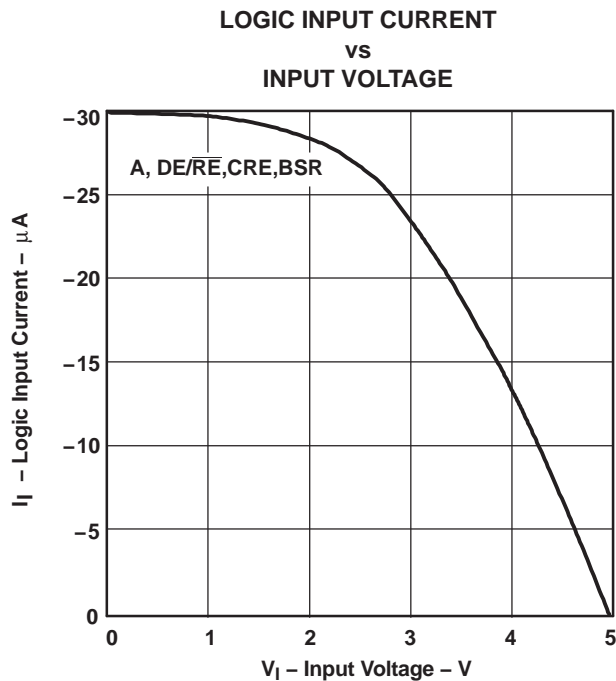


Figure 11.

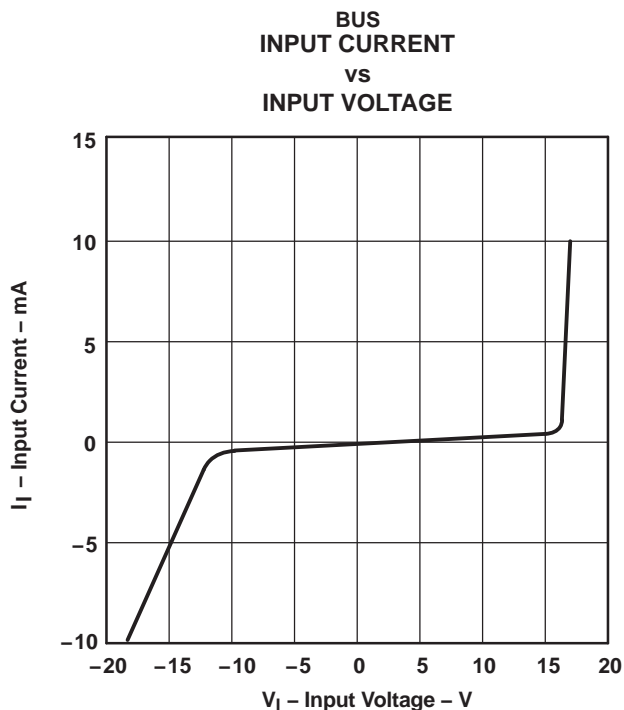


Figure 12.

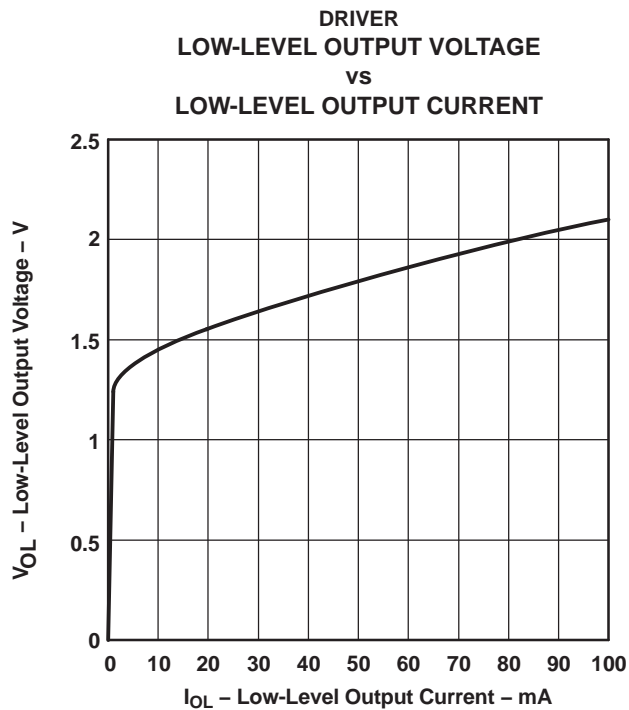


Figure 13.

# TYPICAL CHARACTERISTICS (continued)

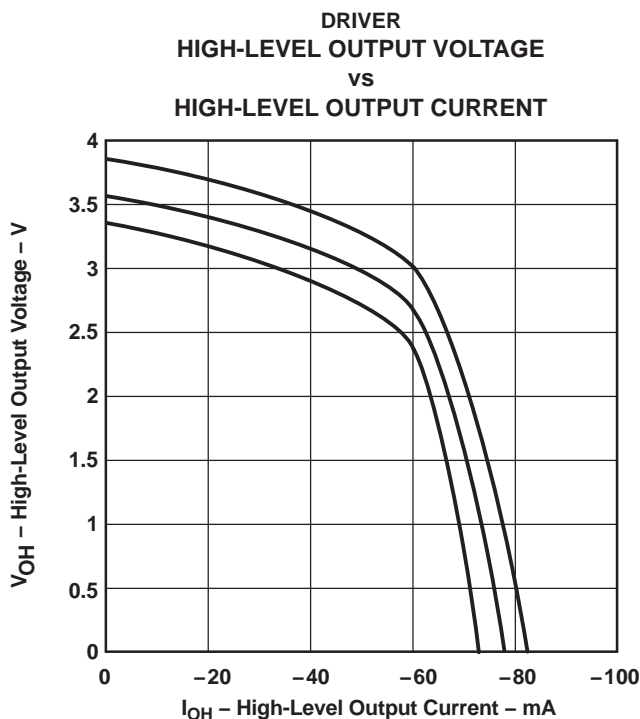


Figure 14.

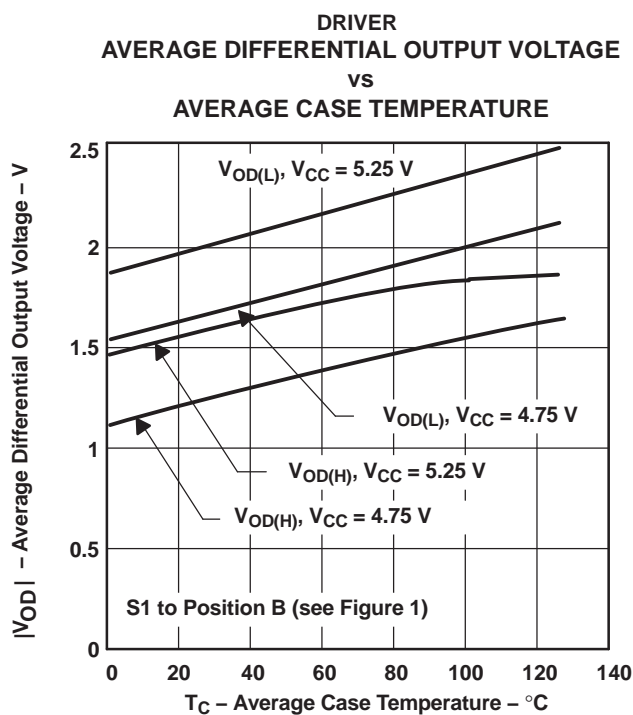


Figure 15.

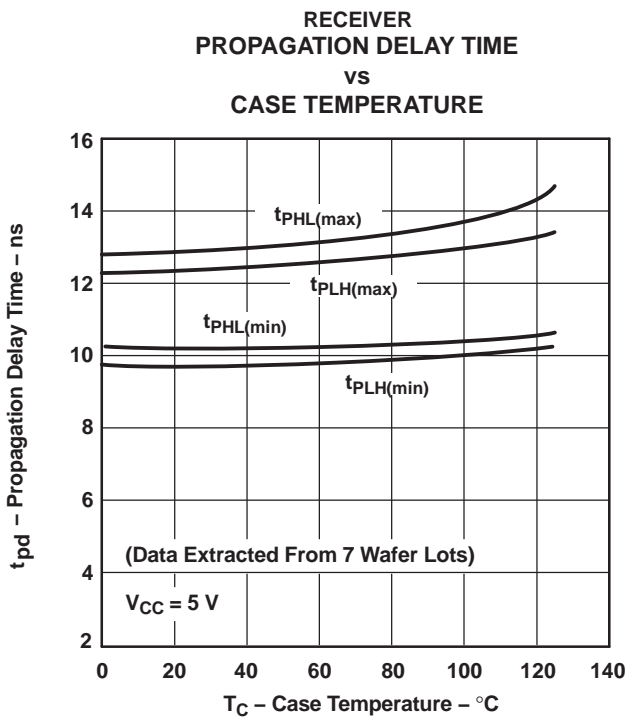


Figure 16.

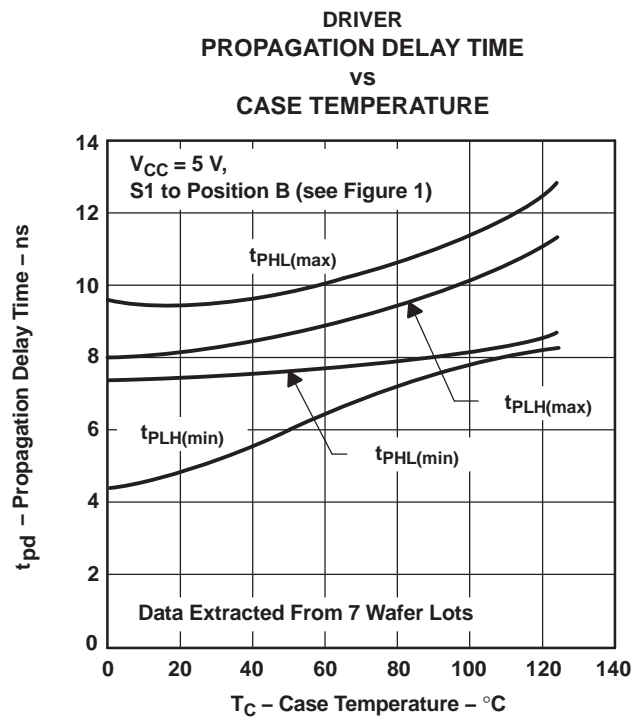
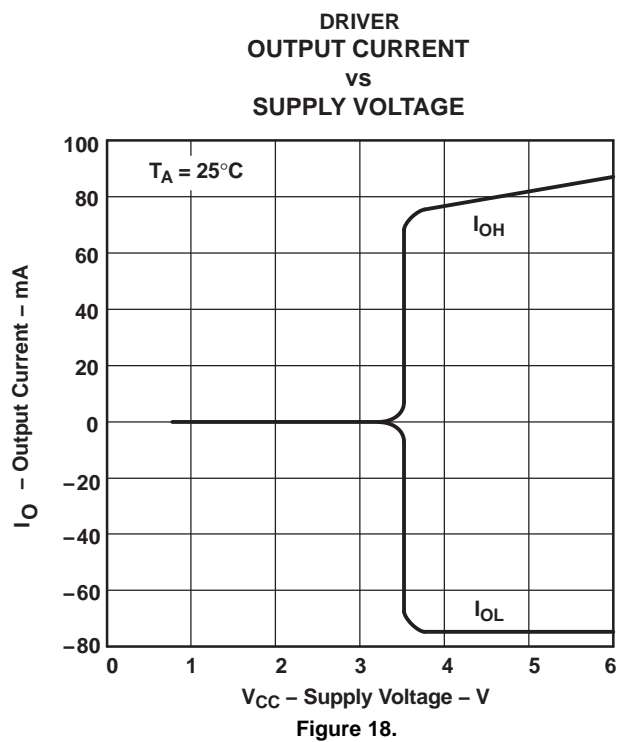


Figure 17.

**TYPICAL CHARACTERISTICS (continued)**





## APPLICATION INFORMATION

**Table 2. Typical Signal and Terminal Assignments<sup>(1)(2)</sup>**

SIGNAL	TERMINAL	SCSI DATA	SCSI CONTROL	IPI DATA	IPI CONTROL
CDE0	54	DIFFSENSE	DIFFSENSE	V <sub>CC</sub>	V <sub>CC</sub>
CDE1	55	GND	GND	XMTA, XMTB	GND
CDE2	56	GND	GND	XMTA, XMTB	SLAVE/MASTER
BSR	2	GND	GND	GND, BSR	GND
$\overline{\text{CRE}}$	3	GND	GND	GND	V <sub>CC</sub>
1A	4	DB0, DB8	ATN	AD7, BD7	NOT USED
1DE/ $\overline{\text{RE}}$	5	DBE0, DBE8	INIT EN	GND	GND
2A	6	DB1, DB9	BSY	AD6, BD6	NOT USED
2DE/ $\overline{\text{RE}}$	7	DBE1, DBE9	BSY EN	GND	GND
3A	8	DB2, DB10	ACK	AD5, BD5	SYNC IN
3DE/ $\overline{\text{RE}}$	9	DBE2, DBE10	INIT EN	GND	GND
4A	10	DB3, DB11	RST	AD4, BD4	SLAVE IN
4DE/ $\overline{\text{RE}}$	11	DBE3, DBE11	GND	GND	GND
5A	19	DB4, DB12	MSG	AD3, BD3	NOT USED
5DE/ $\overline{\text{RE}}$	20	DBE4, DBE12	TARG EN	GND	GND
6A	21	DB5, DB13	SEL	AD2, BD2	SYNC OUT
6DE/ $\overline{\text{RE}}$	22	DBE5, DBE13	SEL EN	GND	GND
7A	23	DB6, DB14	C/D	AD1, BD1	MASTER OUT
7DE/ $\overline{\text{RE}}$	24	DBE6, DBE14	TARG EN	GND	GND
8A	25	DB7, DB15	REQ	AD0, BD0	SELECT OUT
8DE/ $\overline{\text{RE}}$	26	DBE7, DBE15	TARG EN	GND	GND
9A	27	DBP0, DBP1	I/O	AP, BP	ATTENTION IN
9DE/ $\overline{\text{RE}}$	28	DBPE0, DBPE1	TARG EN	XMTA, XMTB	V <sub>CC</sub>

(1) ABBREVIATIONS:

DBn = data bit n, where n = (0, 1, . . . , 15)

DBEn = data bit n enable, where n = (0, 1, . . . , 15)

DBP0 = parity bit for data bits 0 through 7 or IPI bus A

DBPE0 = parity bit enable for P0

DBP1 = parity bit for data bits 8 through 15 or IPI bus B

DBPE1 = parity bit enable for P1

ADn or BDn = IPI Bus A – Bit n (ADn) or Bus B – Bit n (BDn), where n = (0, 1, . . . , 7)

AP or BP = IPI parity bit for bus A or bus B

XMTA or XMTB = transmit enable for IPI bus A or B

BSR = bit significant response

INIT EN = common enable for SCSI initiator mode

TARG EN = common enable for SCSI target mode

(2) Signal inputs are shown as active high. When only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connector terminal assignments.

### Function Tables

#### RECEIVER



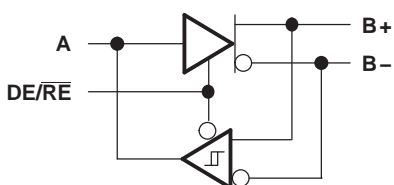
INPUTS		OUTPUT A
B+(B)	B-(B)	
L	H	L
H	L	H

#### DRIVER



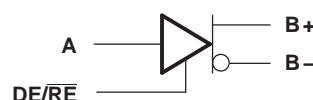
INPUT A	OUTPUTS	
	B+	B-
L	L	H
H	H	L

#### TRANSCIEVER



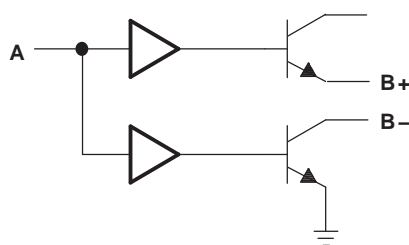
INPUTS				OUTPUTS		
DE/RE	A	B+(B)	B-(B)	A	B+	B-
L	-	L	H	L	-	-
L	-	H	L	H	-	-
H	L	-	-	-	L	H
H	H	-	-	-	H	L

#### DRIVER WITH ENABLE



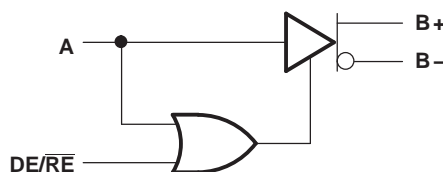
INPUTS		OUTPUTS	
DE/RE	A	B+	B-
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

#### WIRED-OR DRIVER



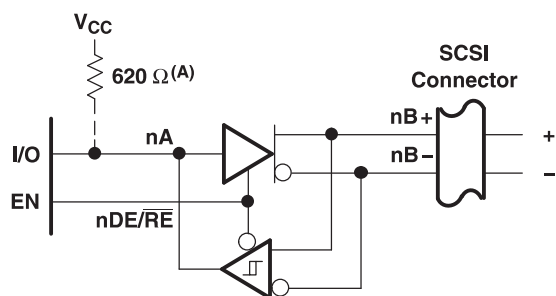
INPUT A	OUTPUTS	
	B+	B-
L	Z	Z
H	H	L

#### TWO-ENABLE INPUT DRIVER

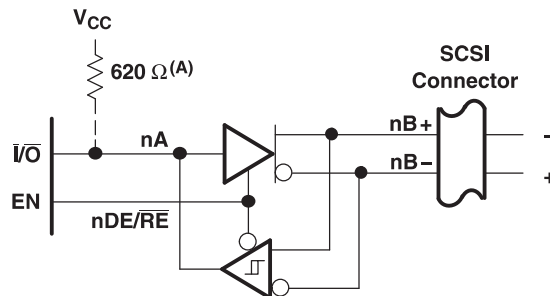


INPUTS		OUTPUTS	
DE/RE	A	B+	B-
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

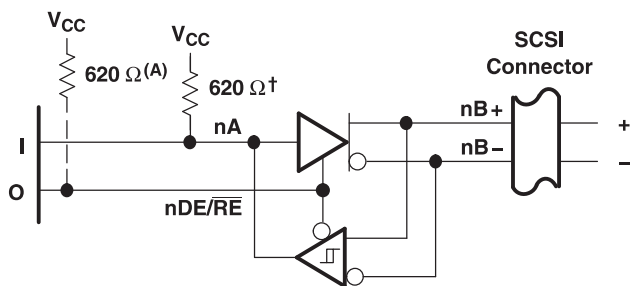
- A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
- B. An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.



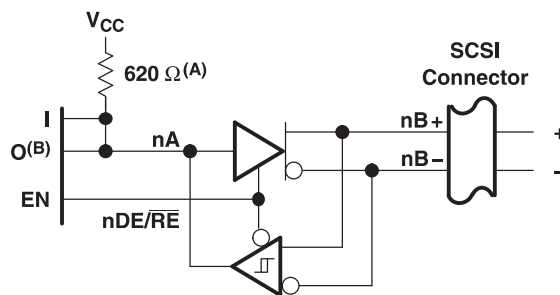
(a) ACTIVE-HIGH BIDIRECTIONAL I/O  
WITH SEPARATE ENABLE



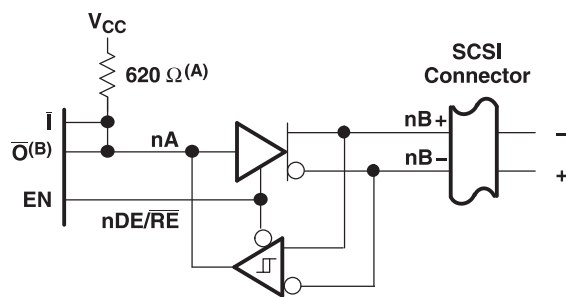
(b) ACTIVE-LOW BIDIRECTIONAL I/O  
WITH SEPARATE ENABLE



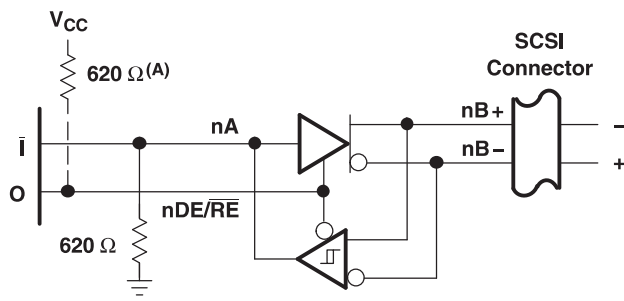
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT,  
AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND  
OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

- A. When 0 is open drain
- B. Must be open-drain or 3-state output
- C. The BSR,  $\overline{\text{CRE}}$ , A, and  $\text{DE}/\overline{\text{RE}}$  inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 19. Typical SCSI Transceiver Connections

## Channel Logic Configurations With Control Input Logic

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and  $C_{RE}$  bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

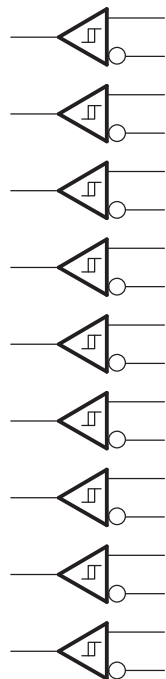


Figure 20. 00000

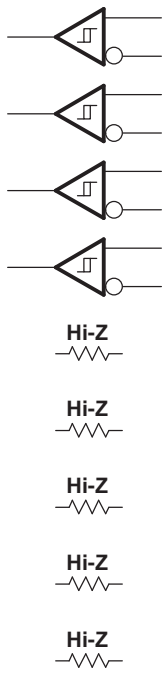


Figure 21. 00001

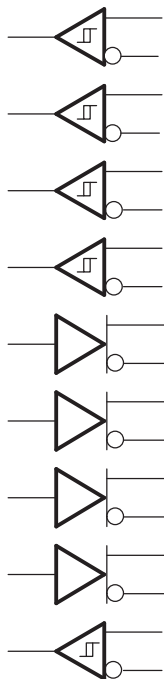


Figure 22. 00010

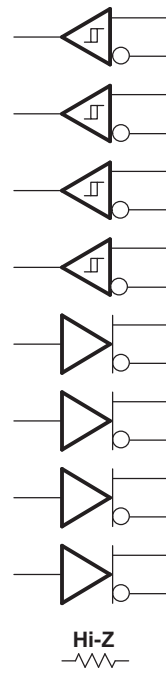


Figure 23. 00011

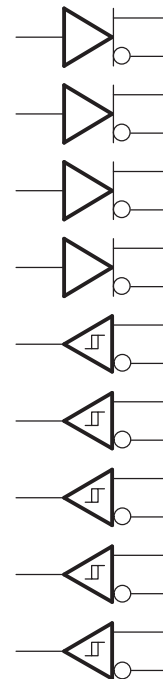


Figure 24. 00100

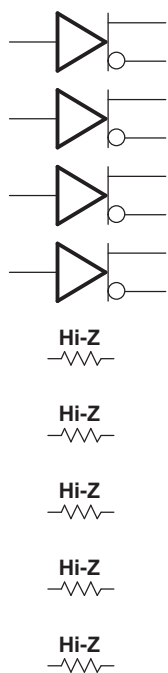


Figure 25. 00101

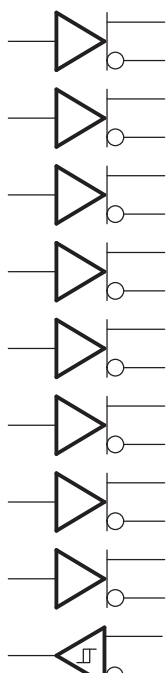


Figure 26. 00110

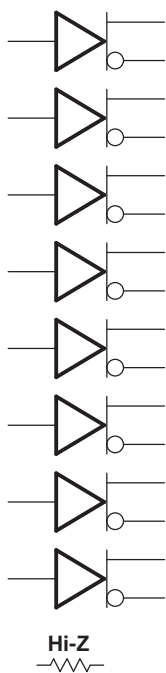


Figure 27. 00111

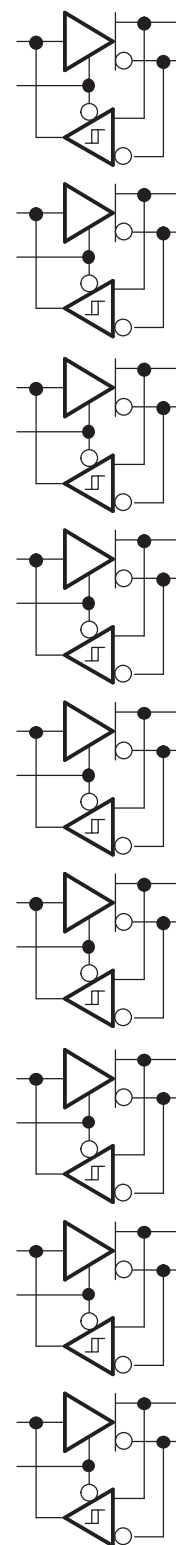


Figure 28. 01000

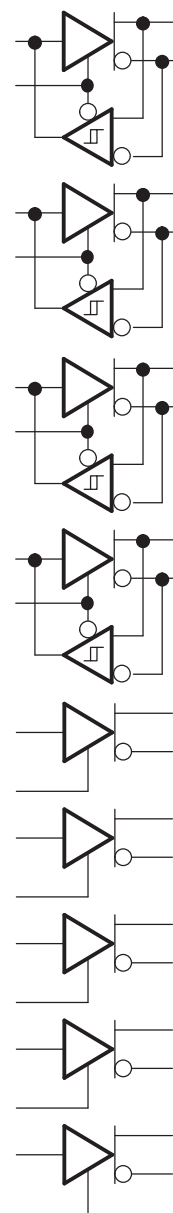
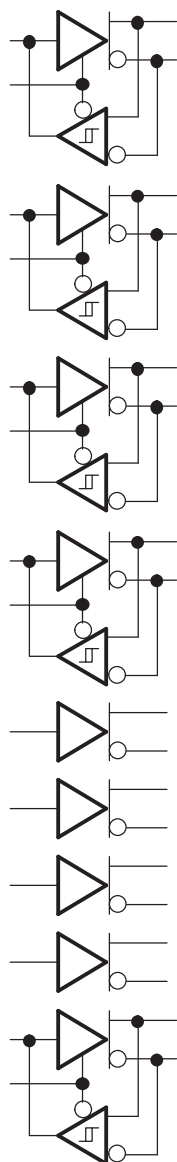
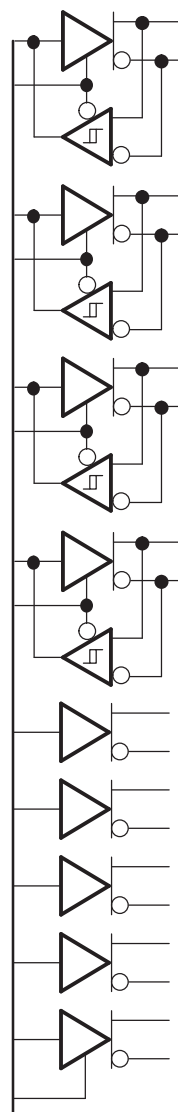


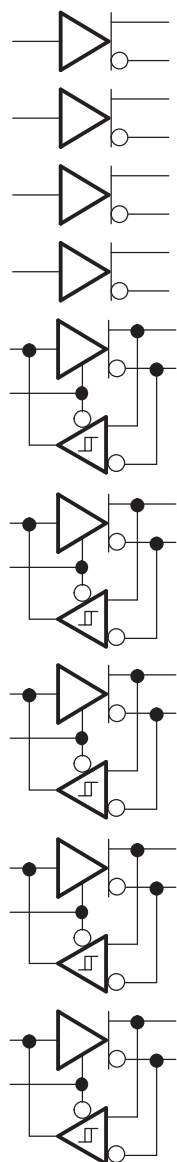
Figure 29. 01001



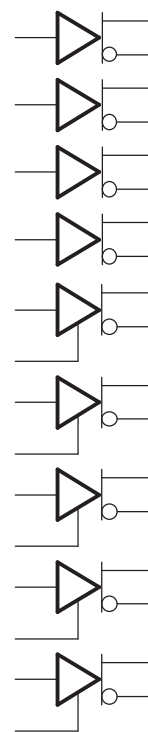
**Figure 30. 01010**



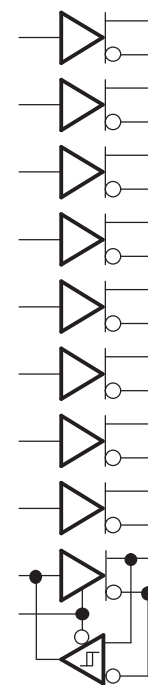
**Figure 31. 01011**



**Figure 32. 01100**



**Figure 33. 01101**



**Figure 34. 01110**

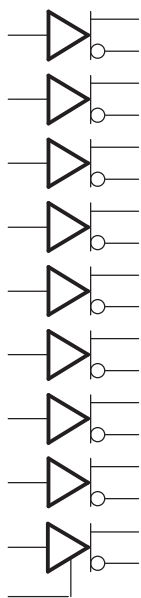


Figure 35. 01111



Figure 36. 10000  
and 10001

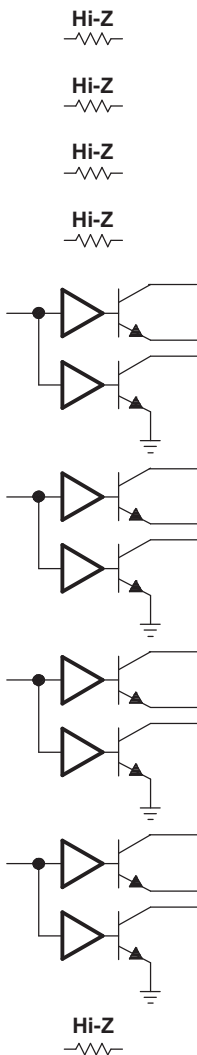


Figure 37. 10010  
and 10011

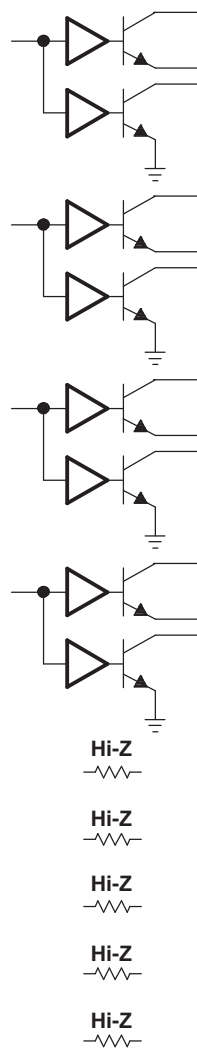


Figure 38. 10100  
and 10101

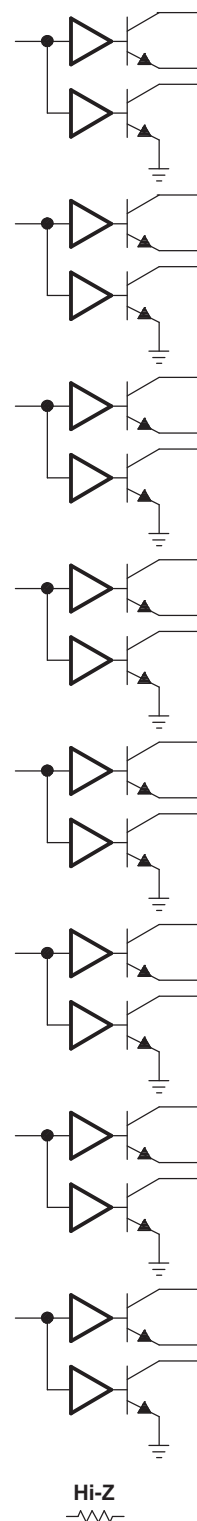
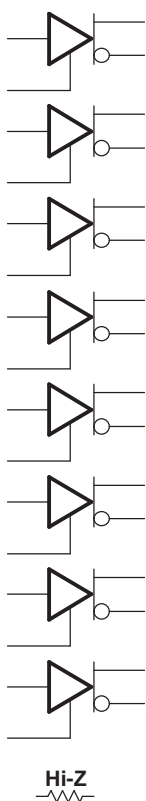
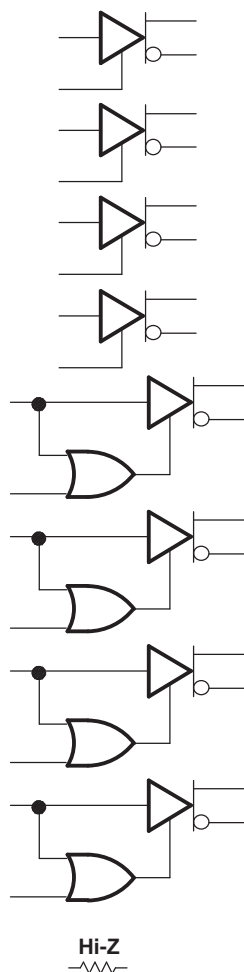


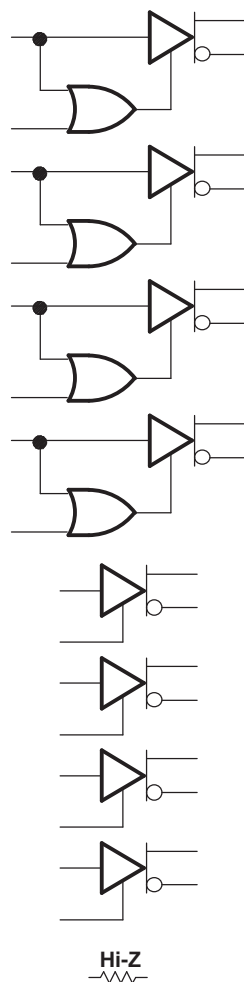
Figure 39. 10110  
and 10111



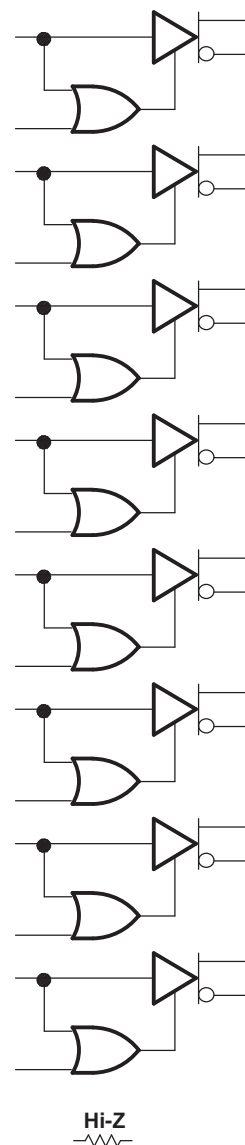
**Figure 40. 11000 and 11001**



**Figure 41. 11010 and 11011**



**Figure 42. 11100 and 11101**



**Figure 43. 11110 and 11111**



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN75976A1MDGGREP</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2E976A1EP
SN75976A1MDGGREP.A	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2E976A1EP
<a href="#">V62/08614-01XE</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2E976A1EP

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN75976A-EP :

- Catalog : [SN75976A](#)

- Military : [SN55976A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

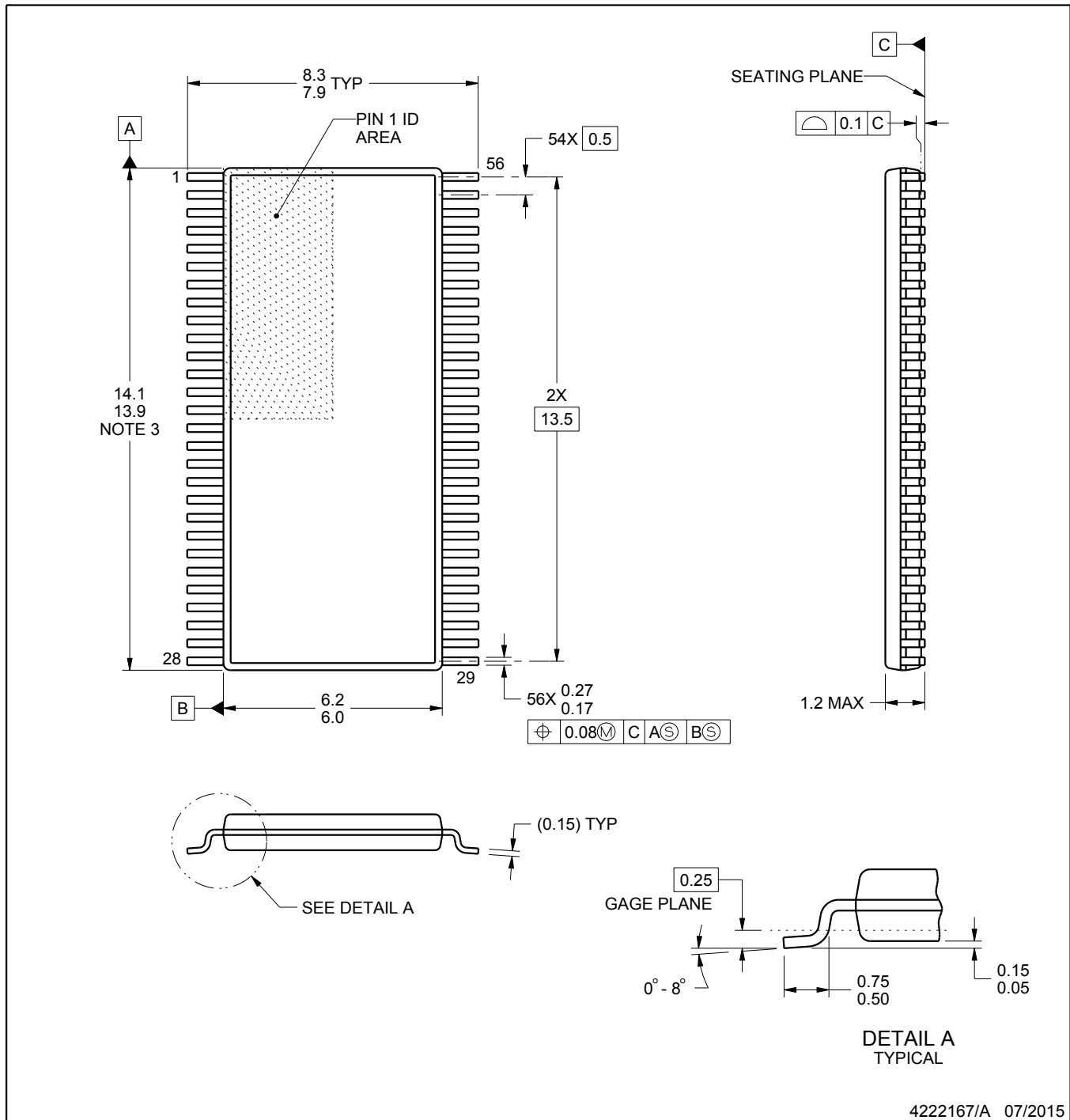
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75976A1MDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75976A1MDGGREP	TSSOP	DGG	56	2000	356.0	356.0	45.0



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## NOTES:

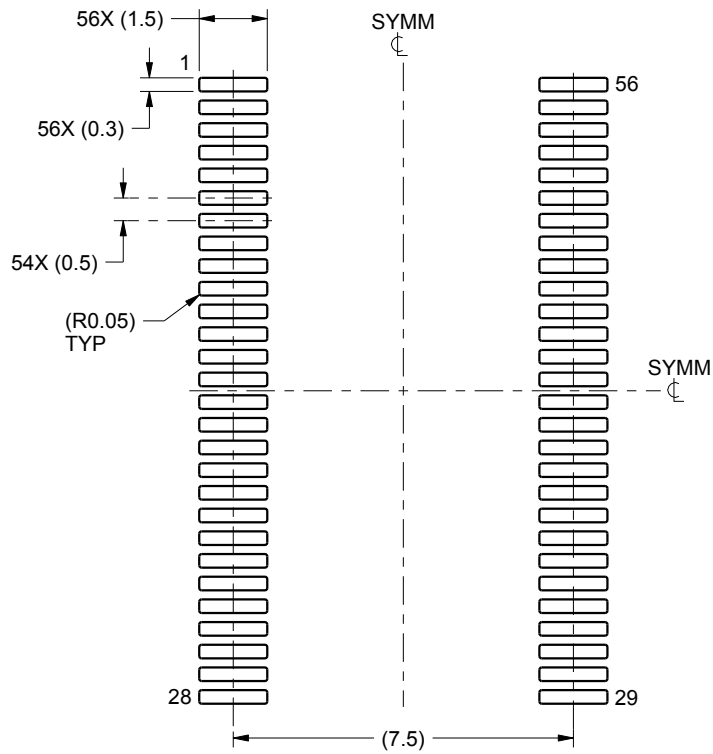
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

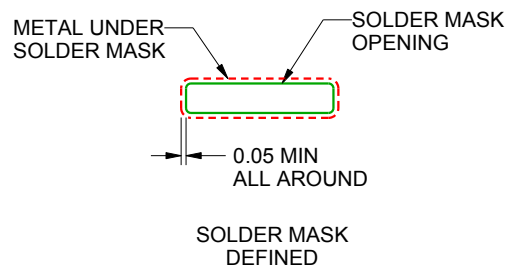
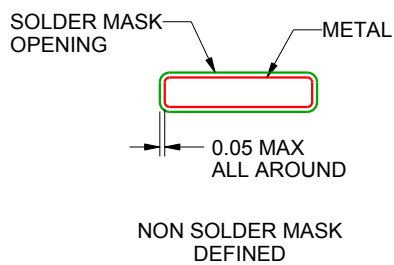
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

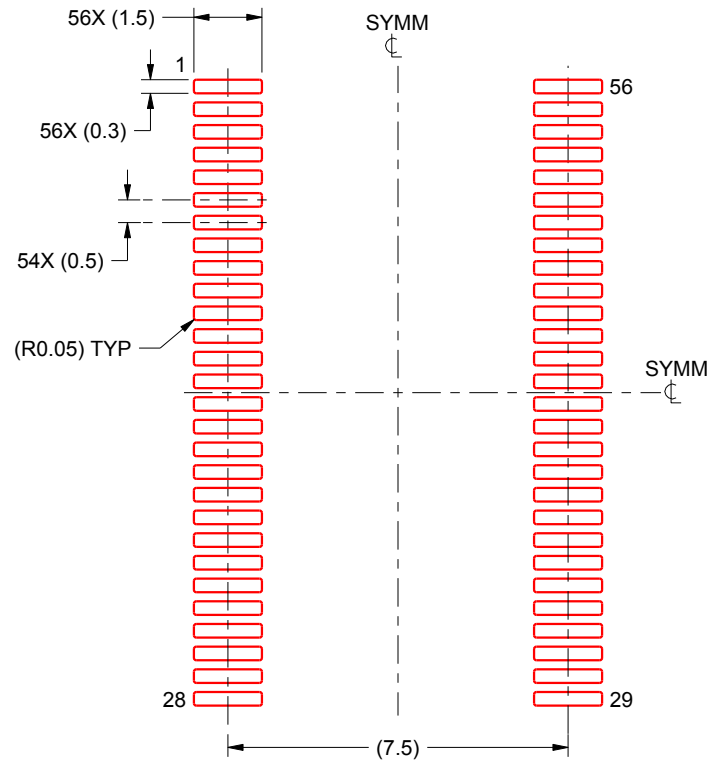
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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