

SN751177、SN751178 双路差分驱动器和接收器

1 特性

- 符合或超出 ANSI 标准 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.10 和 V.11 的要求
- 适用于嘈杂环境中长总线上的多点总线传输
- 驱动器正负电流限制
- 热关断保护
- 驱动器三态输出
- 接收器共模输入电压范围为 -12V 至 12V
- 接收器输入灵敏度： $\pm 200\text{mV}$
- 接收器迟滞： 50mV (典型值)
- 接收器输入阻抗： $12\text{k}\Omega$ (最小值)
- 接收器三态输出 (仅限 SN751177)
- 由 5V 单电源供电

2 应用

- 电机驱动器
- 工厂自动化
- 楼宇自动化

3 说明

SN751177 和 SN751178 双路差分驱动器和接收器是单片集成电路，专为速率高达 10Mbps 的平衡多点总线传输而设计。这些器件旨在提高长总线线路上全双工数据通信性能，符合 ANSI 标准 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.10 和 V.11。

SN751177 和 SN751178 驱动器输出可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。

该接收器具有至少 $12\text{k}\Omega$ 的高输入阻抗，在 -12V 至 12V 的共模输入电压范围内的输入灵敏度为 $\pm 200\text{mV}$ ，典型输入迟滞为 50mV 。失效防护设计可确保在接收器输入处于开路状态时，接收器输出始终为高电平。

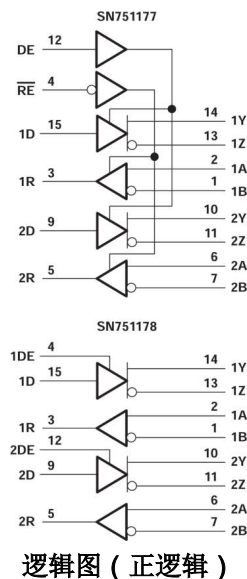
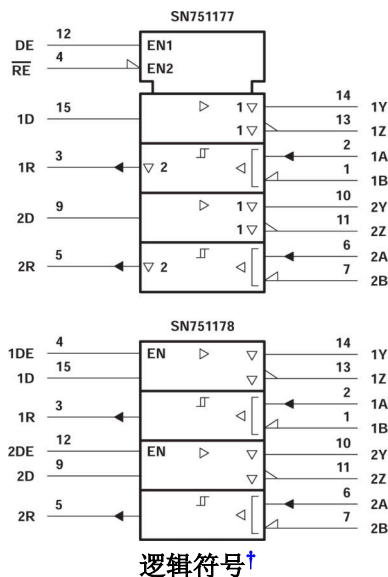
SN751177 和 SN751178 的额定工作温度范围为 -20°C 至 85°C 。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN751177	PDIP (N, 16)	19.3mm x 9.4mm
SN751178	SO (NS, 16)	10.2mm x 7.8mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



[†] 这些符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。



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4 Pin Configuration and Functions

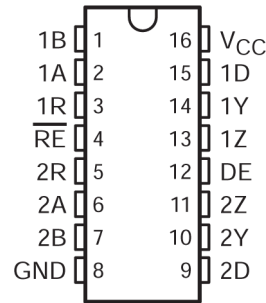


图 4-1. SN751177: N or NS Package (Top View)

PIN			TYPE	DESCRIPTION
NAME	PDIP	SO		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
DE	12	12	I	Driver enable (active high)
GND	8	8	—	Device ground pin
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
RE	4	4	I	Receiver enable pin (active low)
V _{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (inverting) driver output 1
2Z	11	11	O	RS-422 differential (inverting) driver output 2

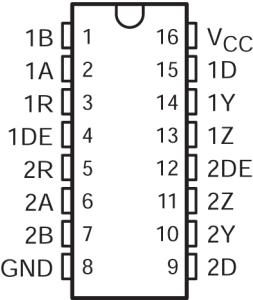


图 4-2. SN751178: N or NS Package
(Top View)

PIN			TYPE	DESCRIPTION
NAME	PDIP	SO		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
1DE	4	4	I	Driver 1 enable (active high)
2DE	12	12	I	Driver 2 enable (active high)
GND	8	8	—	Device ground
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
V _{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (non inverting) driver output 1
2Z	11	11	O	RS-422 differential (non inverting) driver output 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage, (see note ⁽²⁾)		7	V
V _I	Input voltage, (DE, RE, and D inputs)		7	V
V _I	Receiver input voltage range, (A or B inputs)	–25	25	V
V _{ID}	Receiver differential input voltage range, (see note ⁽³⁾)	–25	25	V
V _O	Driver output voltage range	–10	15	V
I _{OL}	Receiver low-level output current		50	mA
T _{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
- (3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

5.2 Thermal Information

THERMAL METRIC ⁽¹⁾		N	NS	UNIT
		16-PINS	16-PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	60.6	88.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.1	46.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	40.6	50.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.5	13.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	40.3	50.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, V _{IH}	DE, RE, and D inputs	2			V
Low-level input voltage, V _{IL}				0.8	V
Common-mode output voltage, V _{OC}	Driver	–7 ⁽¹⁾		12	V
High-level output current, I _{OH}				–60	mA
Low-level output current, I _{OL}				60	mA
Common-mode input voltage, V _{IC}	Receiver			±12	V
Differential input voltage, V _{ID}				±12	V
High-level output current, I _{OH}				–400	μA
Low-level output current, I _{OL}				16	mA

5.3 Recommended Operating Conditions (续)

	MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	-20		85	°C

- (1) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

5.4 Driver Sections

5.4.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18\text{mA}$					-1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = -33\text{mA}$				3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = 33\text{mA}$				1.1		V
$ V_{OD1} $	Differential output voltage	$I_O = 0$			1.5		6	V
$ V_{OD2} $	Differential output voltage	$R_L = 100\ \Omega$, $R_L = 54\ \Omega$, See Note 4	See 图 6-1 See 图 6-1		2 or 1/2 V_{OD1} ⁽²⁾ 1.5			V
V_{OD3}	Differential output voltage	See Note 4			1.5		5	V
$\Delta V_{OD} $	Change in magnitude of differential output voltage (see Note 5)						± 0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$, See 图 6-1			-1 ⁽³⁾		3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage (see Note 5)						± 0.2	V
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7\text{V}$ to 12V					± 100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7\text{V}$ to 12V					± 100	μA
I_{IH}	High-level input current	$V_{IH} = 2.7\text{V}$					20	μA
I_{IL}	Low-level input current	$V_{IL} = 0.4\text{V}$					-100	μA
		$V_O = -7\text{V}$					-250	
I_{OS}	Short-circuit output current (see Note 6)	$V_O = V_{CC}$					250	mA
		$V_O = 12\text{V}$					250	
I_{CC}	Supply current	No load	Outputs enabled			80	110	mA
			Outputs disabled			50	80	

- (1) All typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
 (2) The minimum V_{OD2} with a $100\ \Omega$ load is either $1/2 V_{OD1}$ or 2V , whichever is greater.
 (3) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
 (4) See TIA/EIA-485-A [图 6-3.5](#), Test Termination Measurement 2
 (5) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.
 (6) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

5.4.2 Switching Characteristics

at $V_{CC} = 5\text{V}$, $C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$, See 图 6-3			20	25	ns
$t_{t(OD)}$	Differential output transition time				27	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	$R_L = 27\ \Omega$, See 图 6-4			20	25	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	25	ns

5.4.2 Switching Characteristics (续)

at $V_{CC} = 5V$, $C_L = 50pF$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See 图 6-5		80	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See 图 6-6		40	60	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See 图 6-5		90	120	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See 图 6-6		30	45	ns

5.4.3 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100\ \Omega)$	$V_t (R_L = 54\ \Omega)$
$ V_{OD3} $		V_t (Test Termination Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{OS} $	$ V_{OS} $
$\Delta V_{OC} $	$ V_{OS} - \bar{V}_{OS} $	$ V_{OS} - \bar{V}_{OS} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

5.5 Receiver Sections

5.5.1 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7V$,	$I_O = -0.4mA$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5V$,	$I_O = 16mA$	-0.2 ⁽²⁾			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable clamp voltage	SN751177	$I_I = -18mA$			-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200mV$,	$I_{OH} = -400\ \mu A$	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200mV$	$I_{OL} = 8mA$ $I_{OL} = 16mA$			0.45 0.5	V
I_{OZ}	High-impedance-state output current	SN751177	$V_O = 0.4V$ to $2.4V$			± 20	μA
I_I	Line input current (see Note 7)		Other input at 0V $V_I = 12V$ $V_I = -7V$			1 -0.8	mA
I_{IH}	High-level enable input current	SN751177	$V_{IH} = 2.7V$			20	μA
I_{IL}	Low-level enable input current	SN751177	$V_{IL} = 0.4V$			-100	μA
I_{OS}	Short-circuit output current (see Note 6)			-15		-85	μA
I_{CC}	Supply current		No load, outputs enabled		80	110	mA
r_i	Input resistance			12			k Ω

- (1) All typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.
- (2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
- (3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
- (4) Refer to ANSI Standards TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.

5.5.2 Switching Characteristics

at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output		V _{ID} = −1.5V to 1.5V,	See 图 6-7		20	35	ns
t _{PHL}	Propagation delay time, high- to low-level output					22	35	ns
t _{PZH}	Output enable time to high level	SN751177	See 图 6-8			17	25	ns
t _{PZL}	Output enable time to low level					20	27	ns
t _{PHZ}	Output disable time from high level					25	40	ns
t _{PLZ}	Output disable time from low level					30	40	ns

6 Parameter Measurement Information

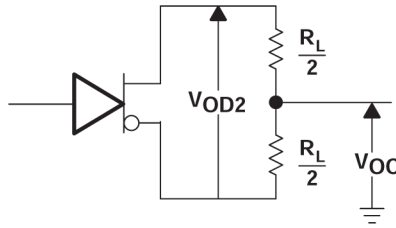


图 6-1. Driver Test Circuit, v_{OD} And v_{OC}

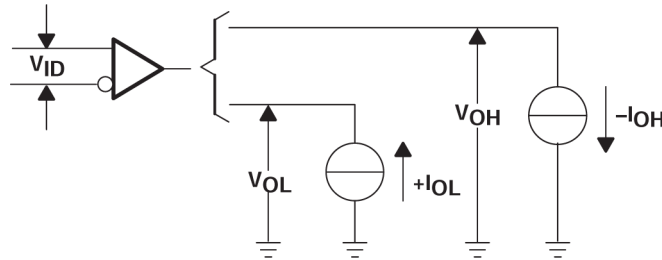
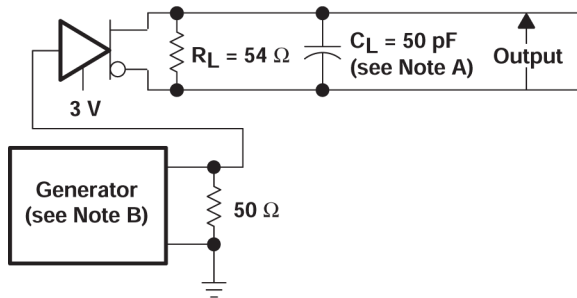
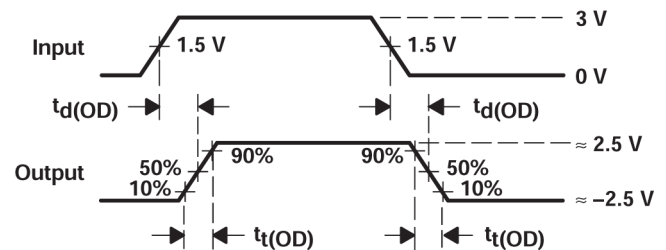


图 6-2. Receiver Test Circuit, v_{OH} And v_{OL}



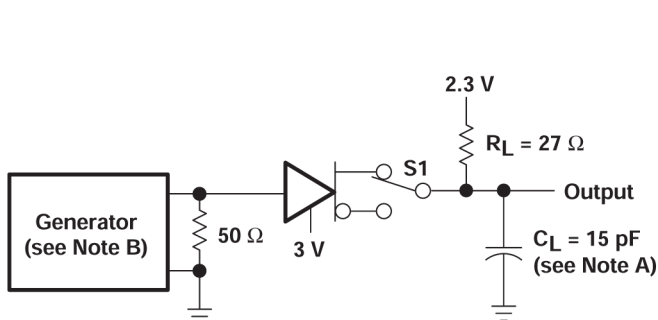
TEST CIRCUIT



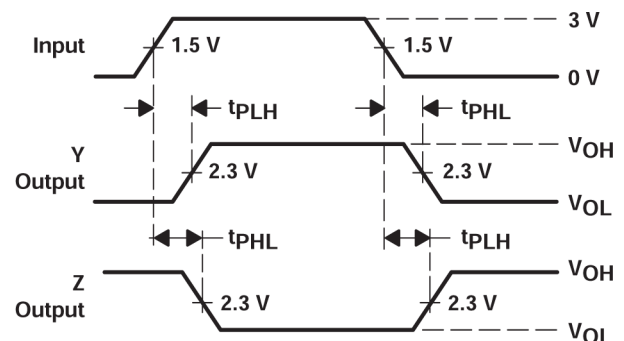
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.

图 6-3. Driver Differential Output-Delay and Transition-Time Test Circuit and Voltage Waveforms



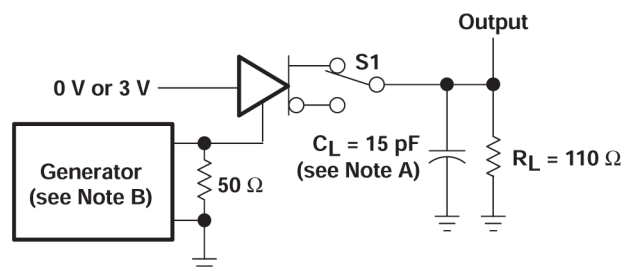
TEST CIRCUIT



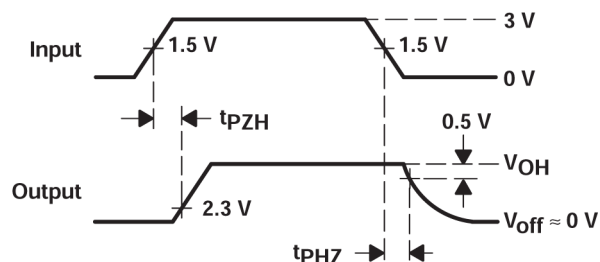
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.

图 6-4. Driver Propagation-Time Test Circuit and Voltage Waveforms



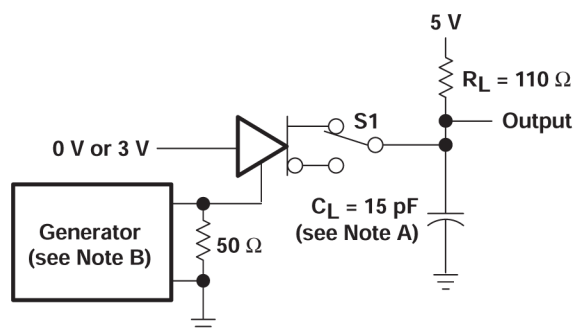
TEST CIRCUIT



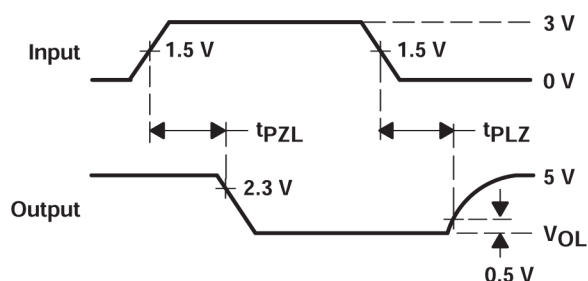
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $PRR \leq 1\text{MHz}$, 50% duty cycle, $Z_0 = 50\ \Omega$, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$.

图 6-5. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms



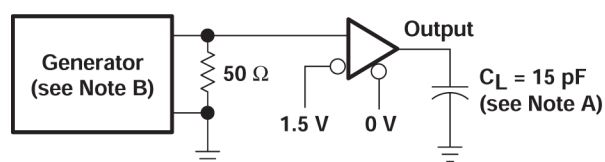
TEST CIRCUIT



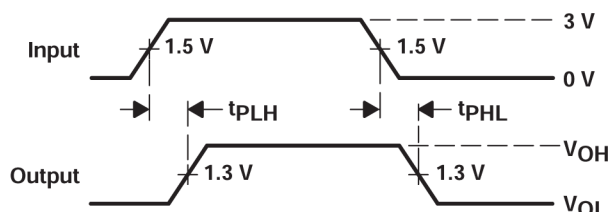
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $PRR \leq 1\text{MHz}$, 50% duty cycle, $Z_0 = 50\ \Omega$, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$.

图 6-6. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms



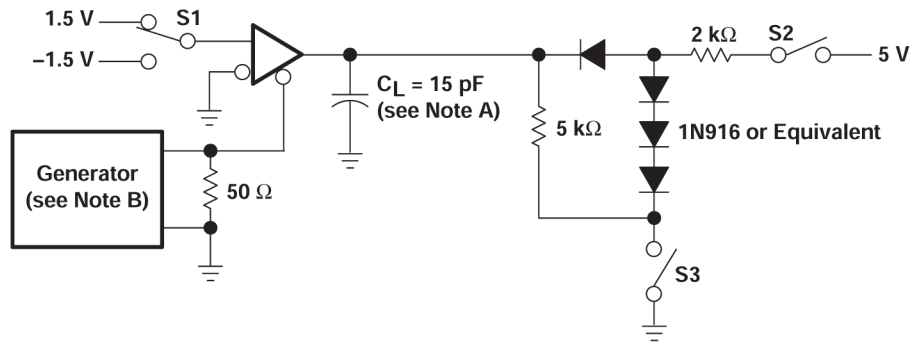
TEST CIRCUIT



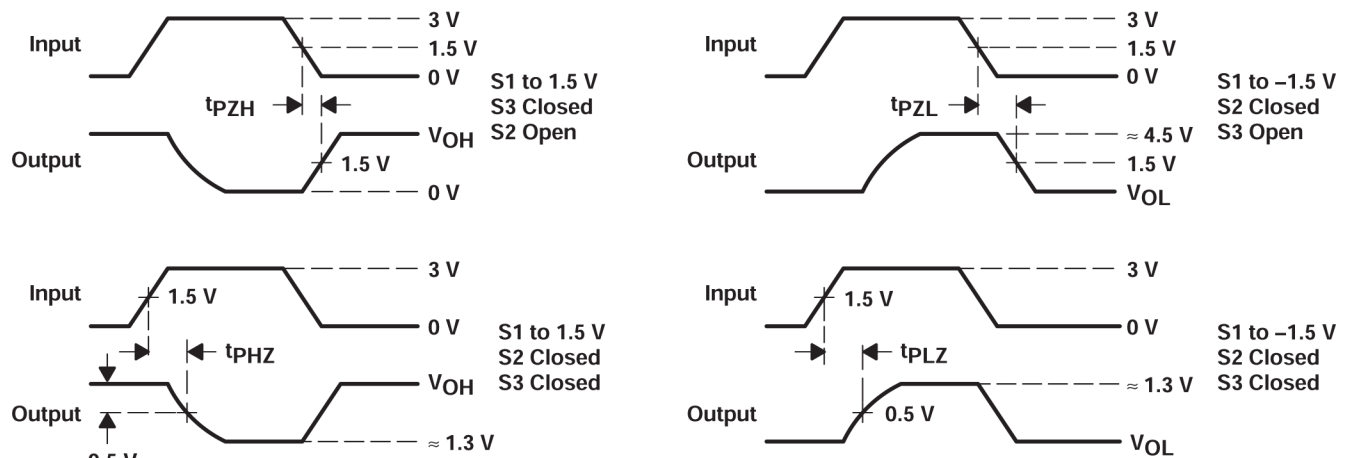
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $PRR \leq 1\text{MHz}$, 50% duty cycle, $Z_0 = 50\ \Omega$, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$.

图 6-7. Receiver Propagation-Time Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.

图 6-8. Receiver Output Enable- and Disable-Time Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. SN751177, SN751178 Functional Table (Each Driver)

INPUT D ⁽¹⁾	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

表 7-2. SN751177 Functional Table (Each Receiver)

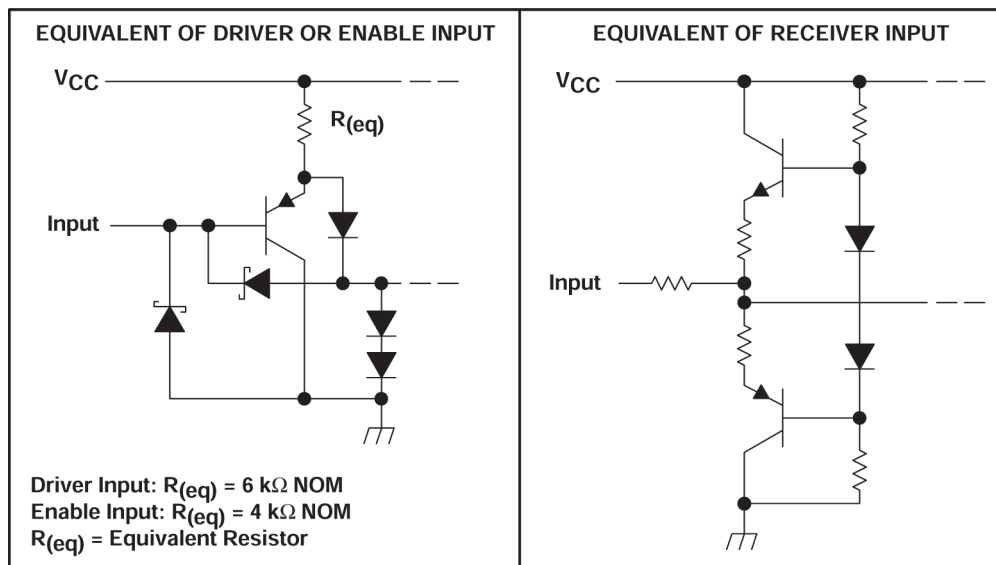
DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R ⁽¹⁾
$V_{ID} \geq 0.2V$	L	H
$-0.2V < V_{ID} < 0.2V$	L	?
$V_{ID} \leq -0.2V$	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 7-3. SN751178 Functional Table (Each Receiver)

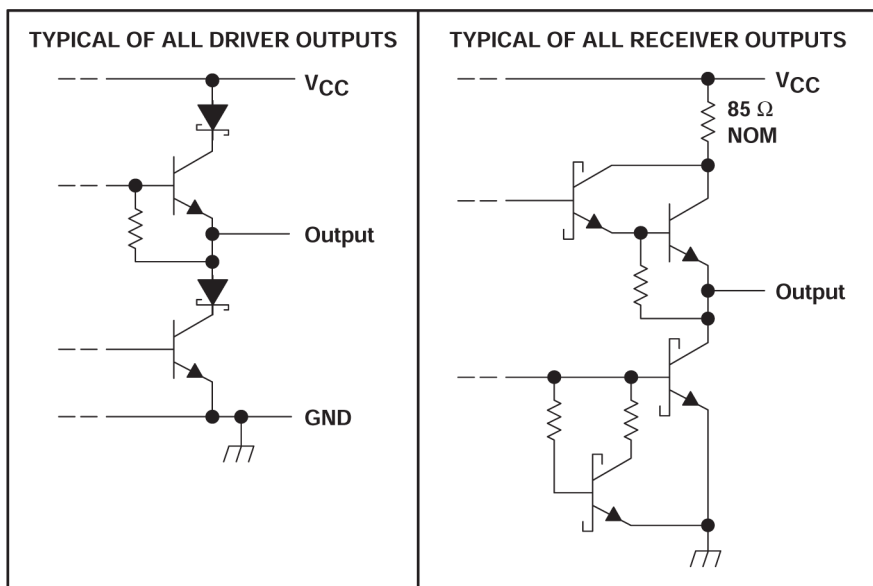
DIFFERENTIAL INPUTS A – B	OUTPUT R ⁽¹⁾
$V_{ID} \geq 0.2V$	H
$-0.2V < V_{ID} < 0.2V$	?
$V_{ID} \leq -0.2V$	L

(1) H = high level, L = low level, ? = indeterminate



A. All resistor values are nominal.

图 7-1. Schematics of Inputs



A. All resistor values are nominal.

图 7-2. Schematics of Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 1999) to Revision E (February 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN751177N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751177N
SN751177N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751177N
SN751177NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751177
SN751177NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751177
SN751177NSRE4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751177
SN751178N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751178N
SN751178N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751178N
SN751178NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751178
SN751178NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751178

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN751177NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN751178NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN751178NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN751177NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN751178NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN751178NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN751177N	N	PDIP	16	25	506	13.97	11230	4.32
SN751177N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN751178N	N	PDIP	16	25	506	13.97	11230	4.32
SN751178N.A	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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