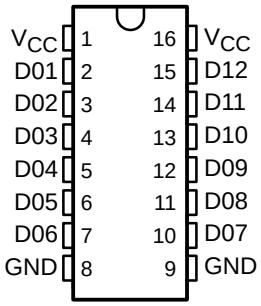
- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current to 200 mA**
- **12-Bit Array Structure Suited for Bus-Oriented Systems**

D, N, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

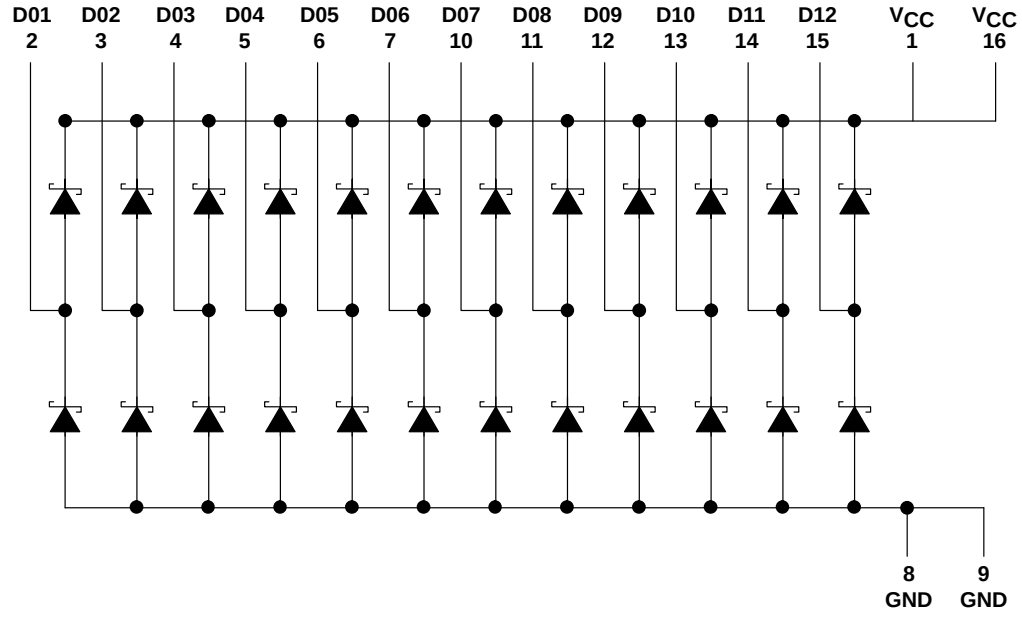
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74S1051N	SN74S1051N
	SOIC – D	Tube	SN74S1051D	S1051
		Tape and reel	SN74S1051DR	
	SOP – NS	Tape and reel	SN74S1051NSR	74S1051
	TSSOP – PW	Tape and reel	SN74S1051PWR	S1051

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic diagrams



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . . 7 V
Continuous forward current, I_F: Any D terminal from GND or to V_{CC} . . . . . 50 mA
Total through all GND or V_{CC} terminals . . . . . 170 mA
Repetitive peak forward current‡, I_{FRM}: Any D terminal from GND or V_{CC} . . . . . 200 mA
Total through all GND or V_{CC} terminals . . . . . 1 A
Package thermal impedance, θ_{JA} (see Note 1): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100$ µs, duty cycle ≤ 20%.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
V_F	Static forward voltage	To V_{CC}	I_F = 18 mA		0.85	1.05	V
			I_F = 50 mA		1.05	1.3	
		From GND	I_F = 18 mA		0.75	0.95	
			I_F = 50 mA		0.95	1.2	
V_{FM}	Peak forward voltage		I_F = 200 mA		1.45		V
I_R	Static reverse current	To V_{CC}	V_R = 7 V			5	µA
		From GND				5	
C_t	Total capacitance	V_R = 0 V,	f = 1 MHz		8	16	pF
		V_R = 2 V,	f = 1 MHz		4	8	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F current = 1 A,	See Note 3		0.8	2	mA
		Total I_F current = 198 mA,	See Note 3		0.02	0.2	

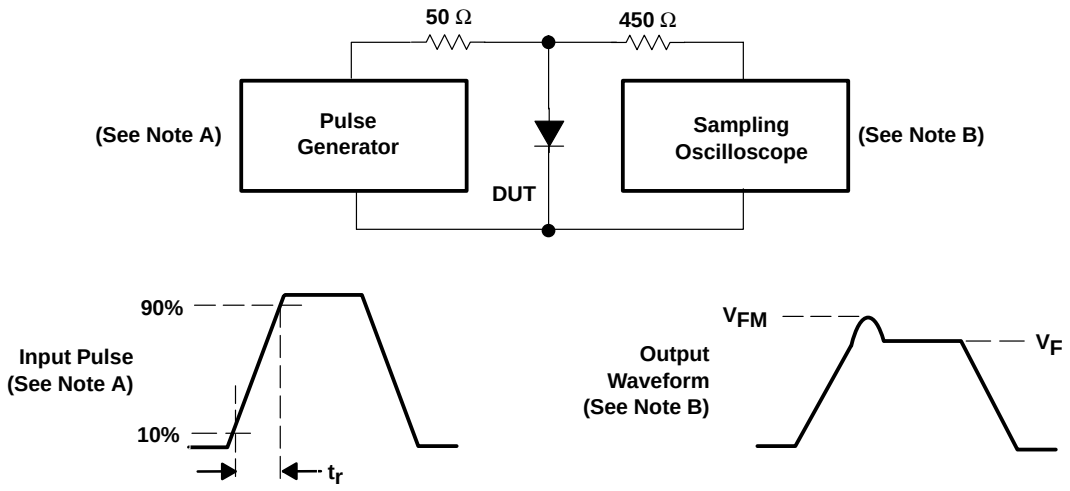
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: I_X is measured under the following conditions with one diode static, all others switching:
Switching diodes: t_w = 100 µs, duty cycle = 20%
Static diode: V_R = 5 V
The static diode input current is the internal crosstalk current, I_X.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

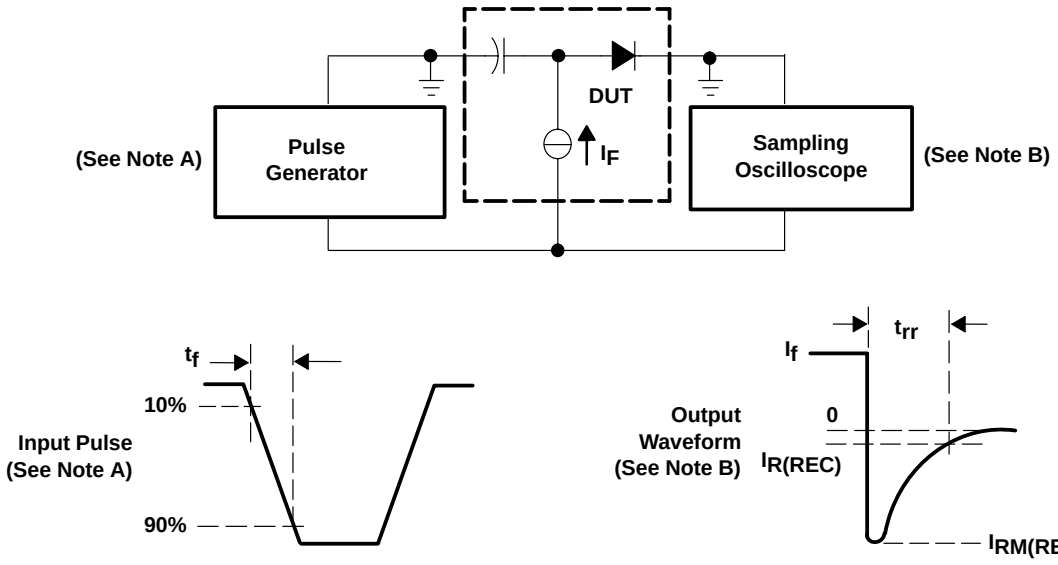
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_r = 20 ns, Z_O = 50 Ω, freq = 500 Hz, duty cycle = 1%.
B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \le 350$ ps, R_i = 50 Ω, $C_i \le 5$ pF.

Figure 1. Forward Recovery Voltage



NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_O = 50 Ω, $t_W \ge 50$ ns, duty cycle = 1%.
B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \le 350$ ps, R_i = 50 Ω, $C_i \le 5$ pF.

Figure 2. Reverse Recovery Time

APPLICATION INFORMATION

Large negative transients at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split-resistor or Thevenin-equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line because a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current-versus-voltage curves for the SN74S1051 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

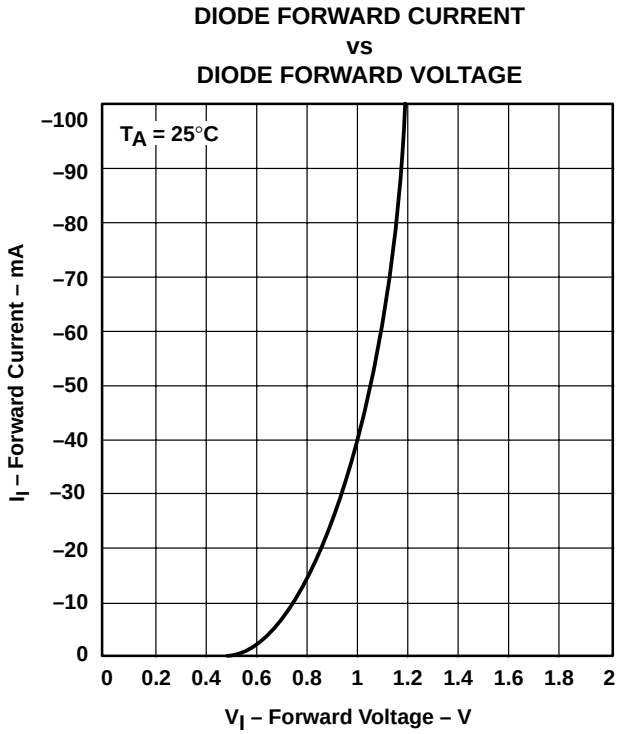


Figure 3. Typical Input Current vs Input Voltage (Lower Diode)

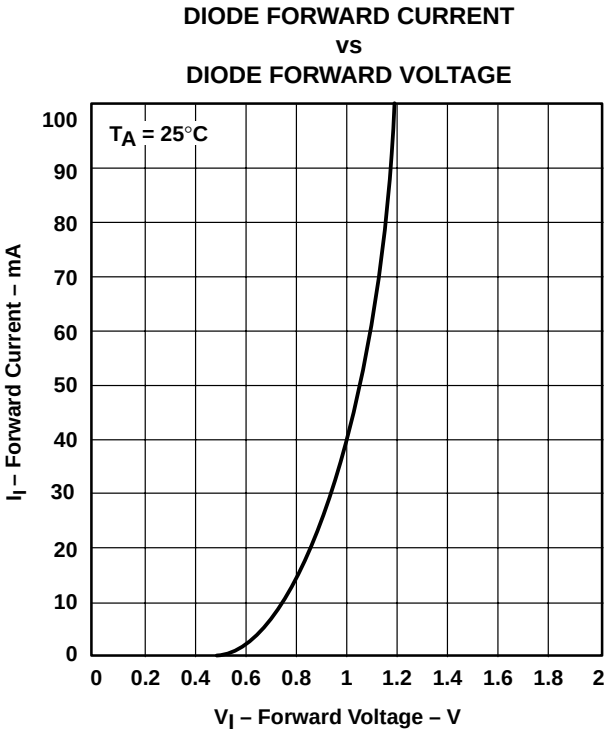


Figure 4. Typical Input Current vs Input Voltage (Upper Diode)

APPLICATION INFORMATION

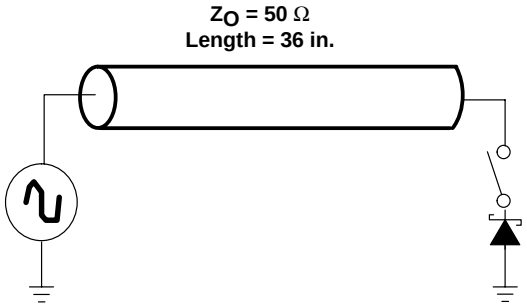


Figure 5. Diode Test Setup

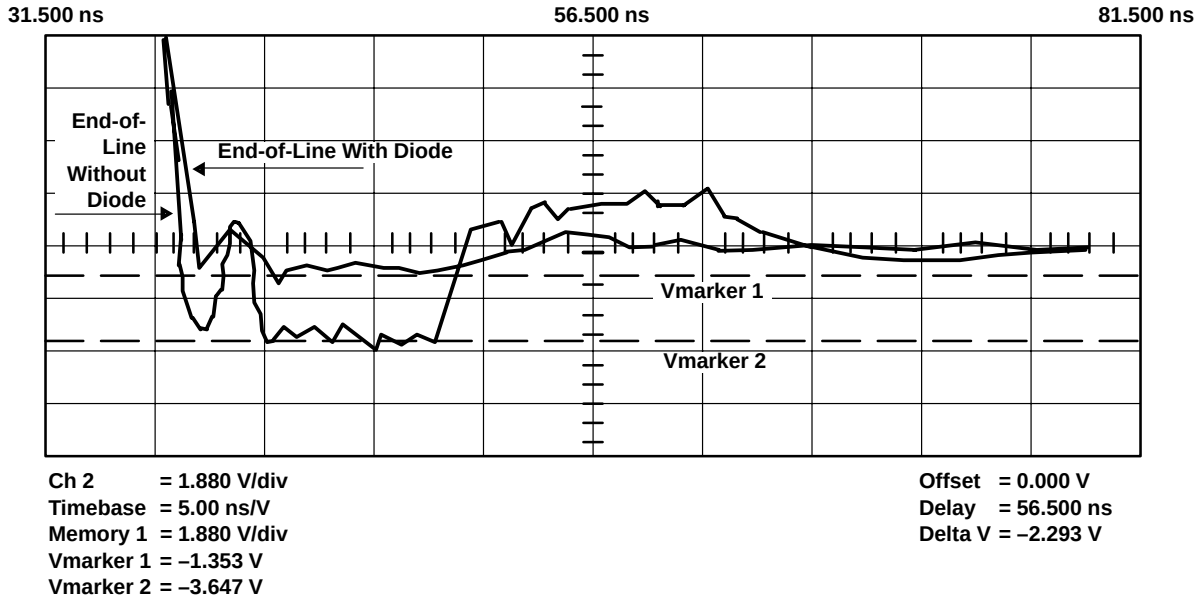


Figure 6. Reduction of Negative Transients at the End of a Transmission Line

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74S1051D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	S1051
SN74S1051DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051
SN74S1051DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051
SN74S1051N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S1051N
SN74S1051N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S1051N
SN74S1051NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74S1051
SN74S1051NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74S1051
SN74S1051PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	S1051
SN74S1051PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051
SN74S1051PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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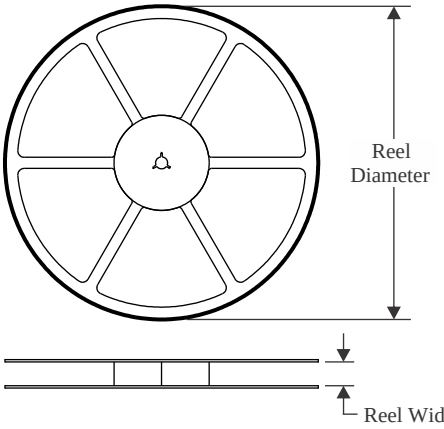
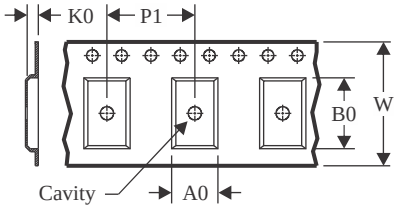
TAPE AND REEL INFORMATION

REEL DIMENSIONS

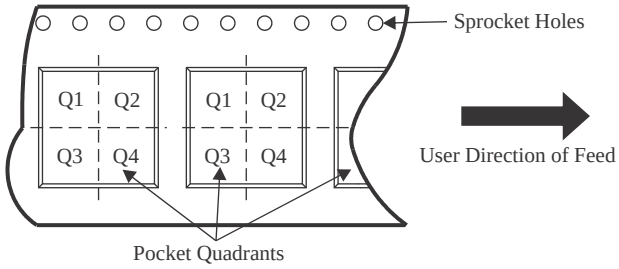


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

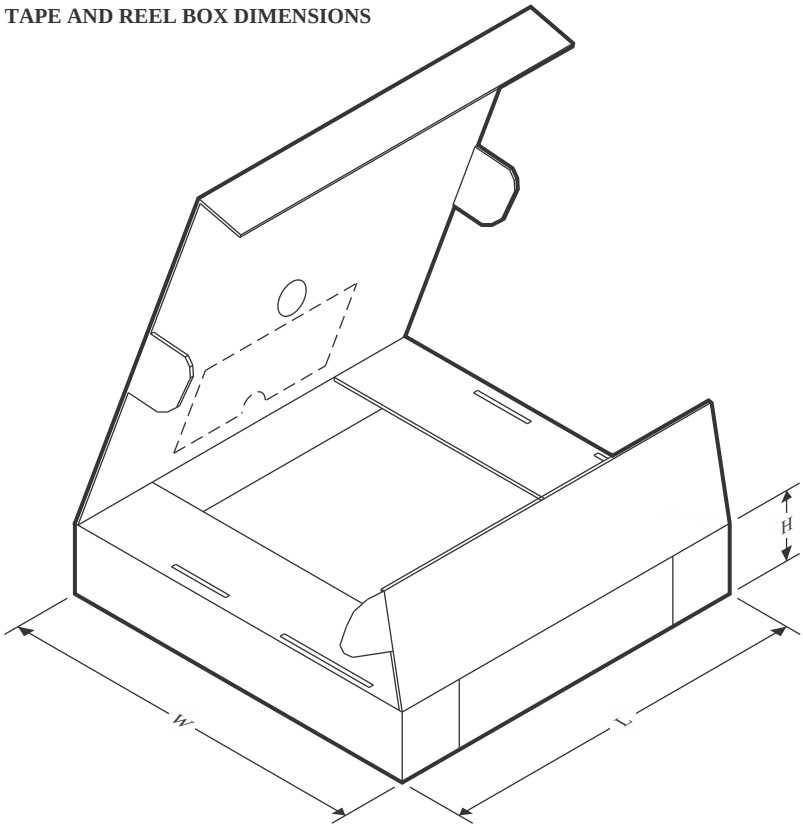
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74S1051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74S1051NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74S1051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

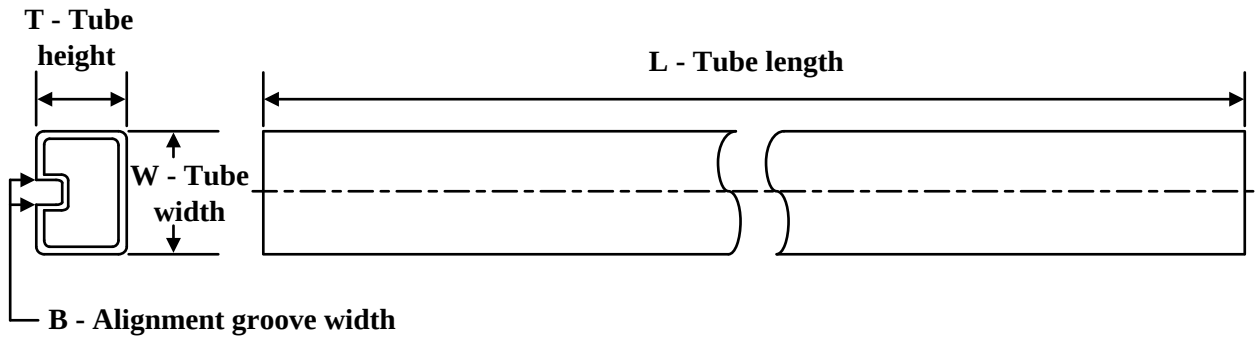
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

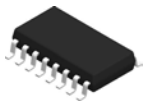
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74S1051DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74S1051NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74S1051PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74S1051N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S1051N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S1051N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74S1051N.A	N	PDIP	16	25	506	13.97	11230	4.32

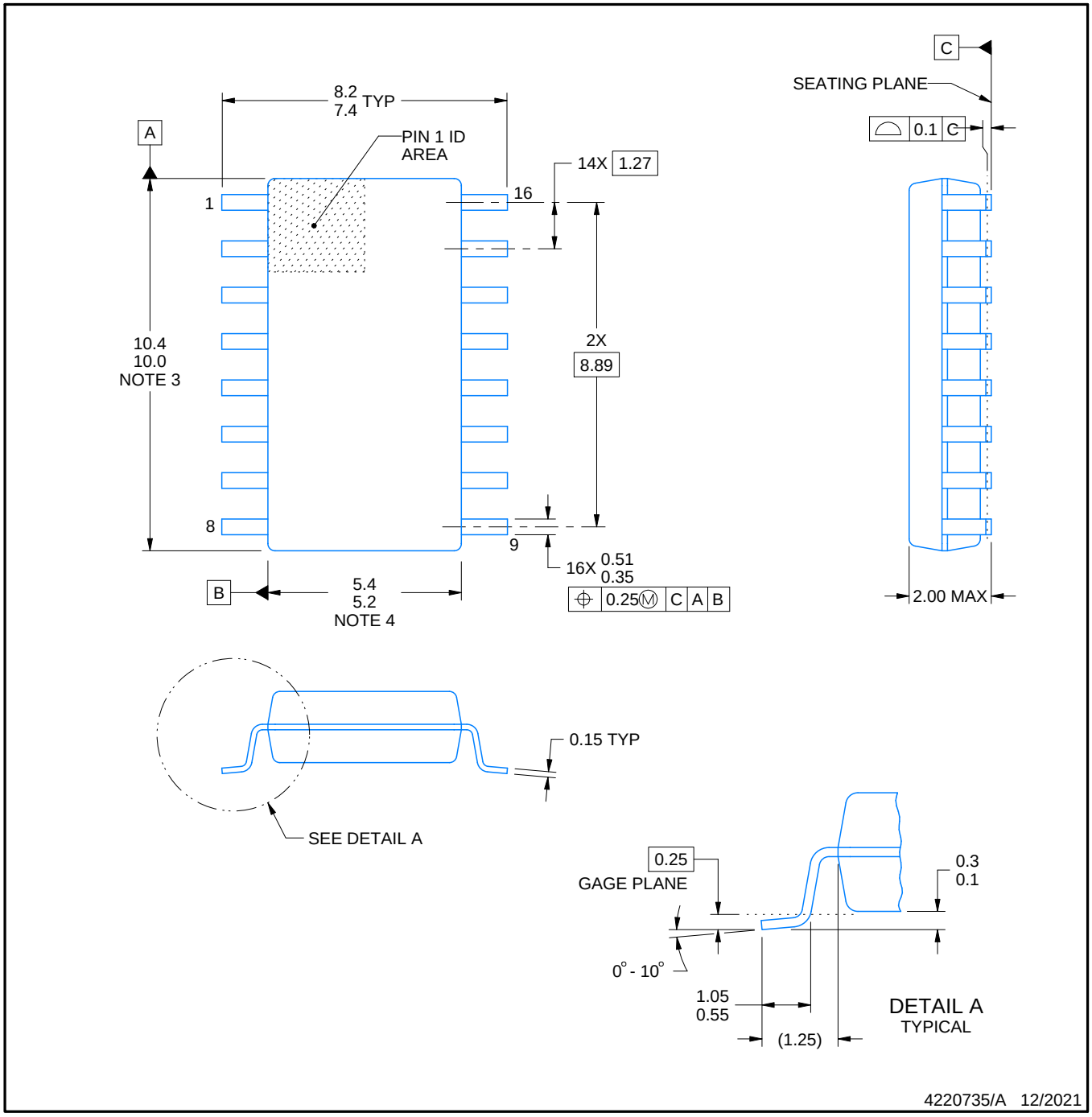


PACKAGE OUTLINE

NS0016A

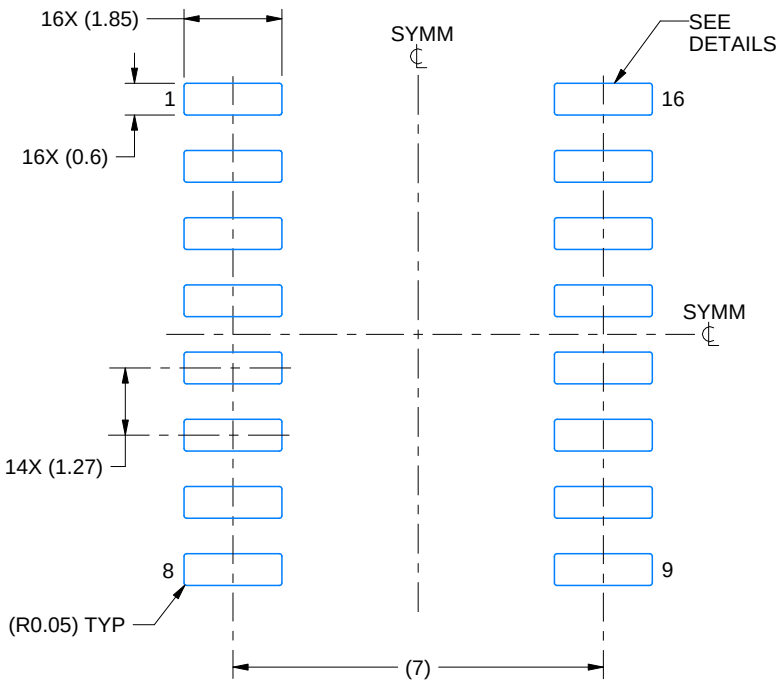
SOP - 2.00 mm max height

SOP

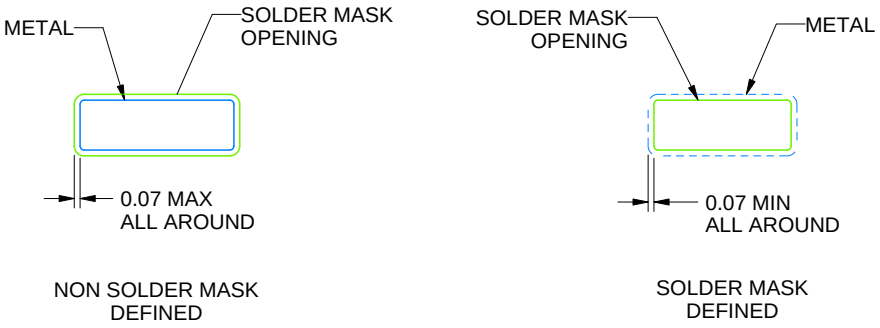


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

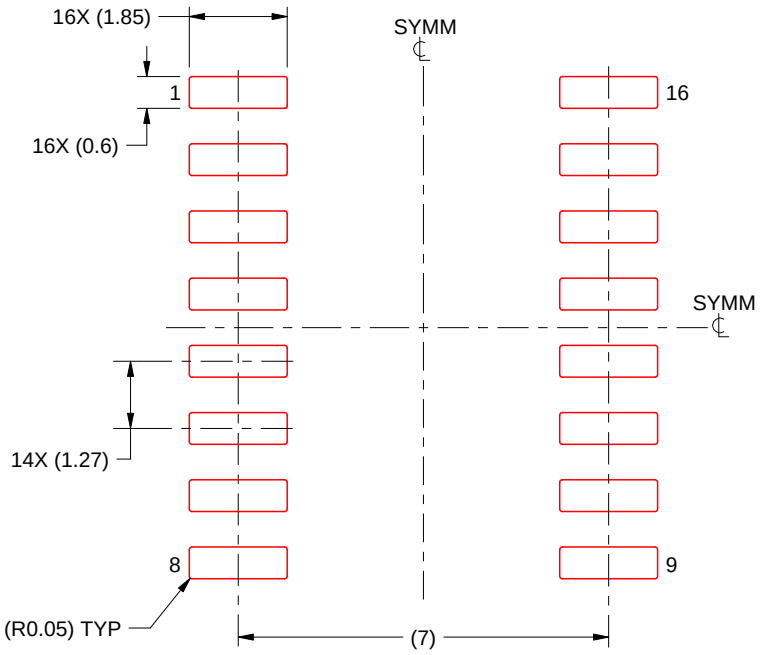
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



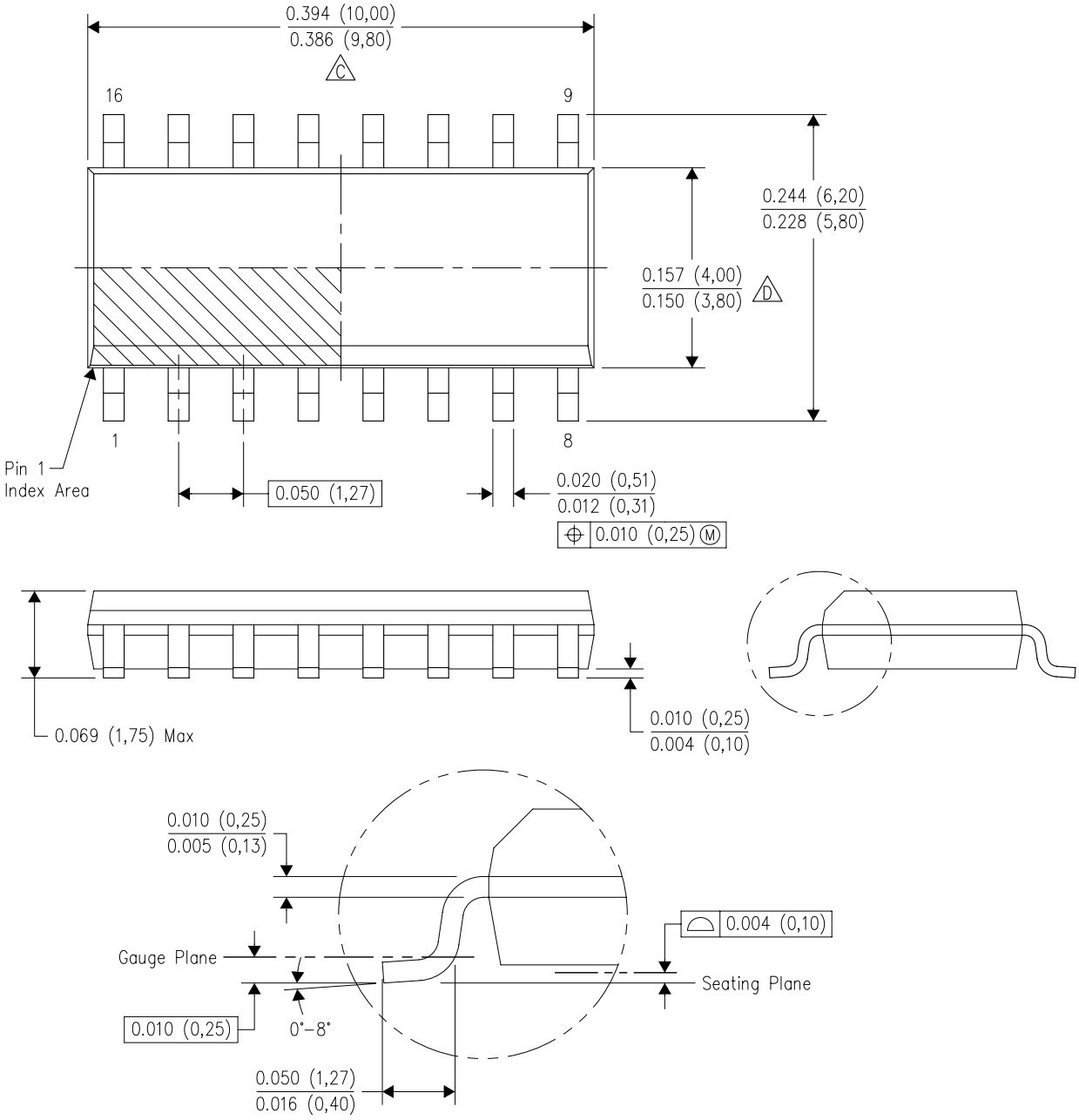
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



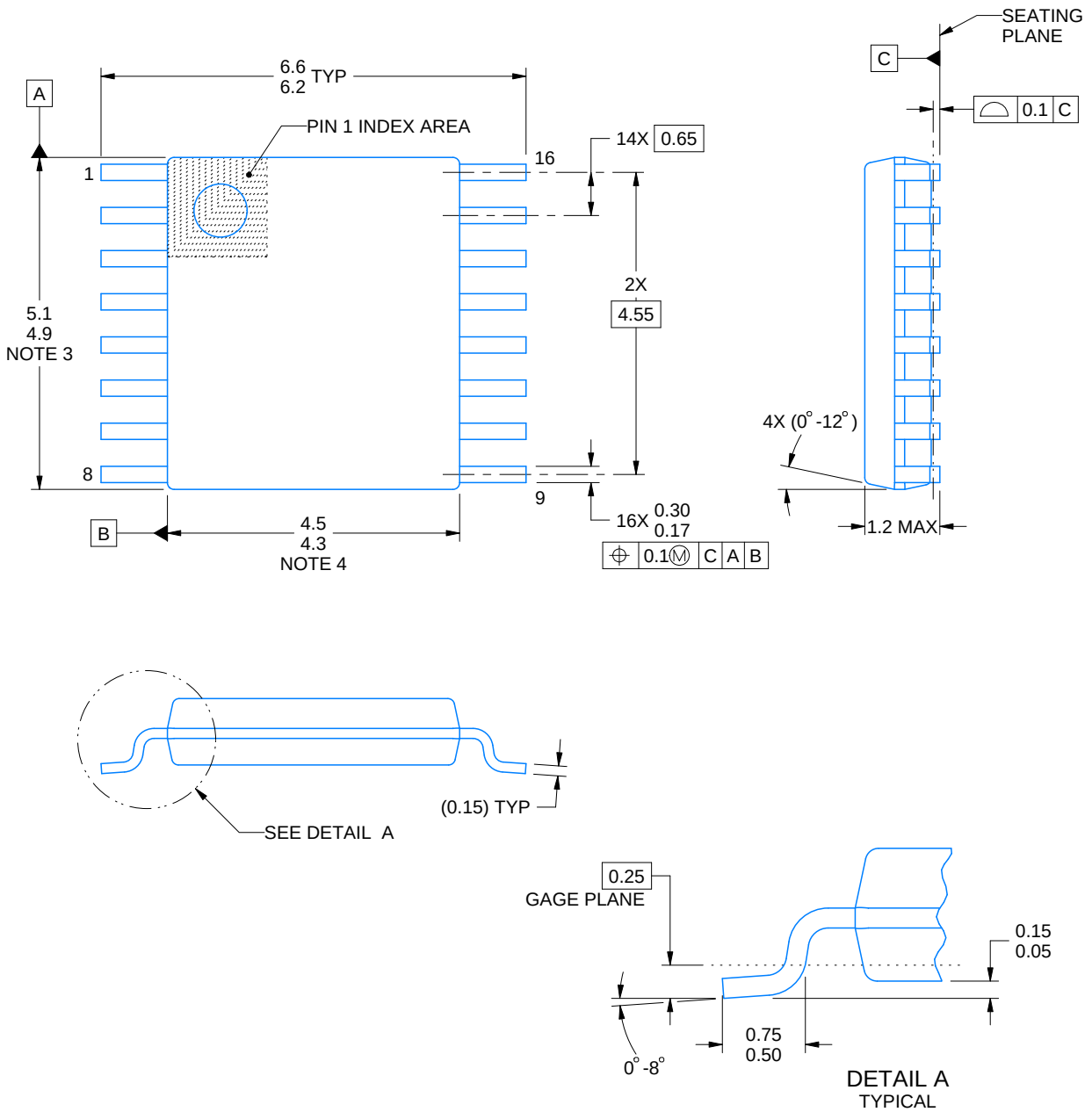
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

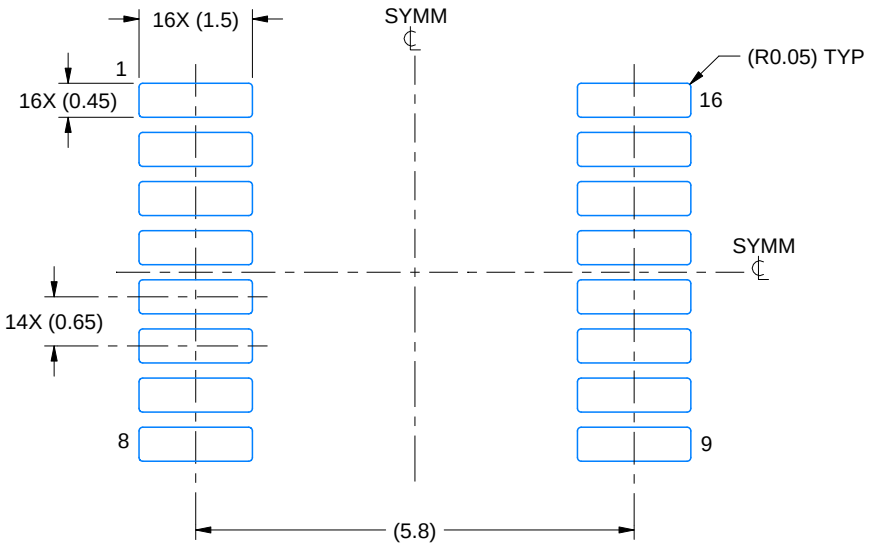
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



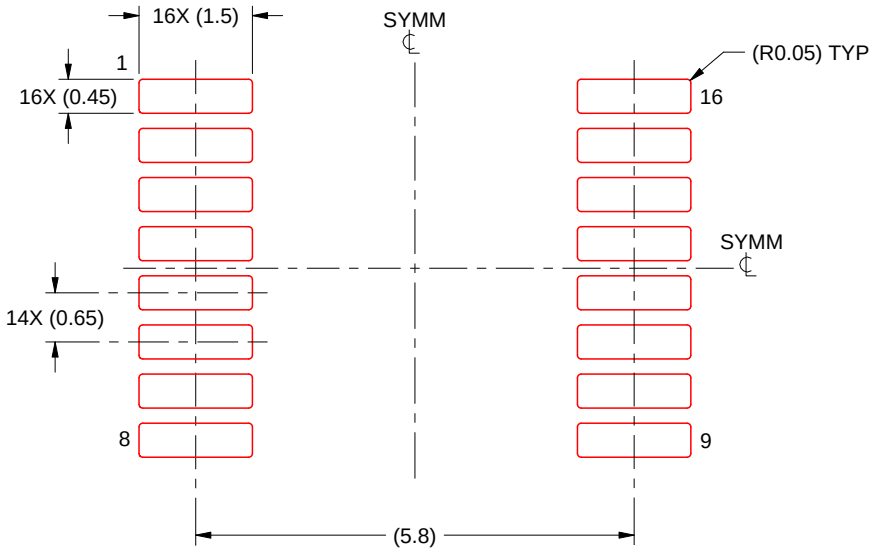
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

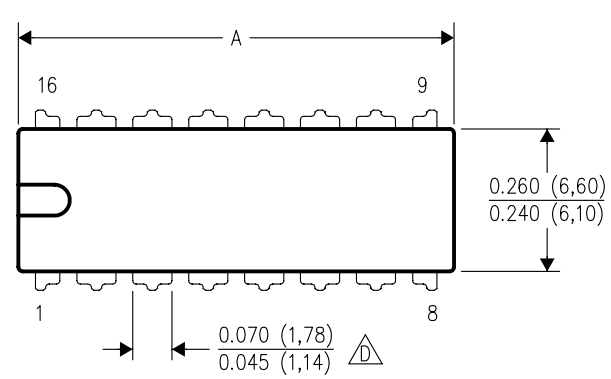
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

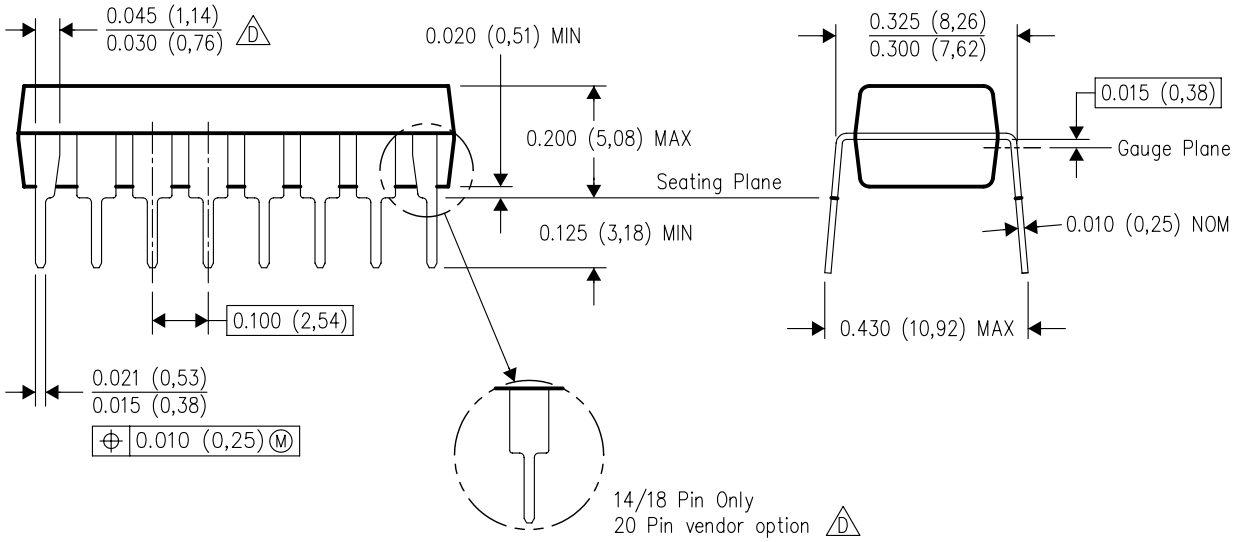
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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