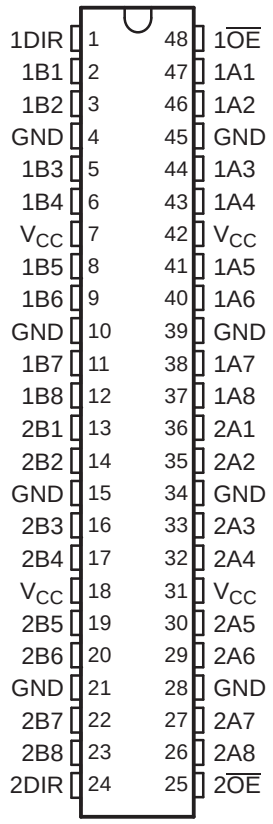
SN54LVT162245A, SN74LVT162245A
3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D – FEBRUARY 2000 – REVISED NOVEMBER 2006

FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Supprt Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LVT162245A . . . WD PACKAGE
SN74LVT162245A . . . DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVT162245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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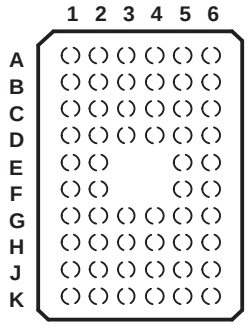
ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT162245AGRDR	LZ245A
	FBGA – ZRD (Pb-free)		SN74LVT162245AZRDR	
	SSOP – DL	Tube of 25	SN74LVT162245ADL	LVT162245A
			SN74LVT162245ADLG4	
		Reel of 1000	SN74LVT162245ADLR	
			74LVT162245ADLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT162245ADGGR	LVT162245A
			74LVT162245ADGGRE4	
	VFBGA – GQL	Reel of 1000	SN74LVT162245AGQLR	LZ245A
	VFBGA – ZQL (Pb-free)		SN74LVT162245AZQLR	
–55°C to 125°C	CFP – WD	Tube	SNJ54LVT162245AWD(2)	SNJ54LVT162245AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) Product preview

GQL OR ZQL PACKAGE
(TOP VIEW)

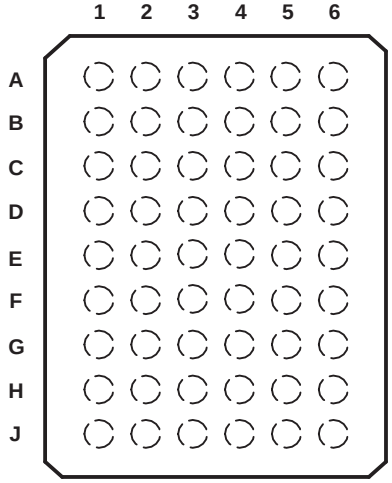


TERMINAL ASSIGNMENTS(1)
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS(1)
(54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
A	1B1	NC	1DIR	$1\overline{OE}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V_{CC}	V_{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V_{CC}	V_{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	$2\overline{OE}$	NC	2A8

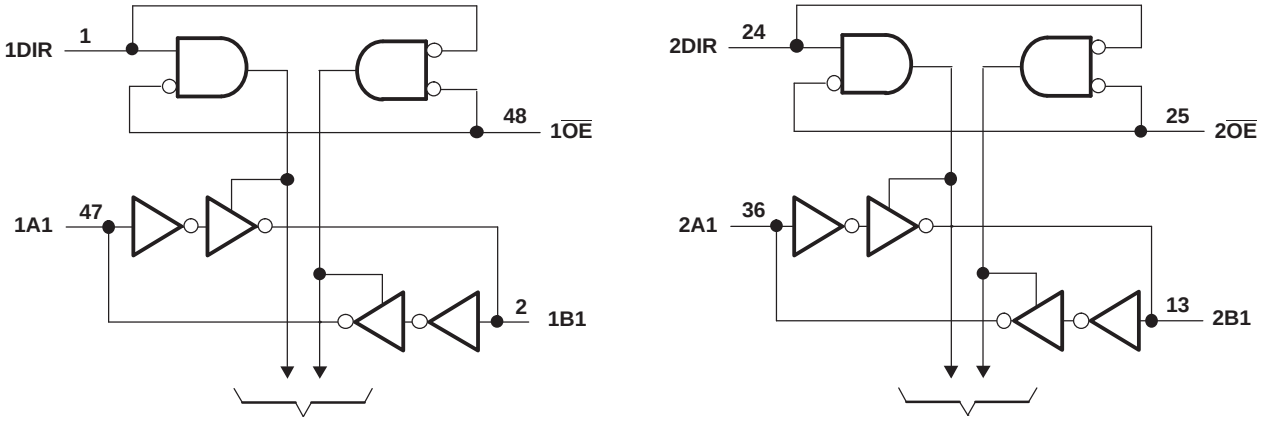
(1) NC – No internal connection

FUNCTION TABLE(1)
(EACH 8-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high state(2)		–0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state	SN54LVT162245A (B port)		96	mA
		SN74LVT162245A (B port)		128	
		A port		30	
I_O	Current into any output in the high state(3)	SN54LVT162245A (B port)		48	mA
		SN74LVT162245A (B port)		64	
		A port		30	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
θ_{JA}	Package thermal impedance(4)	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
		GRD/ZRD package		36	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			SN54LVT162245A(2)		SN74LVT162245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port		–12		–12	mA
		B port		–24		–32	
I_{OL}	Low-level output current	A port		12		12	mA
		B port		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

(1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Product preview

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVT162245A(1)			SN54LVT162245A			UNIT
				MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V_{CC} – 0.2			V
		V_{CC} = 3 V,	I_{OH} = –12 mA	2			2			
	B port	V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V_{CC} – 0.2			
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}	A port	V_{CC} = 2.7 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V,	I_{OL} = 12 mA			0.8			0.8	
	B port	V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B port(3)	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			5			5	
			V_I = 0			–10			–10	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100(4)			±100	µA
I_{OZPD}		V_{CC} = 1.5 to 0 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100(4)			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}(5)		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.3			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF
C_{io}		V_O = 3 V or 0			10			10		pF

(1) Product preview
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(3) Unused pins at V_{CC} or GND
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

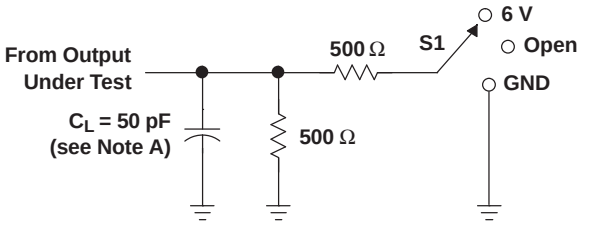
Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162245A(1)				SN74LVT162245A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP(2)	MAX	MIN	MAX	
t_{PLH}	A	B	1	3.5		4	1	2.3	3.3		3.7	ns
t_{PHL}			1	3.5		3.9	1	2.2	3.3		3.5	
t_{PLH}	B	A	1	4.3		5.3	1	2.8	4		4.6	ns
t_{PHL}			1	4.2		4.5	1	2.5	3.4		3.6	
t_{PZH}	$\overline{OE}$	B	1	4.8		5.9	1	2.8	4.6		5.4	ns
t_{PZL}			1	4.8		5.5	1	3	4.6		5.2	
t_{PZH}	$\overline{OE}$	A	1	5.5		7.2	1	3.3	5.3		6.3	ns
t_{PZL}			1	5.4		6.4	1	3.3	5.1		5.8	
t_{PHZ}	$\overline{OE}$	B	1.5	5.5		5.8	1.5	3.8	5.2		5.5	ns
t_{PLZ}			1.5	5.5		5.8	1.5	3.5	5.1		5.4	
t_{PHZ}	$\overline{OE}$	A	1.5	5.8		6.5	1.5	4	5.6		5.9	ns
t_{PLZ}			1.2	6.3		6.3	1.5	3.8	5.5		5.5	
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

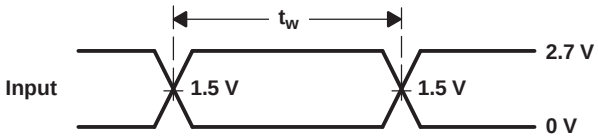
(1) Product preview
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

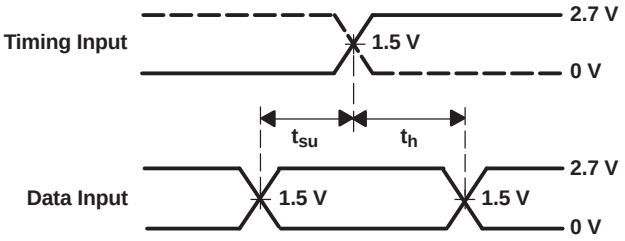


LOAD CIRCUIT

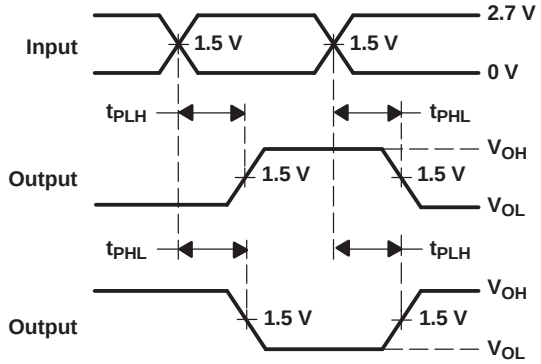
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



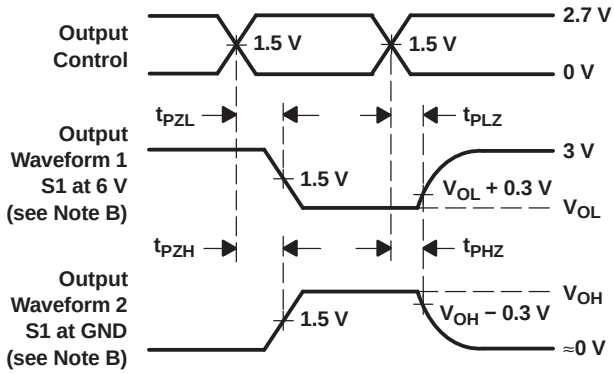
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVT162245ADGGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
74LVT162245ADGGRG4.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
74LVT162245ADLRG4	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
74LVT162245ADLRG4.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADGGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADL.B	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A
SN74LVT162245ADLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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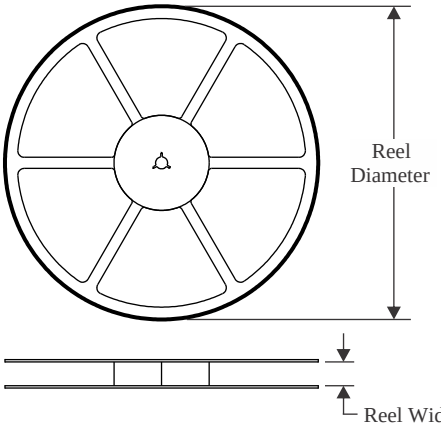
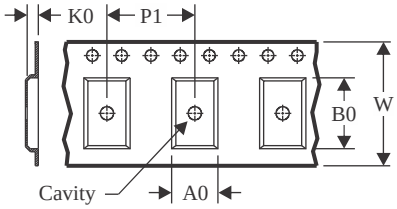
TAPE AND REEL INFORMATION

REEL DIMENSIONS

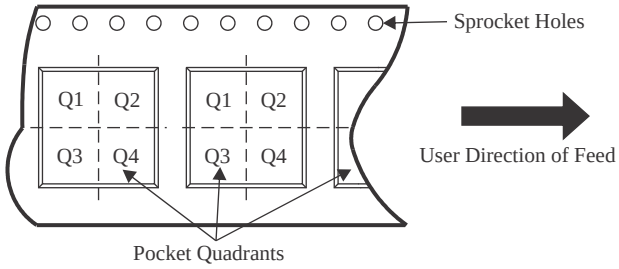


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

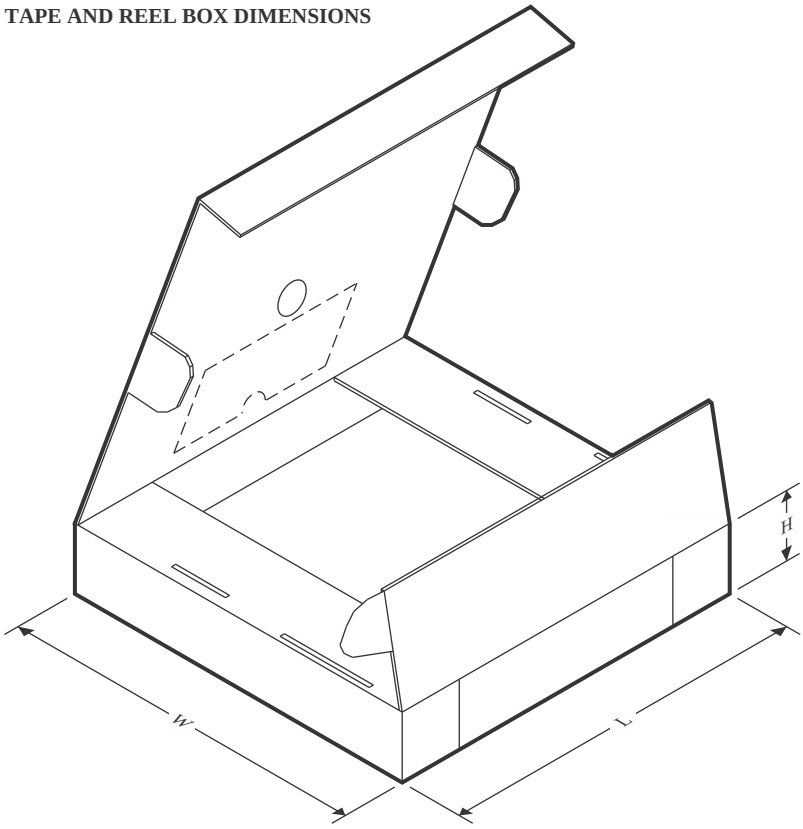
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVT162245ADGGRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74LVT162245ADLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVT162245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

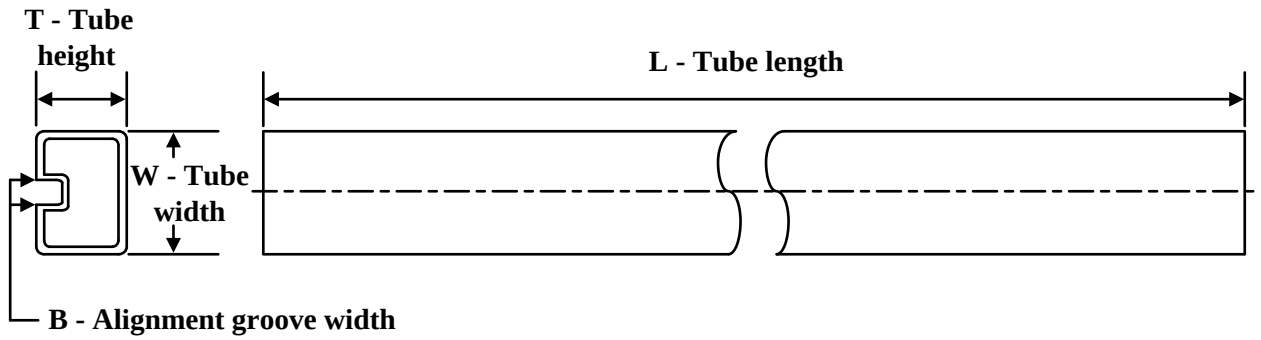
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVT162245ADGGRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
74LVT162245ADLRG4	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVT162245ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

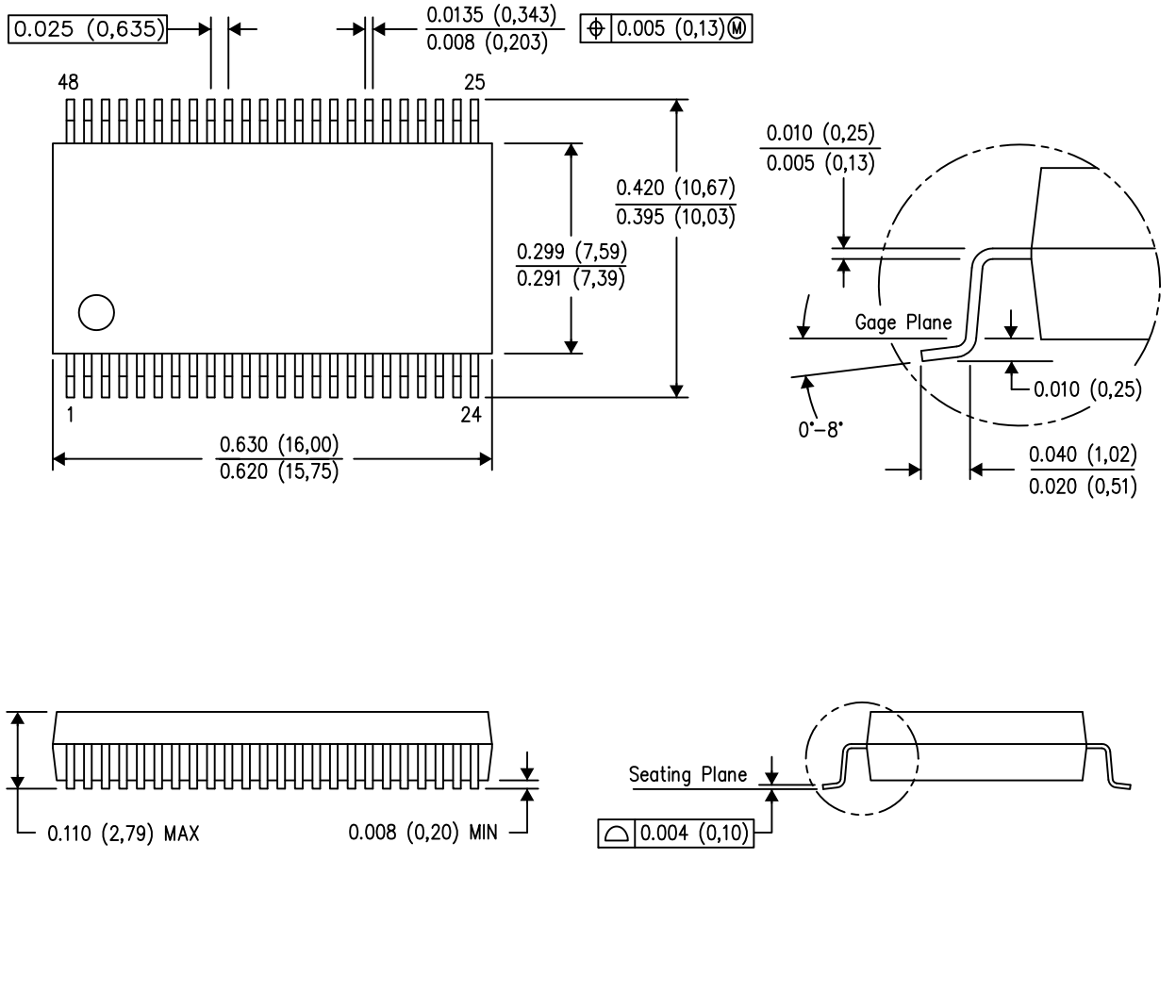
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVT162245ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVT162245ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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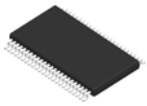
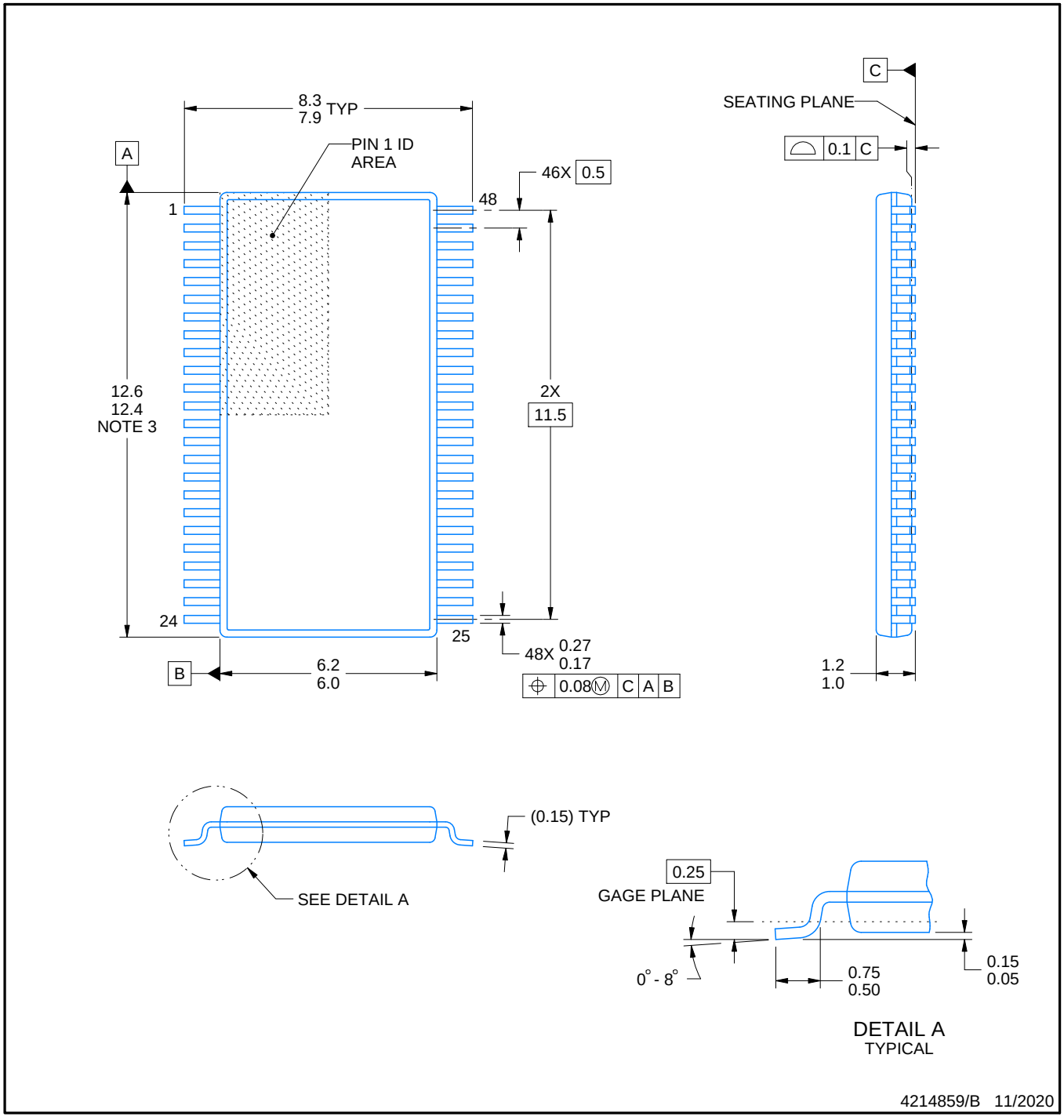


PACKAGE OUTLINE

DGG0048A

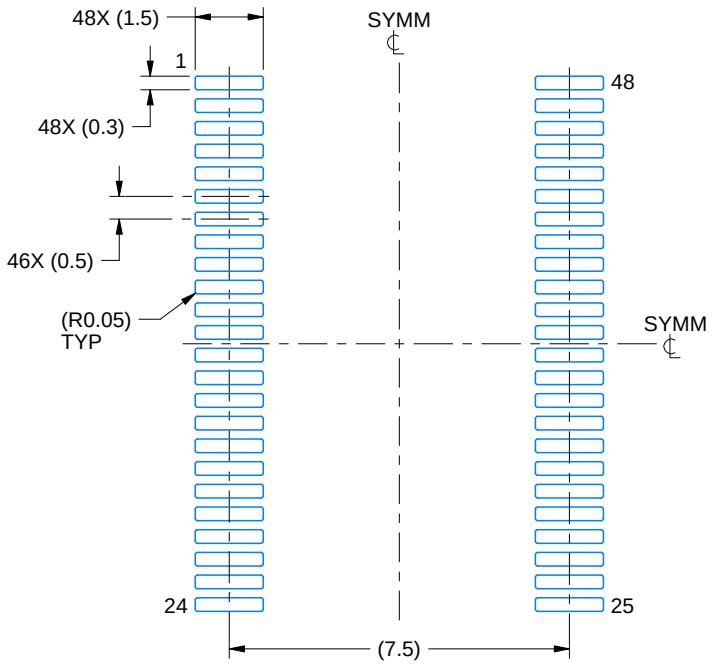
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

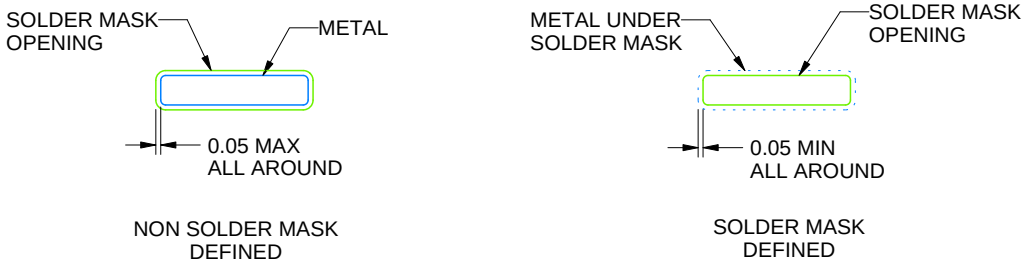


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

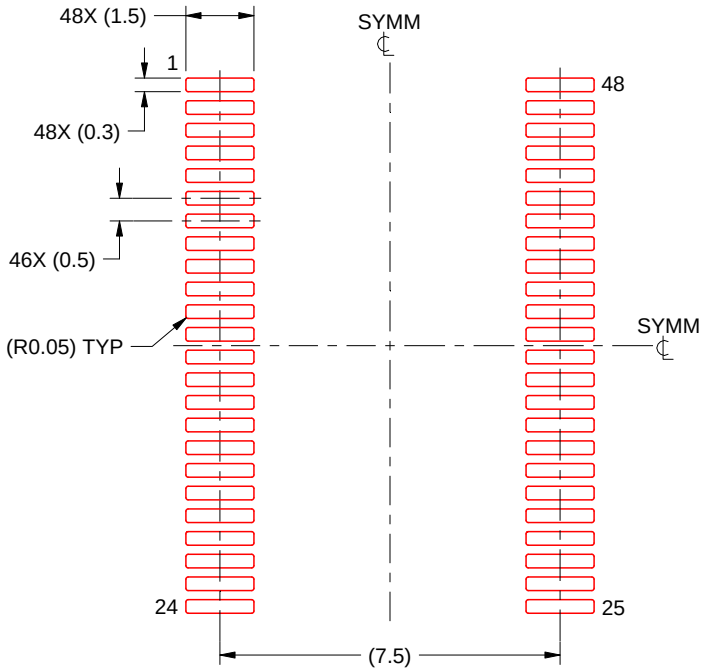


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

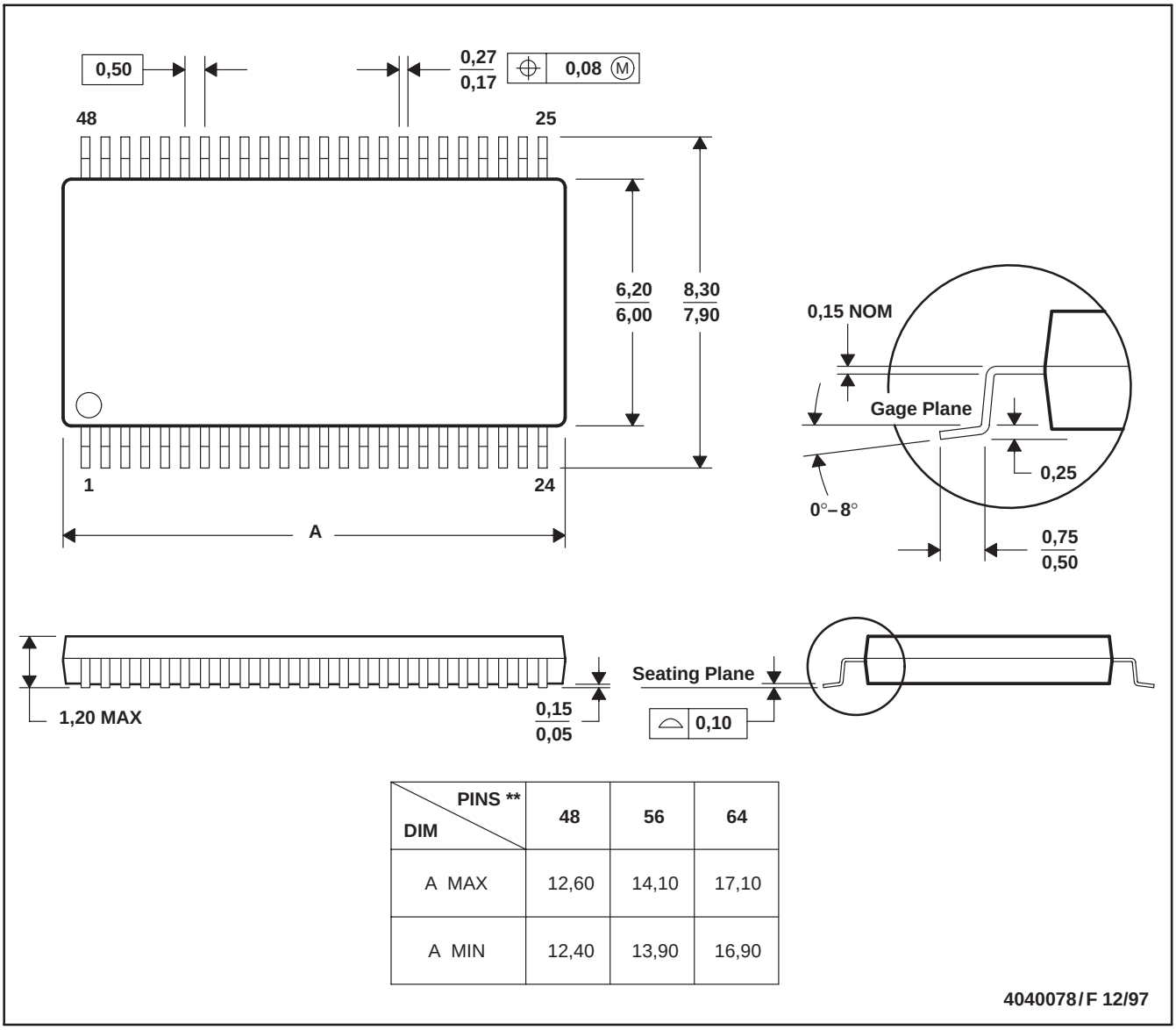
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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