SN74LVC1G34 单路缓冲门

1 特性

- 采用具有 0.5mm 间距的超小型 0.64mm^2 封装 (DPW)
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V
- 支持向下转换到 V_{CC}
- 3.3V 时 t_{pd} 最大值为 3.5ns
- 低功耗，I_{CC} 最大值为 1 µ A
- 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114A)
  - 200V 机器放电模型 (A115A)
  - 1000V 充电器件模型 (C101)

2 应用

- AV 接收器
- 音频接口盒：便携式
- 蓝光播放器与家庭影院
- DVD 录像机和播放器
- 嵌入式 PC
- MP3 播放器/录音机（便携式音频设备）
- 个人数字助理 (PDA)
- 电源：电信/服务器交流/直流电源：单路控制器：模拟式和数字式
- 固态硬盘 (SSD)：客户端和企业级
- 电视：LCD 电视/数字电视和高清电视 (HDTV)
- 平板电脑：企业级
- 视频分析：服务器
- 无线耳机、键盘和鼠标

3 说明

该单路缓冲门设计在 1.65V 至 5.5V V_{CC} 下运行。

SN74LVC1G34 器件以正逻辑执行布尔函数 Y = A。

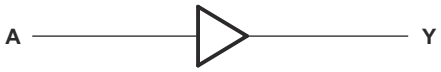
CMOS 器件具有高输出驱动，同时在宽 V_{CC} 工作范围内保持低静态功率耗散。

SN74LVC1G34 器件采用多种封装，包括封装尺寸为 0.8mm × 0.8mm 的超小型 DPW 封装。

封装信息

器件名称	封装 (1)	封装尺寸(2)	本体尺寸（标称值）(3)
SN74LVC1G34	YFP（DSBGA，4）	1.00mm × 1.00mm	0.76mm × 0.76mm
	YZP（DSBGA，5）	1.75mm × 1.25mm	1.38mm × 0.88mm
	YZV（DSBGA，4）	1.25mm × 1.25mm	0.88mm × 0.88mm
	DPW（X2SON，5）	0.80mm × 0.80mm	0.80mm × 0.80mm
	DBV（SOT-23，5）	2.90mm × 2.80mm	2.90mm × 2.80mm
	DCK（SC70，5）	2.00mm × 2.10mm	2.00mm × 2.10mm
	DRL（SOT，5）	1.60mm × 1.60mm	1.60mm × 1.60mm
	DRY（USON，6）	1.45mm × 1.00mm	1.45mm × 1.00mm
	DSF（X2SON，6）	1.00mm × 1.00mm	1.00mm × 1.00mm

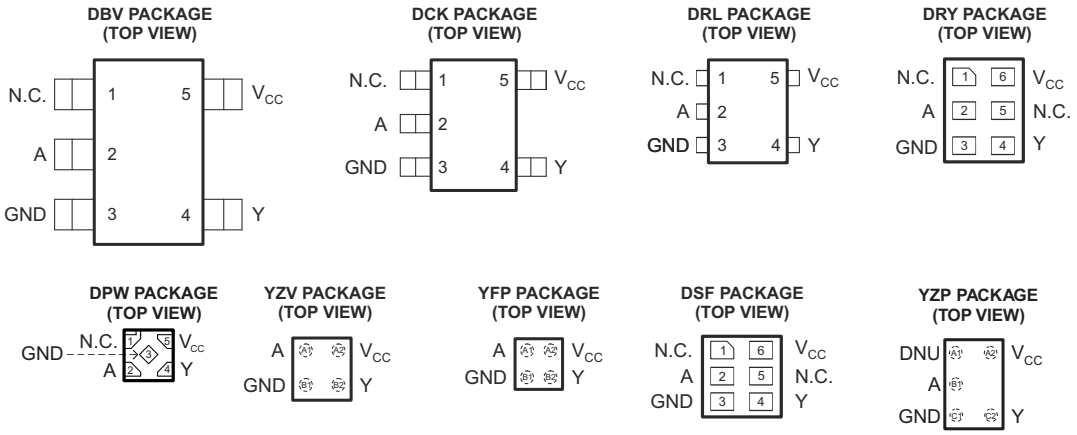
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。



简化版原理图

内容

4 引脚配置和功能



See mechanical drawings for dimensions.
N.C. – No internal connection
DNU – Do not use

表 4-1. 引脚功能

引脚						说明
名称	DRL、DCK、DBV	DPW	DRY、DSF	YZP	YFP、YZV	
NC	1	1	1、5	A1	–	未连接
A	2	2	2	B1	A1	输入
GND	3	3	3	C1	B1	接地
Y	4	4	4	C2	B2	输出
V_{CC}	5	5	6	A2	A2	电源引脚

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）

(1)			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	6.5	V
V_I	输入电压范围		-0.5	6.5	V
V_O	在高阻抗或断电状态对任一输出施加的电压范围(2)		-0.5	6.5	V
V_O	应用到任一处于高电平或低电平状态输出的电压范围(2) (3)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-50	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
T_{stg}	贮存温度范围		-65	150	°C
T_J	最大结温			150	°C

(1) 超出*绝对最大额定值*范围操作可能会导致器件永久损坏。*绝对最大额定值*并不表示器件在这些条件下或在*建议的工作条件*以外的任何其他条件下能够正常运行。如果超出*建议运行条件*但在*绝对最大额定值*范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*建议运行条件*表中提供。

5.2 ESD 等级

			最小值	最大值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)		±2	kV
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)		±1	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

(1)			最小值	最大值	单位
V_{CC}	电源电压	工作	1.65	5.5	V
		仅数据保留	1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	1.7		
		V_{CC} = 3V 至 3.6V	2		
		V_{CC} = 4.5V 至 5.5V	0.7 × V_{CC}		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V		0.7	
		V_{CC} = 3V 至 3.6V		0.8	
		V_{CC} = 4.5V 至 5.5V		0.3 × V_{CC}	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 3V		-16	
				-24	
		V_{CC} = 4.5V		-32	
I_{OL}	低电平输出电流	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
$\Delta t/\Delta v$	输入转换上升或下降速率	V_{CC} = 1.8V ± 0.15V，2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		10	
T_A	自然通风条件下的工作温度	DSBGA 封装	-40	85	°C
		所有其他封装	-40	125	°C

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND，以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢或悬空的影响*，文献编号 SCBA004。

5.4 热性能信息

热指标(1)		SN74LVC1G34						单位
		DBV	DCK	DRL	DRY	YZP	DPW	
		5 引脚	5 引脚	5 引脚	6 引脚	5 引脚	4 引脚	
$R_{\theta JA}$	结至环境热阻	357.1	371.0	243	439	130	340	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	263.7	297.5	78	277	54	215	
$R_{\theta JB}$	结至电路板热阻	264.4	258.6	78	271	51	294	
ψ_{JT}	结至顶部特征参数	195.6	195.6	10	84	1	41	
ψ_{JB}	结至电路板特征参数	262.2	256.2	77	271	50	294	
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	-	-	-	-	-	250	

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	-40°C 至 85°C			-40°C 至 125°C			单位
			最小值	典型值(1)	最大值	最小值	典型值(1)	最大值	
V_{OH}	I_{OH} = –100 μA	1.65V 至 5.5V	V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = -4mA	1.65V	1.2			1.2			
	I_{OH} = -8mA	2.3V	1.9			1.9			
	I_{OH} = -16mA	3V	2.4			2.4			
	I_{OH} = -24mA		2.3			2.3			
	I_{OH} = -32mA	4.5V	3.8			3.8			
V_{OL}	I_{OL} = 100 μA	1.65V 至 5.5V			0.1			0.1	V
	I_{OL} = 4mA	1.65V			0.45			0.45	
	I_{OL} = 8mA	2.3V			0.3			0.3	
	I_{OL} = 16mA	3V			0.4			0.4	
	I_{OL} = 24mA				0.55			0.55	
	I_{OL} = 32mA	4.5V			0.55			0.55	
I_I	V_I = 5.5 V 或 GND	0 至 5.5V			±1			±2	μA
I_{off}	V_I 或 V_O = 5.5V	0			±10			±10	μA
I_{CC}	V_I = 5.5V 或 GND， I_O = 0	1.65V 至 5.5V			1			10	μA
ΔI_{CC}	一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_{CC} 或 GND	3V 至 5.5V			500			500	μA
C_i	V_I = V_{CC} 或 GND	3.3V		3.5					pF

(1) 所有典型值均在 V_{CC} = 3.3V、T_A = 25°C 下测得。

5.6 开关特性，C_L = 15pF

在自然通风条件下的建议工作温度范围内测得，C_L = 15pF（除非另有说明）（请参阅图 6-1）

参数	从（输入）	至（输出）	-40°C 至 85°C								单位
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	2	9.9	1.5	6	1	3.5	1	2.9	ns

5.7 开关特性，–40°C 至 85°C

在自然通风条件下的建议工作温度范围内测得，C_L = 30pF 或 50pF（除非另有说明）（请参阅图 6-2）

参数	从（输入）	至（输出）	-40°C 至 85°C								单位
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	3.2	8.6	1.5	4.4	1.5	4.1	1	3.2	ns

5.8 开关特性，–40°C 至 125°C

在自然通风条件下的建议工作温度范围内测得，C_L = 30pF 或 50pF（除非另有说明）（请参阅图 6-2）

参数	从（输入）	至（输出）	-40°C 至 125°C								单位
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	3.2	9.5	1.5	5.1	1.5	4.7	1	3.9	ns

5.9 工作特性

T_A = 25°C

参数	测试条件	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	单位
		典型值	典型值	典型值	典型值	
C_{pd} 功率耗散电容	f = 10MHz	16	16	16	18	pF

5.10 典型特性

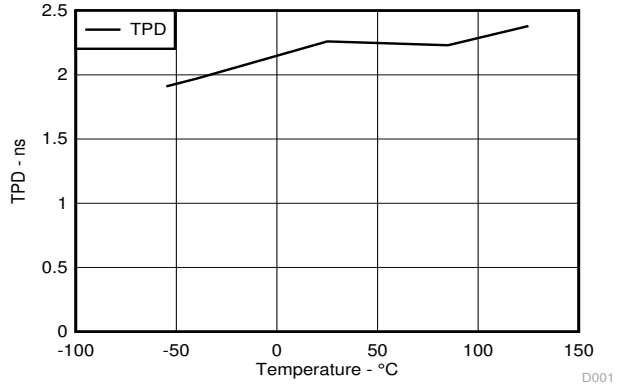


图 5-1. 在 3.3V VCC 电压下的 TPD 随温度变化情况

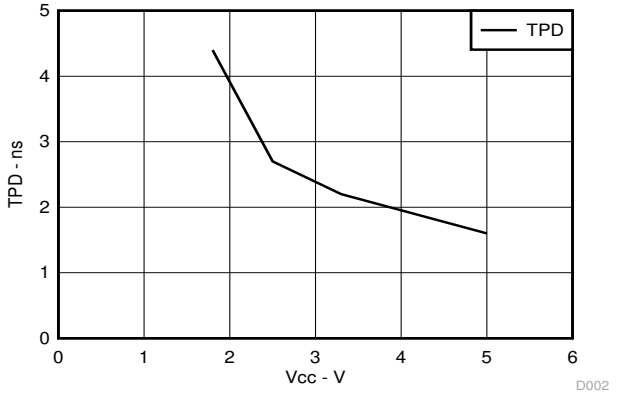
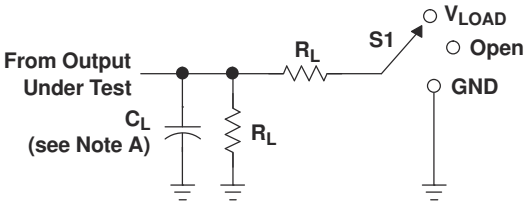


图 5-2. 在 25°C 下 TPD 随温度的变化

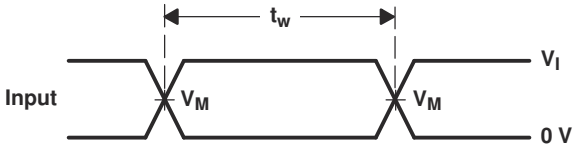
6 参数测量信息



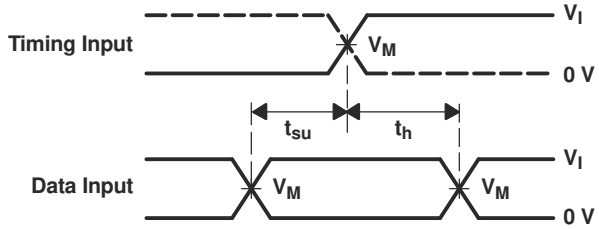
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

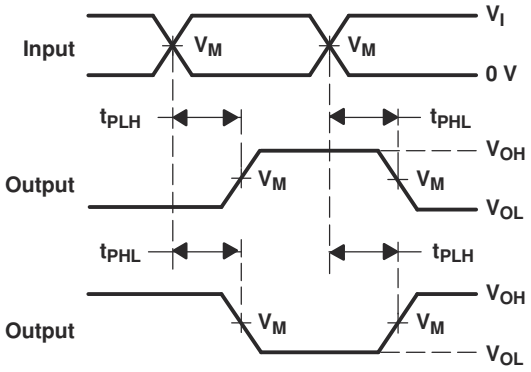
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V



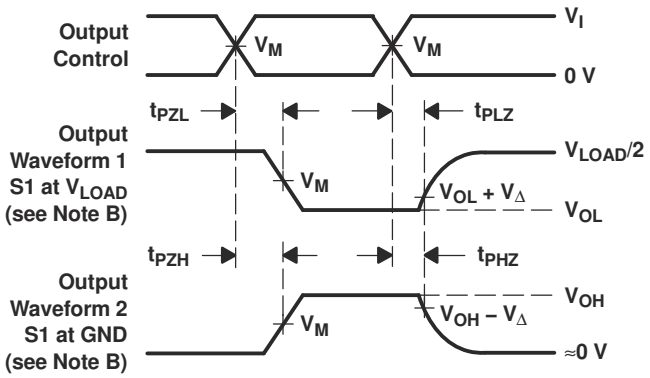
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



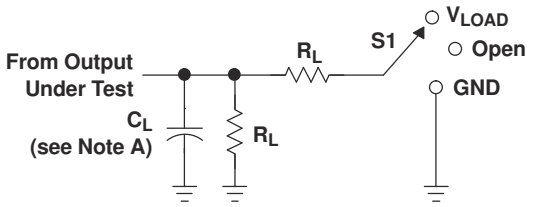
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

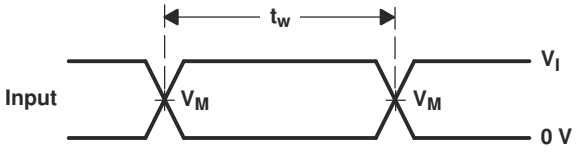
图 6-1. 负载电路和电压波形



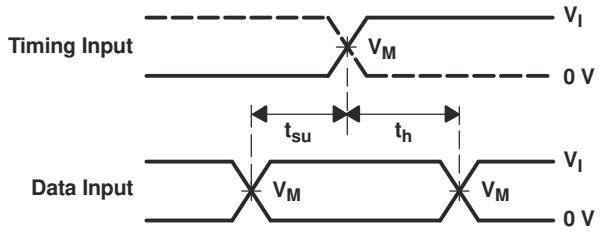
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

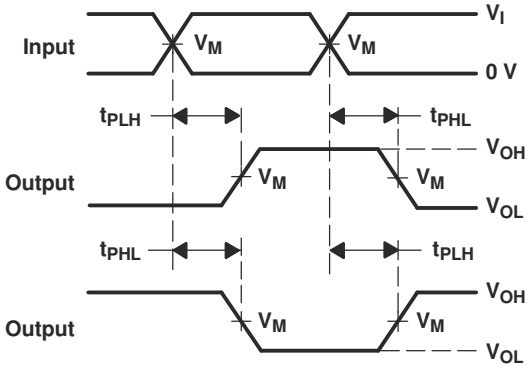
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



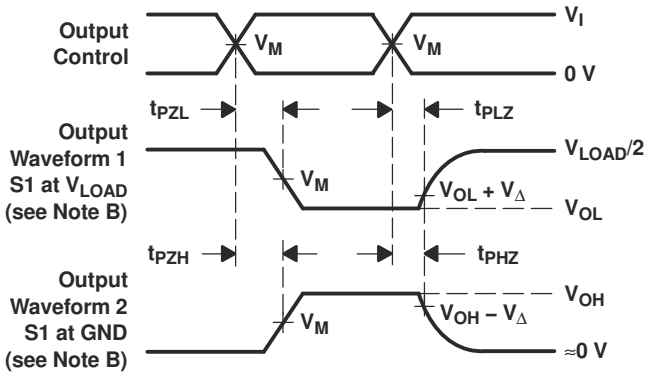
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

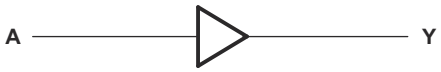
图 6-2. 负载电路和电压波形

7 详细说明

7.1 概述

SN74LVC1G34 器件包含一个缓存门器件并执行布尔函数 Y = A。该器件完全适用于使用 I_{off} 的局部关断应用。I_{off} 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。

7.2 功能方框图



7.3 特性说明

7.4 器件功能模式

功能表

输入 A	输出 Y
H	H
L	L

8 应用和实施

备注

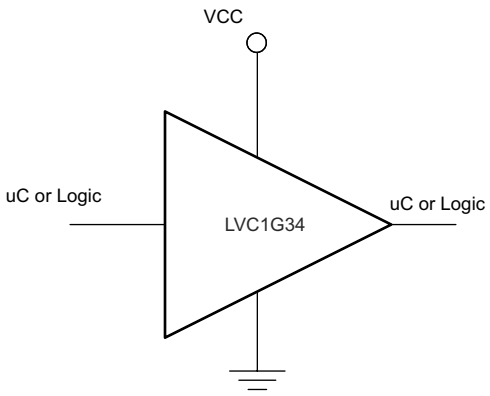
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

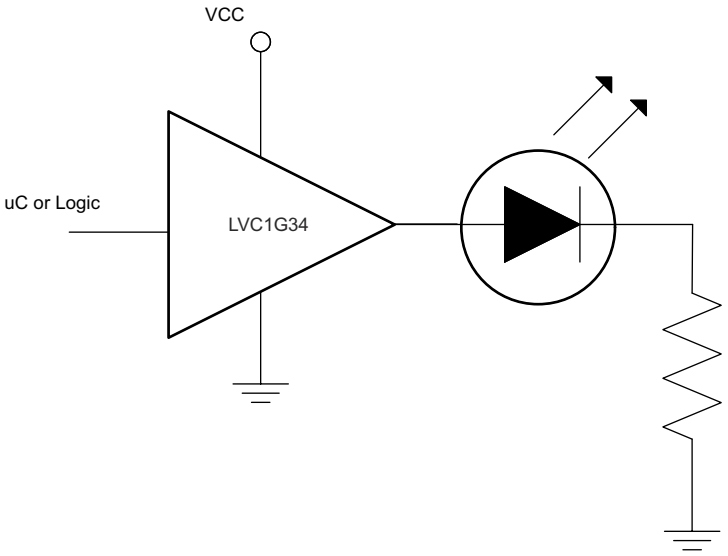
SN74LVC1G34 是一款高驱动 CMOS 器件，可以用作驱动 LED 的缓冲器。它可以在 3.3V 下产生 24mA 驱动电流，因此非常适合驱动多个输出，也适合用于高达 100MHz 的高速应用。

8.2 典型应用

Buffer Function



Basic LED Driver



8.2.1 设计要求

8.2.1.1 电源注意事项

确保所需电源电压在 *电气特性* 中规定的范围内。电源电压决定器件的电气特性，如 *电气特性* 部分所述。

正电压电源必须能够提供的电流等于 最大静态电源电流 I_{CC}（在 *电气特性* 中列出）以及开关所需的任何瞬态电流之和。

地必须能够灌入的电流等于 SN74LVC1G34 所有输出端灌入的总电流加上最大电源电流 I_{CC}（在 *电气特性* 中列出）以及开关所需的任何瞬态电流之和。逻辑器件只能灌入其所接的地可灌入的大小相同的电流。确保不要超过 *绝对最大额定值* 中列出的通过 GND 的最大总电流。

SN74LVC1G34 可以驱动总电容小于或等于 50pF 的负载，同时仍满足所有数据表规格。可以施加更大的容性负载；但建议不要超过 50pF。

SN74LVC1G34 可以驱动由 $R_L \geqslant V_O/I_O$ 描述的总电阻负载，输出电压和电流在 *电气特性* 表中用 V_{OL} 定义。在高电平状态下输出时，公式中的输出电压定义为测量的输出电压与 V_{CC} 引脚处的电源电压之间的差值。

总功耗可以使用 *CMOS 功耗与 Cpd 计算*应用手册中提供的信息进行计算。

可以使用*标准线性和逻辑 (SLL) 封装和器件的热特性*应用手册中提供的信息计算热增量。

小心

绝对最大额定值 中列出的最高结温 $T_{J(max)}$ 是防止损坏器件的附加限制。请勿违反*绝对最大额定值* 中列出的任何值。提供这些限制是为了防止损坏器件。

8.2.1.2 输入注意事项

输入信号必须超过 才能被视为逻辑低电平，超过 才能被视为逻辑高电平。不要超过*绝对最大额定值* 中的最大输入电压范围。

未使用的输入必须端接至 V_{CC} 或地。如果输入完全不使用，则可以直接端接未使用的输入，如果有时要使用输入，但并非始终使用，则可以使用上拉或下拉电阻器连接输入。上拉电阻用于默认高电平状态，下拉电阻用于默认低电平状态。控制器的驱动电流、进入 SN74LVC1G34 的漏电流（如 *电气特性* 中所规定）以及所需输入转换率会限制电阻值。由于这些因素，通常使用 10kΩ 的电阻值。

有关此器件的输入的附加信息，请参阅 *特性描述*。

8.2.1.3 输出注意事项

接地电压用于产生低电平输出电压。根据 *电气特性* 中 V_{OL} 规格所示，向输出端灌入电流将提高输出电压。

未使用的输出可以保持悬空状态。不要将输出直接连接到 V_{CC} 或地。

有关此器件的输出的其他信息，请参阅 *特性说明* 部分。

8.2.1.4 详细设计过程

1. 在 V_{CC} 至 GND 之间添加一个去耦电容器。此电容器需要在物理上靠近器件，在电气上靠近 V_{CC} 和 GND 引脚。*布局* 部分中展示了示例布局。
2. 验证输出端的容性负载是否 ≤ 50pF。这不是硬性限制；但是，根据设计，该限制将优化性能。这可以通过从 SN74LVC1G34 向一个或多个接收器件提供适当大小的短布线来实现。
3. 验证输出端的电阻负载是否大于 $(V_{CC} / I_{O(max)})$ Ω。这可防止超出 *绝对最大额定值* 中的最大输出电流。大多数 CMOS 输入具有以 MΩ 为单位的电阻负载；远大于之前计算的最小值。
4. 逻辑门很少关注热问题；然而，可以使用应用手册 *CMOS 功耗与 Cpd 计算* 中提供的步骤计算功耗和热增量。

8.2.2 应用曲线

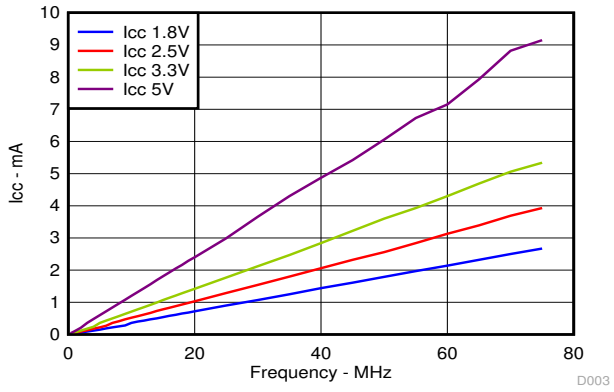


图 8-1. Icc 与频率间的关系

8.3 电源相关建议

电源可以是*建议运行条件*中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。

建议为该器件使用 0.1 µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

8.4 布局

8.4.1 布局指南

- 旁路电容器的放置
  - 靠近器件的正电源端子放置
  - 提供电气短接地返回路径
  - 使用宽布线以最大限度减小阻抗
  - 尽可能将器件、电容器和布线保持在电路板的同一面
- 信号布线几何形状
  - 8mil 至 12mil 布线宽度
  - 布线长度小于 12cm 可最大限度减轻传输线路影响
  - 避免信号布线出现 90° 角
  - 在信号布线下方使用不间断的接地平面
  - 通过接地对信号布线周围的区域进行泛洪填充
  - 并行布线之间必须至少间隔 3 倍电介质厚度
  - 对于长度超过 12cm 的布线
    - 使用阻抗受控的布线
    - 在输出端附近使用串联阻尼电阻进行源端接
    - 避免分支；对必须单独分支的每条信号进行缓冲

8.4.2 布局示例

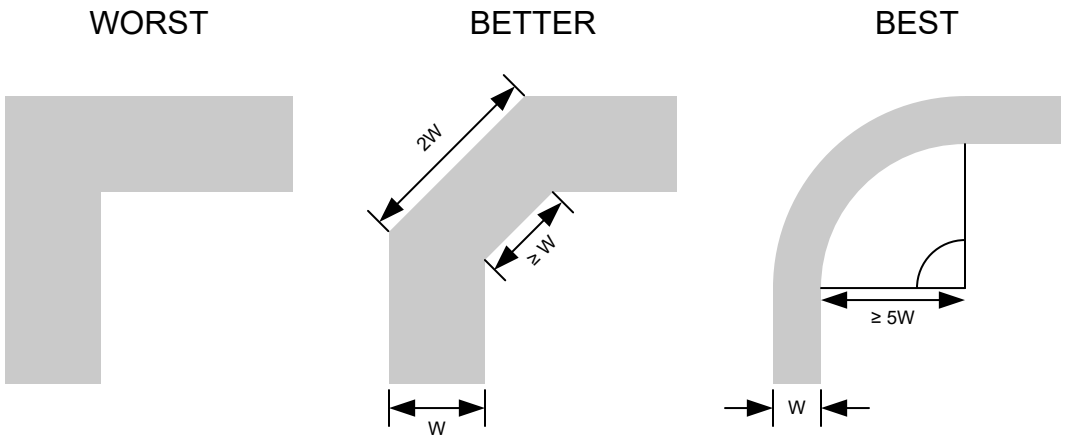


图 8-2. 可改善信号完整性的布线转角示例

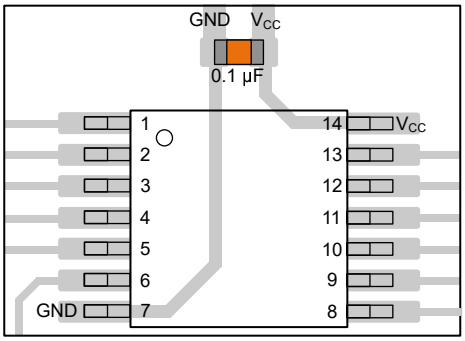


图 8-3. TSSOP 和类似封装的旁路电容器放置示例

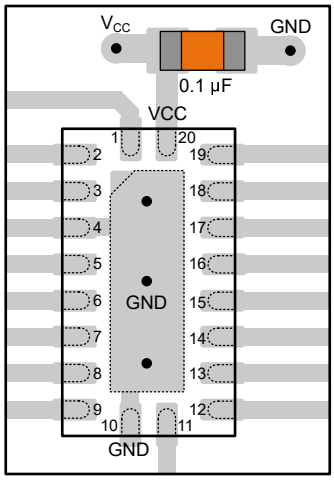


图 8-4. WQFN 和类似封装的旁路电容器放置示例

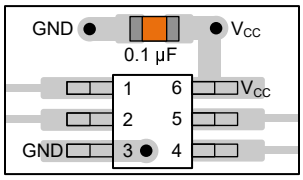


图 8-5. SOT、SC70 和类似封装的旁路电容器放置示例

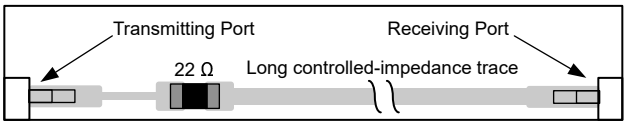


图 8-6. 可改善信号完整性的阻尼电阻放置示例

9 器件和文档支持

TI 提供大量的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

9.1 文档支持

9.1.1 相关文档

欲了解相关文件，请参阅以下内容：

- 德州仪器 (TI)，*CMOS 功耗与 C_{pd} 计算* 应用手册
- 德州仪器 (TI)，*使用逻辑器件进行设计* 应用手册
- 德州仪器 (TI)，*标准线性和逻辑 (SLL) 封装和器件的热特性* 应用手册

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision N (June 2025) to Revision O (October 2025)	Page
• 将 DCK 封装的结至环境热阻值从：278°C/W 更改为：371.0°C/W	5
• 将 DCK 封装的结至外壳（顶部）热阻值从：93°C/W 更改为：297.5°C/W	5
• 将 DCK 封装的结至电路板热阻值从：65°C/W 更改为：258.6°C/W	5
• 将 DCK 封装的结至顶部特征值从：2°C/W 更改为：195.6°C/W	5
• 将 DCK 封装的结至电路板特征值从：64°C/W 更改为：256.2°C/W	5

Changes from Revision M (April 2016) to Revision N (June 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将*器件信息*表更改为*封装信息*	1
• 将 DBV 封装的结至环境热阻值从：229°C/W 更改为：357.1°C/W	5
• 将 DBV 封装的结至外壳（顶部）热阻值从：164°C/W 更改为：263.7°C/W	5
• 将 DBV 封装的结至电路板热阻值从：62°C/W 更改为：264.4°C/W	5
• 将 DBV 封装的结至顶部特征值从：44°C/W 更改为：195.6°C/W	5
• 将 DBV 封装的结至电路板特征值从：62°C/W 更改为：262.2°C/W	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G34DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S)
SN74LVC1G34DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S)
SN74LVC1G34DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S)
SN74LVC1G34DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S
SN74LVC1G34DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S
SN74LVC1G34DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S
SN74LVC1G34DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C345, C34J, C34K, C34R) (C34H, C34S)
SN74LVC1G34DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345, C34J, C34K, C34R) (C34H, C34S)
SN74LVC1G34DBVTE4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S
SN74LVC1G34DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S
SN74LVC1G34DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C345 C34S

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G34DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C95, C9F, C9J, C9R) (C9H, C9P, C9S)
SN74LVC1G34DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C95, C9F, C9J, C9R) (C9H, C9P, C9S)
SN74LVC1G34DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C95, C9F, C9J, C9R) (C9H, C9P, C9S)
SN74LVC1G34DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C95, C9J, C9R) (C9H, C9S)
SN74LVC1G34DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95, C9J, C9R) (C9H, C9S)
SN74LVC1G34DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C95 C9S
SN74LVC1G34DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P4
SN74LVC1G34DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P4
SN74LVC1G34DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C97, C9R)
SN74LVC1G34DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C97, C9R)
SN74LVC1G34DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C9

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G34DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9
SN74LVC1G34YFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9 N
SN74LVC1G34YFPR.B	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9 N
SN74LVC1G34YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N
SN74LVC1G34YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N
SN74LVC1G34YZVR	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9 N
SN74LVC1G34YZVR.B	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9 N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC1G34 :

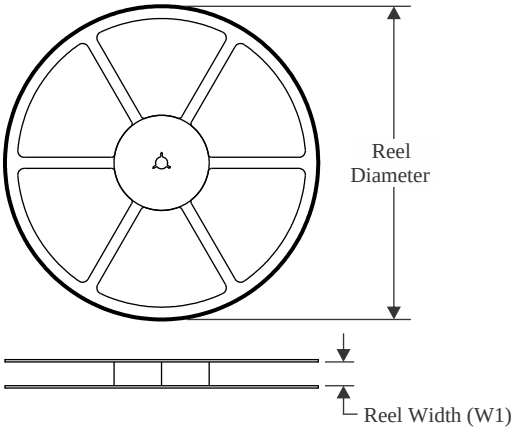
- Automotive : SN74LVC1G34-Q1

NOTE: Qualified Version Definitions:

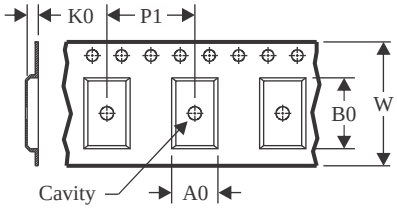
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

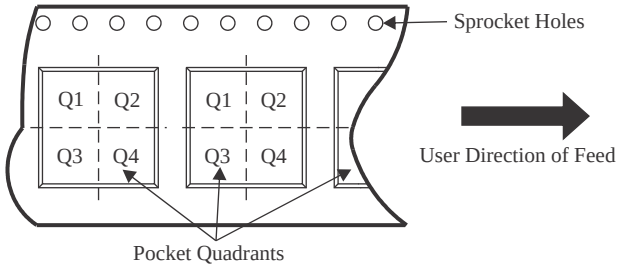


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

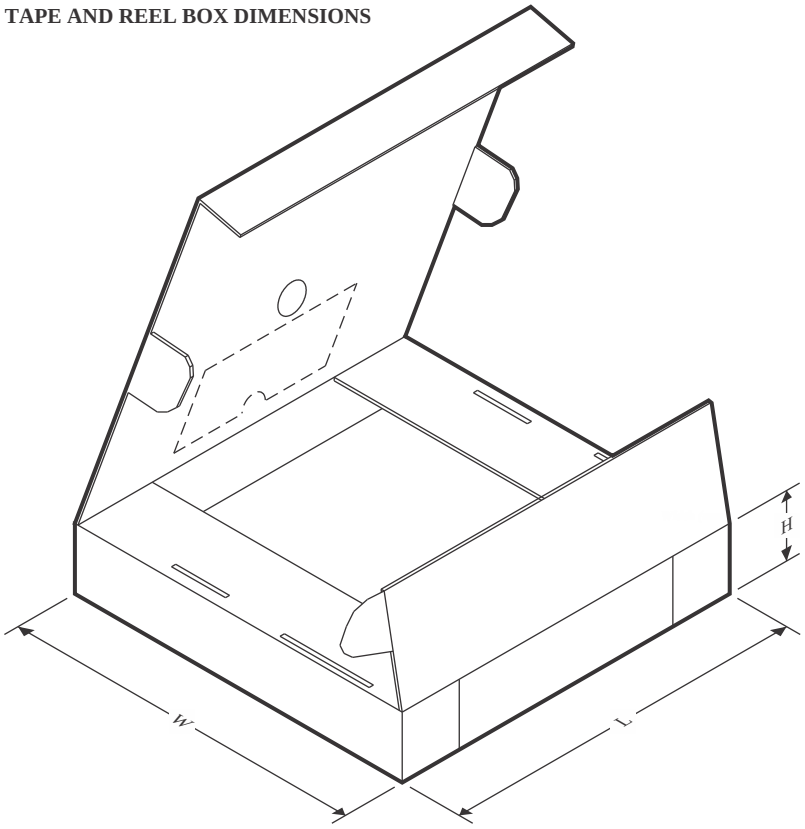


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G34DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G34DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G34DBVTG4	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G34DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G34DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G34DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G34DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G34DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G34DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G34DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G34DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G34DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G34DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G34DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G34YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1
SN74LVC1G34YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G34YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G34DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G34DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G34DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G34DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G34DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G34DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G34DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G34DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G34DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G34DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G34DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G34DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G34DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G34DSFR	SON	DSF	6	5000	184.0	184.0	19.0

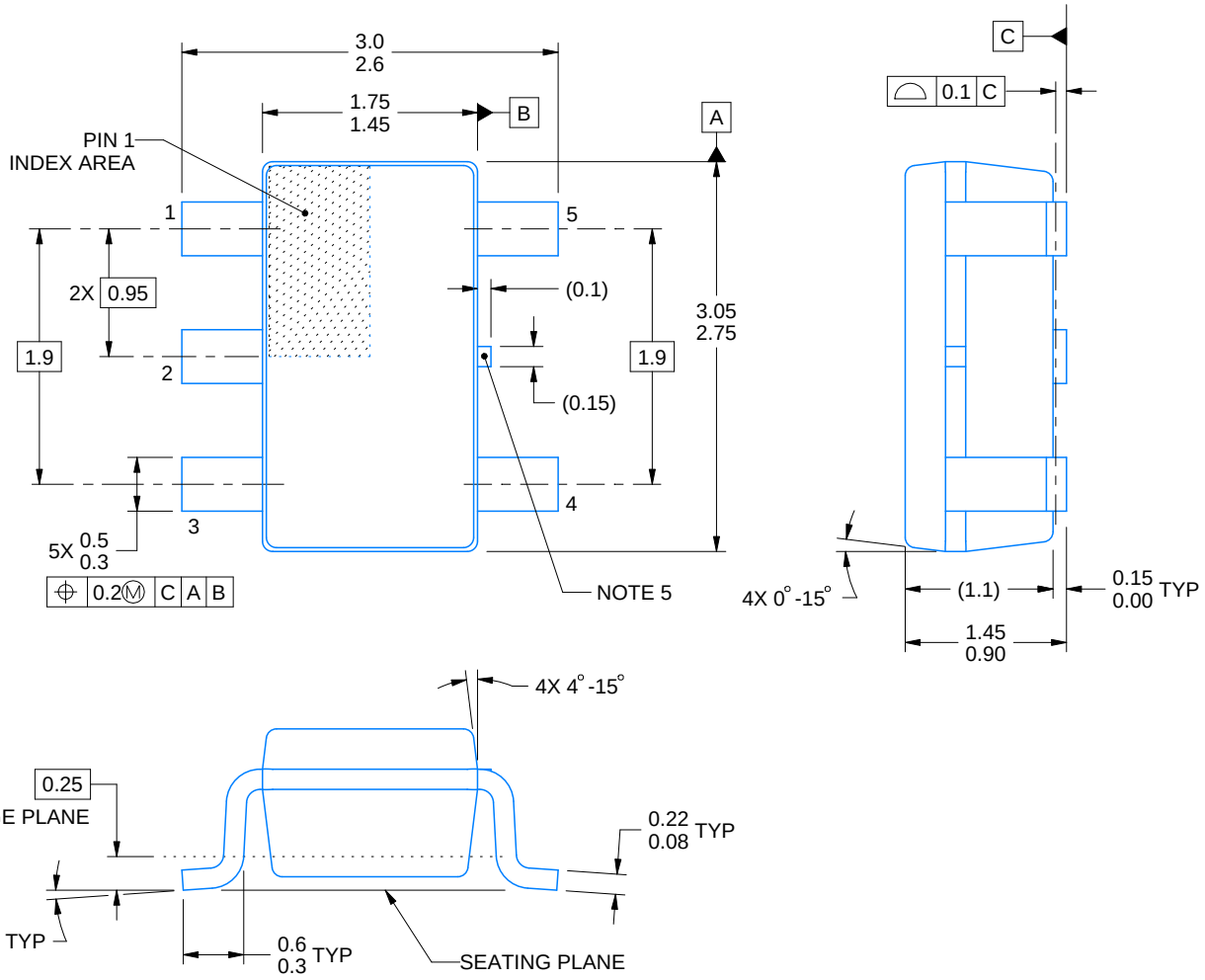
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G34DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G34YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
SN74LVC1G34YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G34YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

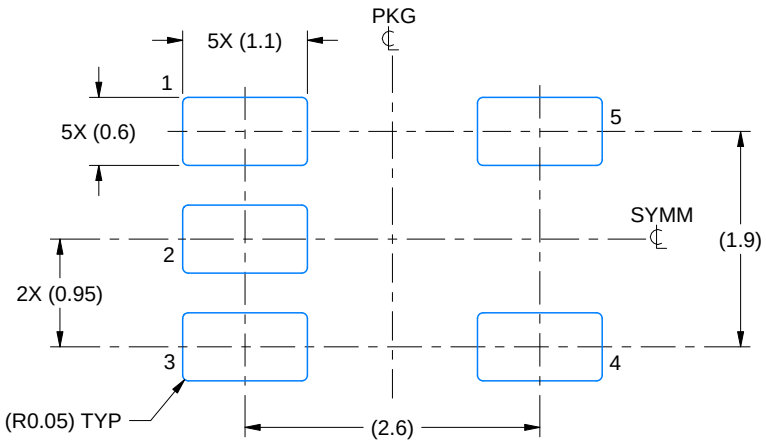
SMALL OUTLINE TRANSISTOR



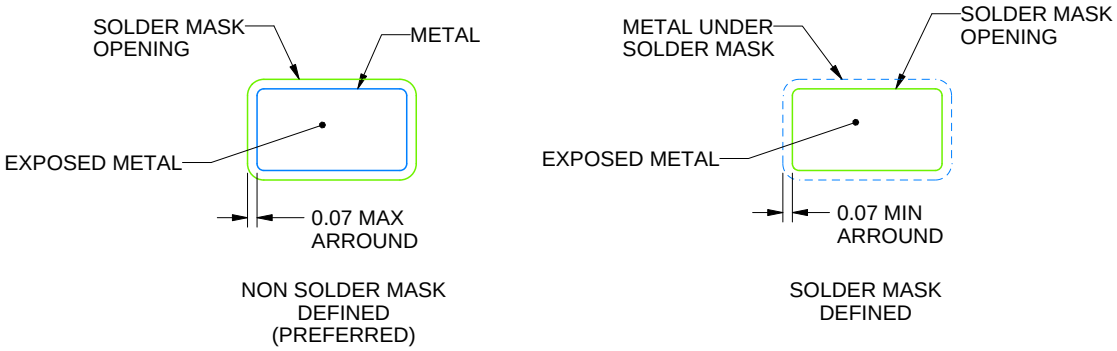
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

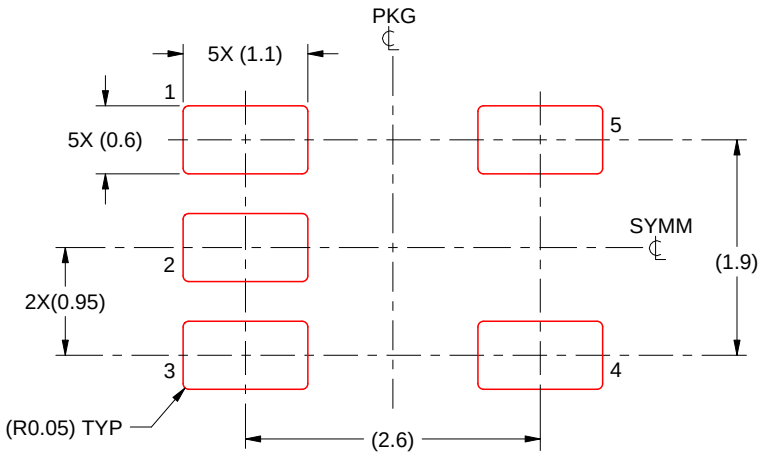


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

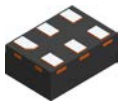
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

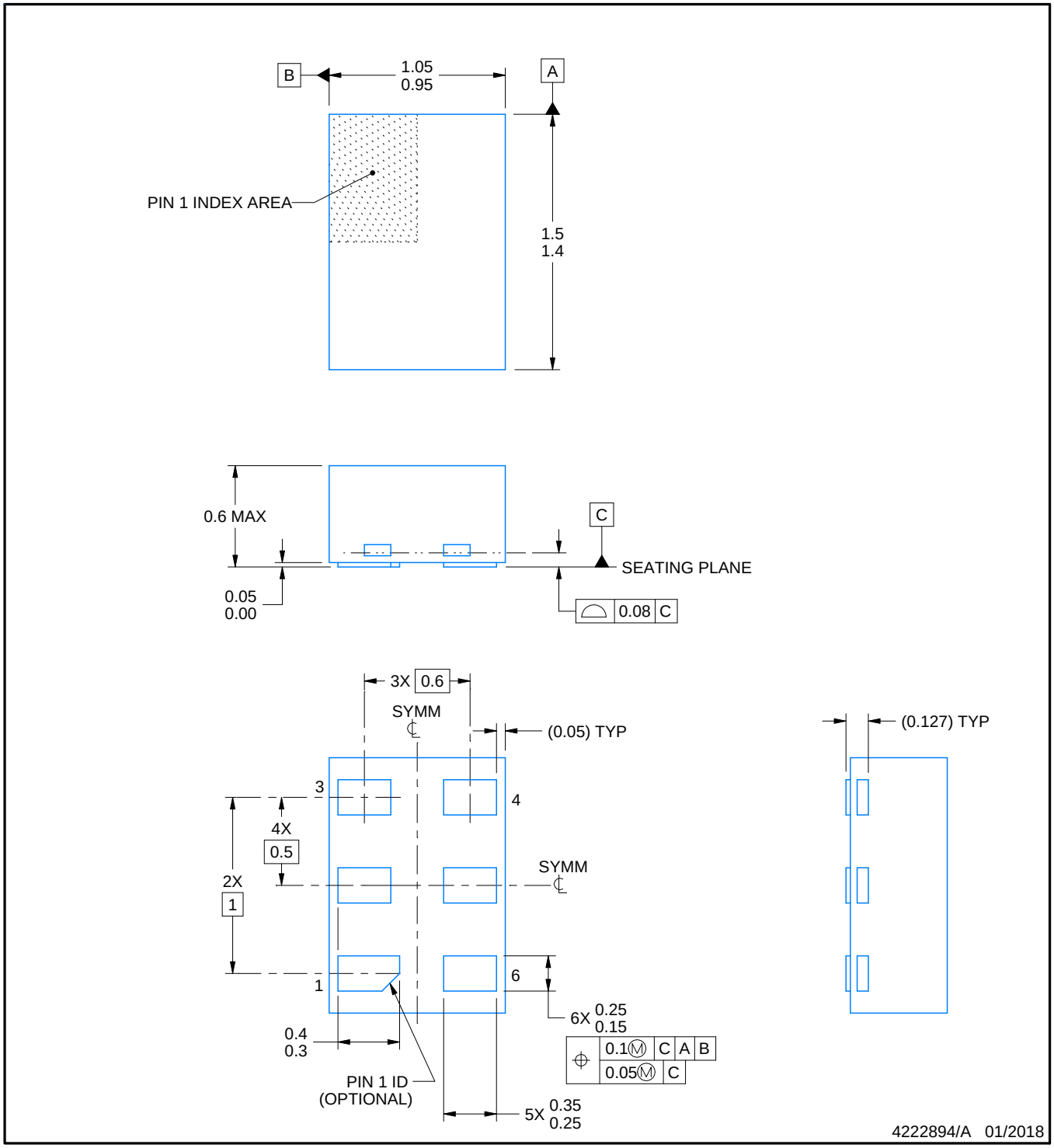
DRY0006A



PACKAGE OUTLINE

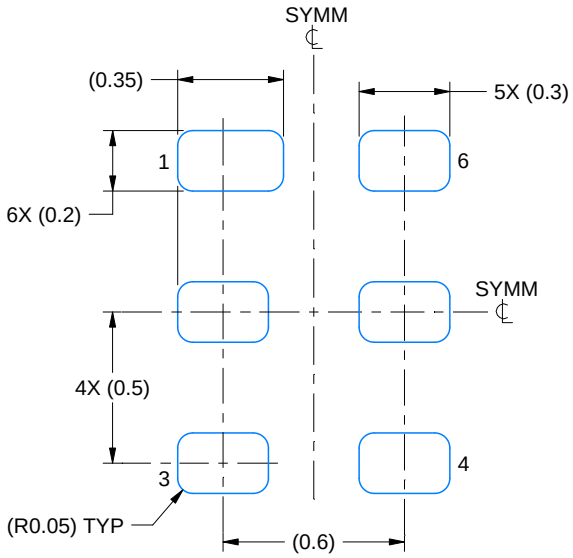
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

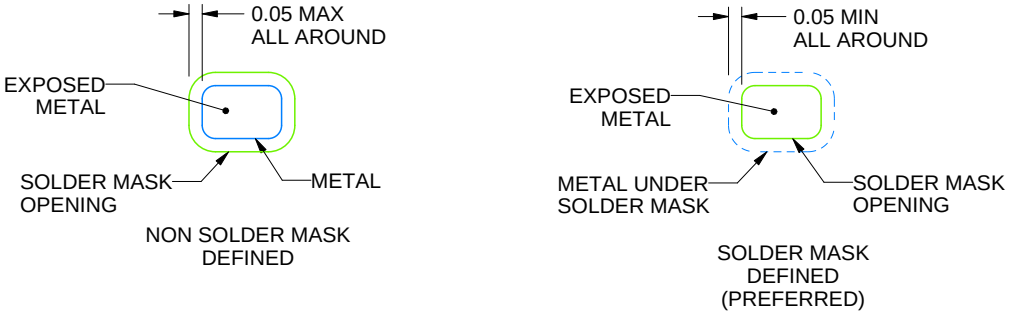


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

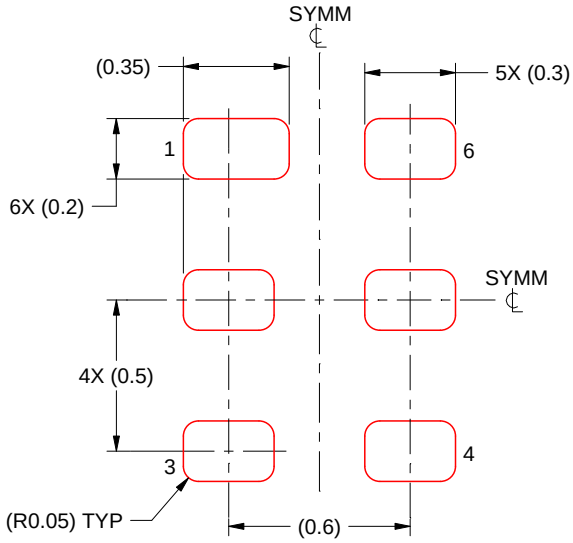
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

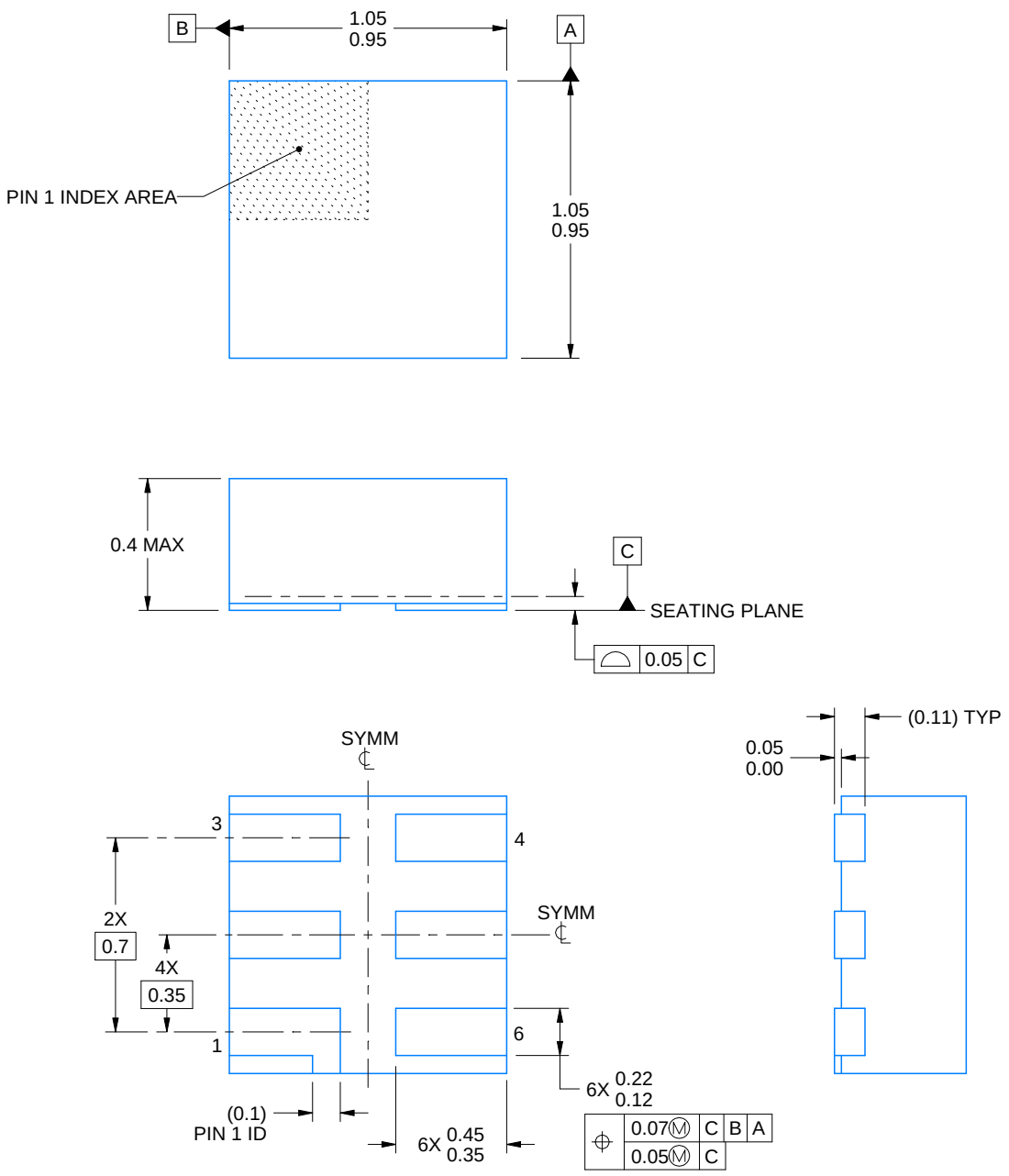
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

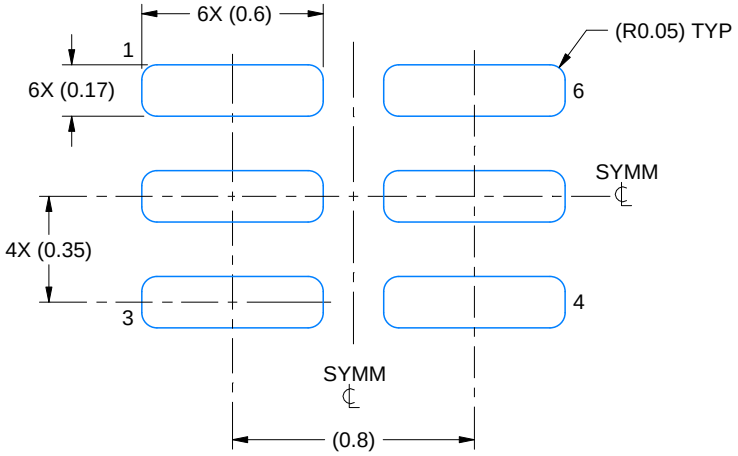
PLASTIC SMALL OUTLINE - NO LEAD



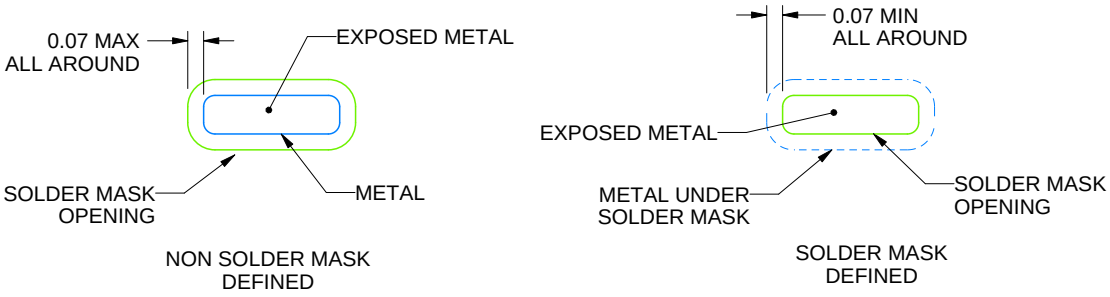
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

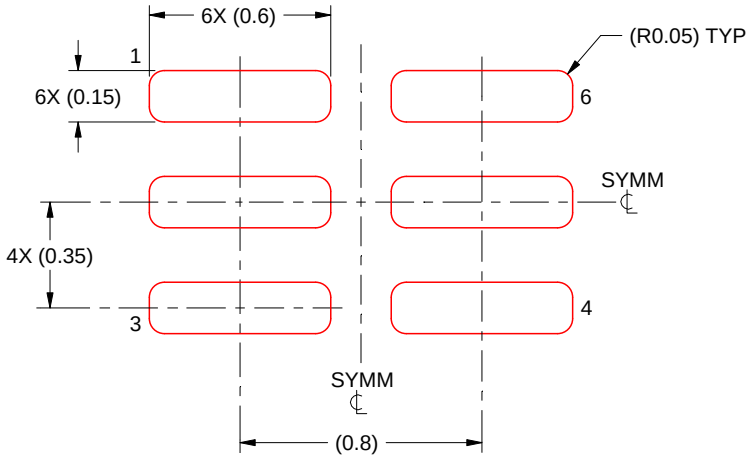
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

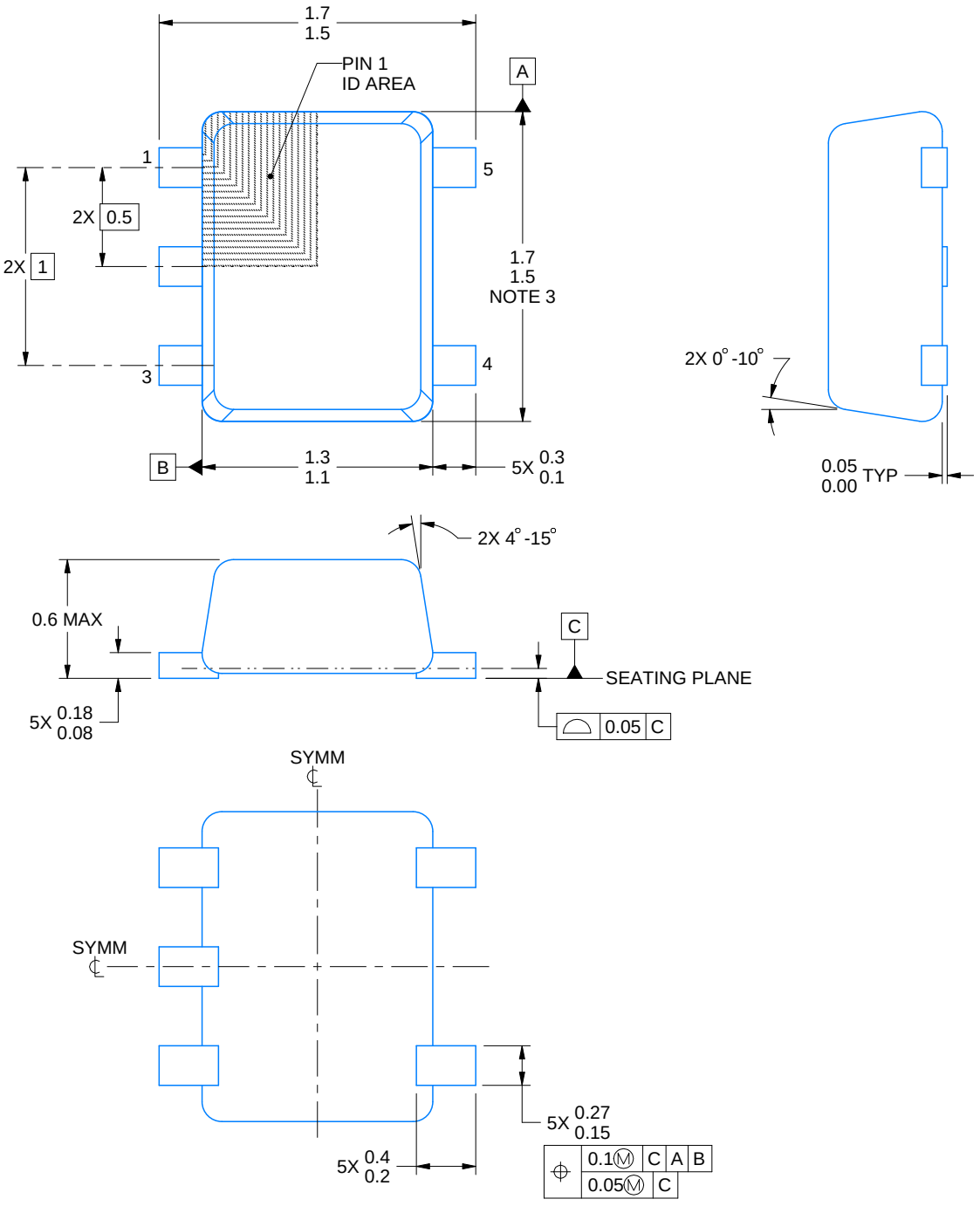
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

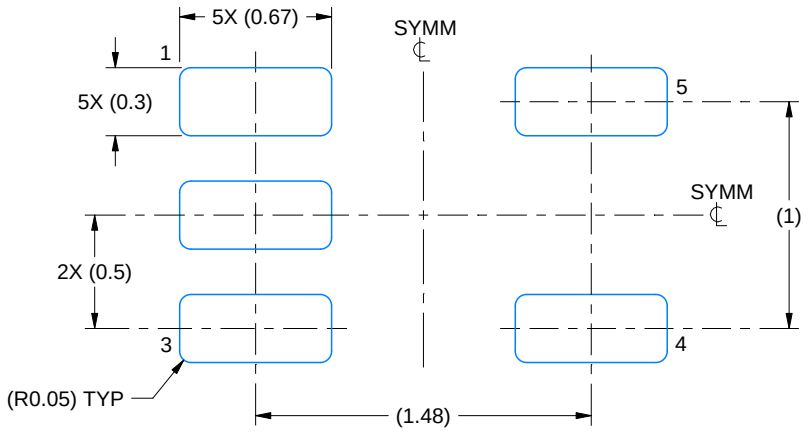
PLASTIC SMALL OUTLINE



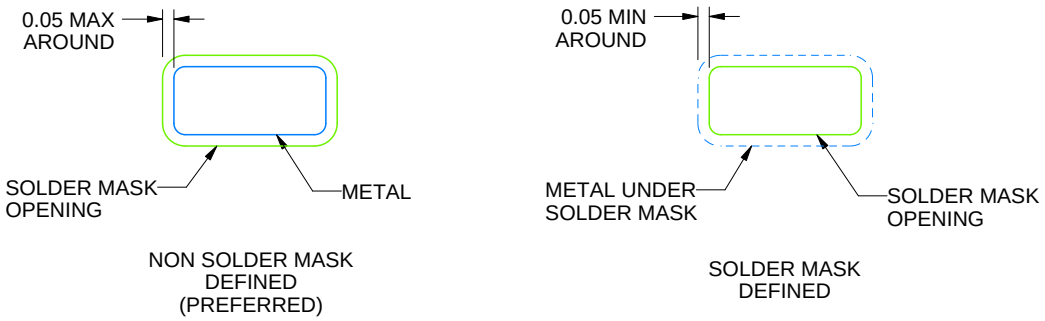
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

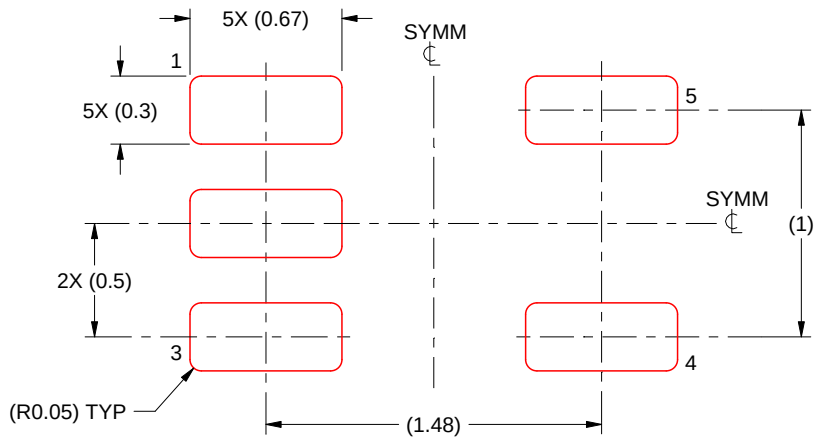


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

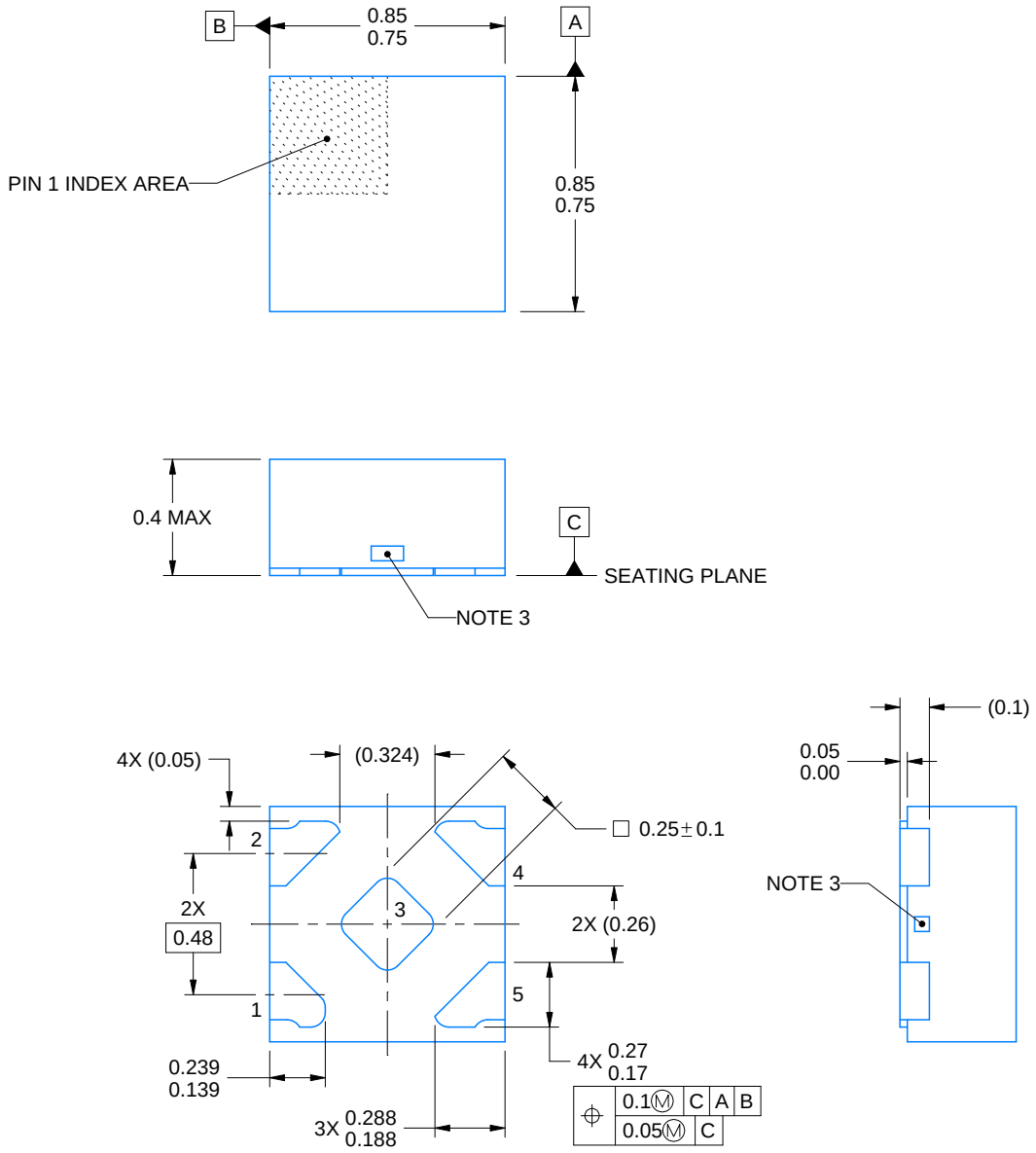
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

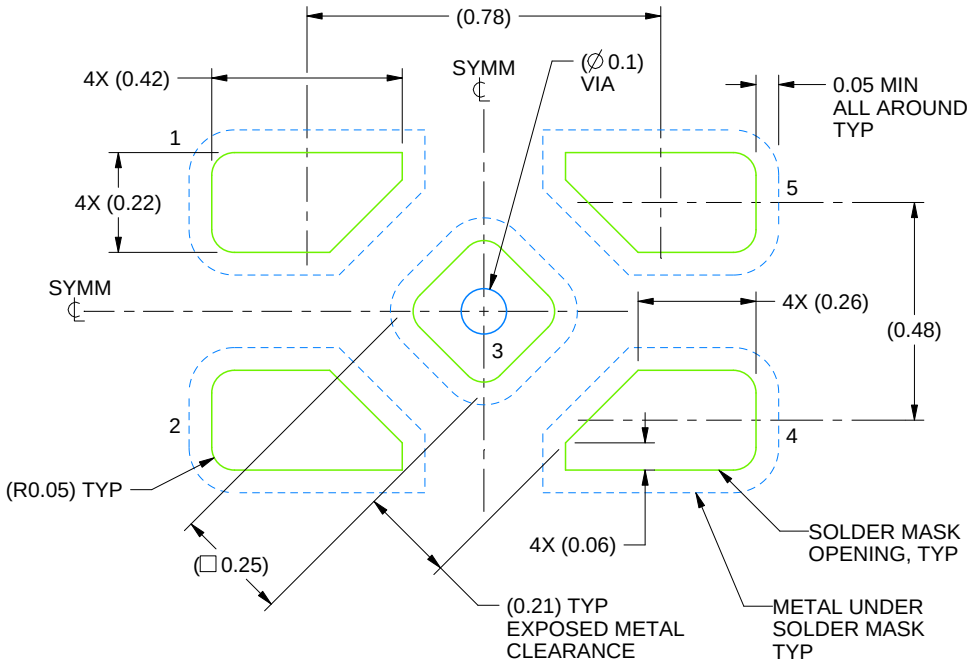
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

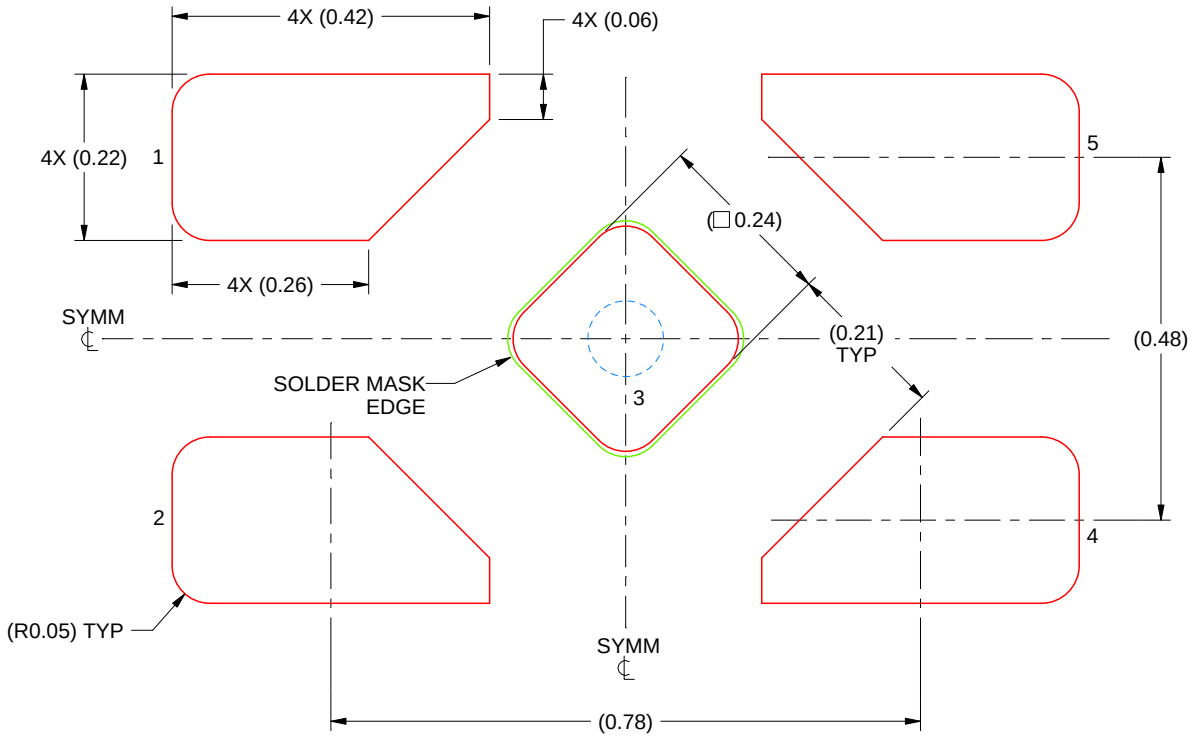
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

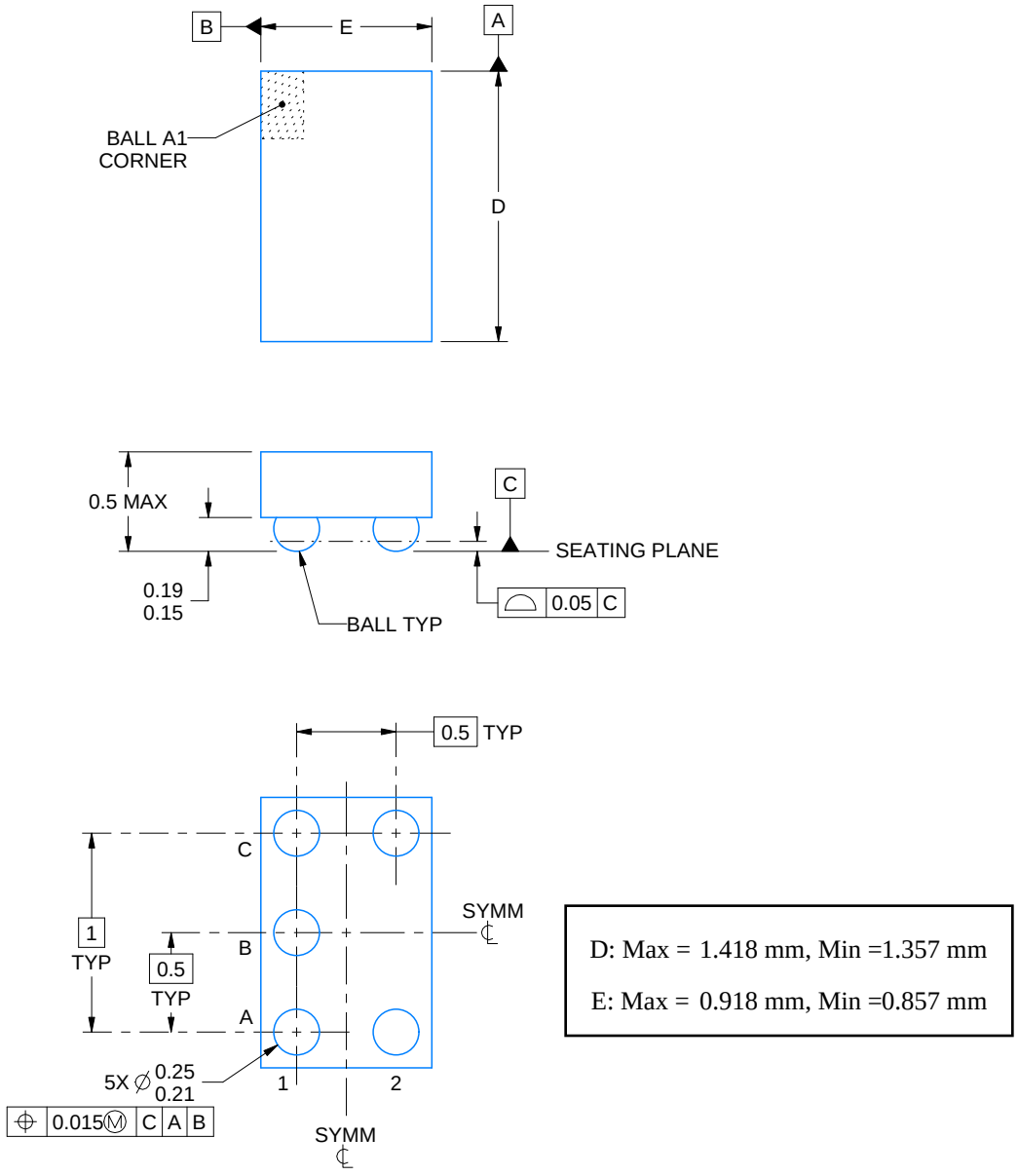
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



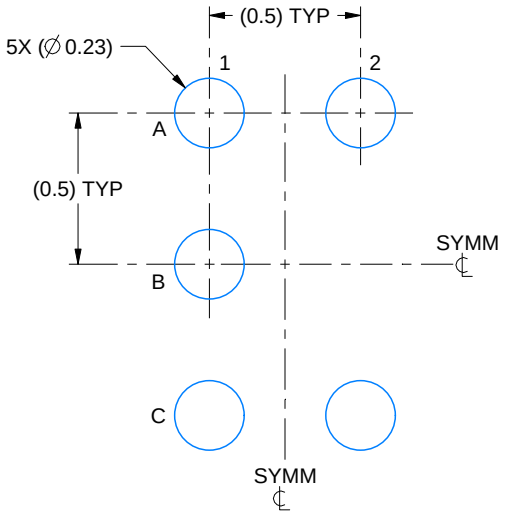
D: Max = 1.418 mm, Min =1.357 mm

E: Max = 0.918 mm, Min =0.857 mm

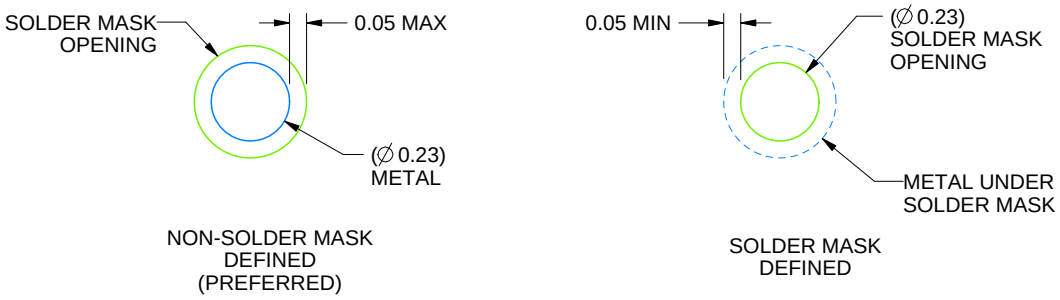
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

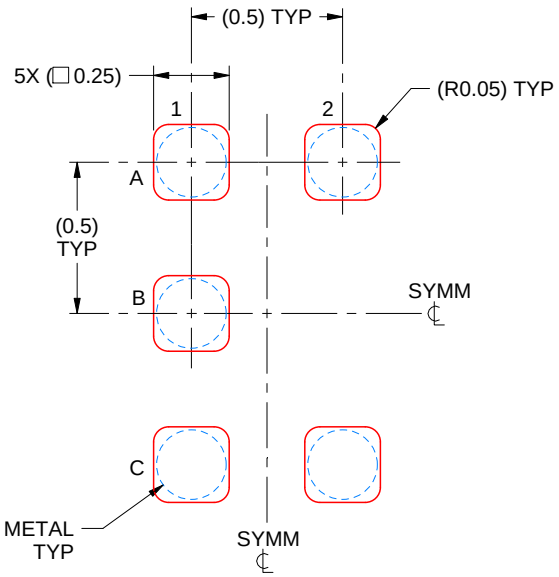


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



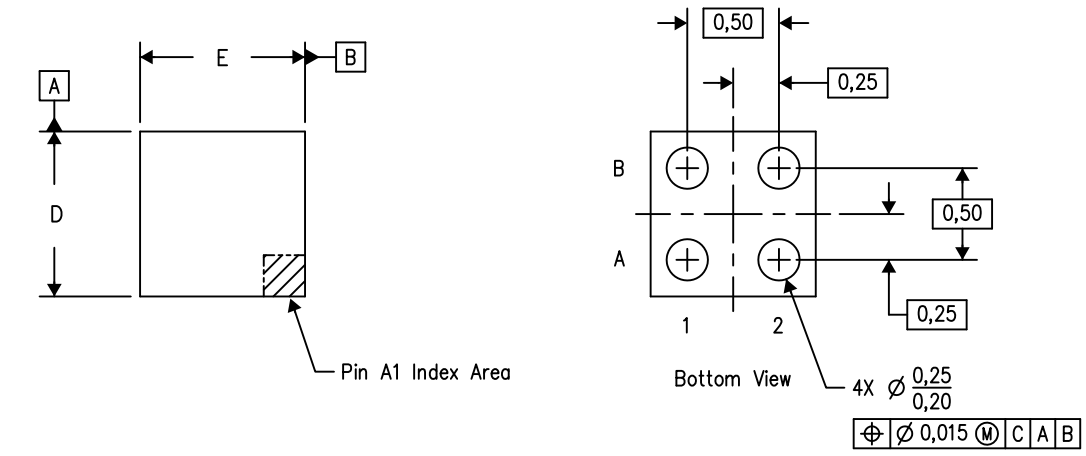
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

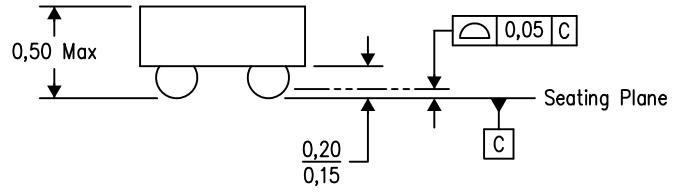
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

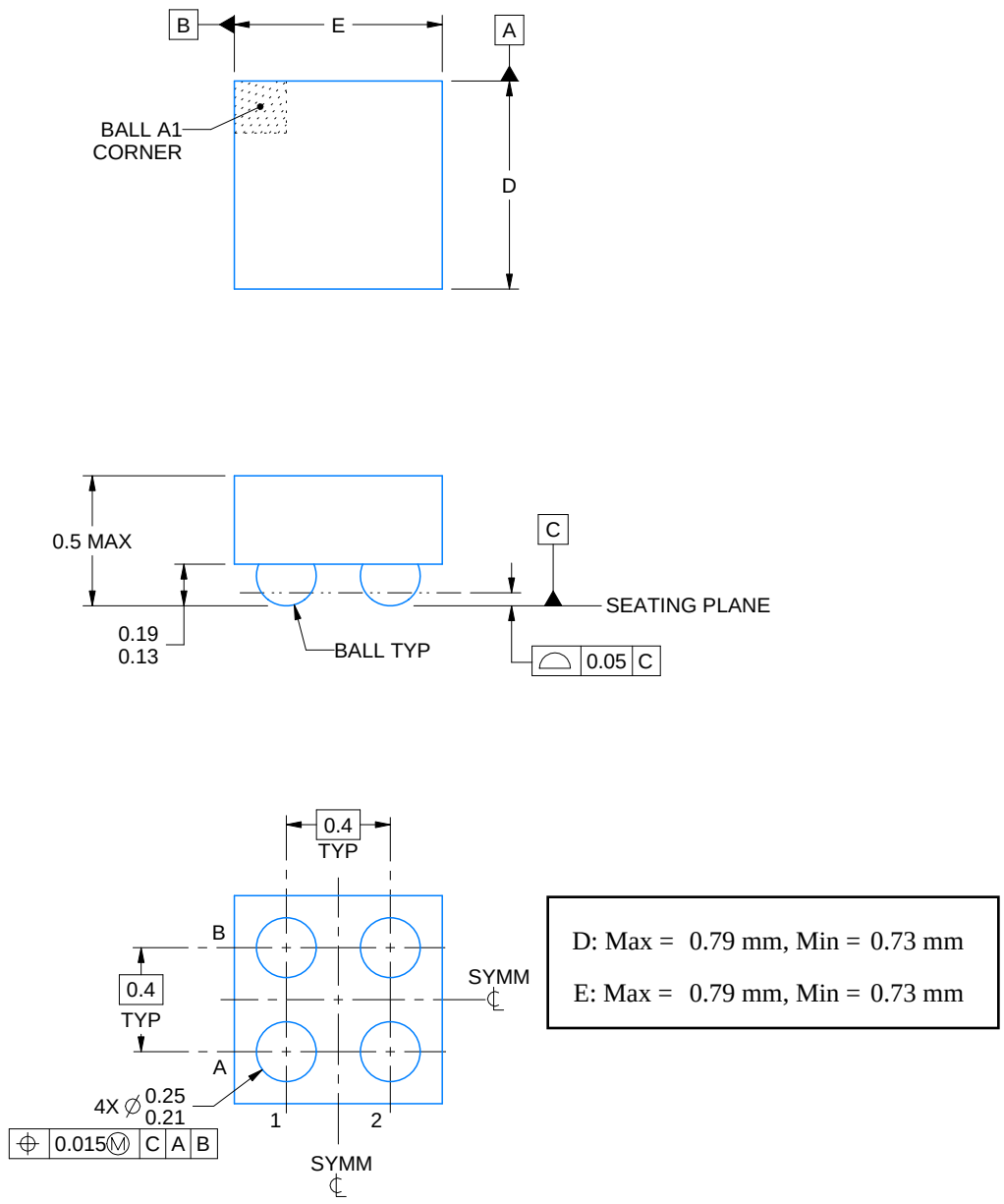
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

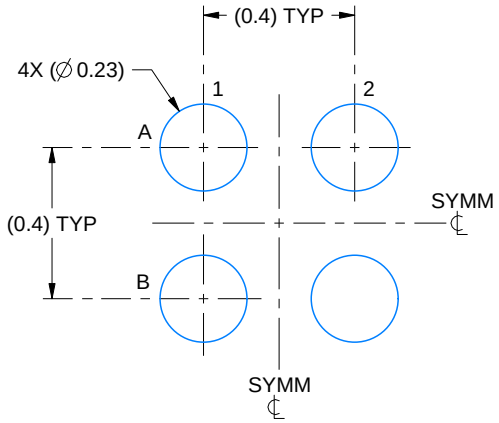
DIE SIZE BALL GRID ARRAY



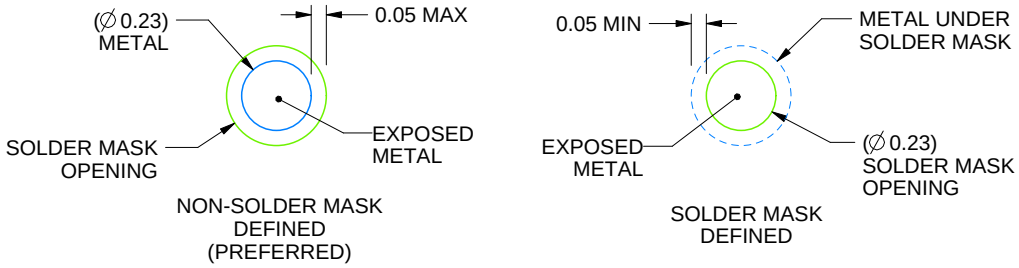
4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

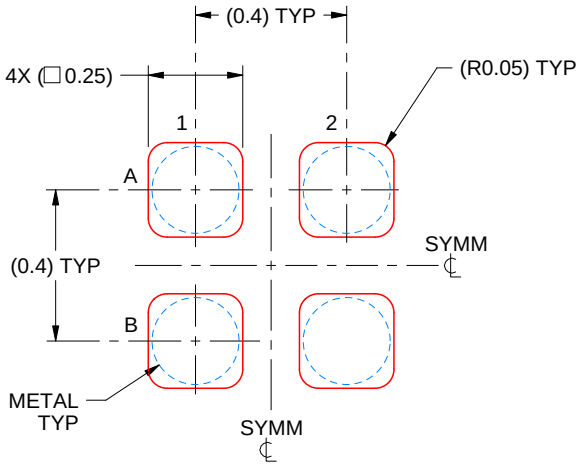
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

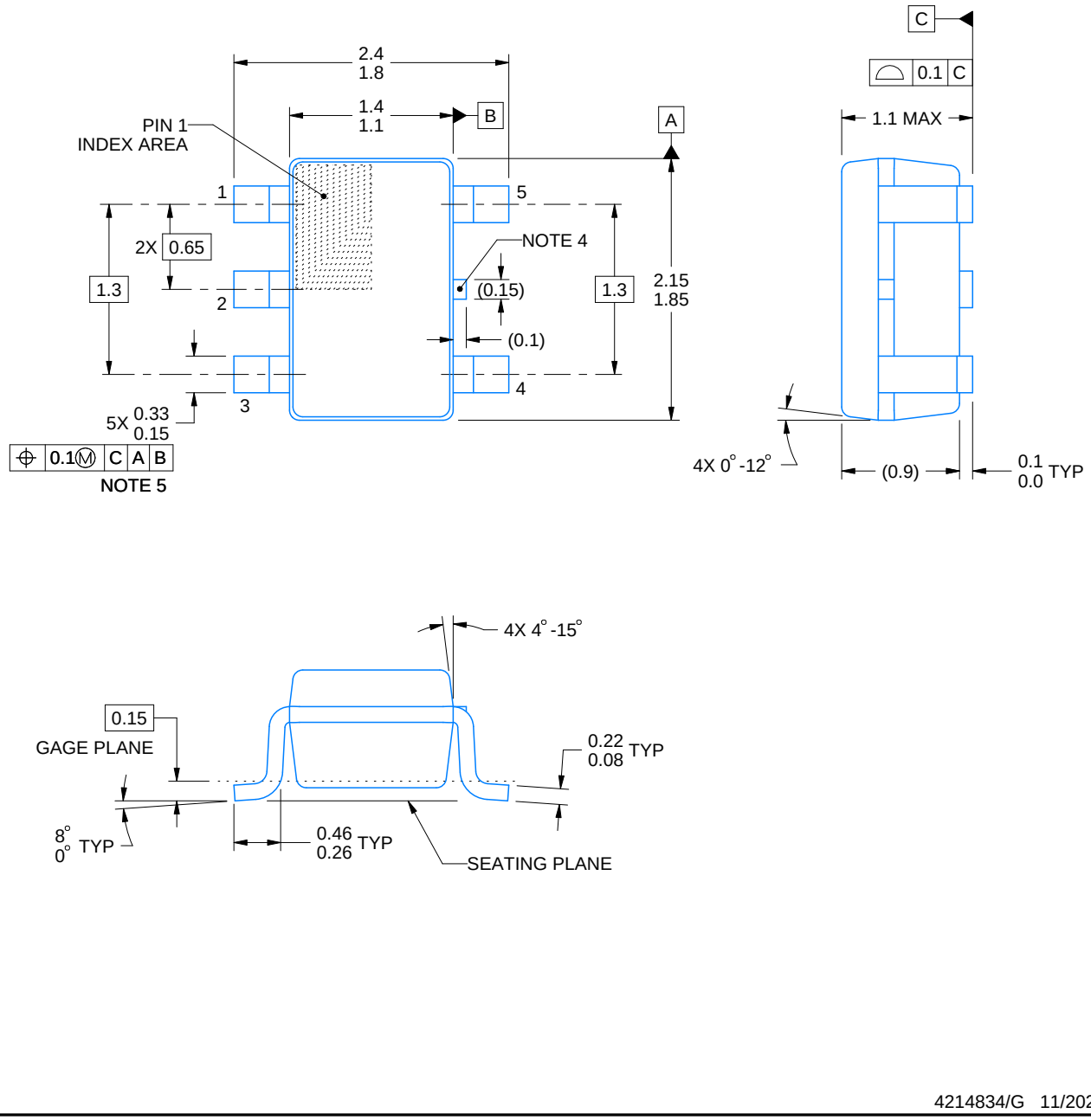
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

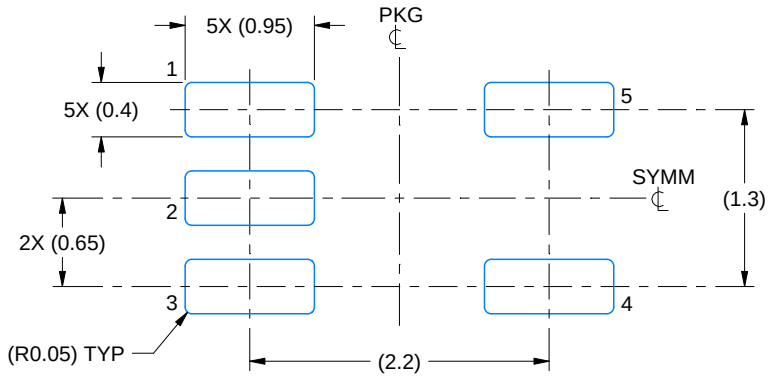
SMALL OUTLINE TRANSISTOR



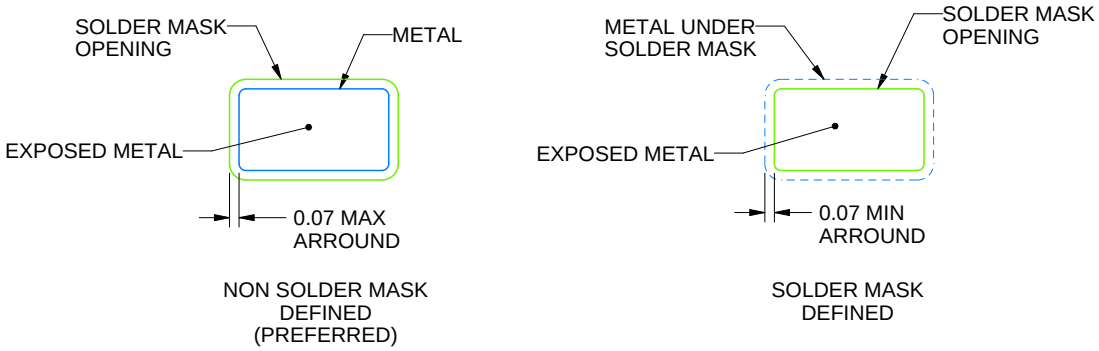
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

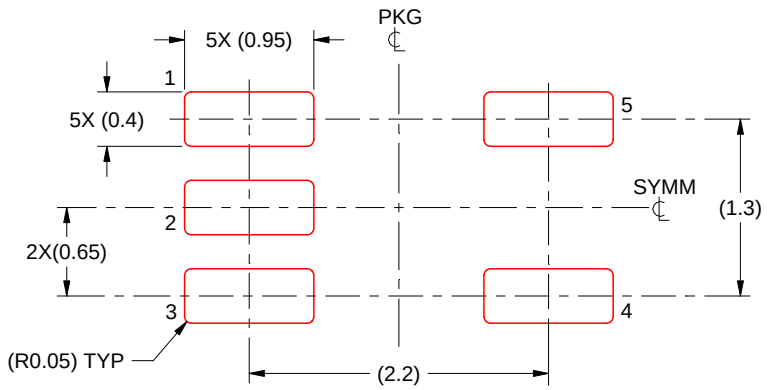


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月