

SN74LVC1G04 单通道反相器门

1 特性

- 采用具有 0.5mm 间距的超小型 0.64mm² 封装 (DPW)
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V，允许降压转换到 V_{CC}
- 3.3V 时 t_{pd} 最大值为 3.3ns
- 低功耗，I_{CC} 最大值为 10 μA
- 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 200V 机器放电模型 (A115-A)
 - 1000V 充电器件模型 (C101)

2 应用

- AV 接收器
- 音频接口盒：便携式
- 蓝光播放器与家庭影院
- 嵌入式 PC
- MP3 播放器/录音机 (便携式音频设备)
- 个人数字助理 (PDA)
- 电源：电信/服务器交流/直流电源：单路控制器：模拟式和数字式
- 固态硬盘 (SSD)：客户端和企业级
- 电视：LCD 电视/数字电视和高清电视 (HDTV)
- 平板电脑：企业级
- 视频分析：服务器
- 无线耳机、键盘和鼠标

3 说明

该单路反相器门设计在 1.65V 至 5.5V V_{CC} 下运行。

SN74LVC1G04 器件执行布尔函数 $Y = \bar{A}$ 。

CMOS 器件具有高输出驱动，同时在宽 V_{CC} 工作范围内保持低静态功率耗散。

SN74LVC1G04 器件采用多种封装，包括外形尺寸为 0.8mm × 0.8mm 的超小型 DPW 封装。

封装信息

器件名称	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 (标称值) ⁽³⁾
SN74LVC1G04	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm
	DRL (SOT-5X3, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm
	DRY (USON, 6)	1.45mm × 1.0mm	1.45mm × 1.0mm
	DSF (X2SON, 6)	1.0mm × 1.0mm	1.0mm × 1.0mm
	YZP (DSBGA, 5)	1.75mm × 1.75mm	1.75mm × 1.25mm
	YZV (DSBGA, 4)	1.25mm × 1.25mm	1.25mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 封装尺寸 (长 × 宽) 为标称值，不包括引脚。



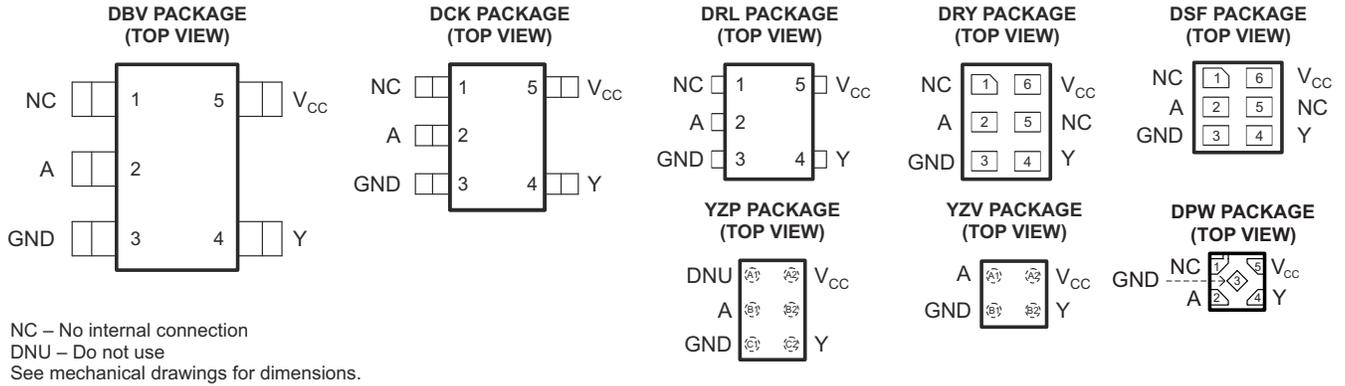
简化版原理图



内容

1 特性	1	7.1 概述.....	10
2 应用	1	7.2 功能方框图.....	10
3 说明	1	7.3 特性说明.....	10
4 引脚配置和功能	3	7.4 器件功能模式.....	10
5 规格	4	8 应用和实施	11
5.1 绝对最大额定值.....	4	8.1 应用信息免责声明.....	11
5.2 ESD 等级.....	4	8.2 应用信息.....	11
5.3 建议运行条件.....	5	8.3 典型应用.....	11
5.4 热性能信息.....	5	8.4 电源相关建议.....	12
5.5 电气特性.....	6	8.5 布局.....	12
5.6 开关特性, $C_L = 15\text{pF}$	6	9 器件和文档支持	13
5.7 开关特性, $C_L = 30\text{pF}$ 或 50pF , -40°C 至 85°C	6	9.1 接收文档更新通知.....	13
5.8 开关特性, $C_L = 15\text{pF}$, -40°C 至 125°C	7	9.2 支持资源.....	13
5.9 开关特性, $C_L = 30\text{pF}$ 或 50pF , -40°C 至 125°C	7	9.3 商标.....	13
5.10 工作特性.....	7	9.4 静电放电警告.....	13
5.11 典型特性.....	7	9.5 术语表.....	13
6 参数测量信息	8	10 修订历史记录	13
7 详细说明	10	11 机械、封装和可订购信息	14

4 引脚配置和功能



引脚功能

引脚						说明
名称	DBV、 DCK、DRL	DSF、DRY	YZP	YZV	DPW	
NC	1	1、5	A1、B2	-	1	无连接
A	2	2	B1	A1	2	输入
GND	3	3	C1	B1	3	接地
Y	4	4	C2	B2	4	输出
V _{CC}	5	6	A2	A2	5	电源端子

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	6.5	V
V_I	输入电压范围		-0.5	6.5	V
V_O	在高阻抗或断电状态对任一输出施加的电压范围 ⁽²⁾		-0.5	6.5	V
V_O	应用到任一处于高电平或低电平状态输出的电压范围 ^{(2) (3)}		-0.5	$V_{CC} + 0.5$	V
I_{IK}	输入钳位电流	$V_I < 0$		-50	mA
I_{OK}	输出钳位电流	$V_O < 0$		-50	mA
I_O	持续输出电流			± 50	mA
	通过 V_{CC} 或 GND 的持续电流			± 100	mA
T_{stg}	贮存温度		-65	150	°C

- (1) 应力超出绝对最大额定值下面列出的值时可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
- (3) V_{CC} 的值在建议运行条件表中提供。

5.2 ESD 等级

		值	单位
$V_{(ESD)}$	静电放电		
	人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准, 所有引脚 ⁽¹⁾	± 2000	V
	充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101, 所有引脚 ⁽²⁾	± 1000	

- (1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
- (2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

(1)		最小值	最大值	单位	
V _{CC}	电源电压	工作	1.65	5.5	V
		仅数据保留	1.5		
V _{IH}	高电平输入电压	V _{CC} = 1.65V 至 1.95V	0.65 × V _{CC}		V
		V _{CC} = 2.3V 至 2.7V	1.7		
		V _{CC} = 3V 至 3.6V	2		
		V _{CC} = 4.5V 至 5.5V	0.7 × V _{CC}		
V _{IL}	低电平输入电压	V _{CC} = 1.65V 至 1.95V		0.35 × V _{CC}	V
		V _{CC} = 2.3V 至 2.7V		0.7	
		V _{CC} = 3V 至 3.6V		0.8	
		V _{CC} = 4.5V 至 5.5V		0.3 × V _{CC}	
V _I	输入电压	0	5.5	V	
V _O	输出电压	0	V _{CC}	V	
I _{OH}	高电平输出电流	V _{CC} = 1.65V		-4	mA
		V _{CC} = 2.3V		-8	
		V _{CC} = 3V		-16	
		V _{CC} = 4.5V		-24	
I _{OL}	低电平输出电流	V _{CC} = 1.65V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 3V		16	
		V _{CC} = 4.5V		24	
Δt/Δv	输入转换上升或下降速率	V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V _{CC} = 3.3V ± 0.3V		10	
		V _{CC} = 5V ± 0.5V		5	
T _A	自然通风条件下的工作温度	-40	125	°C	

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND，以确保器件正常运行。请参阅 TI 应用报告 [CMOS 输入缓慢或悬空的影响](#)，文献编号 SCBA004。

5.4 热性能信息

热指标 ⁽¹⁾	SN74LVC1G04						单位	
	DBV	DCK	DRL	DRY	YZP	DPW		
	5 引脚	5 引脚	5 引脚	6 引脚	5 引脚	4 引脚		
R _{θJA}	结至环境热阻	357.1	371.0	243	439	130	340	°C/W
R _{θJCTop}	结至外壳 (顶部) 热阻	263.7	297.5	78	277	54	215	
R _{θJB}	结至电路板热阻	264.4	258.6	78	271	51	294	
ψ _{JT}	结至顶部特征参数	195.6	195.6	10	84	1	41	
ψ _{JB}	结至电路板特征参数	262.2	256.2	77	271	50	294	
R _{θJCbot}	结至外壳 (底部) 热阻	-	-	-	-	-	250	

(1) 有关新旧热指标的更多信息，请参阅 [半导体和 IC 封装热指标](#) 应用手册。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得 (除非另有说明)

参数	测试条件	V _{CC}	-40°C 至 85°C			建议 -40°C 至 125°C			单位
			最小值	典型值 ⁽¹⁾	最大值	最小值	典型值	最大值	
V _{OH}	I _{OH} = -100 μA	1.65V 至 5.5V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -4mA	1.65V	1.2			1.2			
	I _{OH} = -8mA	2.3V	1.9			1.9			
	I _{OH} = -16mA	3V	2.4			2.4			
	I _{OH} = -24mA		2.3			2.3			
	I _{OH} = -32mA	4.5V	3.8			3.8			
V _{OL}	I _{OL} = 100 μA	1.65V 至 5.5V	0.1			0.1			V
	I _{OL} = 4mA	1.65V	0.45			0.45			
	I _{OL} = 8mA	2.3V	0.3			0.3			
	I _{OL} = 16mA	3V	0.4			0.4			
	I _{OL} = 24mA		0.55			0.55			
	I _{OL} = 32mA	4.5V	0.55			0.55			
I _I	A 输入	V _I = 5.5V 或 GND	0 至 5.5V			±5			μA
I _{off}		V _I 或 V _O = 5.5V	0			±10			μA
I _{CC}		V _I = 5.5V 或 GND I _O = 0	1.65V 至 5.5V			10			μA
ΔI _{CC}		一个输入电压为 V _{CC} - 0.6V , 其他输入电压为 V _{CC} 或 GND	3V 至 5.5V			500			μA
C _i		V _I = V _{CC} 或 GND	3.3V			3.5			pF

(1) 所有典型值均在 V_{CC} = 3.3V、T_A = 25°C 下测得。

5.6 开关特性, C_L = 15pF

在自然通风条件下的建议工作温度范围内测得, C_L = 15pF (除非另有说明)
(请参阅图 6-1)

参数	从 (输入)	至 (输出)	-40°C 至 85°C								单位
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t _{pd}	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

5.7 开关特性, C_L = 30pF 或 50pF, -40°C 至 85°C

在自然通风条件下的建议工作温度范围内测得, C_L = 30pF 或 50pF (除非另有说明)
(请参阅图 6-2)

参数	从 (输入)	至 (输出)	-40°C 至 85°C								单位
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t _{pd}	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

5.8 开关特性, $C_L = 15\text{pF}$, -40°C 至 125°C

在自然通风条件下的建议工作温度范围内测得, $C_L = 15\text{pF}$ (除非另有说明)
(请参阅图 6-1)

参数	从 (输入)	至 (输出)	-40°C 至 125°C								单位
			$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 5\text{V} \pm 0.5\text{V}$		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

5.9 开关特性, $C_L = 30\text{pF}$ 或 50pF , -40°C 至 125°C

在自然通风条件下的建议工作温度范围内测得, $C_L = 30\text{pF}$ 或 50pF (除非另有说明)
(请参阅图 6-2)

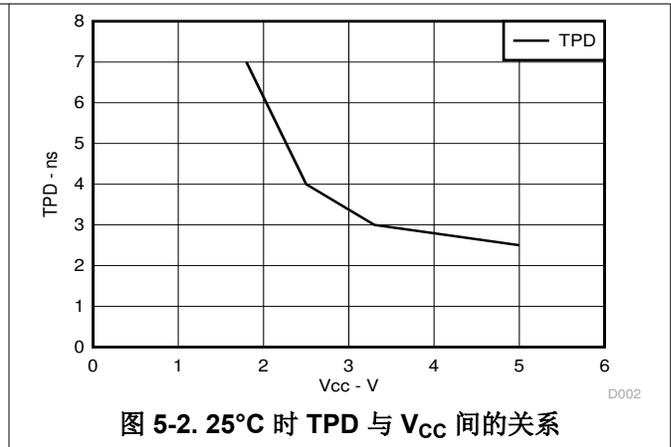
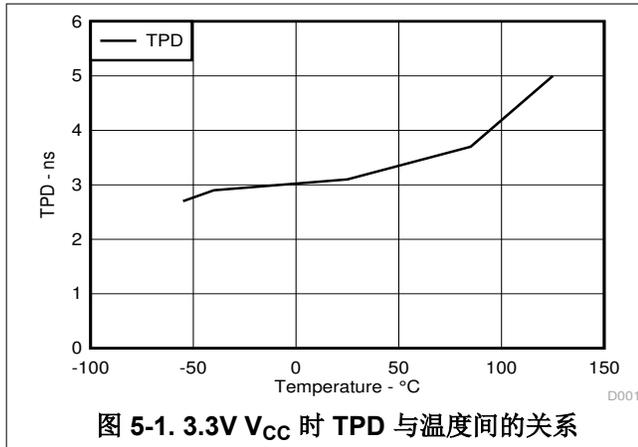
参数	从 (输入)	至 (输出)	-40°C 至 125°C								单位
			$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 5\text{V} \pm 0.5\text{V}$		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

5.10 工作特性

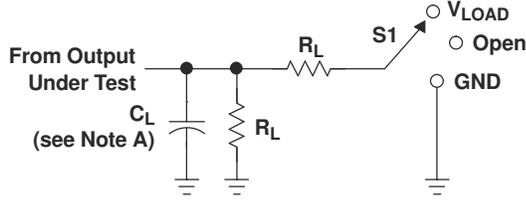
在自然通风条件下的工作温度范围内测得 (除非另有说明)

参数	测试条件	$V_{CC} = 1.8\text{V}$	$V_{CC} = 2.5\text{V}$	$V_{CC} = 3.3\text{V}$	$V_{CC} = 5.0\text{V}$	单位
		典型值	典型值	典型值	典型值	
C_{pd} 功率耗散电容	$f = 10\text{MHz}$	16	18	18	20	pF

5.11 典型特性



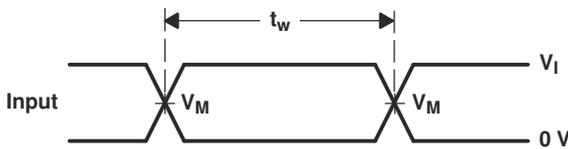
6 参数测量信息



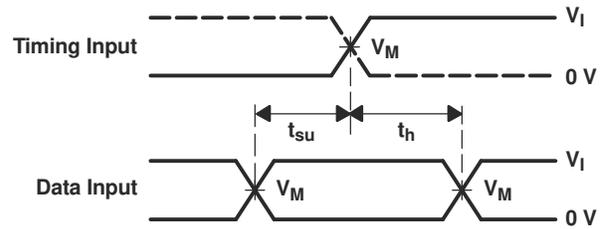
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

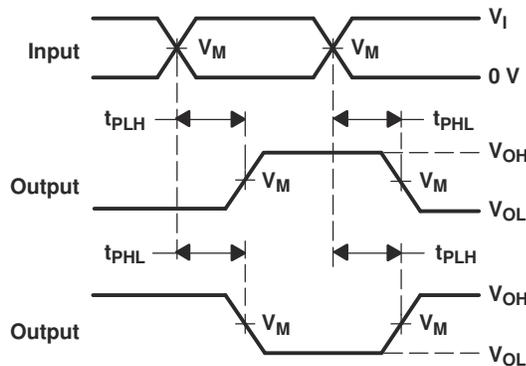
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



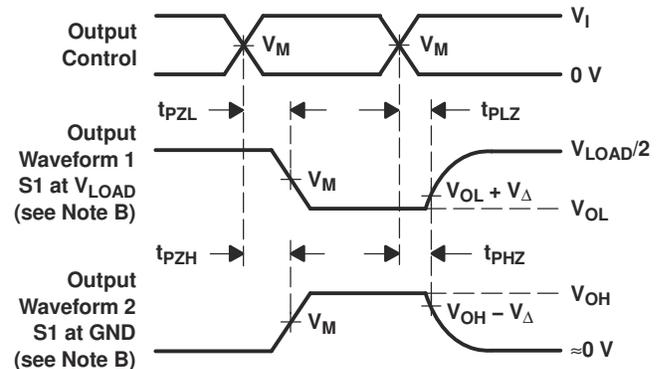
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



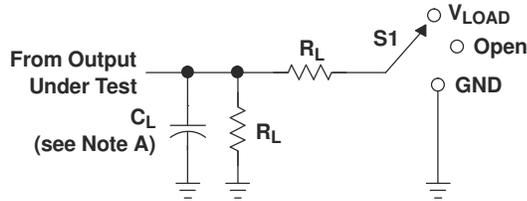
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

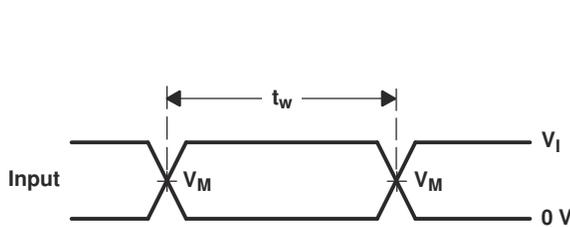
图 6-1. 负载电路和电压波形



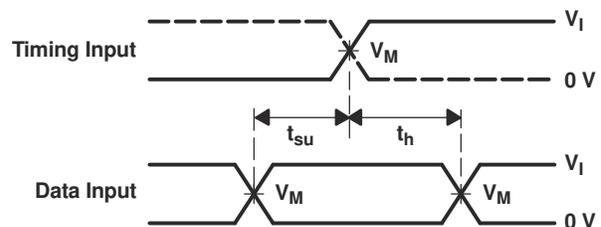
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

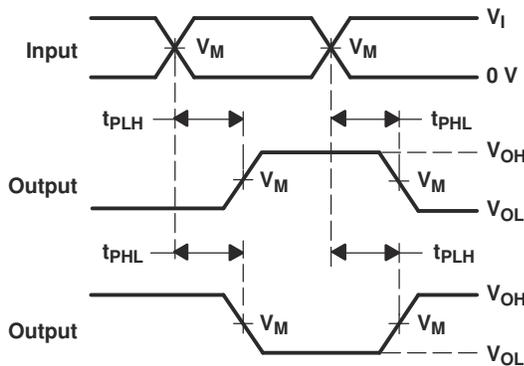
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



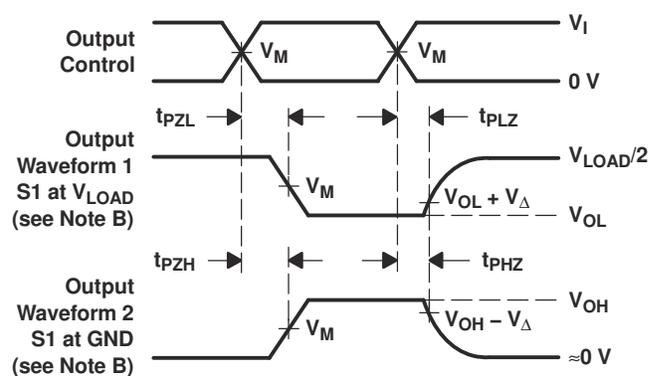
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

图 6-2. 负载电路和电压波形

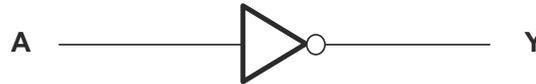
7 详细说明

7.1 概述

SN74LVC1G04 器件包含反相门并执行布尔函数 $Y = \bar{A}$ 。该器件完全适用于使用 I_{off} 的局部关断应用。 I_{off} 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。

DPW 封装技术是 IC 封装中的一项重大突破。其小巧的 0.64mm^2 的封装尺寸较之其他封装选项可显著节省布板空间，同时仍保留方便制造的 0.5mm 传统引线间距。

7.2 功能方框图



7.3 特性说明

- 宽工作电压范围。
 - 可在 1.65V 至 5.5V 范围内工作。
- 支持降压转换。
- 输入电压高达 5.5V 。
- I_{off} 特性允许在 V_{CC} 为 0V 时在输入和输出上产生电压。

7.4 器件功能模式

功能表

输入 A	输出 Y
H	L
L	H

8 应用和实施

8.1 应用信息免责声明

备注

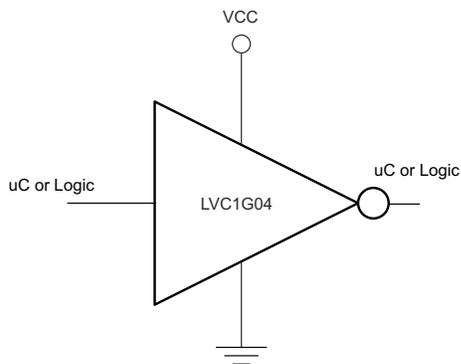
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.2 应用信息

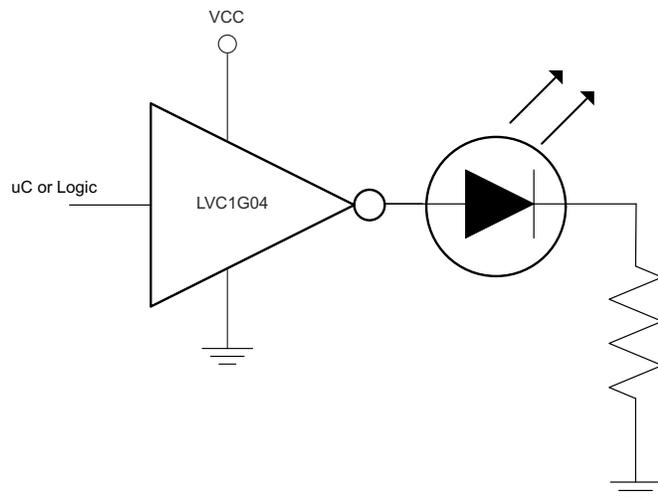
SN74LVC1G04 是一款高驱动 CMOS 器件，可用于实现具有高输出驱动的反转逻辑，例如 LED 应用。它可以在 3.3V 下产生 24mA 驱动电流，因此非常适合驱动多个输出，也适用于高达 100MHz 的高速应用。输入可耐受 5.5V 电压，允许将其降压转换至 V_{CC} 。

8.3 典型应用

Inverter Logic Function



Basic LED Driver



8.3.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.3.2 详细设计过程

1. 建议的输入条件

- 上升时间和下降时间规格：请参阅[建议运行条件](#)表中的 $\Delta t / \Delta V$ 。
- 指定的高电平和低电平：请参阅[建议运行条件](#)表中的 V_{IH} 和 V_{IL} 。
- 输入可耐受过压，允许它们在任何有效 V_{CC} 下高达[建议运行条件](#)表中的 (V_I 最大值)。

2. 建议的输出条件

- 每路输出的负载电流不应超过 (I_O 最大值) 以及该器件的总电流 (通过 V_{CC} 或 GND 的持续电流)。这些限值位于[绝对最大额定值](#)表中。
- 输出不应被拉至高于 V_{CC} 。

8.3.3 应用曲线

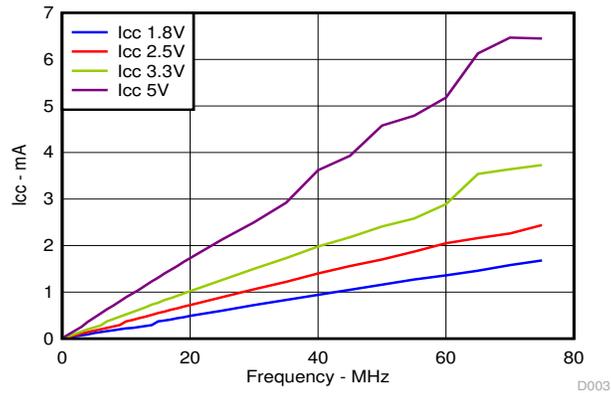


图 8-1. I_{cc} 与频率间的关系

8.4 电源相关建议

电源可以是建议运行条件表中最小和最大电源电压额定值之间的任意电压。

每个 VCC 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 $0.1\ \mu\text{f}$ ；如果有多个 VCC 引脚，则建议每个电源引脚使用 $0.01\ \mu\text{f}$ 或 $0.022\ \mu\text{f}$ 。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\ \mu\text{f}$ 和 $1\ \mu\text{F}$ 电容器通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

8.5 布局

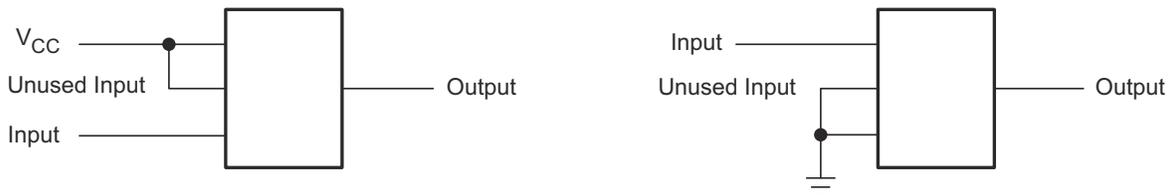
8.5.1 布局指南

当使用多位逻辑器件时，输入不应悬空。

在许多情况下，未使用数字逻辑器件的全部或部分功能；例如，仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。下一段指定在所有情况下都必须遵守的规则。

数字逻辑器件的所有未使用输入必须连接至高或低偏置以防悬空。应根据器件的功能为任何特定未使用的输入施加逻辑电平。通常，将这些输入连接到 GND 或 VCC，具体情况视合理性或便利性而定。

8.5.2 布局示例



9 器件和文档支持

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision AE (June 2025) to Revision AF (October 2025)	Page
• 将 DCK 封装的结至环境热阻值从：229°C/W 更改为：371.0°C/W.....	5
• 将 DCK 封装的结至外壳（顶部）热阻值从：93°C/W 更改为：297.5°C/W.....	5
• 将 DCK 封装的结至电路板热阻值从：65°C/W 更改为：258.6°C/W.....	5
• 将 DCK 封装的结至顶部特征值从：2°C/W 更改为：195.6°C/W.....	5
• 将 DCK 封装的结至电路板特征值从：64°C/W 更改为：256.2°C/W.....	5

Changes from Revision AD (April 2014) to Revision AE (June 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 将 器件信息 表更改为 封装信息	1
• 将 T_{stg} 移至 绝对最大额定值表 中.....	4
• 将处理额定值更改为 ESD 等级.....	4
• 将 DBV 封装的结至环境热阻值从：278°C/W 更改为：357.1°C/W.....	5
• 将 DBV 封装的结至外壳（顶部）热阻值从：164°C/W 更改为：263.7°C/W.....	5
• 将 DBV 封装的结至电路板热阻值从：62°C/W 更改为：264.4°C/W.....	5
• 将 DBV 封装的结至顶部特征值从：44°C/W 更改为：195.6°C/W.....	5
• 将 DBV 封装的结至电路板特征值从：62°C/W 更改为：262.2°C/W.....	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G04DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVTE4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DCK3	Last Time Buy	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G04DCK3.B	Last Time Buy	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)
SN74LVC1G04DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4.B	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRG4	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
SN74LVC1G04DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
SN74LVC1G04DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKTE4	Active	Production	SC70 (DCK) 5	250 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTE4.B	Active	Production	SC70 (DCK) 5	250 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
SN74LVC1G04DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
SN74LVC1G04DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G04DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)
SN74LVC1G04DRY2	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRY2.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	Call TI Nipdau	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
SN74LVC1G04YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
SN74LVC1G04YZVR	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7
SN74LVC1G04YZVR.B	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G04 :

- Automotive : [SN74LVC1G04-Q1](#)
- Enhanced Product : [SN74LVC1G04-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

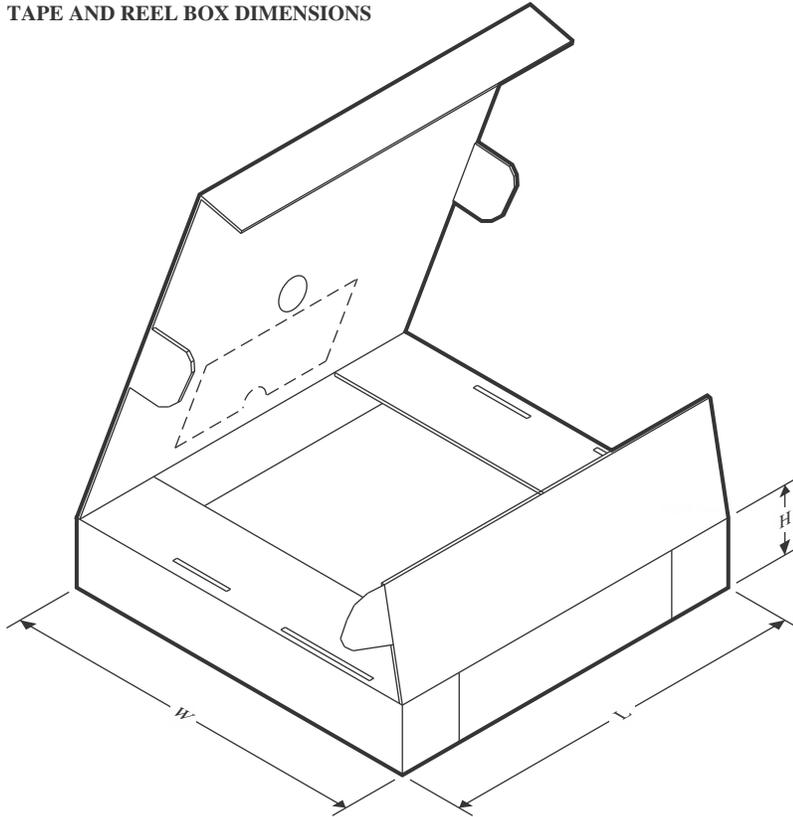
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

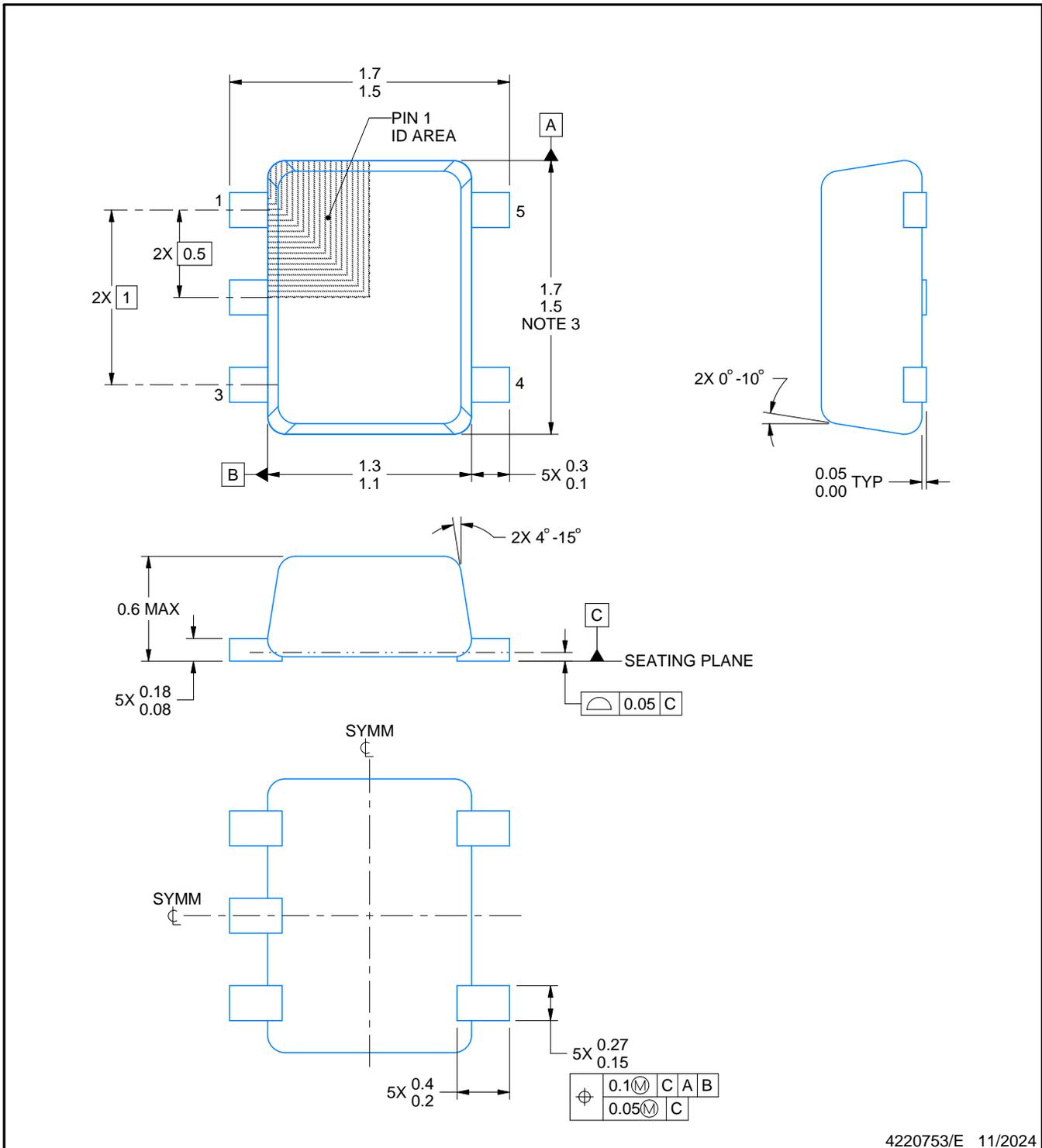
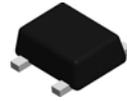
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G04DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G04DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G04DSF2G4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G04DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G04YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04YZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G04DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2G4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G04YZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0



4220753/E 11/2024

NOTES:

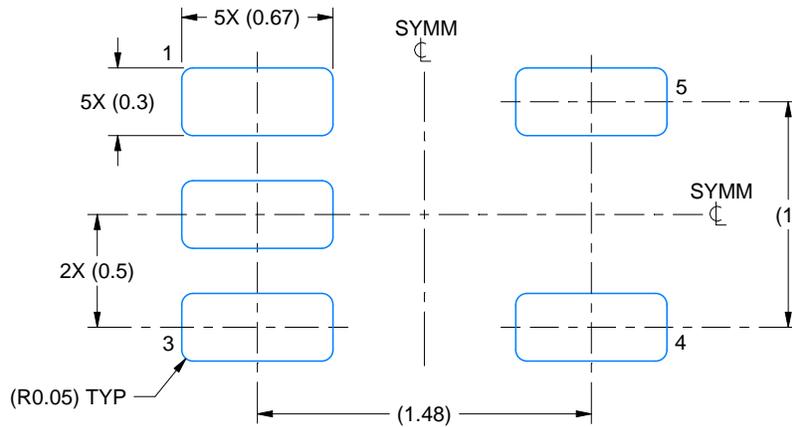
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

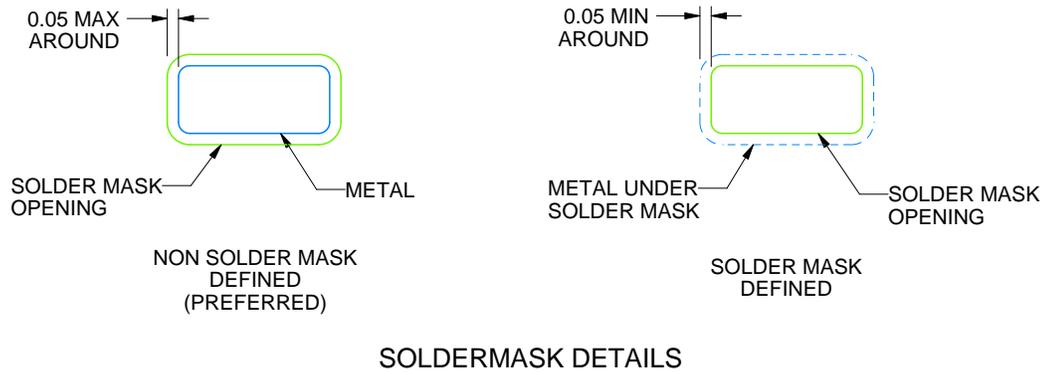
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

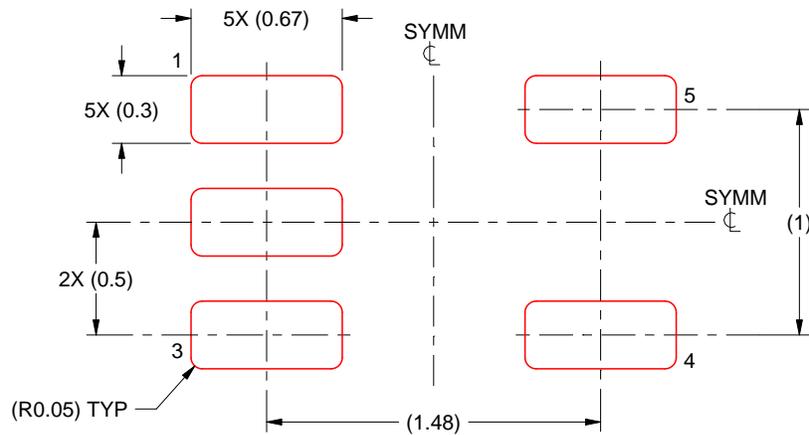
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

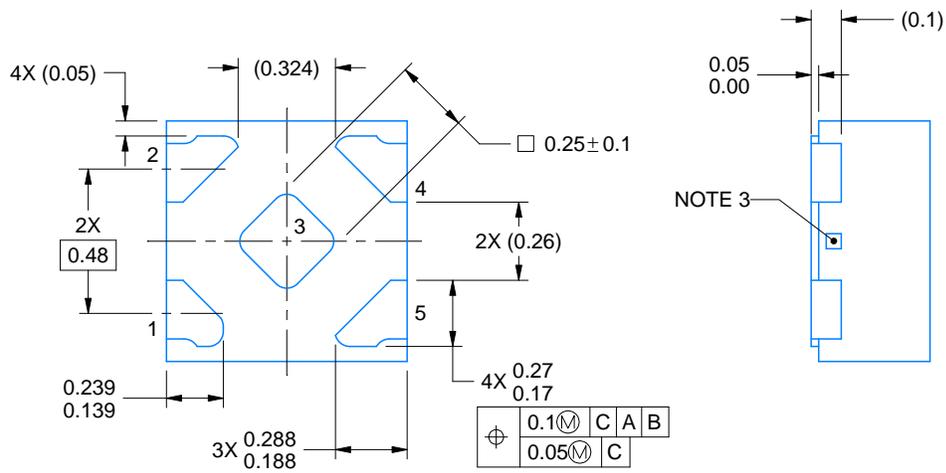
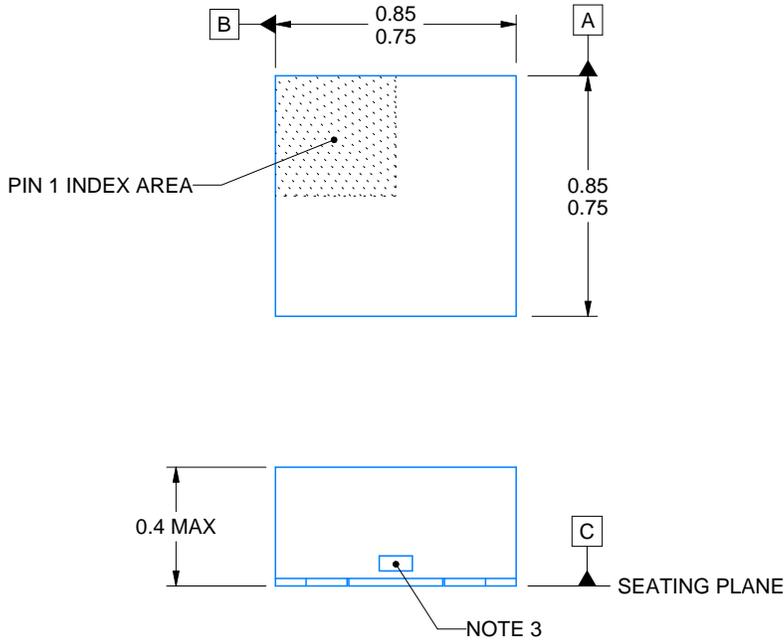
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

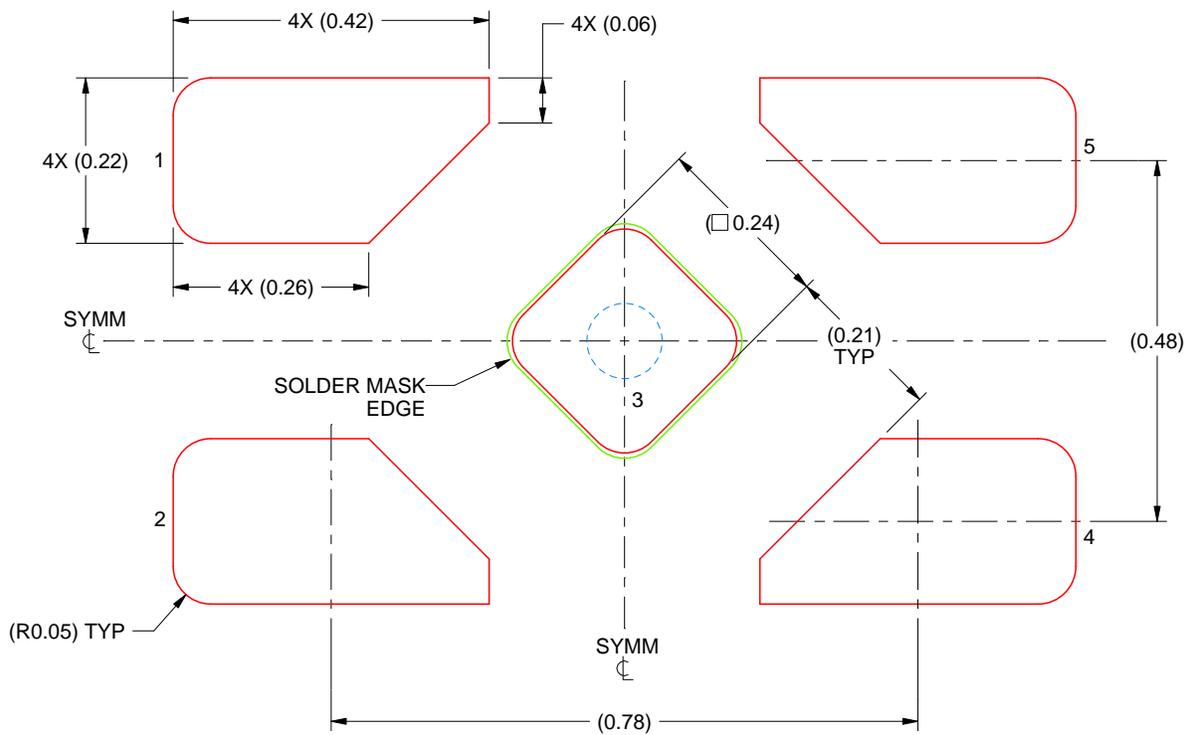
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

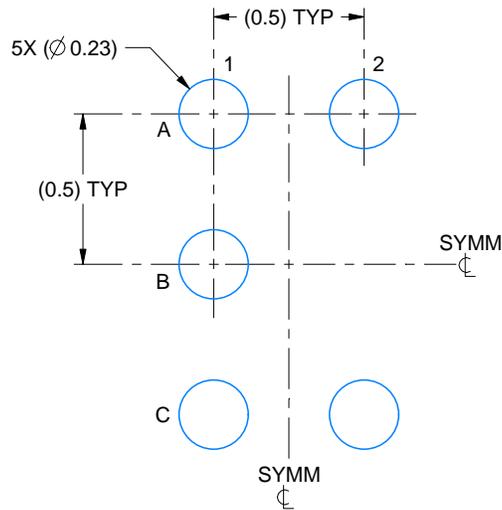
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

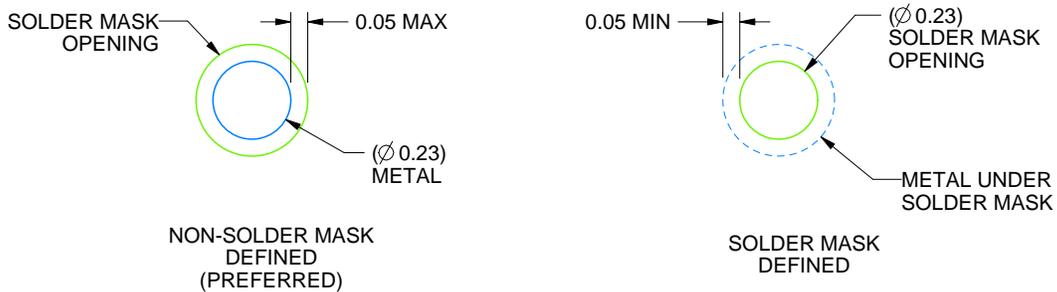
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

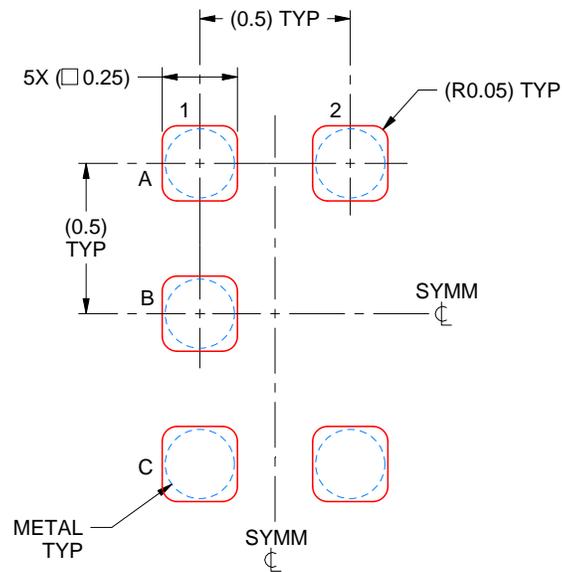
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

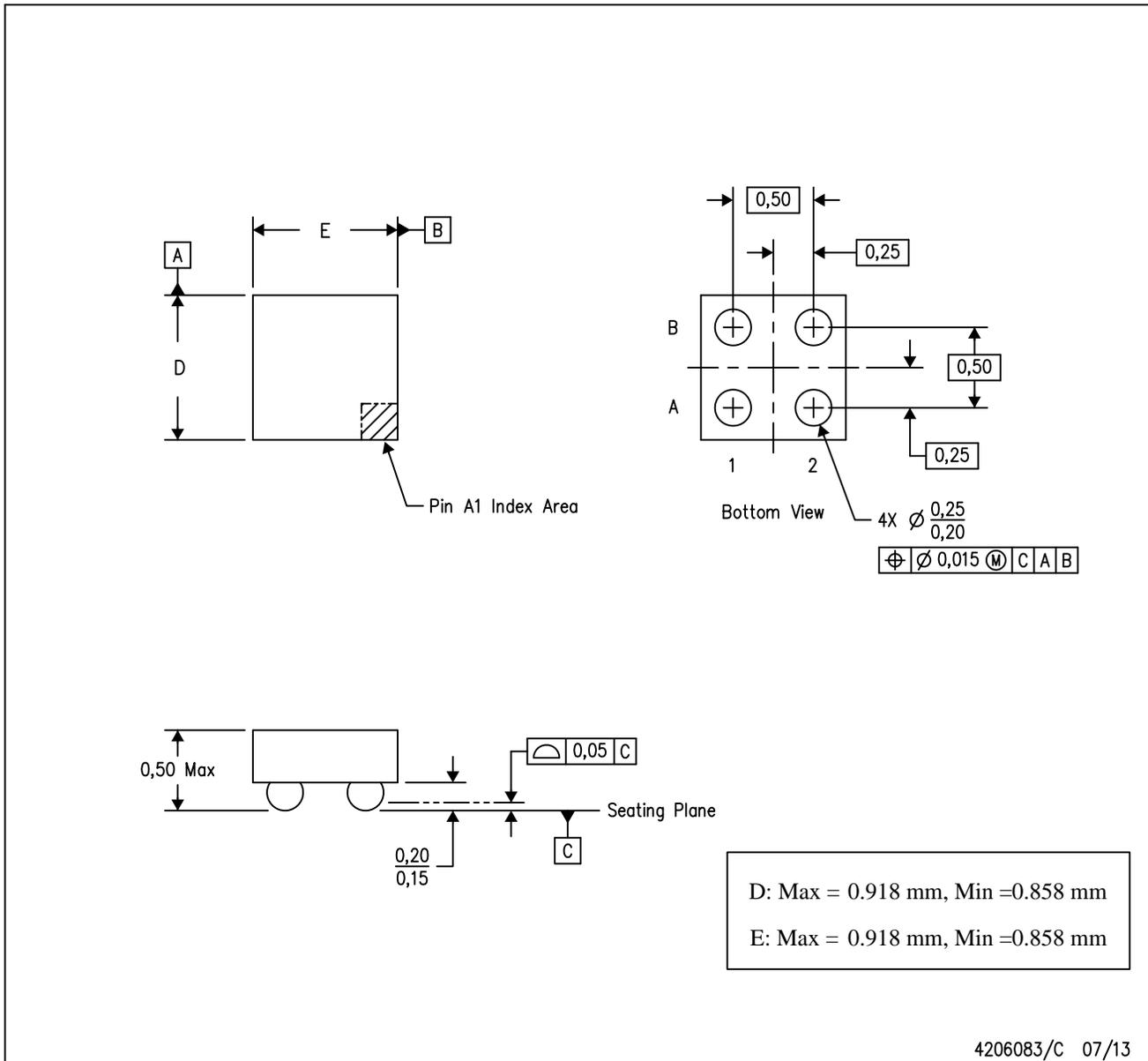
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

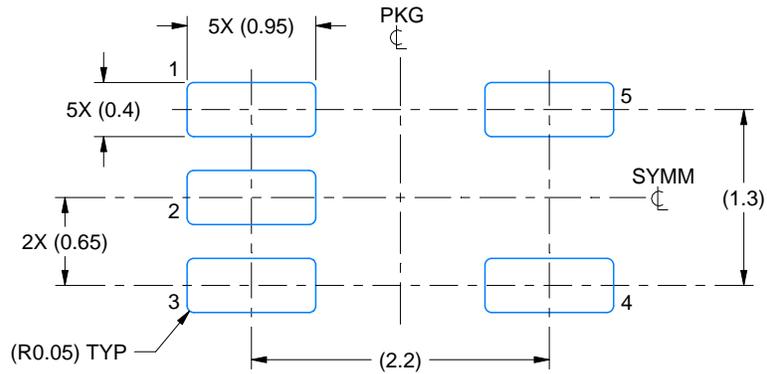
NanoFree is a trademark of Texas Instruments.

EXAMPLE BOARD LAYOUT

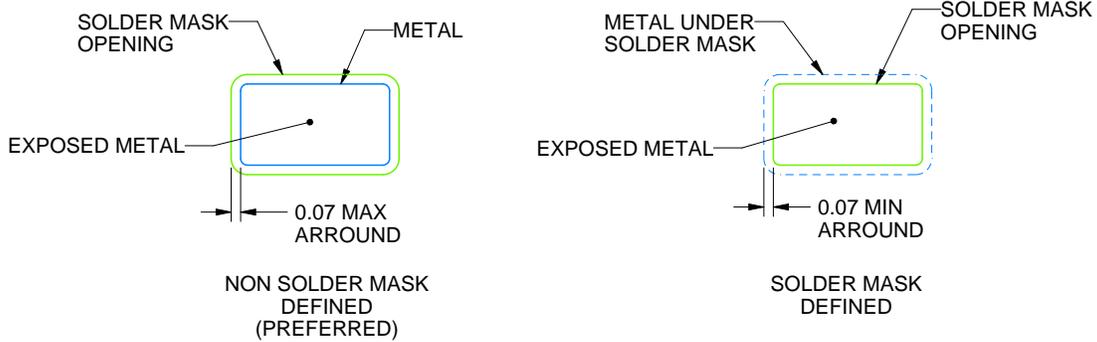
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

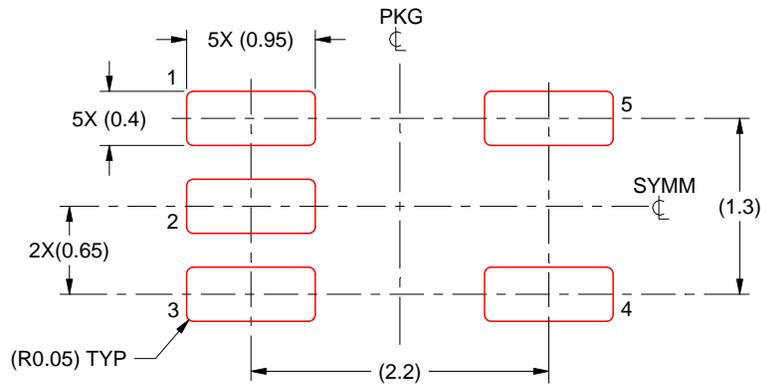
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

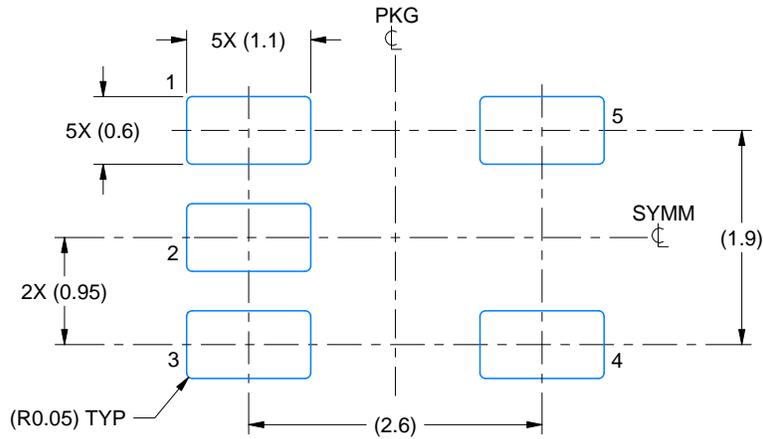
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

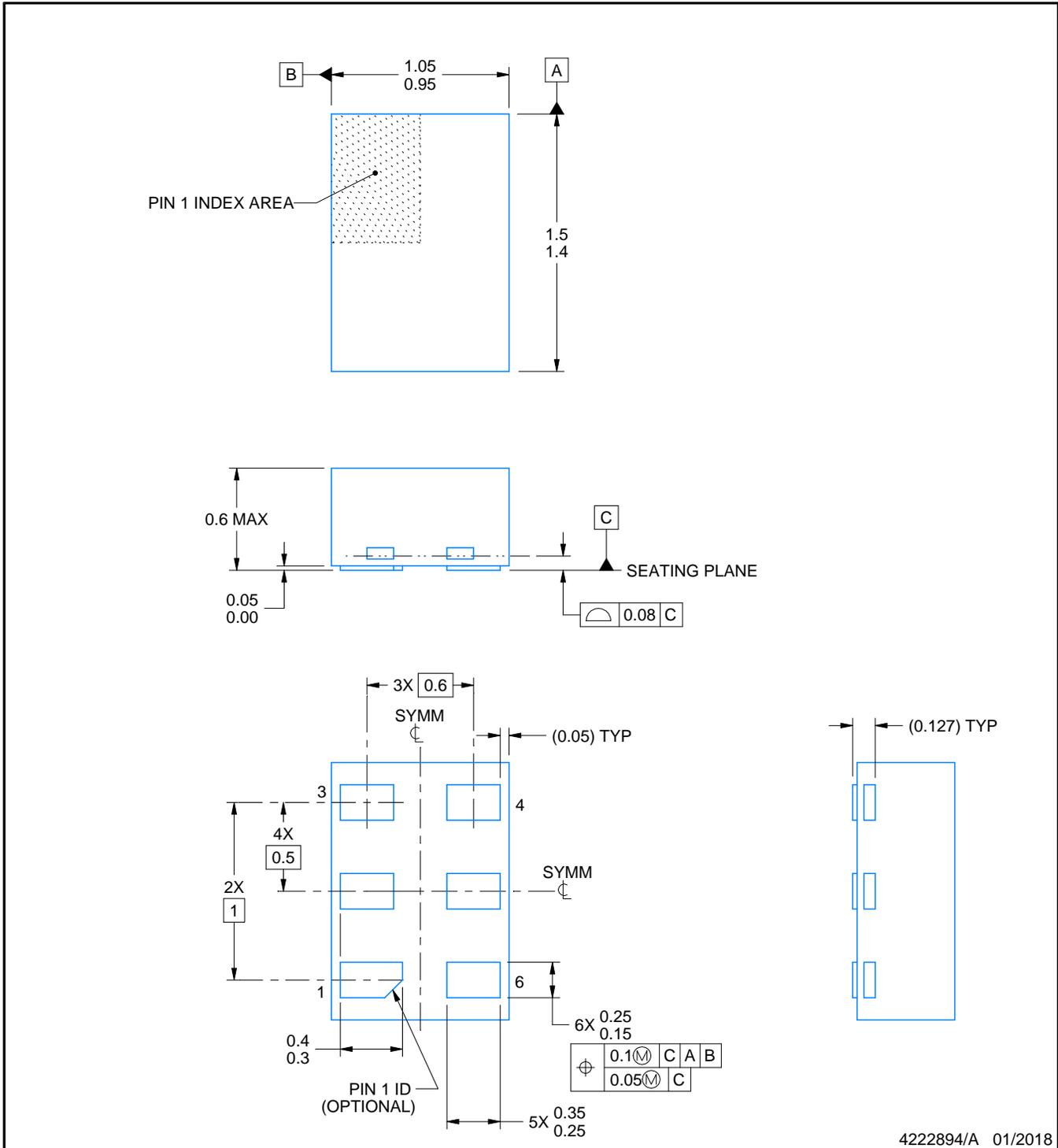
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



4222894/A 01/2018

NOTES:

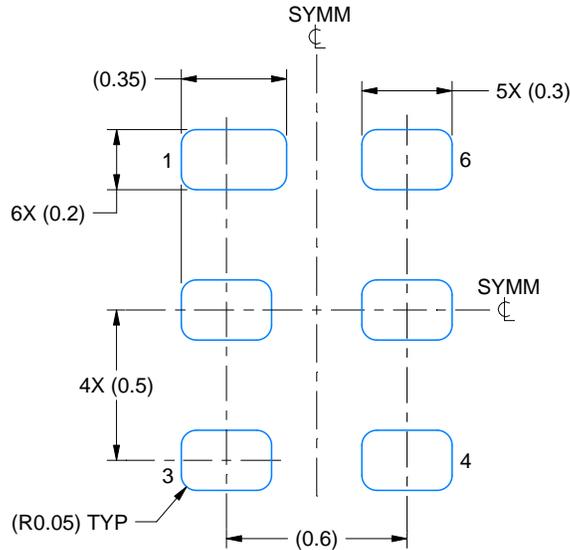
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

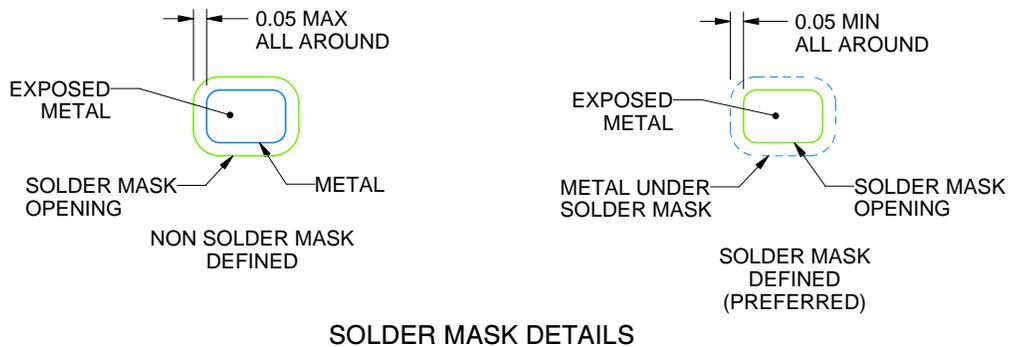
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

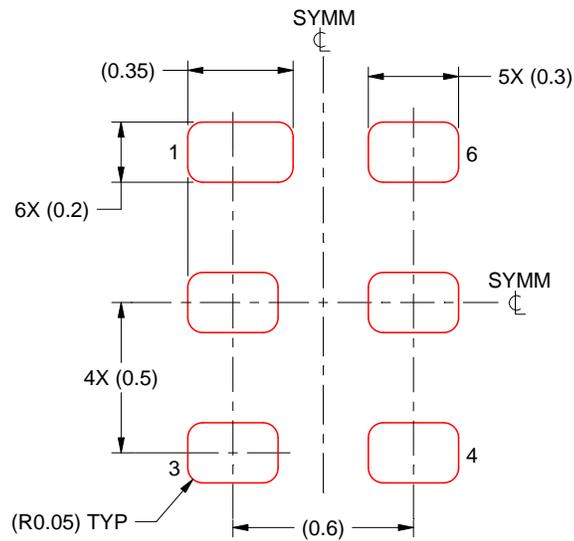
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

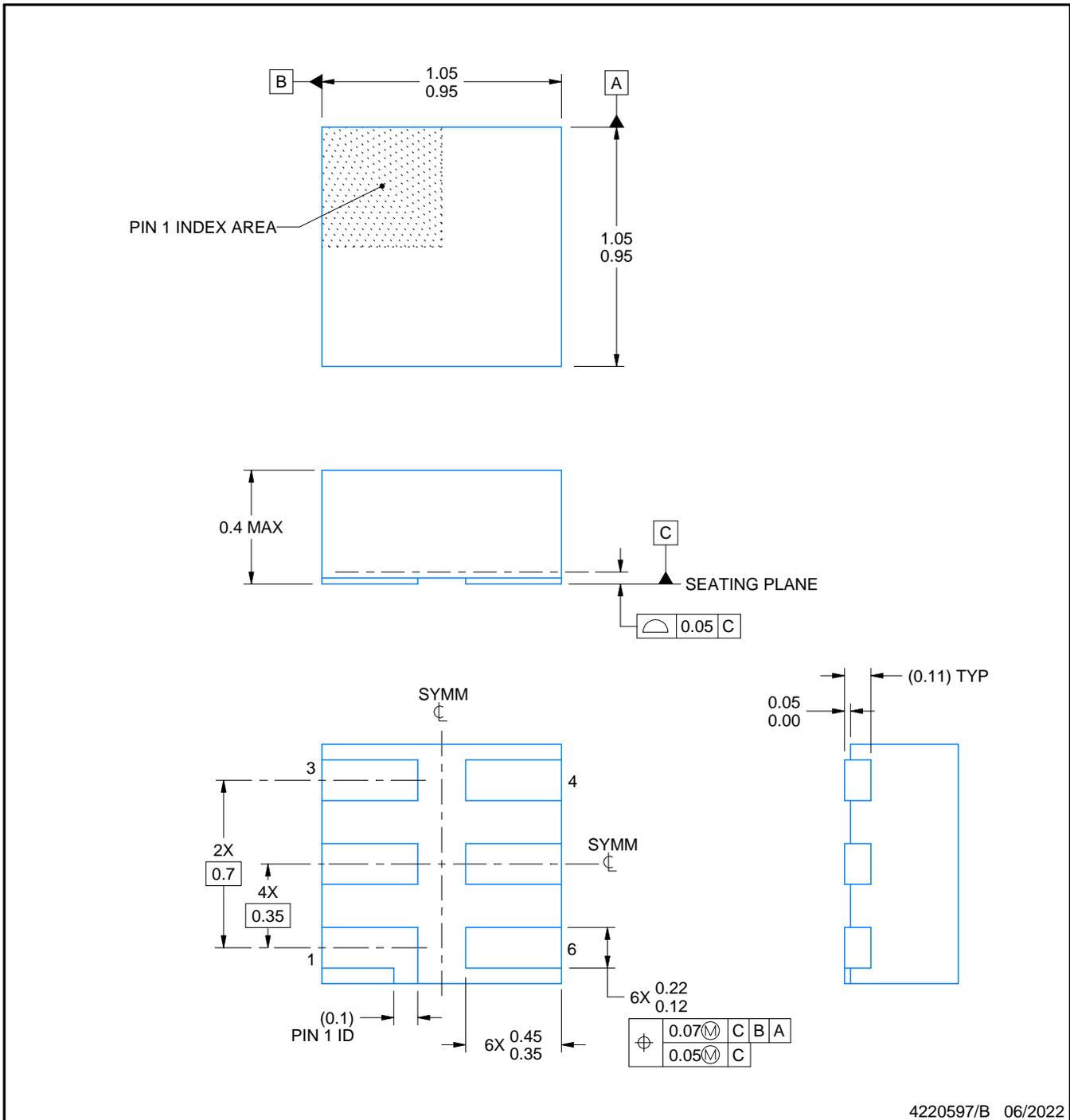


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

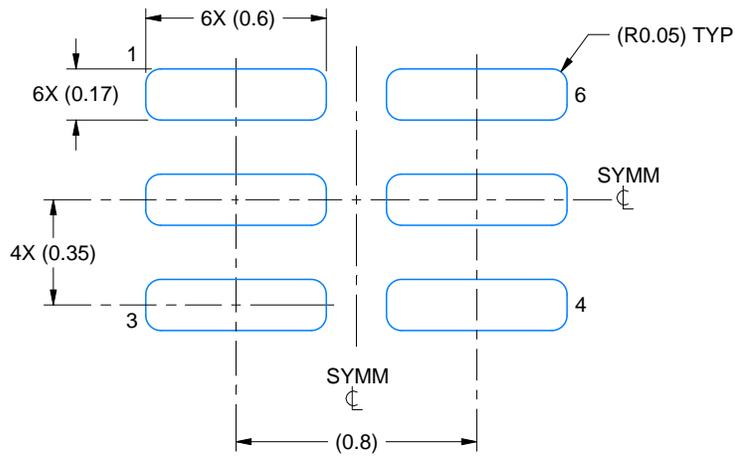
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

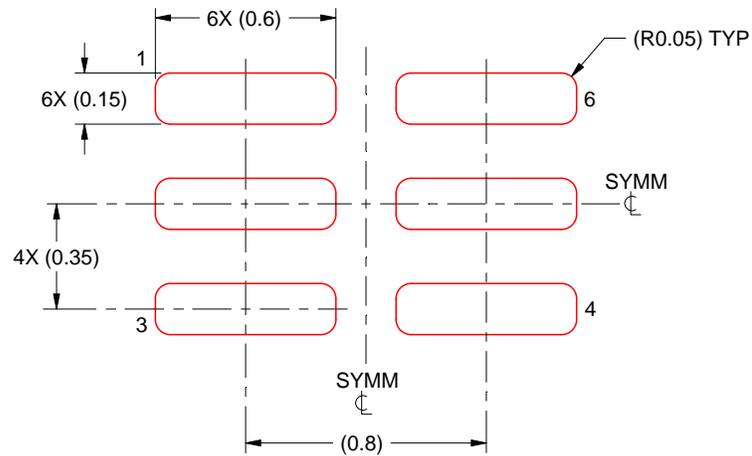
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月