

SNx4LVC08A 四通道双输入正与门

1 特性

- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 1000V 充电器件模型 (C101)
 - 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。
- SN74LVC08A 的工作电压范围为 1.65V 至 3.6V
- SN54LVC08A 的工作电压范围为 2.0V 至 3.6V
- SNx4LVC08A 的额定工作温度范围为 -40°C 至 +85°C 和 -40°C 至 +125°C
- SN54LVC08A 的额定工作温度范围为 -55°C 至 +125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时， t_{pd} 最大值为 4.1ns
- V_{OLP} (输出接地反弹) 典型值 <0.8V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值 >2V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$)

2 应用

- 服务器
- LED 显示屏
- 网络交换机
- I/O 扩展器
- 基站处理器板

3 说明

SN54LVC08A 四通道双输入正与门旨在 2.7V 至 3.6V V_{CC} 下运行，SN74LVC08A 四通道双输入正与门旨在 1.65V 至 3.6V V_{CC} 下运行。

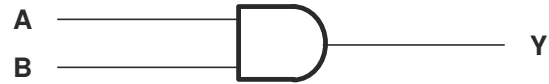
SNx4LVC08A 器件以正逻辑执行布尔函数 $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将该此类器件用作转换器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SNx4LVC08A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5mm × 4.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.50mm × 3.50mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.89mm × 8.89mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55mm × 6.7mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm

- (1) 有关更多信息，请参阅第 11 节。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图，每个逻辑门
(正逻辑)



Table of Contents

1 特性	1	7 Detailed Description	11
2 应用	1	7.1 Overview.....	11
3 说明	1	7.2 Functional Block Diagram.....	11
4 Pin Configuration and Functions	3	7.3 Feature Description.....	11
5 Specifications	5	7.4 Device Functional Modes.....	12
5.1 Absolute Maximum Ratings.....	5	8 Application and Implementation	13
5.2 ESD Ratings.....	5	8.1 Application Information.....	13
5.3 Recommended Operating Conditions, SN54LVC08A.....	5	8.2 Typical Application.....	13
5.4 Recommended Operating Conditions, SN74LVC08A.....	6	8.3 Layout.....	14
5.5 Thermal Information.....	6	9 Device and Documentation Support	16
5.6 Electrical Characteristics, SN54LVC08A.....	7	9.1 Documentation Support (Analog).....	16
5.7 Electrical Characteristics, SN74LVC08A.....	7	9.2 Receiving Notification of Documentation Updates....	16
5.8 Switching Characteristics, SN54LVC08A.....	8	9.3 支持资源.....	16
5.9 Switching Characteristics, SN74LVC08A.....	8	9.4 Trademarks.....	16
5.10 Operating Characteristics.....	8	9.5 静电放电警告.....	16
5.11 Typical Characteristics.....	9	9.6 术语表.....	16
6 Parameter Measurement Information	10	10 Revision History	16
		11 Mechanical, Packaging, and Orderable Information	18

4 Pin Configuration and Functions

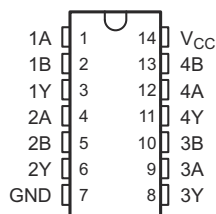


图 4-1. D, DB, NS, J, W, or PW Package 14-Pin SOIC, SSOP, SOP, CDIP, or TSSOP (Top View)

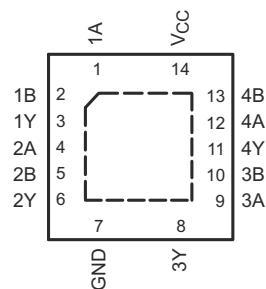


图 4-2. BQA or RGY Package 14-Pin WQFN or VQFN (Top View)

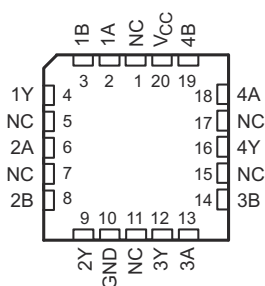


图 4-3. FK Package 20-Pin LCCC (Top View)

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, SSOP, SOP, CDIP, TSSOP, VQFN,WQFN	LCCC		
1A	1	2	I	Channel 1 input A
1B	2	3	I	Channel 1 input B
1Y	3	4	O	Channel 1 output
2A	4	6	I	Channel 2 input A
2B	5	8	I	Channel 2 input B
2Y	6	9	O	Channel 2 output
GND	7	10	Ground	Ground
3Y	8	12	O	Channel 3 output
3A	9	13	I	Channel 3 input A
3B	10	14	I	Channel 3 input B
4Y	11	16	O	Channel 4 output
4A	12	18	I	Channel 4 input A
4B	13	19	I	Channel 4 input B
V _{CC}	14	20	Power	Positive supply
Thermal Information ⁽¹⁾			—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.
NC ⁽²⁾	—	1	—	No connect
		5		
		7		
		11		
		15		
		17		

(1) For BQA package only.

(2) NC – No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		- 0.5	6.5	V
V _I	Input voltage ⁽²⁾		- 0.5	6.5	V
V _O	Output voltage ^{(2) (3)}		- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		- 50	mA
I _{OK}	Output clamp current	V _O < 0		- 50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
P _{tot}	Power dissipation ^{(4) (5)}	T _A = - 40°C to +125°C		500	mW
T _J	Junction temperature		- 65	150	°C
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
	Machine Model (MM) A115-A	200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions, SN54LVC08A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LVC08A		UNIT
			- 55°C to +125°C		
			MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 2.7V to 3.6V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7V to 3.6V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7V		- 12	mA
		V _{CC} = 3V		- 24	
I _{OL}	Low-level output current	V _{CC} = 2.7V		12	mA
		V _{CC} = 3V		24	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	SN54LVC08A		UNIT
	- 55°C to +125°C		
	MIN	MAX	
$\Delta t / \Delta v$ Input transition rise or fall rate	8		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Recommended Operating Conditions, SN74LVC08A

See⁽¹⁾

			SN74LVC08A						UNIT
			T _A = 25°C		– 40°C to +85°C		– 40°C to +125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		1.7		1.7		
		V _{CC} = 2.7V to 3.6V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	0.7		0.7		0.7		
		V _{CC} = 2.7V to 3.6V	0.8		0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V	– 4		– 4		– 4		mA
		V _{CC} = 2.3V	– 8		– 8		– 8		
		V _{CC} = 2.7 V	– 12		– 12		– 12		
		V _{CC} = 3V	– 24		– 24		– 24		
I _{OL}	Low-level output current	V _{CC} = 1.65V	4		4		4		mA
		V _{CC} = 2.3V	8		8		8		
		V _{CC} = 2.7V	12		12		12		
		V _{CC} = 3V	24		24		24		
Δ t/ Δ v	Input transition rise or fall rate		8		8		8		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC08A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (LCCC)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	98.6	112.8	95.1	127.7	51.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.8	56.0	65.3	52.7	56.0	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	53.3	60.2	53.9	69.5	27.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.6	16.4	25.3	17.9	8.9	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.9	53.0	59.6	53.6	68.9	27.7	°C/W

THERMAL METRIC ⁽¹⁾	SN74LVC08A						UNIT
	BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (LCCC)	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	50.1	—	—	—	—	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics, SN54LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC08A			UNIT
			- 55°C to +125°C			
			MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = - 100 μ A	2.7V to 3.6V	V _{CC} - 0.2			V
	I _{OH} = - 12 mA	2.7V	2.2			
		3V	2.4			
		I _{OH} = - 24 mA	3V	2.2		
V _{OL}	I _{OL} = 100 μ A	2.7V to 3.6V	0.2			V
	I _{OL} = 12 mA	2.7V	0.4			
	I _{OL} = 24 mA	3V	0.55			
I _I	V _I = 5.5 V or GND	3.6V	±5			μ A
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	10			μ A
Δ I _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			μ A
C _i	V _I = V _{CC} or GND	3.3V	5			pF

(1) $T_A = 25^\circ C$

5.7 Electrical Characteristics, SN74LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC08A						UNIT	
			T _A = 25°C			- 40°C to +85°C		- 40°C to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = - 100 μ A	1.65V to 3.6V	V _{CC} - 0.2			V _{CC} - 0.2		V _{CC} - 0.3		V
	I _{OH} = - 4 mA	1.65V	1.29			1.2		1.05		
	I _{OH} = - 8 mA	2.3V	1.9			1.7		1.55		
	I _{OH} = - 12 mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
I _{OH} = - 24 mA	3V	2.3			2.2		2			
V _{OL}	I _{OL} = 100 μ A	1.65V to 3.6V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6V	±1			±5		±20		μ A
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	1			10		40		μ A
Δ I _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			500		5000		μ A

SN54LVC08A, SN74LVC08A

ZHCSV61U – JANUARY 1993 – REVISED MARCH 2024

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC08A						UNIT	
			T _A = 25°C			– 40°C to +85°C		– 40°C to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
C _i	V _I = V _{CC} or GND	3.3V	5						pF	

5.8 Switching Characteristics, SN54LVC08A

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

For recommended operating conditions (unless otherwise noted) (see Logic Chart and Timing Waveforms)					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC08A	UNIT
				- 55°C to +125°C	
				MIN MAX	
t _{pd}	A or B	Y	2.7V	4.8	ns
			3.3V ± 0.3V	1 4.1	

5.9 Switching Characteristics, SN74LVC08A

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

SN74LVC08A											
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			– 40°C to +85°C		– 40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.8V ± 0.15V	1	5	9.3	1	9.8	1	11.3	ns
			2.5V ± 0.2V	1	2.9	6.4	1	6.9	1	9	
			2.7V	1	3	4.6	1	4.8	1	6	
			3.3V ± 0.3V	1	2.6	3.9	1	4.1	1	5.5	
t _{sk(o)}			3.3V ± 0.3V					1		1.5	ns

5.10 Operating Characteristics

 T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7	pF
			2.5 V	9.8	
			3.3 V	10	

5.11 Typical Characteristics

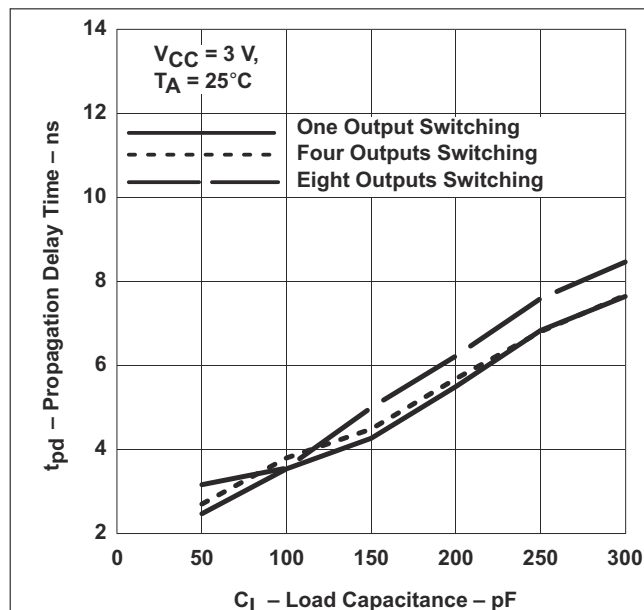


图 5-1. Propagation Delay (Low to High Transition) vs Load Capacitance

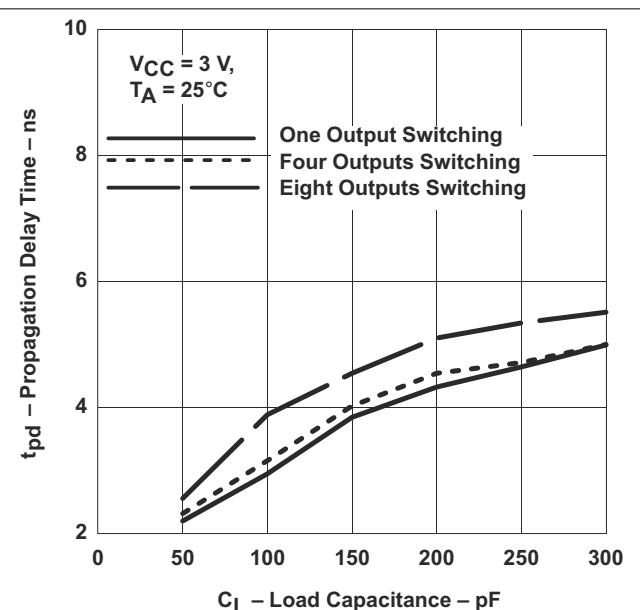
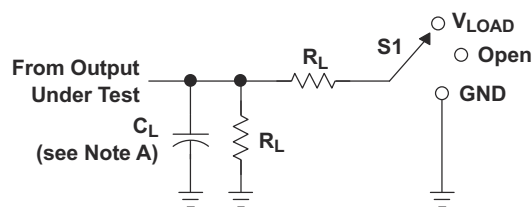


图 5-2. Propagation Delay (High to Low Transition) vs Load Capacitance

6 Parameter Measurement Information

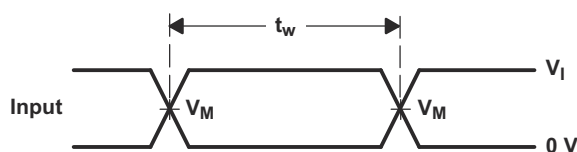
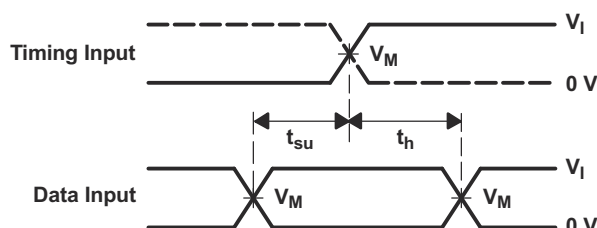
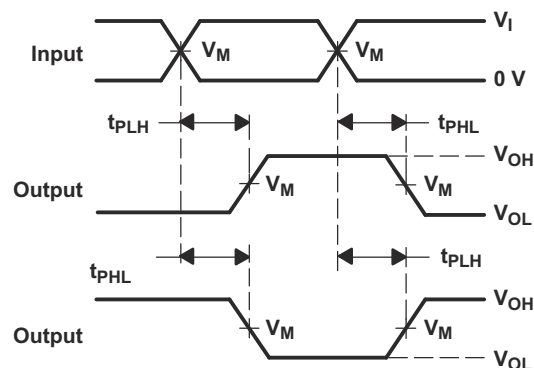
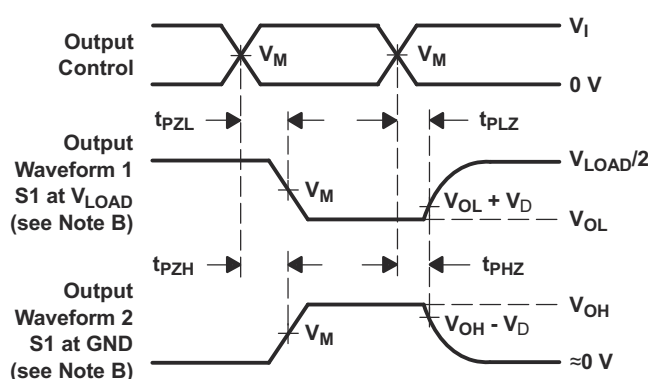
Load Circuit and Voltage Waveforms



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ W}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

7 Detailed Description

7.1 Overview

The SN74LVC08 device contains four 2-input positive AND gate device and performs the Boolean function $Y = A \times B$. This device is useful when multiple AND function is used in the system.

7.2 Functional Block Diagram

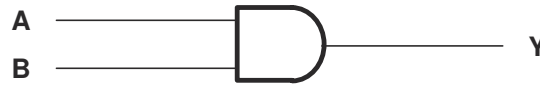


图 7-1. Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the 节 5.1 must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the 节 5.6 and 节 5.7. The worst case resistance is calculated with the maximum input voltage, given in the 节 5.1, and the maximum input leakage current, given in the 节 5.6 and 节 5.7, using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t / \Delta v$ in 节 5.3 and 节 5.4 to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs to this device have negative clamping diodes. The outputs to this device have both positive and negative clamping diodes as shown in 图 7-2.

小心

Voltages beyond the values specified in the 节 5.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

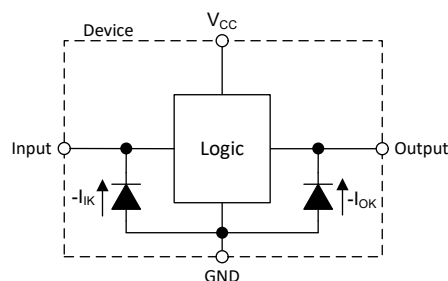


图 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [节 5.1](#).

7.4 Device Functional Modes

[表 7-1](#) lists the functional modes for the SN54LVC08A and SN74LVC08A devices.

表 7-1. Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74LVC08A is used to drive CMOS device and used for implementing AND logic. The LVC family can support current drive of about 24 mA at 3-V V_{CC} . The inputs for SN74LVC08A are 5.5-V tolerant allowing it to translate down to V_{CC} .

8.2 Typical Application

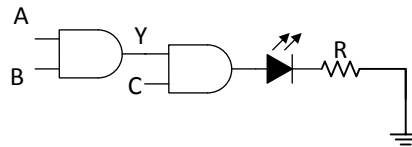


图 8-1. Three Input AND Gate Implementation and Driving LED

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

SN74LVC08A contains four AND gates in one package which can be used for individual AND function or to implement complex Boolean logic. 图 8-1 shows an example of implementing 3input AND function. AB are inputs for AND gate which are connected to another AND gate. $Z = A \times B \times C$. SN74LVC08A support high drive current of 24 mA which can be used to drive LEDs of even Drive low current signal FETs, an example is shown in 图 8-1 TI recommends to use a series resistance to limit the current. If V_{CC} is 3 V, and LED current should be 10 mA, and the forward-voltage of LED is 2.5 V, then R as shown in 图 8-1 is calculated using 方程式 1:

$$R = (V_{CC} - V_{LED}) / I \quad (1)$$

$$R = (3 - 2.5) / 0.01 = 50 \, \Omega$$

8.2.3 Application Curves

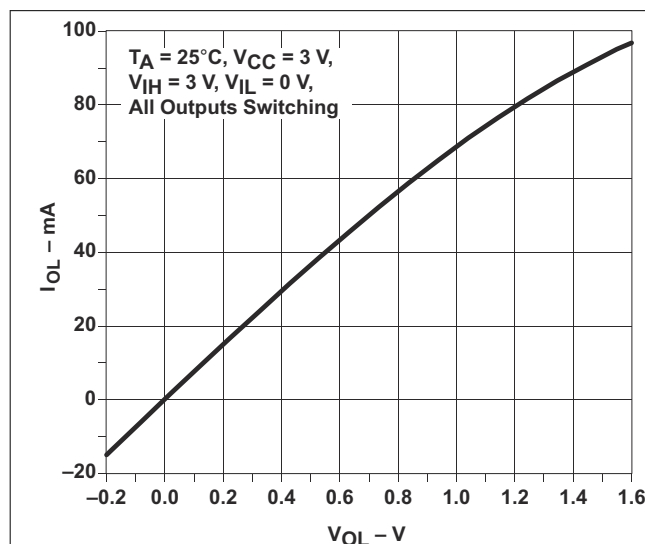


图 8-2. Output Drive Current (I_{OL})
vs LOW-level Output Voltage (V_{OL})

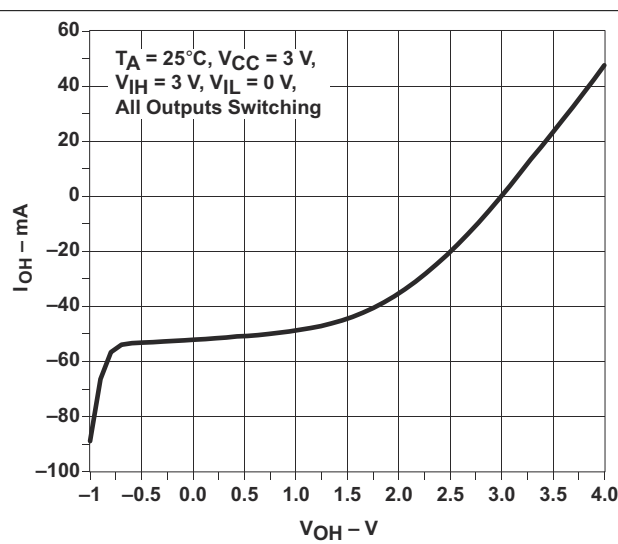


图 8-3. Output Drive Current (I_{OH})
vs HIGH-level Output Voltage (V_{OH})

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1- μ F capacitor. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 8-4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.3.2 Layout Examples

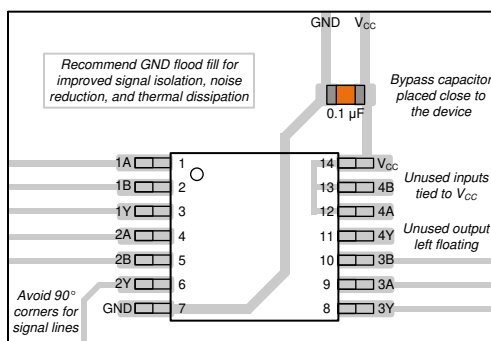


图 8-4. Example Layout

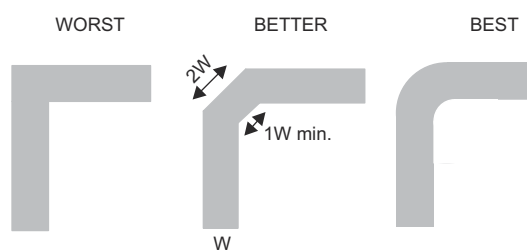


图 8-5. Trace Example

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC08A	Click here	Click here	Click here	Click here	Click here
SN74LVC08A	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.3.1 Community Resources

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision T (July 2019) to Revision U (March 2024)	Page
• 更新了数据表的结构布局.....	1
• 向 <i>器件信息</i> 表中添加了 BQA 封装.....	1
• Added BQA package to <i>Pin Configuration and Functions</i> section.....	3

• Removed Machine Model from <i>Features</i> section and <i>ESD Ratings</i> table.....	5
• Added BQA package to <i>Thermal Information</i> table	6
• Updated <i>Layout Example</i>	15

Changes from Revision S (August 2015) to Revision T (July 2019)	Page
• 更改了“特性”列表的顺序和内容.....	1
• 删除了整个数据表中的 I_{off}	1
• 删除了器件选项表，请参阅数据表末尾的机械、封装和可订购信息	1
• Added $V_O > V_{CC}$ to Output clamp current.....	5
• Changed MAX value for Output clamp current, I_{OK} and Continuous output current, I_O from: – 50 to: ± 50	5
• Changed values in the Thermal Information table to align with JEDEC standards.	6
• Added <i>Balanced High-Drive CMOS Push-Pull Outputs, Standard CMOS Inputs, Clamp Diodes, and Over-voltage Tolerant Inputs</i>	11
• Deleted sentence referencing " I_{off} support....." in the Feature Description section.	11
• Changed Inputs and Output in <i>Truth Table</i>	12
• Added figure: <i>Trace Example</i> in <i>Layout Examples</i>	14
• Added <i>Related Documentation</i> and <i>Receiving Notification of Documentation Updates</i>	16

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9753401Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9753401Q2A SNJ54LVC 08AFK	Samples
5962-9753401QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9753401QC A SNJ54LVC08AJ	Samples
5962-9753401QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9753401QD A SNJ54LVC08AW	Samples
SN74LVC08ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08ADBRE4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08ANSRE4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC08A	Samples
SN74LVC08APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC08APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08APWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC08A	Samples
SN74LVC08ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC08A	Samples
SN74LVC08ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC08A	Samples
SNJ54LVC08AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9753401Q2A SNJ54LVC 08AFK	Samples
SNJ54LVC08AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9753401QC A SNJ54LVC08AJ	Samples
SNJ54LVC08AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9753401QD A SNJ54LVC08AW	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC08A, SN74LVC08A :

- Catalog : [SN74LVC08A](#)
- Automotive : [SN74LVC08A-Q1](#), [SN74LVC08A-Q1](#)
- Enhanced Product : [SN74LVC08A-EP](#), [SN74LVC08A-EP](#)
- Military : [SN54LVC08A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC08ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC08ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC08ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC08ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC08ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC08ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC08ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC08ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC08APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC08APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC08APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC08APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC08ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC08ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC08ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC08ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC08ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC08ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC08ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC08ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC08ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC08APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC08APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC08APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC08APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC08ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

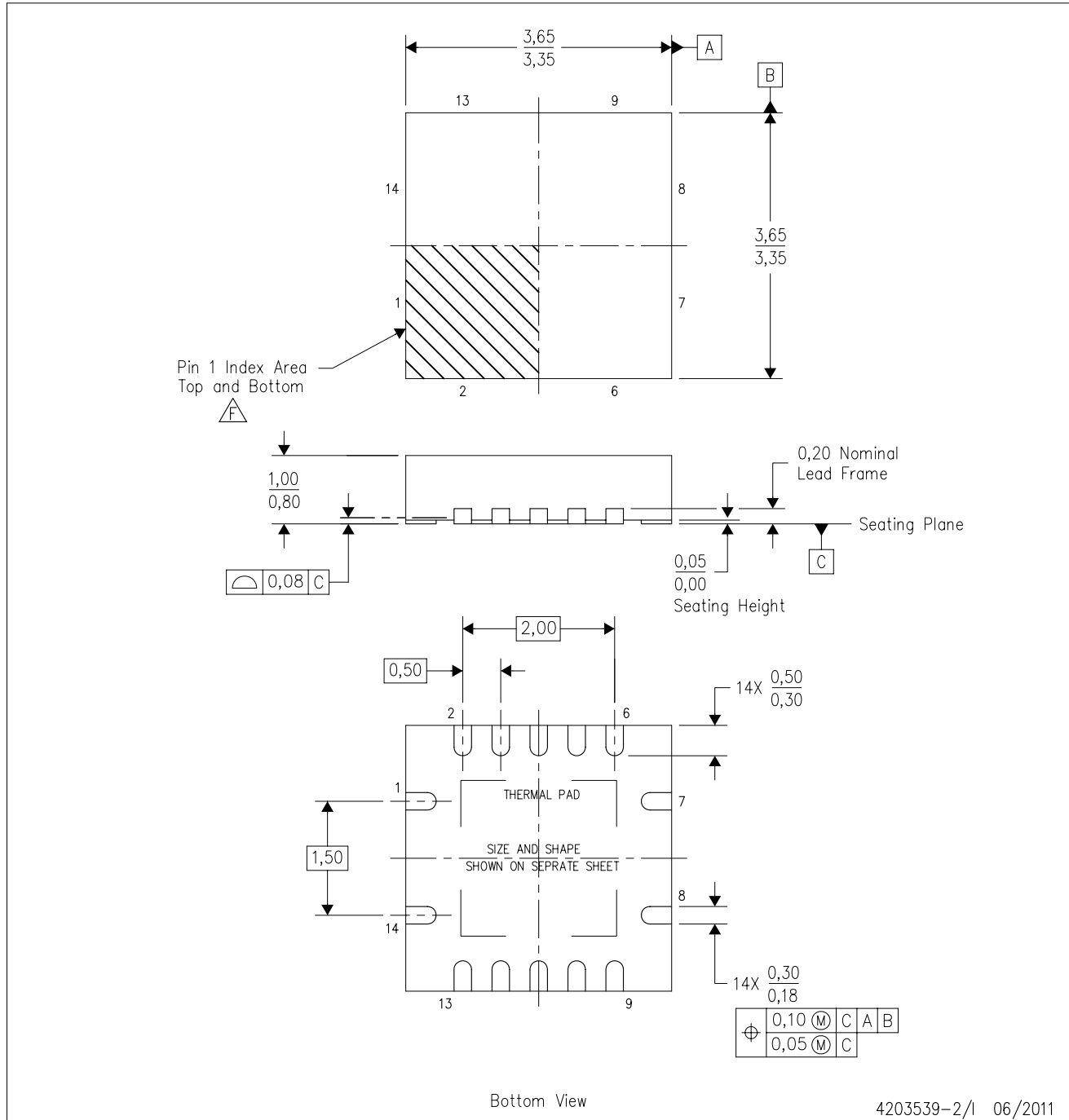
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9753401Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9753401QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC08AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC08ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC08ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC08APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC08APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC08AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC08AW	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

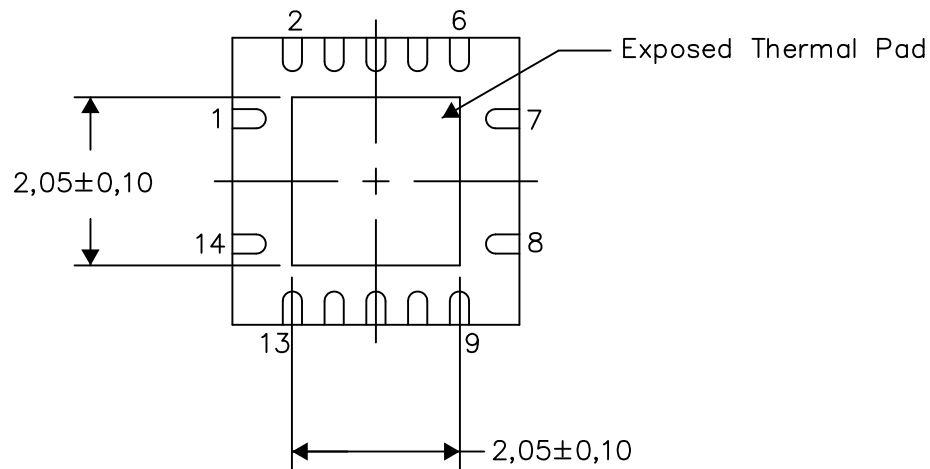
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

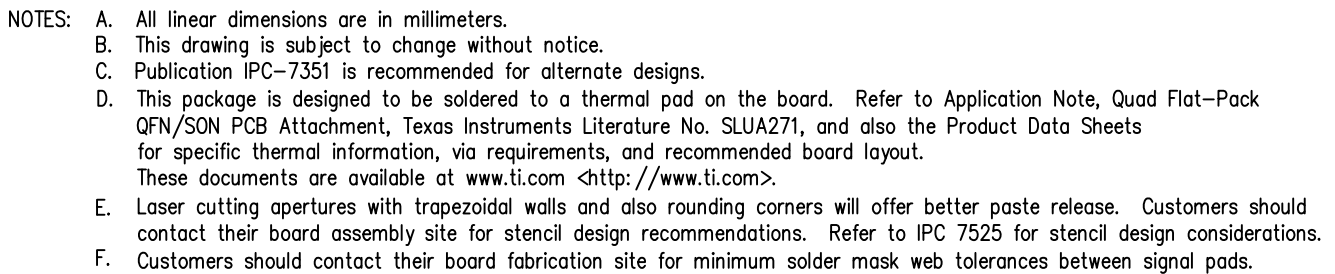


Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters



GENERIC PACKAGE VIEW

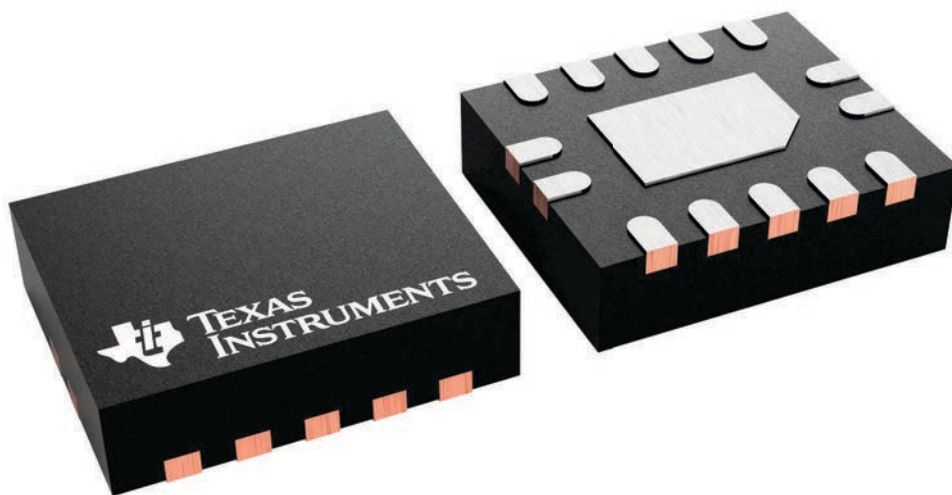
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

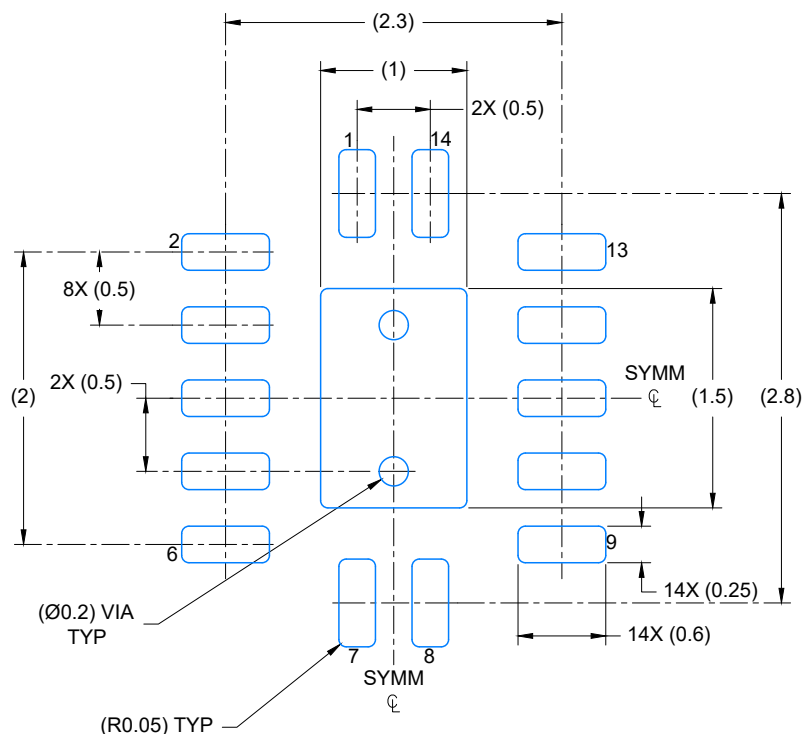


4227145/A

WQFN - 0.8 mm max height

4224636/A 11/2018

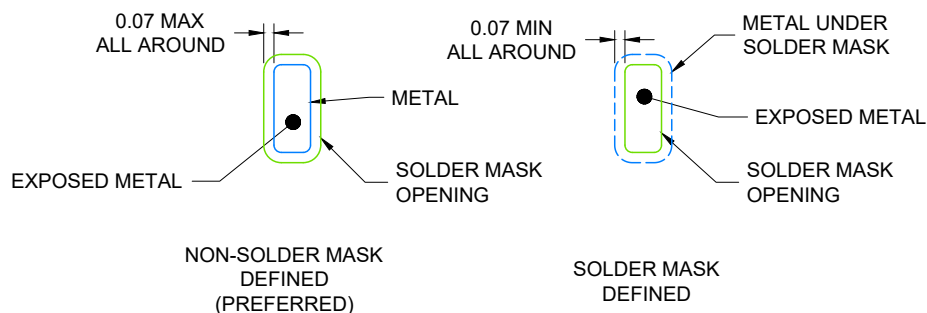
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

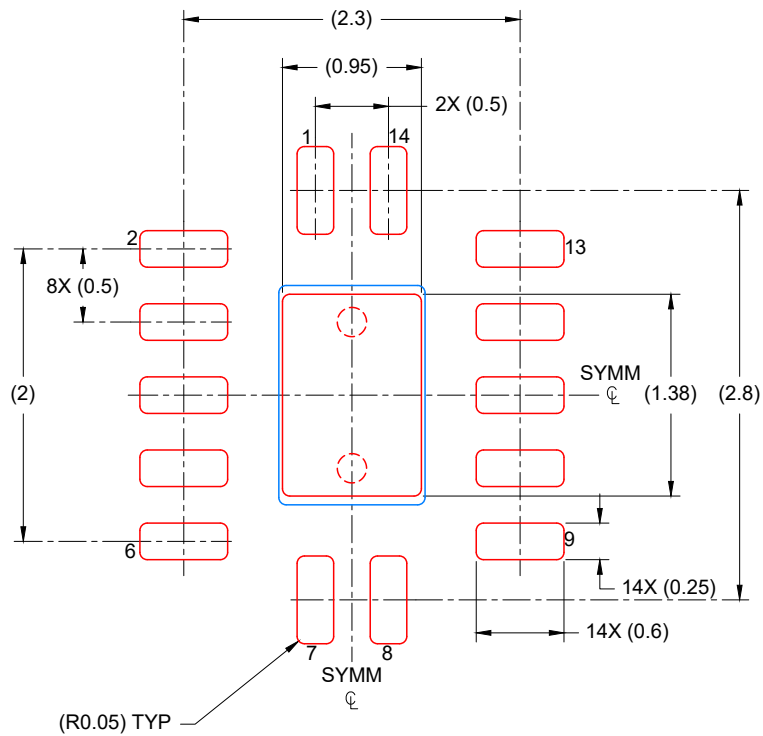
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

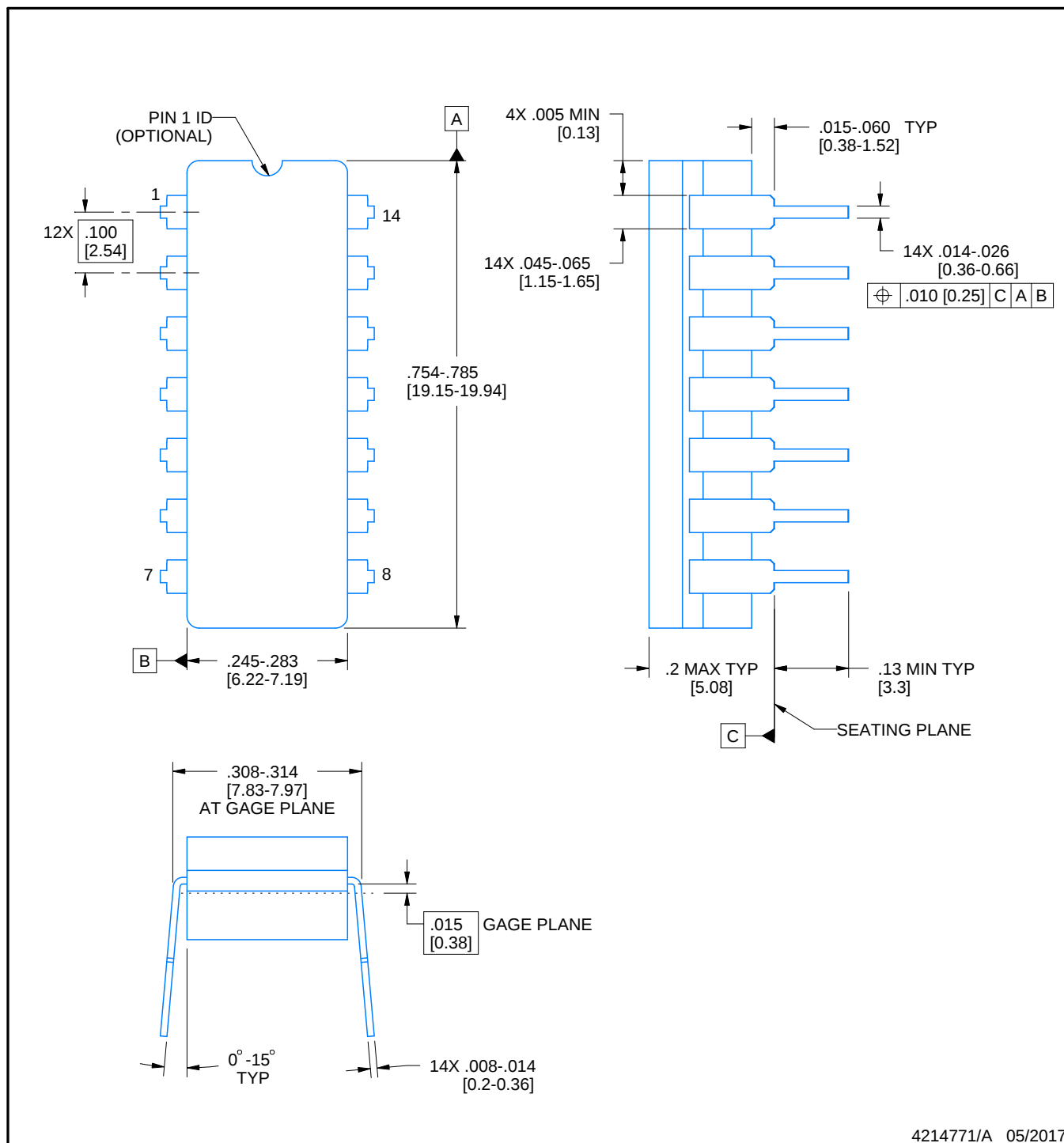


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

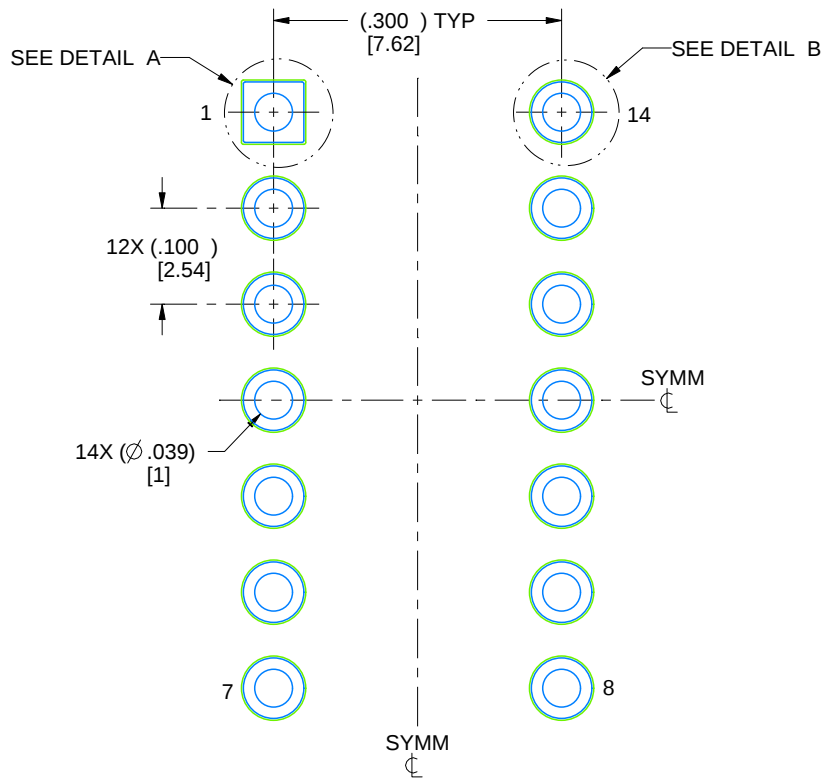
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

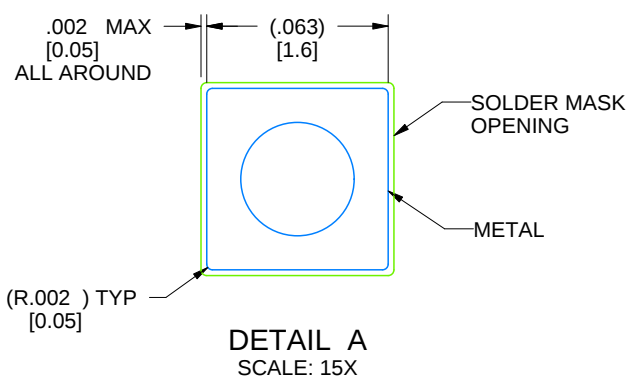
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



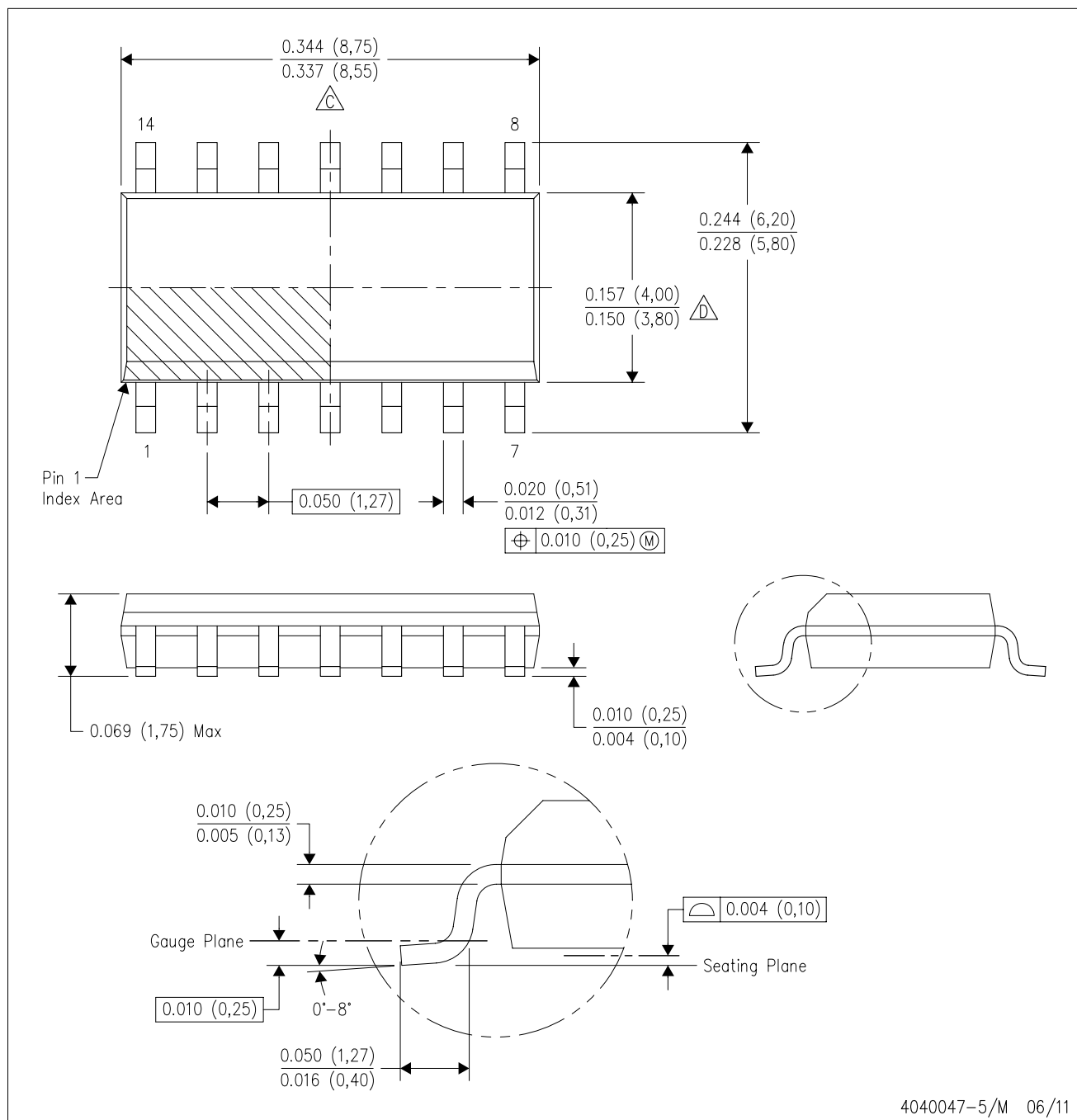
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

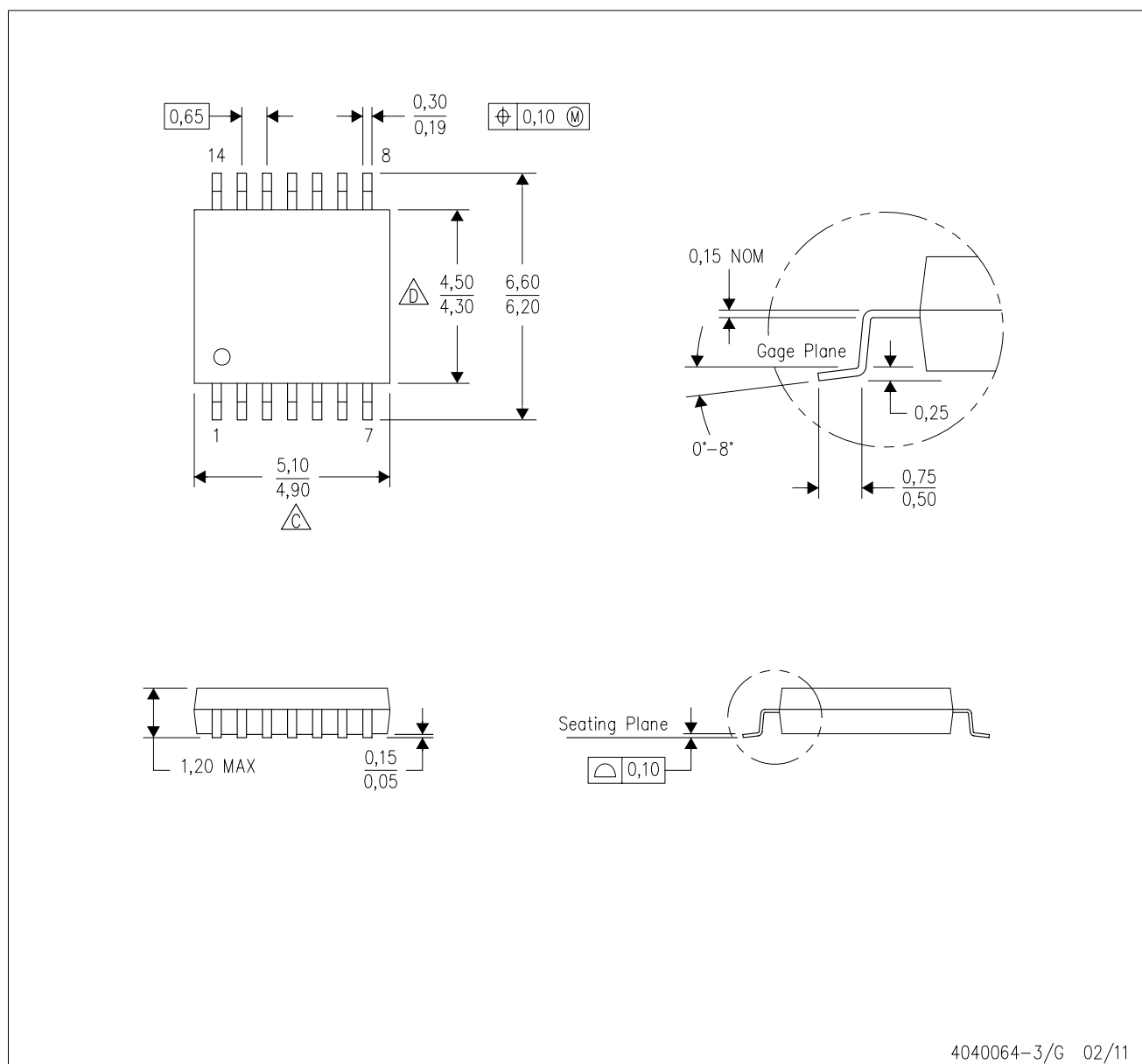
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

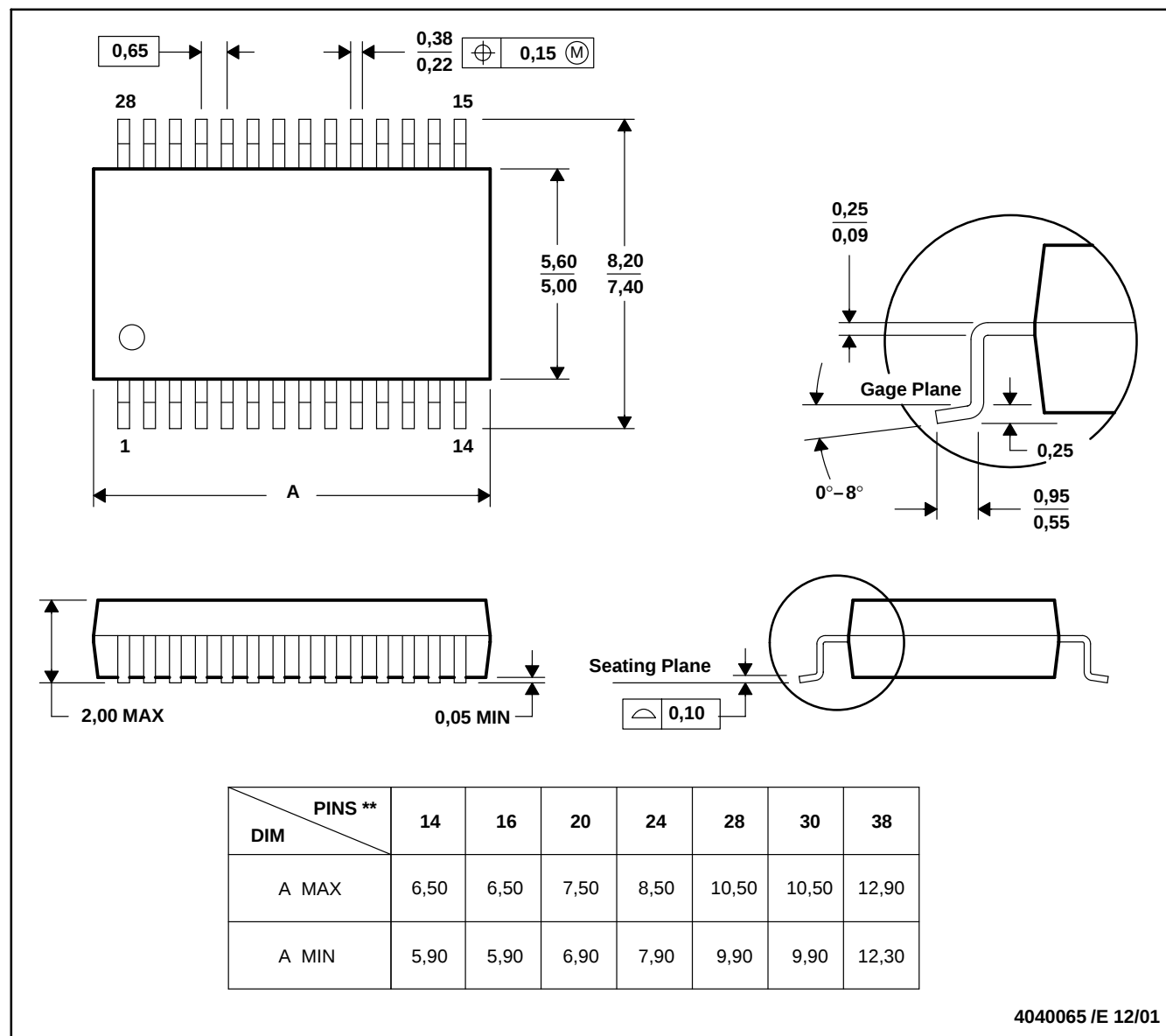


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-150

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