

# SN74LV573A 具有三态输出的八路透明 D 类锁存器

## 1 特性

- $V_{CC}$  工作范围为 2V 至 5.5V
- 电压为 5V 时,  $t_{pd}$  最大值为 8ns
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时,  $V_{OLP}$  (输出接地反弹) 典型值小于 0.8V, 闩锁性能超过 250mA
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时,  $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值大于 2.3V
- 所有端口上均支持混合模式电压运行
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范

## 2 应用

- 缓冲寄存器
  - 双向总线驱动器
  - 工作寄存器
- 连接至其他七个通道

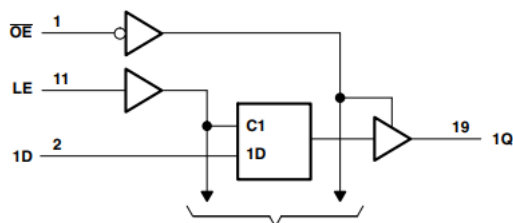
## 3 说明

'LV573A 器件为八路透明 D 类锁存器, 可在 2V 至 5.5V  $V_{CC}$  下运行。

### 封装信息<sup>(1)</sup>

| 器件型号       | 封装              | 封装尺寸 (标称值)       |
|------------|-----------------|------------------|
| SN74LV573A | NS (SO, 20)     | 12.6 mm × 5.3 mm |
|            | DW (SOIC, 20)   | 12.8mm × 7.5mm   |
|            | DB (SSOP, 20)   | 7.2 mm × 5.3 mm  |
|            | PW (TSSOP, 20)  | 6.5mm × 4.4mm    |
|            | DGV (TVSOP, 20) | 5mm × 4.4mm      |
|            | RGY (VQFN, 20)  | 4.5mm × 3.5mm    |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)

## Table of Contents

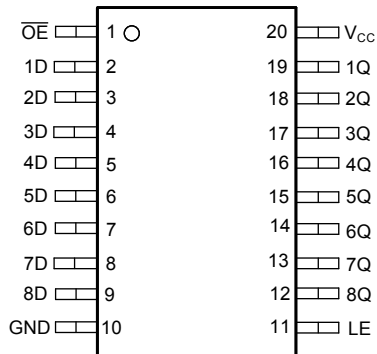
|  |   |  |    |
|--|---|--|----|
| <b>1 特性</b> .....  | 1 | 6.13 Operating Characteristics.....                              | 8  |
| <b>2 应用</b> .....  | 1 | <b>7 Parameter Measurement Information</b> .....                 | 9  |
| <b>3 说明</b> .....  | 1 | <b>8 Detailed Description</b> .....                              | 10 |
| <b>4 Revision History</b> .....                                  | 2 | 8.1 Overview.....  | 10 |
| <b>5 Pin Configuration and Functions</b> .....                   | 3 | 8.2 Functional Block Diagram.....                                | 10 |
| <b>6 Specifications</b> .....                                    | 4 | 8.3 Device Functional Modes.....                                 | 11 |
| 6.1 Absolute Maximum Ratings.....                                | 4 | <b>9 Application and Implementation</b> .....                    | 12 |
| 6.2 ESD Ratings.....   | 4 | 9.1 Power Supply Recommendations.....                            | 12 |
| 6.3 Recommended Operating Conditions.....                        | 4 | 9.2 Layout.....  | 12 |
| 6.4 Thermal Information.....                                     | 5 | <b>10 Device and Documentation Support</b> .....                 | 13 |
| 6.5 Electrical Characteristics.....                              | 5 | 10.1 Documentation Support.....                                  | 13 |
| 6.6 Timing Requirements, $V_{CC} = 2.5 V \pm 0.2 V$ .....        | 6 | 10.2 接收文档更新通知.....   | 13 |
| 6.7 Timing Requirements, $V_{CC} = 3.3 V \pm 0.3 V$ .....        | 6 | 10.3 支持资源.....   | 13 |
| 6.8 Timing Requirements, $V_{CC} = 5 V \pm 0.5 V$ .....          | 6 | 10.4 静电放电警告.....   | 13 |
| 6.9 Switching Characteristics, $V_{CC} = 2.5 V \pm 0.2 V$ .....  | 7 | 10.5 术语表.....  | 13 |
| 6.10 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$ ..... | 7 | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | 13 |
| 6.11 Switching Characteristics, $5 V \pm 0.5 V$ .....            | 8 |  |    |
| 6.12 Noise Characteristics.....                                  | 8 |  |    |

## 4 Revision History

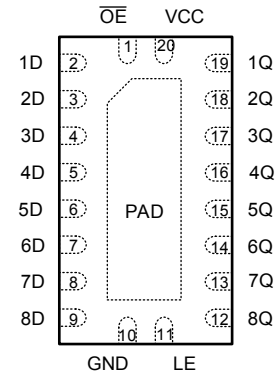
注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (April 2005) to Revision J (March 2023)   | Page |
|---|------|
| • 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....                       | 1    |
| • Updated thermal values for PW package from $R_{\theta JA} = 131.8$ to $128.2$ , all values in $^{\circ}C/W$ ..... | 5    |

## 5 Pin Configuration and Functions



DB, DGV, DW, NS, or PW Packages Top View



RGY Package Top View

表 5-1. Pin Functions

| PIN |                 | I/O <sup>1</sup> | DESCRIPTION        |
|-----|-----------------|------------------|--------------------|
| NO. | NAME            |                  |                    |
| 1   | OE              | I                | Output enable      |
| 2   | 1D              | I                | 1D input           |
| 3   | 2D              | I                | 2D input           |
| 4   | 3D              | I                | 3D input           |
| 5   | 4D              | I                | 4D input           |
| 6   | 5D              | I                | 5D input           |
| 7   | 6D              | I                | 6D input           |
| 8   | 7D              | I                | 7D input           |
| 9   | 8D              | I                | 8D input           |
| 10  | GND             | —                | Ground             |
| 11  | LE              | I                | Latch enable input |
| 12  | 8Q              | O                | 8Q output          |
| 13  | 7Q              | O                | 7Q output          |
| 14  | 6Q              | O                | 6Q output          |
| 15  | 5Q              | O                | 5Q output          |
| 16  | 4Q              | O                | 4Q output          |
| 17  | 3Q              | O                | 3Q output          |
| 18  | 2Q              | O                | 2Q output          |
| 19  | 1Q              | O                | 1Q output          |
| 20  | V <sub>CC</sub> | —                | Power pin          |

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN                                   | MAX                   | UNIT |
|------------------|---|---------------------------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage  | - 0.5                                 | 7                     | V    |
| V <sub>I</sub>   | Input voltage <sup>(1)</sup>  | - 0.5                                 | 7                     | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(1)</sup> | - 0.5                                 | 7                     | V    |
| V <sub>O</sub>   | Output voltage range applied in the high or low state <sup>(1) (2)</sup>                    | - 0.5                                 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>  | V <sub>I</sub> < 0                    | ±20                   | mA   |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>   | V <sub>O</sub> < 0                    | -50                   | mA   |
| I <sub>O</sub>   | Continuous output current   | V <sub>O</sub> = 0 to V <sub>CC</sub> | ±35                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND   |                                       | ±70                   | mA   |
| T <sub>stg</sub> | Storage temperature   | - 65                                  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|                    |                         | VALUE                                      | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-Body Model (A114-A) <sup>(1)</sup>   | ±2000 |
|                    |                         | Charged-Device Model (C101) <sup>(2)</sup> | ±1000 |
|                    |                         | Machine Model (A115-A)                     | ±200  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                           | MIN                              | MAX                   | UNIT            |
|-----------------|---------------------------|----------------------------------|-----------------------|-----------------|
| V <sub>CC</sub> | Supply voltage            | 2                                | 5.5                   | V               |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 2 V            | 1.5                   | V               |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                 |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                 |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                 |
| V <sub>IL</sub> | Low-level input voltage   | V <sub>CC</sub> = 2 V            | 0.5                   | V               |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 |                 |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 |                 |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 |                 |
| V <sub>I</sub>  | Input voltage             | 0                                | 5.5                   | V               |
| V <sub>O</sub>  | Output voltage            | High or low state                | 0                     | V <sub>CC</sub> |
|                 |                           | 3-state                          | 0                     | 5.5             |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 2 V            | - 50                  | ns              |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V | - 2                   |                 |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V   | - 8                   |                 |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V | - 16                  |                 |

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | MIN                              | MAX | UNIT |
|-----------------|------------------------------------|----------------------------------|-----|------|
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            | 50  | ns   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | 2   |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 8   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 16  |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V | 200 | ns   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 100 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 20  |      |
| T <sub>A</sub>  | Operating free-air temperature     | - 40                             | 85  | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application report (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC   |   | SN74LV573A  |           |           |         |            |            | UNIT |
|------------------|---|-------------|-----------|-----------|---------|------------|------------|------|
|                  |   | DGV (TVSOP) | DW (SOIC) | DB (SSOP) | NS (SO) | PW (TSSOP) | RGY (VQFN) |      |
|                  |   | 20 PINS     | 20 PINS   | 20 PINS   | 20 PINS | 20 PINS    | 20 PINS    |      |
| R <sub>θJA</sub> | Junction-to-ambient thermal resistance <sup>(1)</sup> | 92          | 109.1     | 122.7     | 84.6    | 128.2      | 37         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS   | V <sub>CC</sub> | MIN                   | TYP | MAX  | UNIT |
|------------------|---|-----------------|-----------------------|-----|------|------|
| V <sub>OH</sub>  | I <sub>OH</sub> = -50 μA                                    | 2 V to 5.5 V    | V <sub>CC</sub> - 0.1 |     |      | V    |
|                  | I <sub>OH</sub> = -2 mA                                     | 2.3 V           | 2                     |     |      |      |
|                  | I <sub>OH</sub> = -8 mA                                     | 3 V             | 2.48                  |     |      |      |
|                  | I <sub>OH</sub> = -16 mA                                    | 4.5 V           | 3.8                   |     |      |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA                                     | 2 V to 5.5 V    |                       |     | 0.1  | V    |
|                  | I <sub>OL</sub> = 2 mA                                      | 2.3 V           |                       |     | 0.4  |      |
|                  | I <sub>OL</sub> = 8 mA                                      | 3 V             |                       |     | 0.44 |      |
|                  | I <sub>OL</sub> = 16 mA                                     | 4.5 V           |                       |     | 0.55 |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      |                       |     | ± 1  | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |     | ±5   | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 20   | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               |                       |     | 5    | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V           |                       | 1.8 |      | pF   |

### 6.6 Timing Requirements, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

| PARAMETER |                | TEST CONDITIONS  | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|-----------|----------------|------------------|--------------------------|-----|-----|-----|------|
|           |                |                  | MIN                      | MAX |     |     |      |
| $t_w$     | Pulse duration | LE high          | 5                        |     | 5   |     | ns   |
| $t_{su}$  | Setup time     | Data before LE ↓ | 3.5                      |     | 3.5 |     | ns   |
| $t_h$     | Hold time      | Data after LE ↓  | 1.5                      |     | 1.5 |     | ns   |

### 6.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

| PARAMETER |                | TEST CONDITIONS  | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|-----------|----------------|------------------|--------------------------|-----|-----|-----|------|
|           |                |                  | MIN                      | MAX |     |     |      |
| $t_w$     | Pulse duration | LE high          | 5                        |     | 5   |     | ns   |
| $t_{su}$  | Setup time     | Data before LE ↓ | 3.5                      |     | 3.5 |     | ns   |
| $t_h$     | Hold time      | Data after LE ↓  | 1.5                      |     | 1.5 |     | ns   |

### 6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

| PARAMETER |                | TEST CONDITIONS  | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|-----------|----------------|------------------|--------------------------|-----|-----|-----|------|
|           |                |                  | MIN                      | MAX |     |     |      |
| $t_w$     | Pulse duration | LE high          | 5                        |     | 5   |     | ns   |
| $t_{su}$  | Setup time     | Data before LE ↓ | 3.5                      |     | 3.5 |     | ns   |
| $t_h$     | Hold time      | Data after LE ↓  | 1.5                      |     | 1.5 |     | ns   |

### 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted; see [Load Circuit and Voltage Waveforms](#))

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                  |                   | SN74LV573A |     | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------------------|-------------------|------------|-----|------|
|             |                 |             |                      | MIN                      | TYP              | MAX               | MIN        | MAX |      |
| $t_{pd}$    | D               | Q           | $C_L = 15\text{ pF}$ |                          | 8.9 <sup>1</sup> | 15.8 <sup>1</sup> | 1          | 18  | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 9.6 <sup>1</sup> | 16.2 <sup>1</sup> | 1          | 19  |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 9.3 <sup>1</sup> | 16.2 <sup>1</sup> | 1          | 19  |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 6.7 <sup>1</sup> | 12.6 <sup>1</sup> | 1          | 15  |      |
| $t_{pd}$    | D               | Q           | $C_L = 50\text{ pF}$ |                          | 10.9             | 18.7              | 1          | 21  | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 11.6             | 19.1              | 1          | 23  |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 11.4             | 19                | 1          | 22  |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 8.6              | 17.3              | 1          | 19  |      |
| $t_{sk(o)}$ |                 |             |                      |                          |                  |                   | 2          | 2   |      |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted; see [Load Circuit and Voltage Waveforms](#))

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                  |                   | SN74LV573A |      | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------------------|-------------------|------------|------|------|
|             |                 |             |                      | MIN                      | TYP              | MAX               | MIN        | MAX  |      |
| $t_{pd}$    | D               | Q           | $C_L = 15\text{ pF}$ |                          | 6.2 <sup>1</sup> | 11 <sup>1</sup>   | 1          | 13   | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 6.8 <sup>1</sup> | 11.9 <sup>1</sup> | 1          | 14   |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 6.6 <sup>1</sup> | 11.5 <sup>1</sup> | 1          | 13.5 |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 4.9 <sup>1</sup> | 11 <sup>1</sup>   | 1          | 13   |      |
| $t_{pd}$    | D               | Q           | $C_L = 50\text{ pF}$ |                          | 7.7              | 14.5              | 1          | 16.5 | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 8.2              | 15.4              | 1          | 17.5 |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 8                | 15                | 1          | 17   |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 6.2              | 14.5              | 1          | 16.5 |      |
| $t_{sk(o)}$ |                 |             |                      |                          |                  |                   | 1.5        | 1.5  |      |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.11 Switching Characteristics, 5 V ± 0.5 V

over operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted; see [Load Circuit and Voltage Waveforms](#))

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |                  |                  | SN74LV573A |     | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------------------|------------------|------------|-----|------|
|             |                 |             |                      | MIN                      | TYP              | MAX              | MIN        | MAX |      |
| $t_{pd}$    | D               | Q           | $C_L = 15\text{ pF}$ |                          | 4.3 <sup>1</sup> | 6.8 <sup>1</sup> | 1          | 8   | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 4.7 <sup>1</sup> | 7.7 <sup>1</sup> | 1          | 9   |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 4.7 <sup>1</sup> | 7.7 <sup>1</sup> | 1          | 9   |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 3.5 <sup>1</sup> | 7.7 <sup>1</sup> | 1          | 9   |      |
| $t_{pd}$    | D               | Q           | $C_L = 50\text{ pF}$ |                          | 5.3              | 8.8              | 1          | 10  | ns   |
| $t_{pd}$    | LE              | Q           |                      |                          | 5.7              | 9.7              | 1          | 11  |      |
| $t_{en}$    | $\overline{OE}$ | Q           |                      |                          | 5.7              | 9.7              | 1          | 11  |      |
| $t_{dis}$   | $\overline{OE}$ | Q           |                      |                          | 4.2              | 9.7              | 1          | 11  |      |
| $t_{sk(o)}$ |                 |             |                      |                          |                  |                  | 1          | 1   |      |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

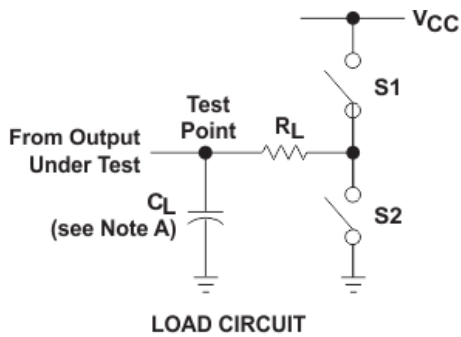
| PARAMETER   |  | SN74LV573A |      |      | UNIT |
|-------------|--|------------|------|------|------|
|             |  | MIN        | TYP  | MAX  |      |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |            | 0.6  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |            | -0.5 | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |            | 2.9  |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31       |      |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |            |      | 0.99 | V    |

## 6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                               |                 |         | TEST CONDITIONS                            | $V_{CC}$ | TYP  | UNIT |
|-----------|-------------------------------|-----------------|---------|--|----------|------|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled | D to Q  | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 16   | pF   |
|           |                               |                 |         |  | 5 V      | 18   |      |
|           |                               |                 | LE to Q |  | 3.3 V    | 18.2 |      |
|           |                               |                 |         |  | 5 V      | 21.3 |      |

## 7 Parameter Measurement Information



| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |

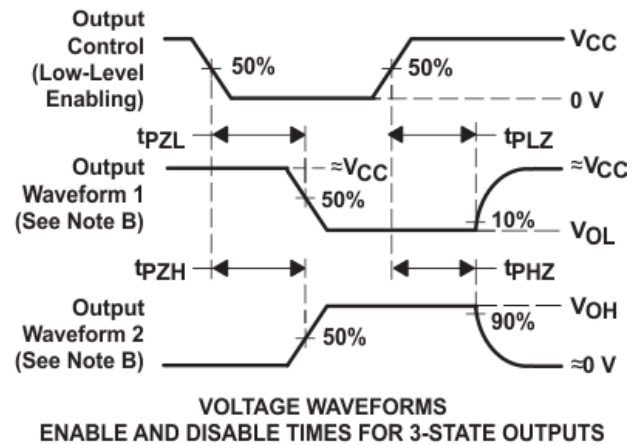
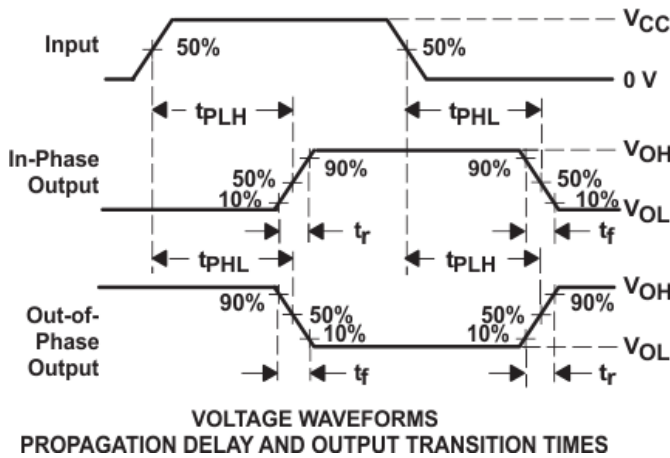
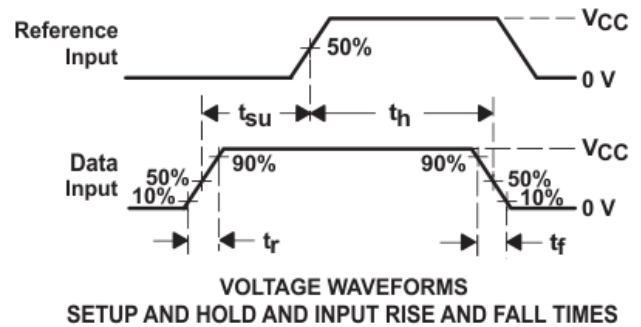
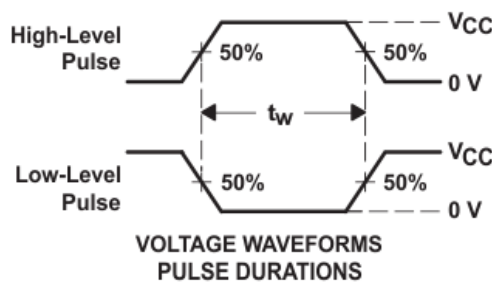


图 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The 'LV573A devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram

To seven other channels

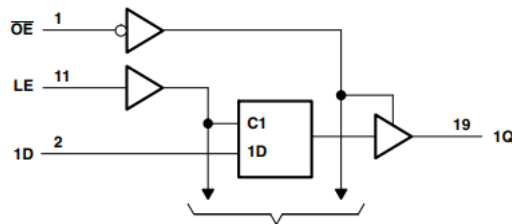


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV573A.

**表 8-1. Function Table (Each Latch)**

| INPUTS |    |   | OUTPUT         |
|--------|----|---|----------------|
| OE     | LE | D | Q              |
| L      | H  | H | H              |
| L      | H  | L | L              |
| L      | L  | X | Q <sub>0</sub> |
| H      | X  | X | Z              |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [§ 6.3](#) table. The total current through Ground or  $V_{CC}$  must not exceed  $\pm 70$  mA as per [§ 6.1](#) table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  pins, then TI recommends 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- $\mu$ F and 1- $\mu$ F capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

### 9.2 Layout

#### 9.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Layout Diagram](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

##### 9.2.1.1 Layout Example

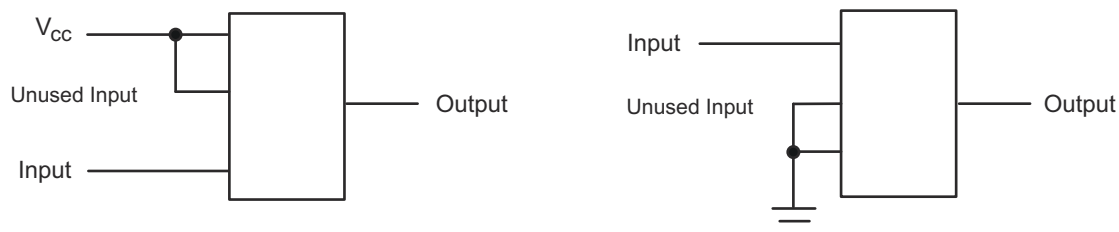


图 9-1. Layout Diagram

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 10-1. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV573A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

#### 10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 10.3 支持资源

**TI E2E™ 支持论坛**是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

#### Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 10.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LV573ADBR</a>  | NRND          | Production           | SSOP (DB)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573ADBR.A                | NRND          | Production           | SSOP (DB)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573ADBRG4                | NRND          | Production           | SSOP (DB)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| <a href="#">SN74LV573ADGVR</a> | NRND          | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573ADGVR.A               | NRND          | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| <a href="#">SN74LV573ADW</a>   | Obsolete      | Production           | SOIC (DW)   20   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV573A              |
| <a href="#">SN74LV573ADWR</a>  | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573ADWR.A                | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| <a href="#">SN74LV573ANSR</a>  | Active        | Production           | SOP (NS)   20    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV573A            |
| SN74LV573ANSR.A                | Active        | Production           | SOP (NS)   20    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV573A            |
| <a href="#">SN74LV573APW</a>   | Obsolete      | Production           | TSSOP (PW)   20  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV573A              |
| <a href="#">SN74LV573APWR</a>  | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573APWR.A                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| SN74LV573APWRG4                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV573A              |
| <a href="#">SN74LV573ARGYR</a> | NRND          | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | LV573A              |
| SN74LV573ARGYR.A               | NRND          | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | LV573A              |
| SN74LV573ARGYRG4               | NRND          | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | LV573A              |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV573ADBR  | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV573ADGVR | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV573ADWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LV573ANSR  | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LV573APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LV573ARGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.71    | 4.71    | 1.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV573ADBR  | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV573ADGVR | TVSOP        | DGV             | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV573ADWR  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74LV573ANSR  | SOP          | NS              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74LV573APWR  | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV573ARGYR | VQFN         | RGY             | 20   | 3000 | 353.0       | 353.0      | 32.0        |

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

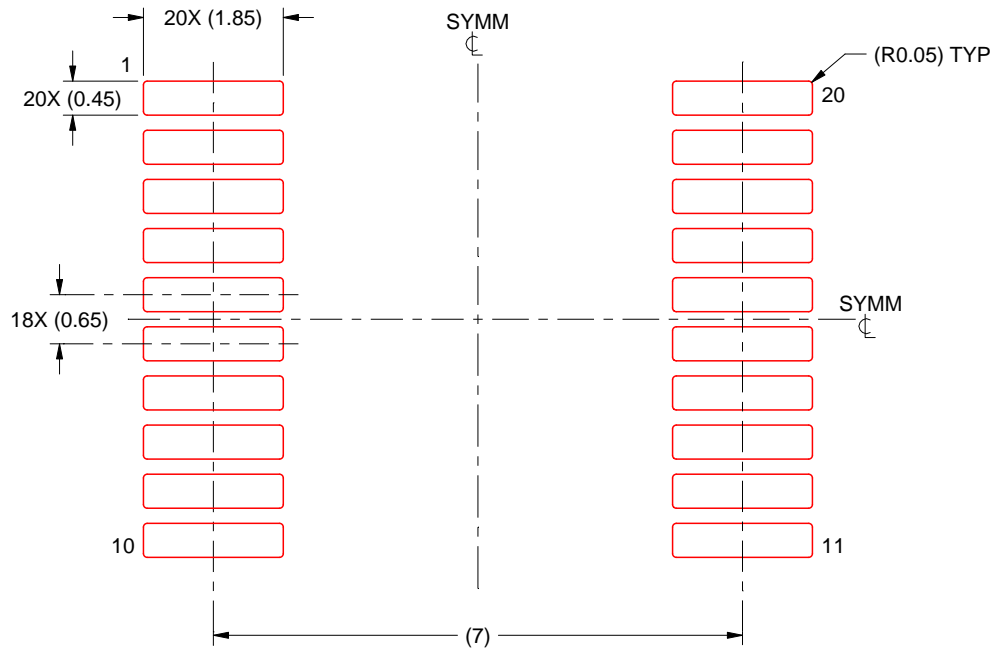
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

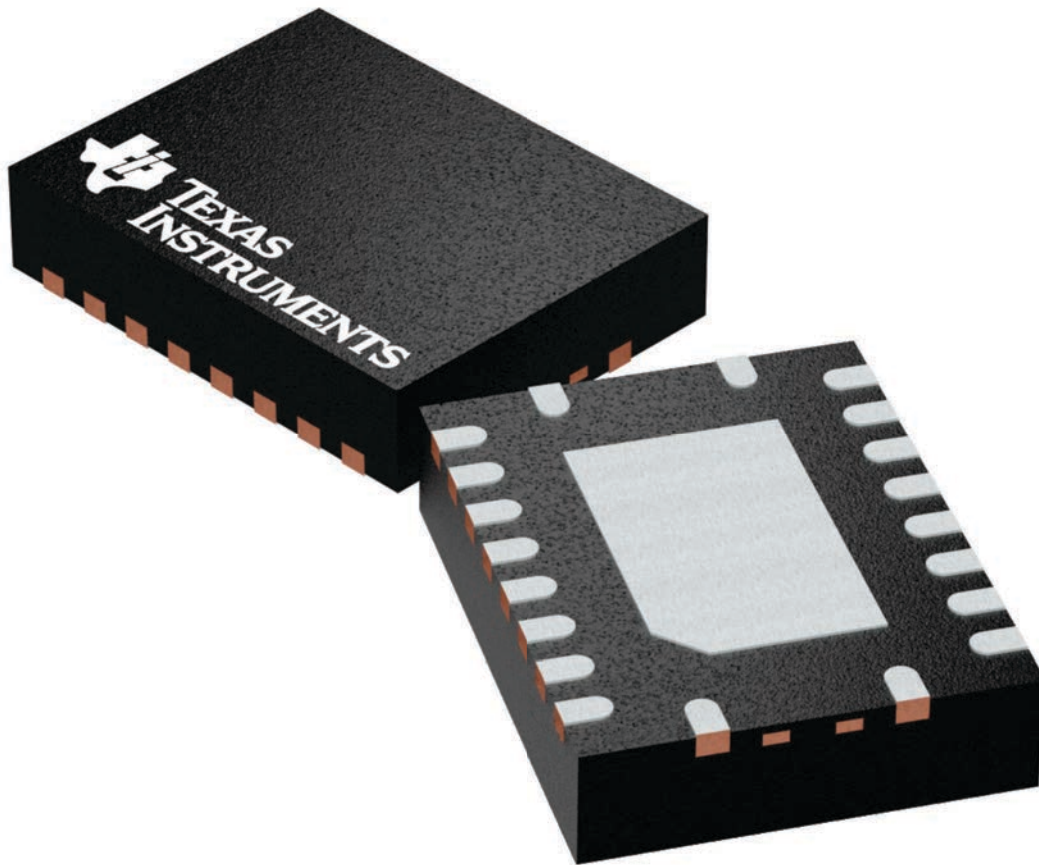
**RGY 20**

**VQFN - 1 mm max height**

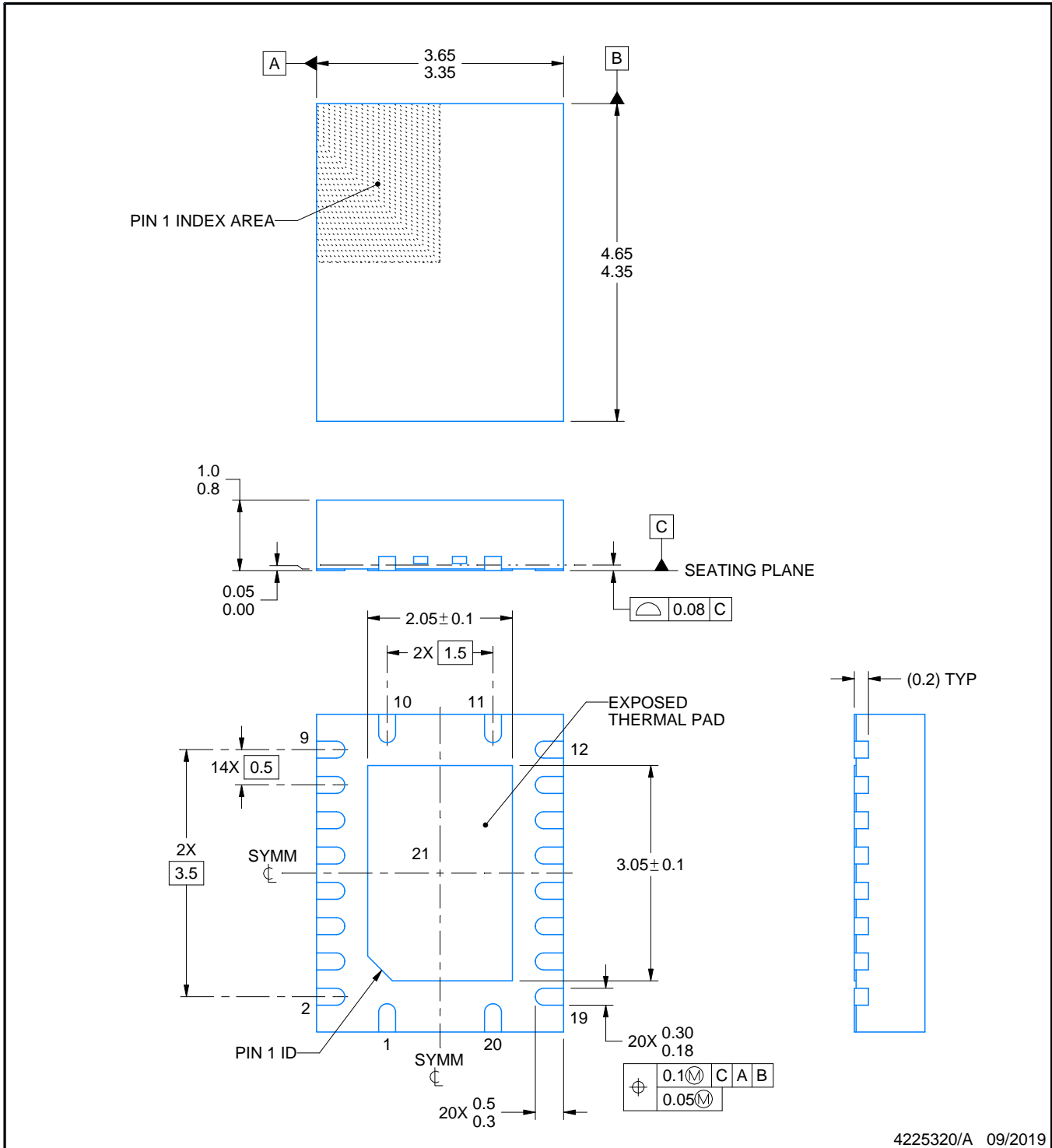
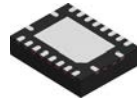
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

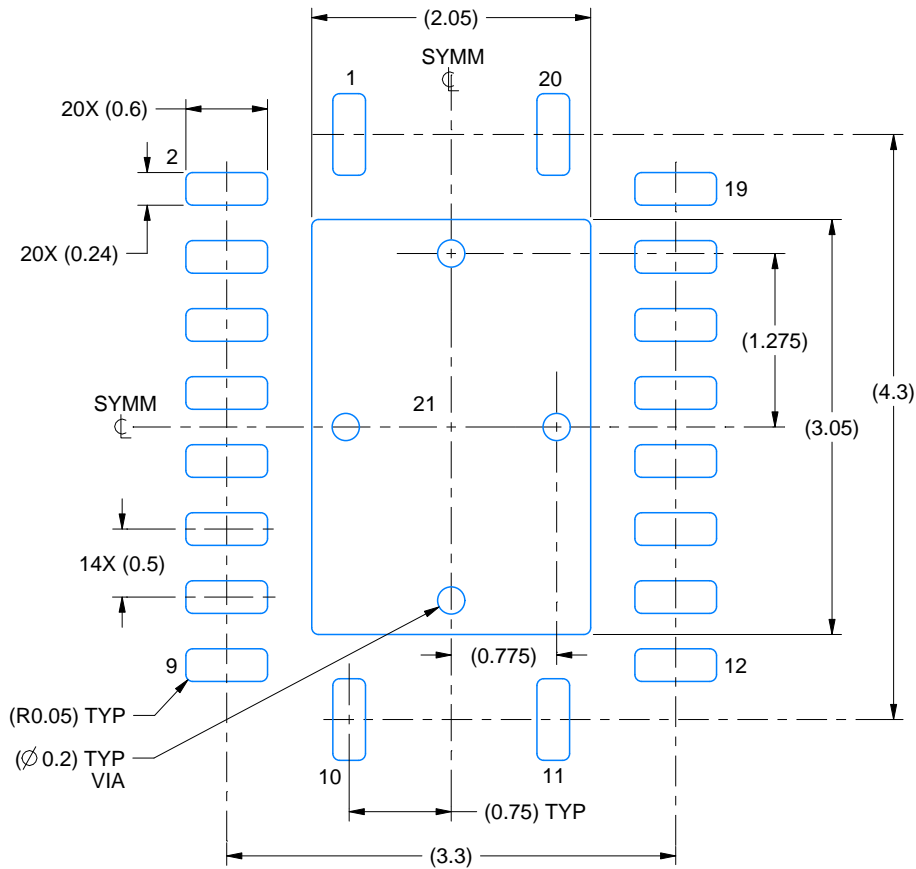
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

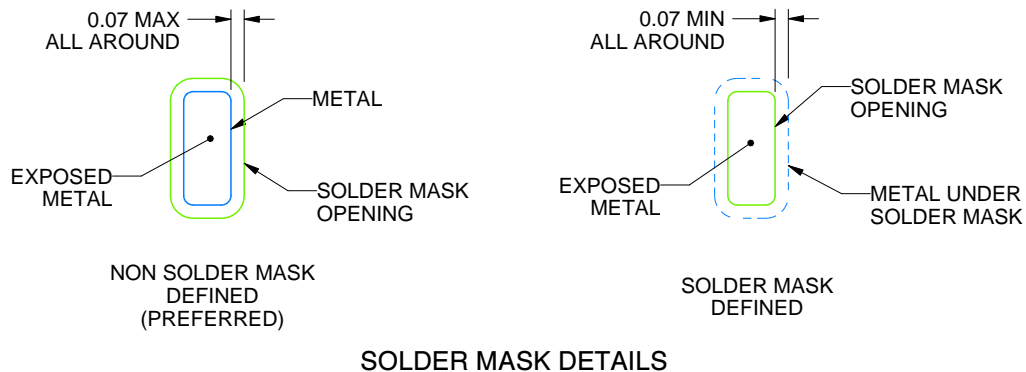
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

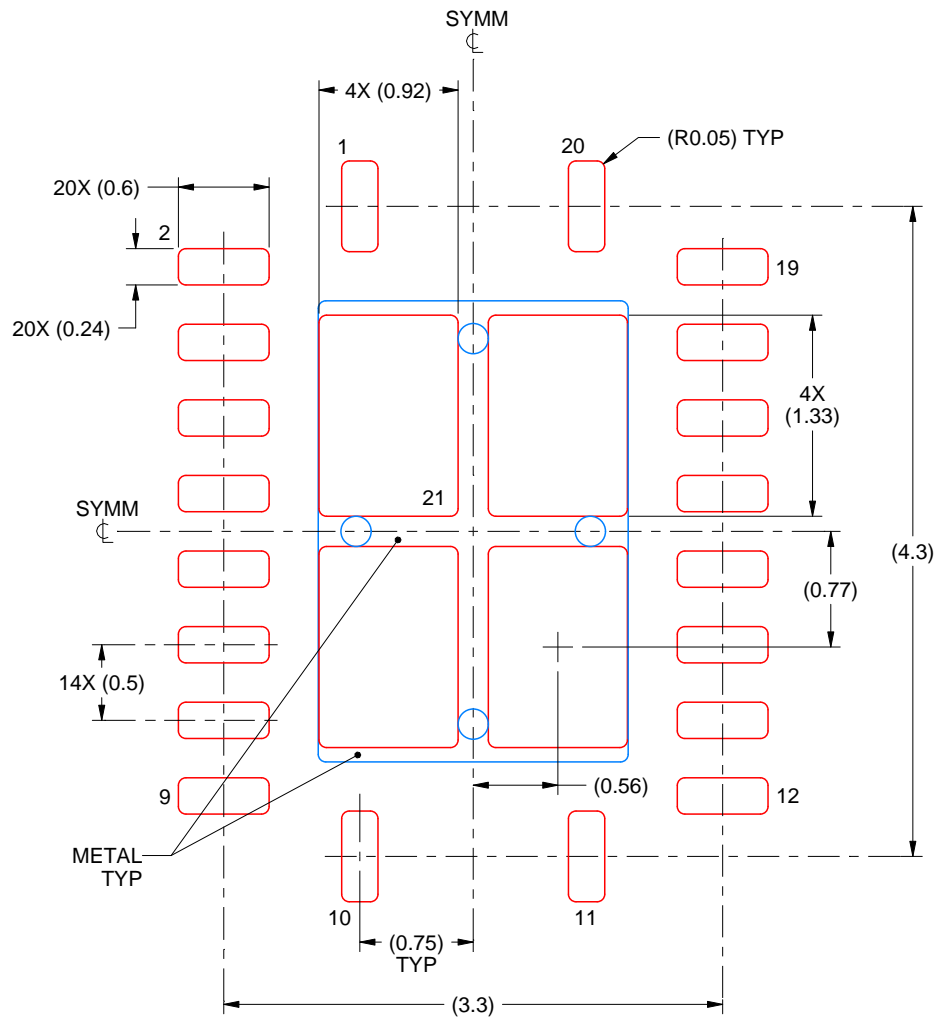
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

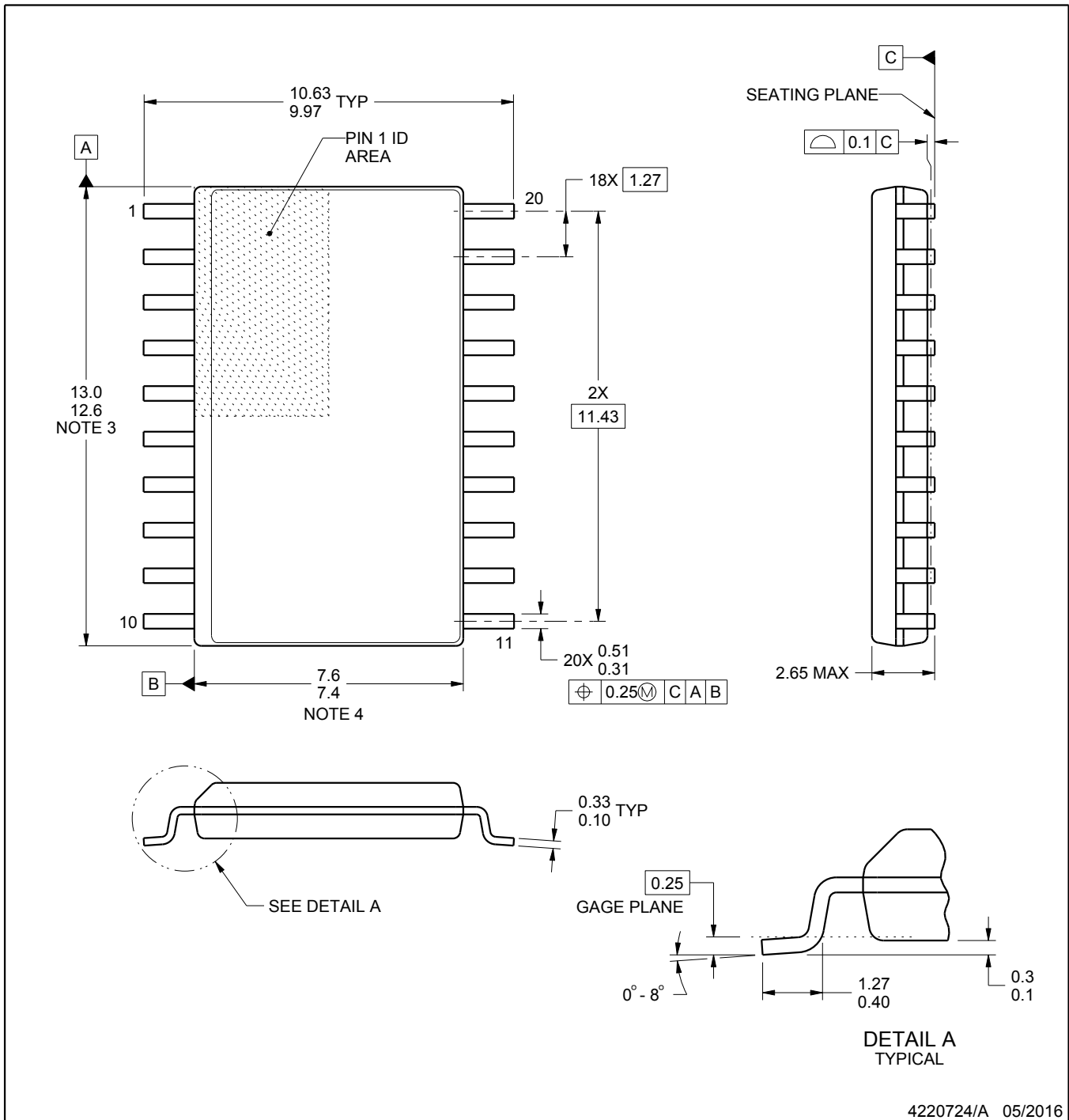
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月