

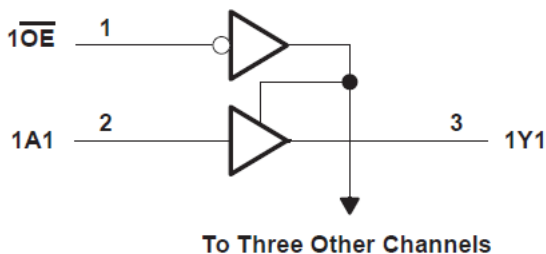
## SN74LV367A 具有三态输出的六路缓冲器和线路驱动器

### 1 应用

- 输出扩展
- LED 矩阵控制
- 7 段显示控制

### 2 特性

- $V_{CC}$  工作电压范围为 2V 至 5.5V
- 5V 时  $t_{pd}$  最大值为 7ns
- $V_{OLP}$  (输出接地反弹) 典型值  
小于 0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值  
大于 2.3V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- 支持所有端口上的混合模式电压运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范



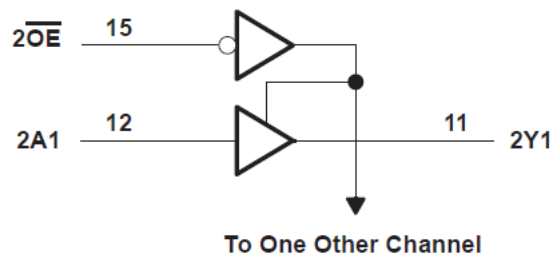
### 3 说明

LV367A 器件是六路缓冲器和线路驱动器, 旨在 2V 至 5.5V  $V_{CC}$  电压下运行。

#### 封装信息<sup>(1)</sup>

| 器件型号       | 封装              | 封装尺寸 (标称值)       |
|------------|-----------------|------------------|
| SN74LV367A | D (SOIC, 16)    | 9mm × 3.90mm     |
|            | DGV (TVSOP, 16) | 3.60mm × 4.40mm  |
|            | NS (SOP, 16)    | 10.20mm × 5.30mm |
|            | PW (TSSOP, 16)  | 5.00mm × 4.40mm  |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision H (December 2022) to Revision I (March 2023)</b>   | <b>Page</b> |
|---|-------------|
| • 从封装信息表中删除了 DB 封装并更新了文档的结构布局.....  | <b>1</b>    |
| • Updated thermal values for D package from $R_{\theta JA} = 73$ to 107.7, all values in $^{\circ}\text{C/W}$ ..... | <b>5</b>    |
| <b>Changes from Revision G (April 1998) to Revision H (December 2022)</b>   | <b>Page</b> |
| • 更新了整个文档中的表格、图和交叉参考的格式.....  | <b>1</b>    |

## 5 Pin Configurations and Functions

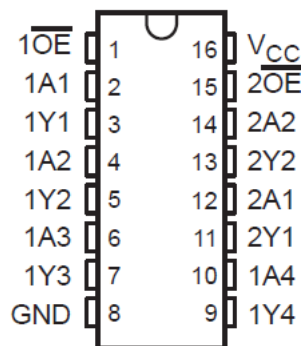


图 5-1. D, DGV, NS, or PW Package (Top View)

表 5-1. Pin Functions

| PIN |                 | TYPE | DESCRIPTION     |
|-----|-----------------|------|-----------------|
| NO. | NAME            |      |                 |
| 1   | 1 OE            | I    | Output Enable 1 |
| 2   | 1A1             | I    | 1A1 Input       |
| 3   | 1Y1             | O    | 1Y1 Output      |
| 4   | 1A2             | I    | 1A2 Input       |
| 5   | 1Y2             | O    | 1Y2 Output      |
| 6   | 1A3             | I    | 1A3 Input       |
| 7   | 1Y3             | O    | 1Y3 Output      |
| 8   | GND             | —    | Ground Pin      |
| 9   | 1Y4             | O    | 1Y4 Output      |
| 10  | 1A4             | I    | 1A4 Input       |
| 11  | 2Y1             | O    | 2Y1 Output      |
| 12  | 2A1             | I    | 2A1 Input       |
| 13  | 2Y2             | O    | 2Y2 Output      |
| 14  | 2A2             | I    | 2A2 Input       |
| 15  | 2 OE            | I    | Output Enable 2 |
| 16  | V <sub>CC</sub> | —    | Power Pin       |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |   | MIN                   | MAX            | UNIT        |
|-----------|---|-----------------------|----------------|-------------|
| $V_{CC}$  | Supply voltage range  | - 0.5                 | 7              | V           |
| $V_I$     | Input voltage range <sup>(2)</sup>  | - 0.5                 | 7              | V           |
| $V_O$     | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | - 0.5                 | 7              | V           |
| $V_O$     | Output voltage range applied in the high or low state <sup>(2) (3)</sup>                    | - 0.5                 | $V_{CC} + 0.5$ | V           |
| $I_{IK}$  | Input clamp current   | $V_I < 0$             |                | - 20 mA     |
| $I_{OK}$  | Output clamp current  | $V_O < 0$             |                | - 50 mA     |
| $I_O$     | Continuous output current   | $V_O = 0$ to $V_{CC}$ |                | $\pm 35$ mA |
|           | Continuous current through $V_{CC}$ or GND  |                       |                | $\pm 70$ mA |
| $T_{stg}$ | Storage temperature range   | - 65                  | 150            | °C          |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 6.2 ESD Ratings

|             |   | VALUE      | UNIT |
|-------------|---|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge   |            |      |
|             | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | $\pm 2000$ | V    |
|             | Machine Model (MM), per JEDEC specification                           | $\pm 200$  |      |
|             | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | $\pm 1000$ |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |                                  | MIN                   | MAX                   | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                     |                                  | 2                     | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   |                       | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                       |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            |                       | 0.5                   | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | V <sub>CC</sub> × 0.3 |      |
| V <sub>I</sub>  | Input voltage                      |                                  | 0                     | 5.5                   | V    |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0                     | V <sub>CC</sub>       | V    |
|                 |                                    | 3-state                          | 0                     | 5.5                   |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            |                       | – 50                  | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | – 2                   | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | – 8                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | – 16                  |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            |                       | 50                    | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 2                     | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 8                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 16                    |      |
| Δ t / Δ v       | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 200                   | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 100                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 20                    |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | – 40                  | 85                    | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | SN74LV367A |         |         |         | UNIT |
|-------------------------------|--|------------|---------|---------|---------|------|
|                               |  | D          | DGV     | NS      | PW      |      |
|                               |  | 16 PINS    | 16 PINS | 16 PINS | 16 PINS |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 107.7      | 120     | 64      | 131.2   | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                 |                    | V <sub>CC</sub> | SN74LV367A            |     |     | UNIT |
|------------------|---|--------------------|-----------------|-----------------------|-----|-----|------|
|                  |   |                    |                 | MIN                   | TYP | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = - 50 μA                       |                    | 2 V to 5.5 V    | V <sub>CC</sub> - 0.1 |     |     | V    |
|                  | I <sub>OH</sub> = - 2 mA                        |                    | 2.3 V           | 2                     |     |     |      |
|                  | I <sub>OH</sub> = - 8 mA                        |                    | 3 V             | 2.48                  |     |     |      |
|                  | I <sub>OH</sub> = - 16 mA                       |                    | 4.5             | 3.8                   |     |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA                         |                    | 2 V to 5.5 V    | 0.1                   |     |     | V    |
|                  | I <sub>OL</sub> = 2 mA                          |                    | 2.3 V           | 0.4                   |     |     |      |
|                  | I <sub>OL</sub> = 8 mA                          |                    | 3 V             | 0.44                  |     |     |      |
|                  | I <sub>OL</sub> = 16 mA                         |                    | 4.5 V           | 0.55                  |     |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                   |                    | 0 to 5.5 V      | ±1                    |     |     | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND         |                    | 5.5 V           | ±5                    |     |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND,        | I <sub>O</sub> = 0 | 5.5 V           | 20                    |     |     | μA   |
| I <sub>off</sub> | V <sub>O</sub> = or V <sub>O</sub> = 0 to 5.5 V |                    | 0               | 5                     |     |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND         |                    | 3.3 V           | 3                     |     |     | pF   |
| C <sub>O</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND         |                    | 3.3 V           | 5.2                   |     |     | pF   |

## 6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |      |      | SN74LV367A |     | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|------|------|------------|-----|------|
|             |                 |                |                      | MIN                      | TYP  | MAX  | MIN        | MAX |      |
| $t_{pd}$    | A               | Y              | $C_L = 15\text{ pF}$ |                          | 6.4  | 12.7 | 1          | 16  | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 6.9  | 14.9 | 1          | 20  |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 6.4  | 14.9 | 1          | 20  |      |
| $t_{pd}$    | A               | Y              | $C_L = 50\text{ pF}$ |                          | 8.6  | 17.5 | 1          | 21  | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 9.4  | 19.7 | 1          | 25  |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 10.1 | 19.7 | 1          | 25  |      |
| $t_{sk(o)}$ |                 |                |                      |                          |      | 2    |            | 2   |      |

## 6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |      | SN74LV367A |      | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|-----|------|------------|------|------|
|             |                 |                |                      | MIN                      | TYP | MAX  | MIN        | MAX  |      |
| $t_{pd}$    | A               | Y              | $C_L = 15\text{ pF}$ |                          | 4.7 | 8.3  | 1          | 10   | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 5.1 | 10.5 | 1          | 12.5 |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 4.9 | 10.5 | 1          | 12.5 |      |
| $t_{pd}$    | A               | Y              | $C_L = 50\text{ pF}$ |                          | 6.2 | 11.8 | 1          | 13.5 | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 6.8 | 14   | 1          | 16   |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 7.3 | 13.6 | 1          | 15.5 |      |
| $t_{sk(o)}$ |                 |                |                      |                          |     | 1.5  |            | 1.5  |      |

## 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |     | SN74LV367A |      | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|-----|-----|------------|------|------|
|             |                 |                |                      | MIN                      | TYP | MAX | MIN        | MAX  |      |
| $t_{pd}$    | A               | Y              | $C_L = 15\text{ pF}$ |                          | 3.6 | 5.9 | 1          | 7    | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 3.8 | 7.2 | 1          | 8.5  |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 2.6 | 7.2 | 0          | 8.5  |      |
| $t_{pd}$    | A               | Y              | $C_L = 50\text{ pF}$ |                          | 4.5 | 7.9 | 1          | 9    | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                      |                          | 4.9 | 9.2 | 1          | 10.5 |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                      |                          | 4.5 | 9.2 | 0          | 10.5 |      |
| $t_{sk(o)}$ |                 |                |                      |                          |     | 1   |            | 1    |      |

## 6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER   |  | MIN  | TYP   | MAX   | UNIT |
|-------------|--|------|-------|-------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |      | 0.3   | 0.8   | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |      | – 0.3 | – 0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |      | 3     |       | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31 |       |       | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |      |       | 0.99  | V    |

## 6.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$ 

| PARAMETER                              | TEST CONDITIONS                            | $V_{CC}$ | TYP  | UNIT |
|--|--|----------|------|------|
| $C_{pd}$ Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 14.9 | pF   |
|  |  | 5 V      | 17.4 |      |

## 6.11 Typical Characteristics

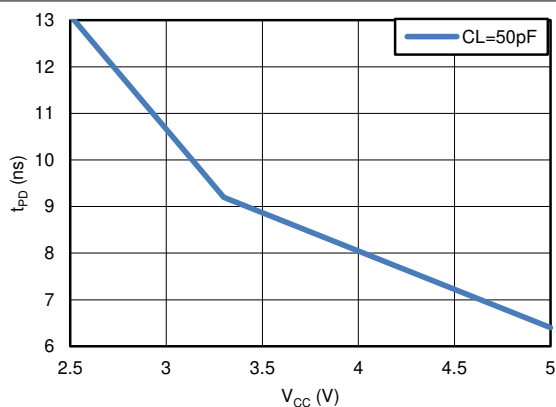
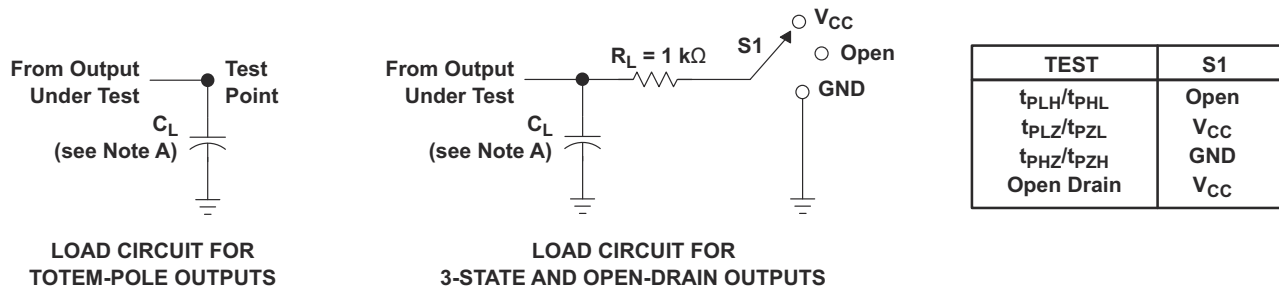


图 6-1. TPD vs  $V_{CC}$

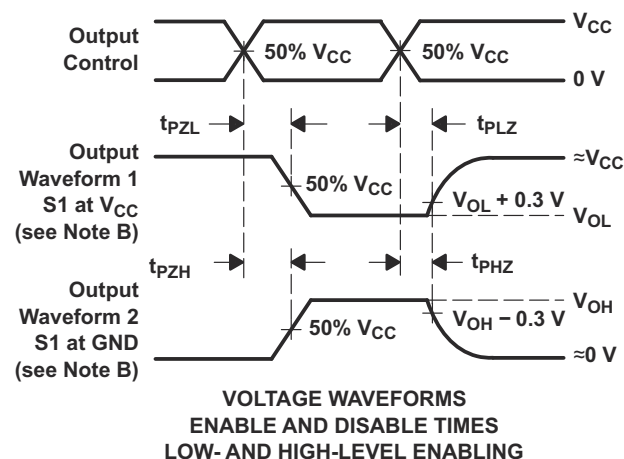
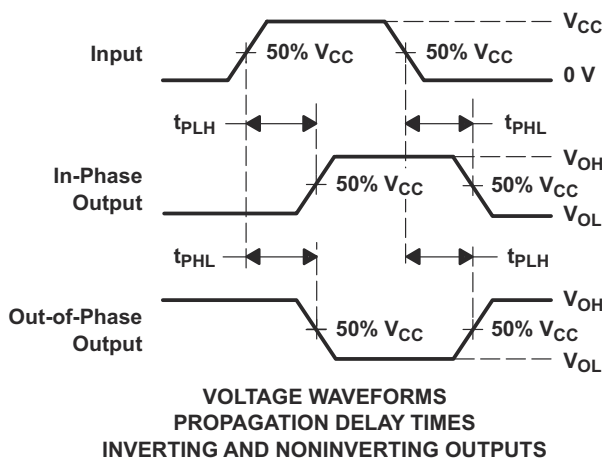
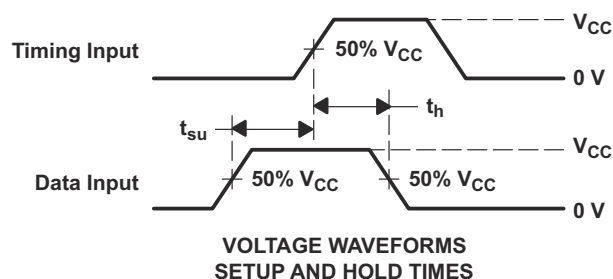
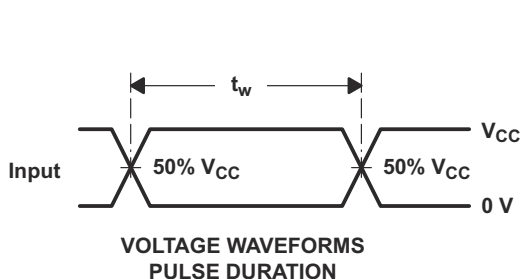


## 7 Parameter Measurement Information



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The 'LV367A devices are hex buffers and line drivers designed for 2 V to 5.5 V  $V_{CC}$  operation. These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV367A devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ( $\overline{1OE}$  and  $\overline{2OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



图 8-1. Logic Diagram (Positive Logic)

## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k $\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

### 8.3.4 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.5 Clamp Diode Structure

图 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

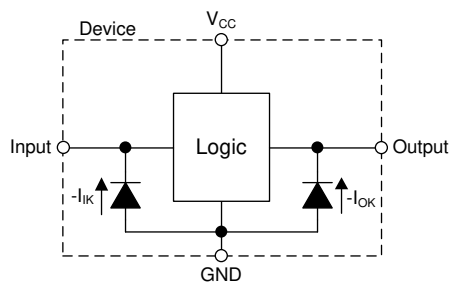


图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

表 8-1. Function Table  
(Each Buffer/ Driver)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| OE     | A | Y      |
| L      | H | H      |
| L      | L | L      |
| H      | X | Z      |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The SN74LV367A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are 5 V tolerant allowing for down translation to  $V_{CC}$ .

### 9.2 Typical Application

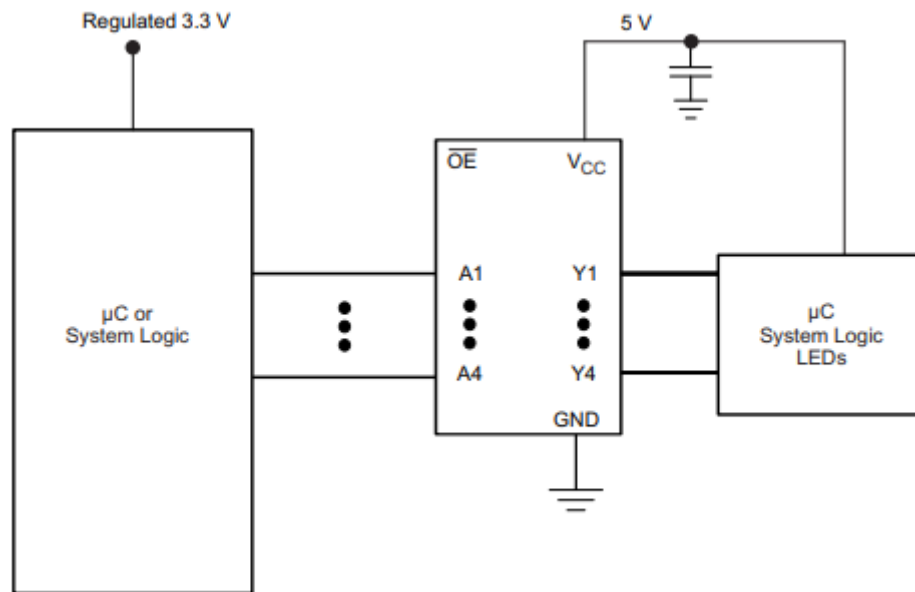


图 9-1. Expanding IOs to Drive LEDs

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu F$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01  $\mu F$  or 0.022  $\mu F$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1  $\mu F$  and 1.0  $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input

depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example

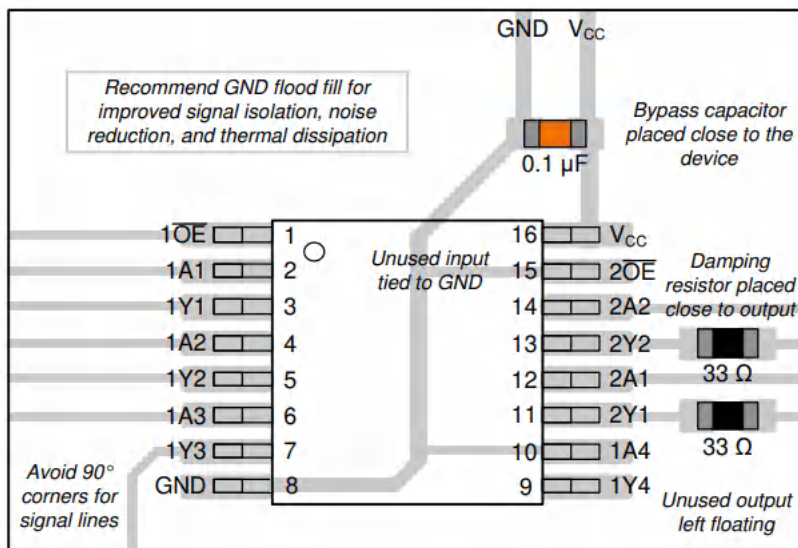


图 9-2. Layout Example for the SN74LV367A

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application report](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application report](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LV367AD</a>    | Obsolete      | Production           | SOIC (D)   16    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV367A              |
| <a href="#">SN74LV367ADGVR</a> | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV367A              |
| SN74LV367ADGVR.A               | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV367A              |
| <a href="#">SN74LV367ADR</a>   | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV367A              |
| SN74LV367ADR.A                 | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV367A              |
| <a href="#">SN74LV367ANSR</a>  | Active        | Production           | SOP (NS)   16    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV367A            |
| SN74LV367ANSR.A                | Active        | Production           | SOP (NS)   16    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV367A            |
| <a href="#">SN74LV367APWR</a>  | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | (LV367A, T9044PW)   |
| SN74LV367APWR.A                | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | (LV367A, T9044PW)   |
| <a href="#">SN74LV367APWT</a>  | Obsolete      | Production           | TSSOP (PW)   16  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV367A              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV367ADGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV367ADR   | SOIC         | D               | 16   | 2500 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| SN74LV367ADR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV367ANSR  | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV367APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV367APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV367ADGVR | TVSOP        | DGV             | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV367ADR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LV367ADR   | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LV367ANSR  | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV367APWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV367APWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月