- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

- Applications:

  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

  Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

  Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities
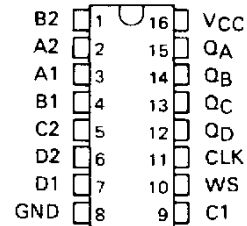
description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.
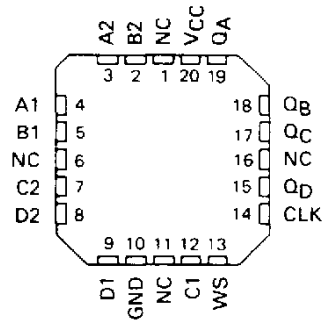
Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of -55°C to 125°C; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C.

SN54298, SN54LS298 . . . J OR W PACKAGE
SN74298 . . . N PACKAGE
SN74LS298 . . . D OR N PACKAGE
(TOP VIEW)

```
        ┌──┬──┐
   B2 ┃1  U 16┃ Vcc
   A2 ┃2    15┃ QA
   A1 ┃3    14┃ QB
   B1 ┃4    13┃ QC
   C2 ┃5    12┃ QD
   D2 ┃6    11┃ CLK
   D1 ┃7    10┃ WS
  GND ┃8     9┃ C1
        └─────┘
```

SN54LS298 . . . FK PACKAGE
(TOP VIEW)

```
            A2  B2  NC  VCC  QA
            3   2   1   20  19
      A1 ┃4               18┃ QB
      B1 ┃5               17┃ QC
      NC ┃6               16┃ NC
      C2 ┃7               15┃ QD
      D2 ┃8               14┃ CLK
            9  10  11  12  13
            D1  GND NC  C1  WS
```

NC - No internal connection

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.
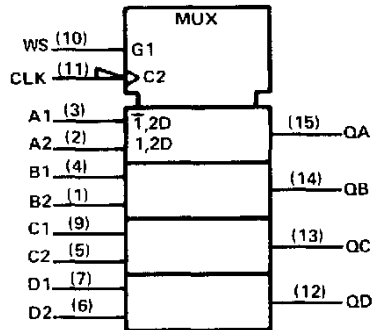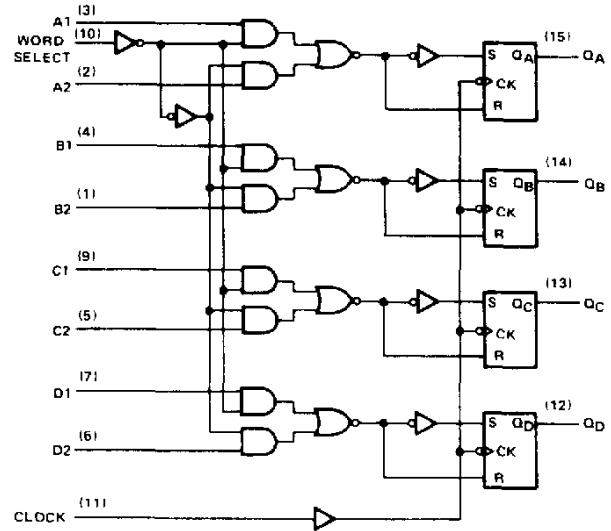
SN54298, SN54LS298, SN74298, SN74LS298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE
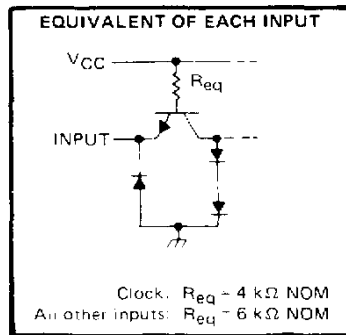
logic symbol[†]

[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
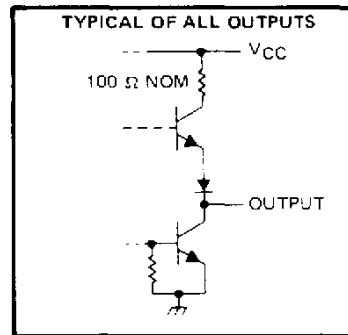
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

schematics of inputs and outputs

'298
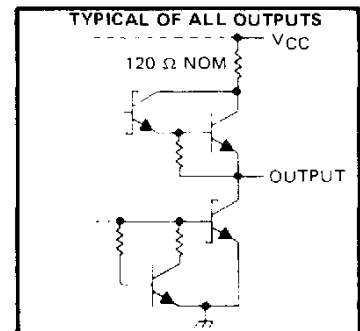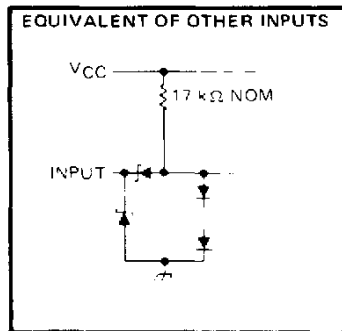
EQUIVALENT OF EACH INPUT

Clock, R_{eq} ≈ 4 kΩ NOM
All other inputs: R_{eq} ≈ 6 kΩ NOM

TYPICAL OF ALL OUTPUTS

100 Ω NOM

'LS298

EQUIVALENT OF DATA INPUTS

15 kΩ NOM

EQUIVALENT OF OTHER INPUTS

17 kΩ NOM

TYPICAL OF ALL OUTPUTS

120 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Operating free-air temperature range: SN54298 . . . . −55°C to 125°C
SN74298 . . . . 0°C to 70°C
Storage temperature . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54298			SN74298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	µA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{su}	Data	15			15			ns
	Word select	25			25			
Hold time, t_h	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	MIN	TYP[‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 µA	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX SN54298	−20		−57	mA
		SN74298	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		39	65	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 3		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output			21	32	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.
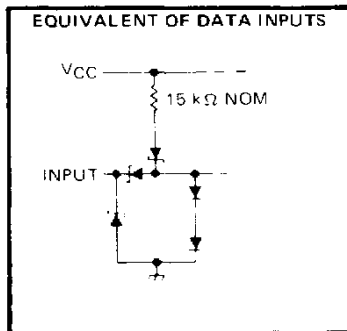
SN54LS298, SN74LS298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54LS298 . . . . −55°C to 125°C
                              SN74LS298 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS298			SN74LS298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{su}	Data	15			15			ns
	Word select	25			25			
Hold time, t_h	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS298			SN74LS298			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = $ MIN,	$I_I = -18$ mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = $ MIN, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max, $I_{OH} = -400\,\mu$A		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = $ MIN, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max	$I_{OL} = 4$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 8$ mA					0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = $ MAX,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = $ MAX,	$V_I = 2.7$ V			20			20	μA
I_{IL}	Low-level input current	$V_{CC} = $ MAX,	$V_I = 0.4$ V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current[§]	$V_{CC} = $ MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	$V_{CC} = $ MAX,	See Note 2		13	21		13	21	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15$ pF, $R_L = 2$ kΩ, See Note 3		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output			21	32	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.
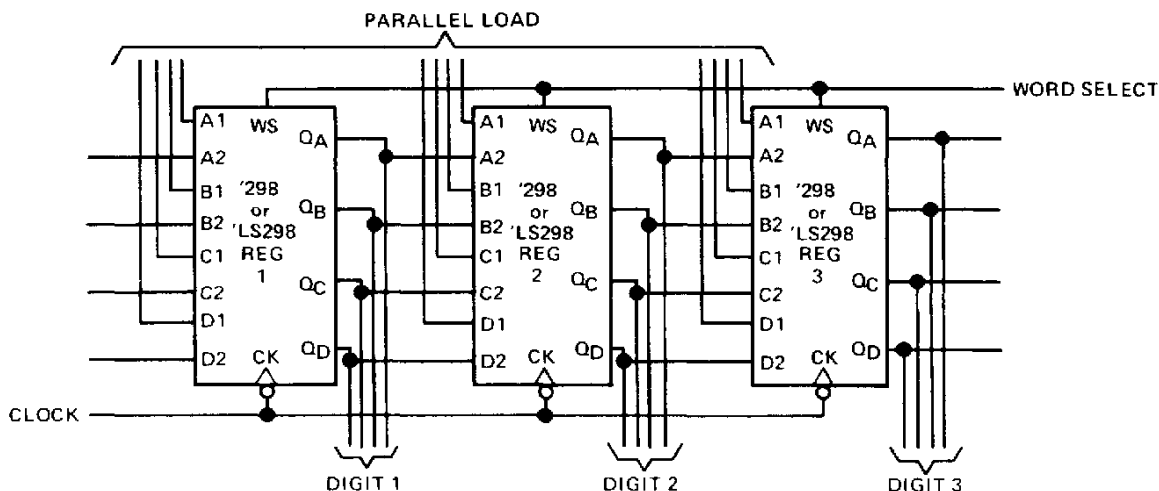
When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 or 'LS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one place/two-place shift register.
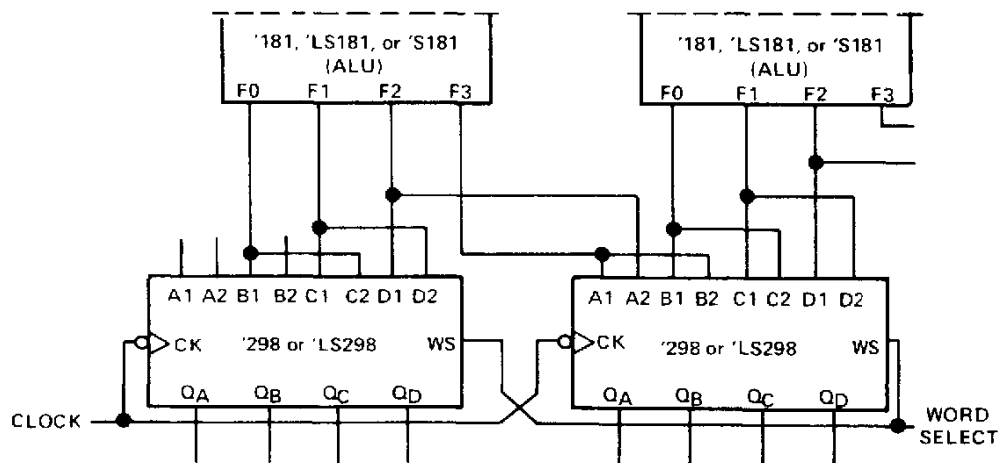
When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS298N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS298N
SN74LS298N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS298N

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS298N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS298N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS298N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS298N.A	N	PDIP	16	25	506	13.97	11230	4.32

N (R−PDIP−T**)　　　　　　　　PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A　MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A　MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16　　　　　　9

0.260 (6,60)
0.240 (6,10)

1　　　　　　8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option /D\

4040049/E 12/2002

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　/C\　Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
　　　/D\　The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER