

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

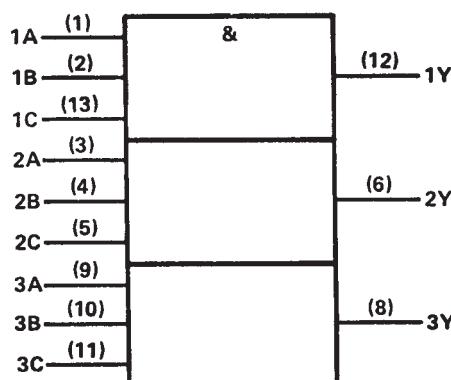
These devices contain three independent 3-input AND gates.

The SN54LS11 and SN54S11 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS11 and SN74S11 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

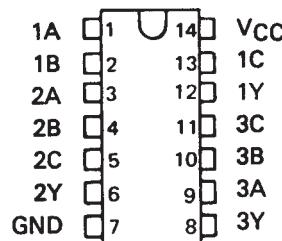
### logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

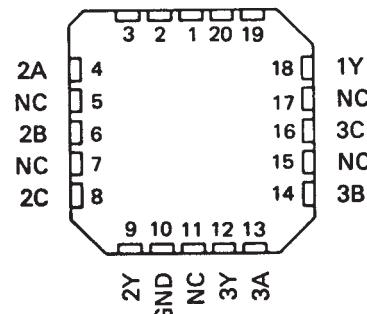
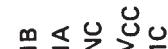
SN54LS11, SN74S11 . . . J OR W PACKAGE  
SN74LS11, SN74S11 . . . D OR N PACKAGE

(TOP VIEW)



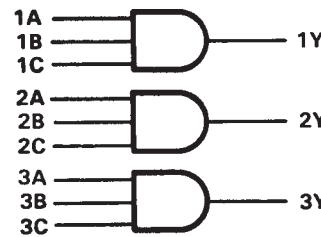
SN54LS11, SN54S11 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

### logic diagram (positive logic)



$$Y = A \cdot B \cdot C \text{ or}$$

$$Y = \overline{A} + \overline{B} + \overline{C}$$

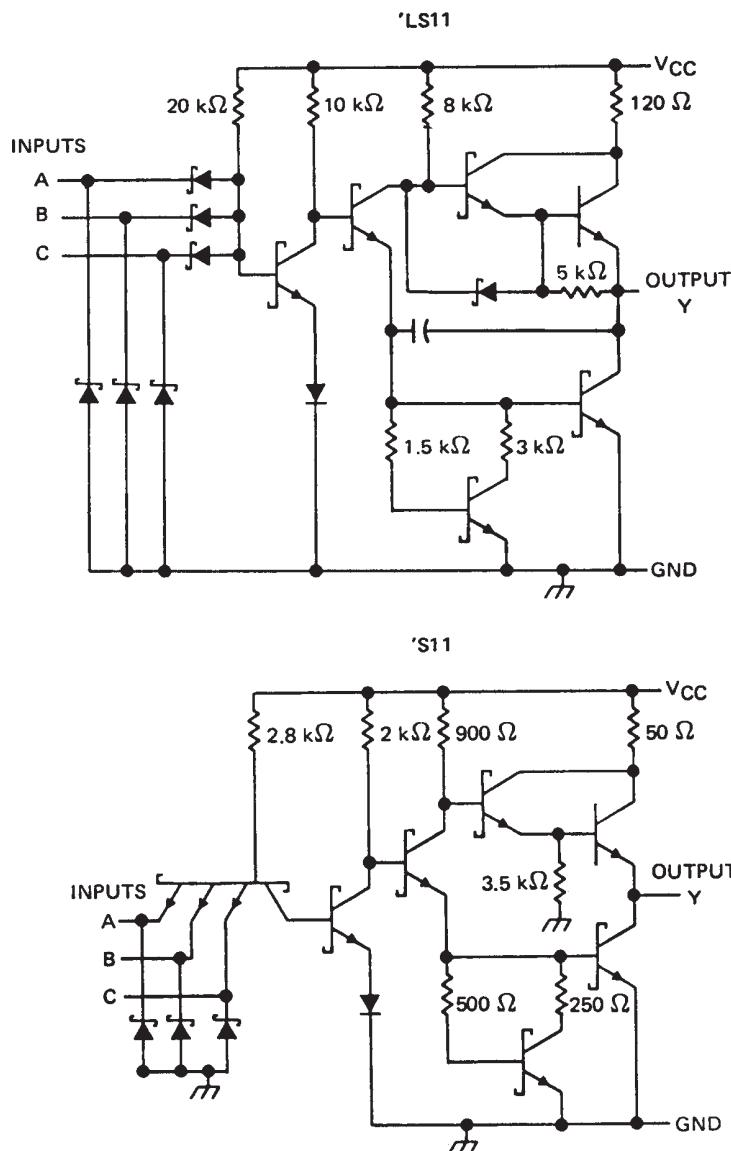
SN54LS11, SN54S11,

SN74LS11, SN74S11

## TRIPLE 3-INPUT POSITIVE-AND GATES

SDLS131 - APRIL 1985 - REVISED MARCH 1988

### schematics (each gate)



Resistor values shown are nominal.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 1) . . . . .	7 V
Input voltage: 'S11 . . . . .	5.5 V
'LS11 . . . . .	7 V
Operating free-air temperature range: SN54' . . . . .	-55°C to 125°C
SN74' . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS11			SN74LS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			4			8	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS11			SN74LS11			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20	-100	-20	-100			mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V	1.8	3.6		1.8	3.6		mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V	3.3	6.6		3.3	6.6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B or C	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF	8	15		ns
				10	20		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS11, SN54S11,  
SN74LS11, SN74S11

## TRIPLE 3-INPUT POSITIVE-AND GATES

SDLS131 – APRIL 1985 – REVISED MARCH 1988

### recommended operating conditions

		SN54S11			SN74S11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-1			-1	mA
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	-55		125	0		70	$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54S11			SN74S11			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			50			50	$\mu\text{A}$
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
$I_{CCH}$	$V_{CC} = \text{MAX}$ , $V_I = 4.5 \text{ V}$	13.5	24		13.5	24		mA
$I_{CCL}$	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$	24	42		24	42		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A, B or C	Y	$R_L = 280 \Omega$ , $C_L = 15 \text{ pF}$	4.5	7		ns
$t_{PHL}$				5	7.5		ns
$t_{PLH}$		Y	$R_L = 280 \Omega$ , $C_L = 50 \text{ pF}$	6			ns
$t_{PHL}$				7.5			ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/08001BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BCA
JM38510/08001BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BCA
JM38510/08001BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BDA
JM38510/08001BDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BDA
JM38510/31001BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BCA
JM38510/31001BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BCA
JM38510/31001BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BDA
JM38510/31001BDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BDA
M38510/08001BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BCA
M38510/08001BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08001BDA
M38510/31001BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BCA
M38510/31001BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31001BDA
SN54LS11J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS11J
SN54LS11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS11J
SN54S11J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S11J
SN54S11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S11J
SN74LS11D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	LS11
SN74LS11DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS11
SN74LS11DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS11
SN74LS11N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS11N

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS11N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS11N
SN74LS11NE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS11N
<b>SN74LS11NSR</b>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS11
SN74LS11NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS11
<b>SNJ54LS11FK</b>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 11FK
SNJ54LS11FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 11FK
<b>SNJ54LS11J</b>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS11J
SNJ54LS11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS11J
<b>SNJ54LS11W</b>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS11W
SNJ54LS11W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS11W
<b>SNJ54S11J</b>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S11J
SNJ54S11J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S11J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54LS11, SN74LS11 :**

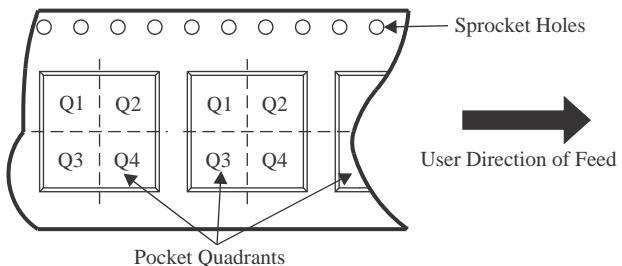
- Catalog : [SN74LS11](#)
- Military : [SN54LS11](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


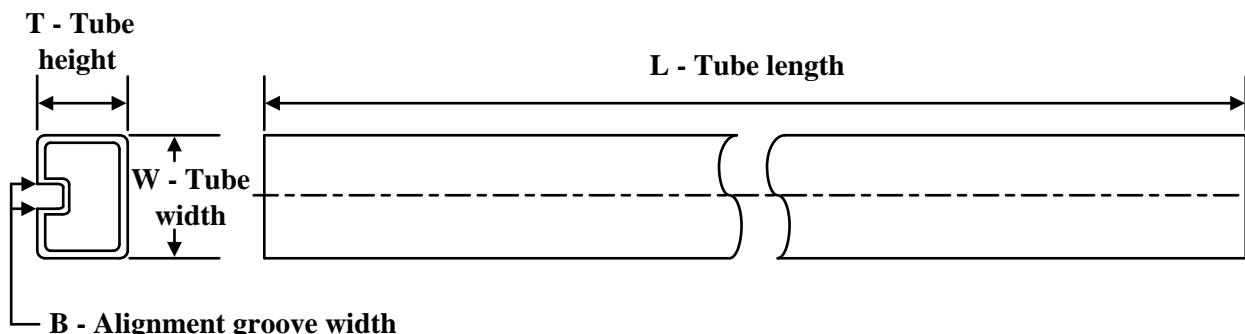
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS11NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS11DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS11NSR	SOP	NS	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

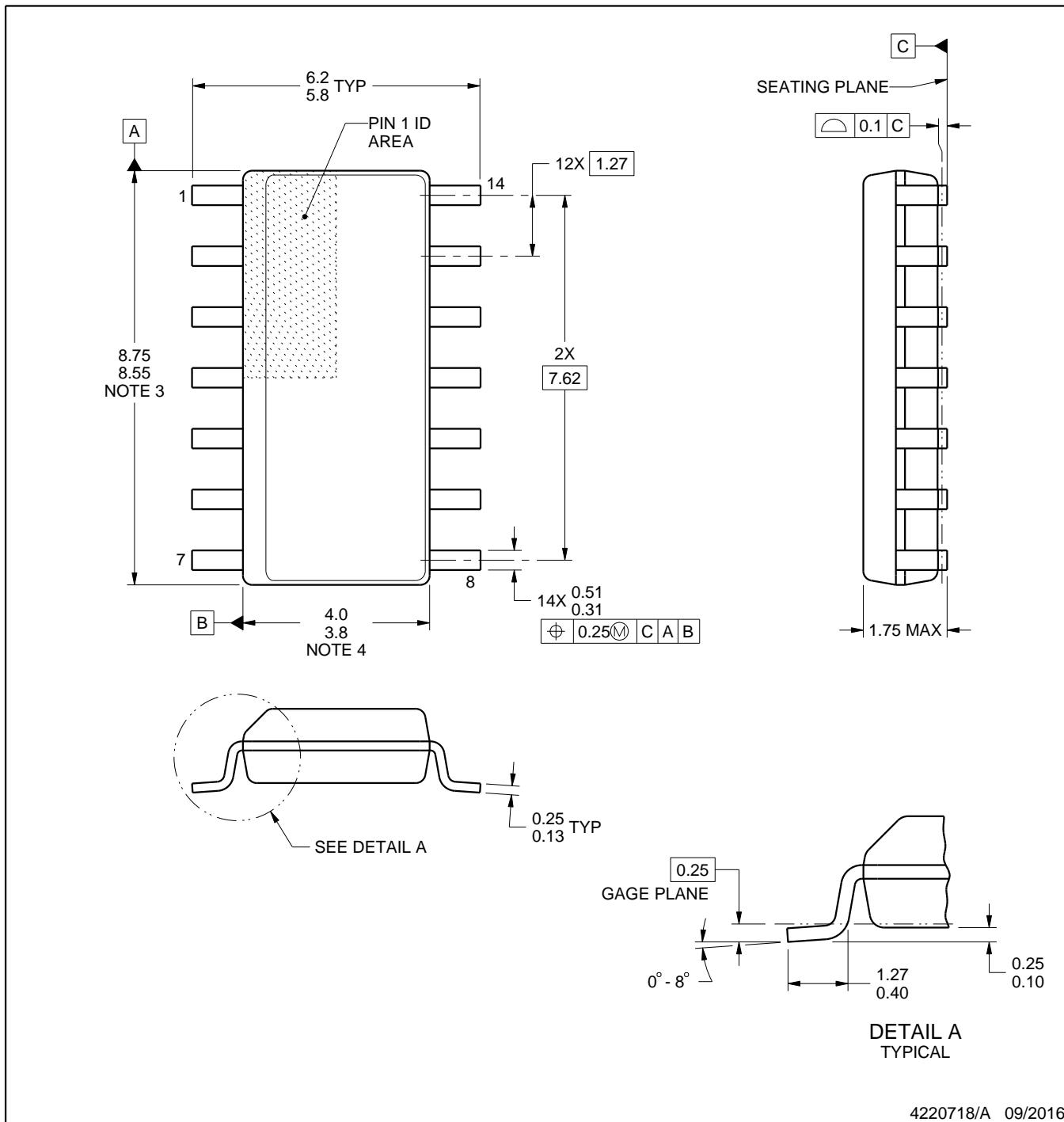
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/08001BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/08001BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31001BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31001BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/08001BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31001BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS11N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS11N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS11N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS11N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS11NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS11NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS11FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS11FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS11W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS11W.A	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

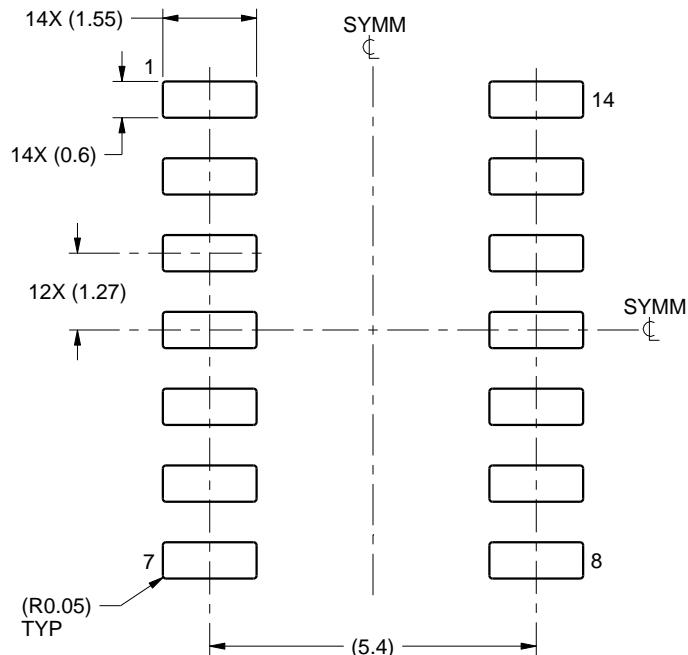
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

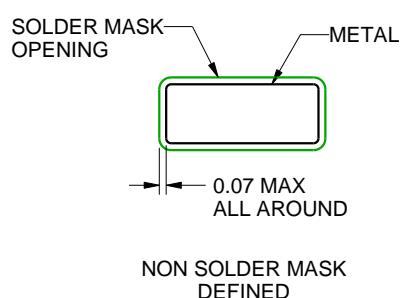
D0014A

SOIC - 1.75 mm max height

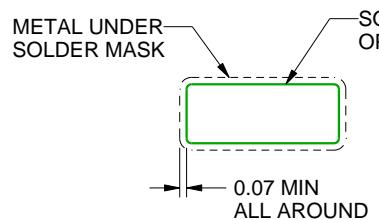
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

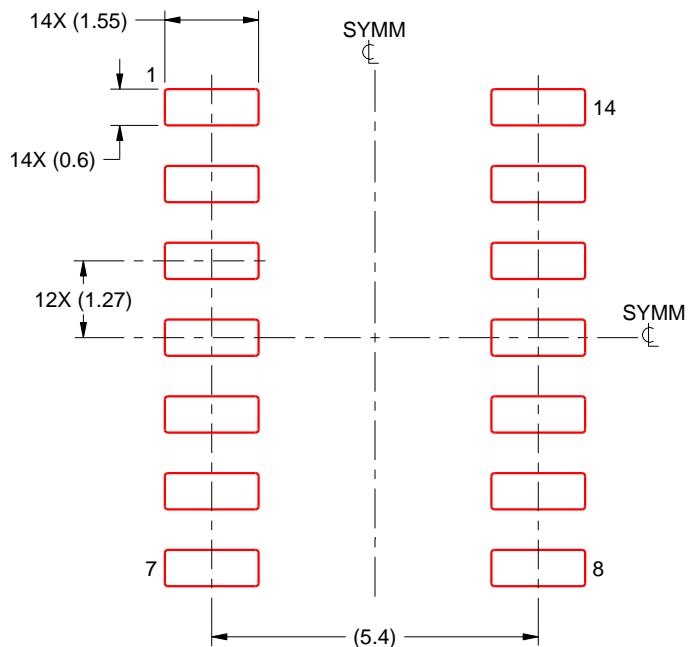
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**D0014A**

**SOIC - 1.75 mm max height**

## SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X**

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

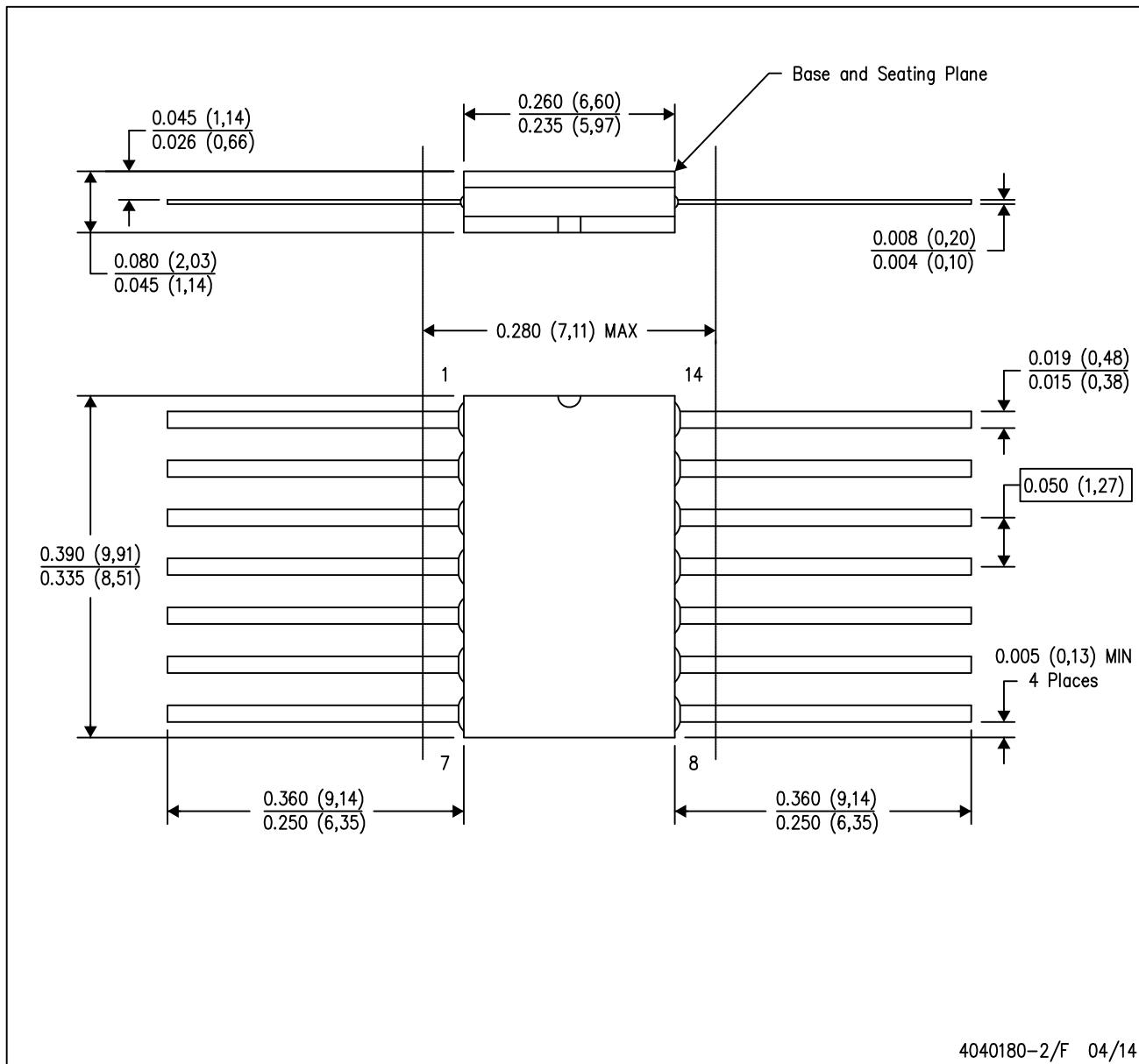


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

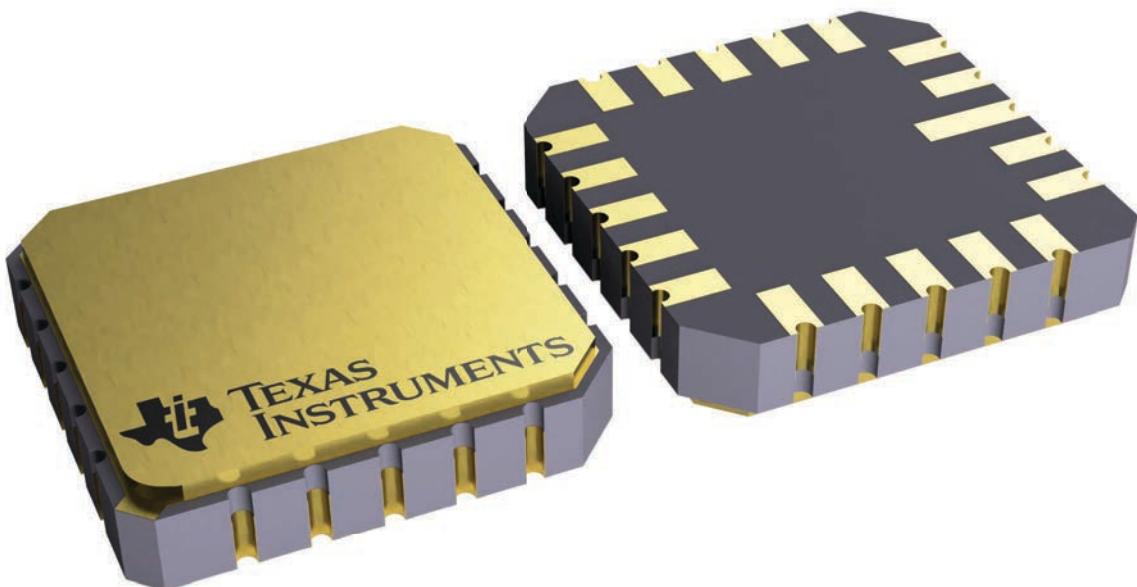
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



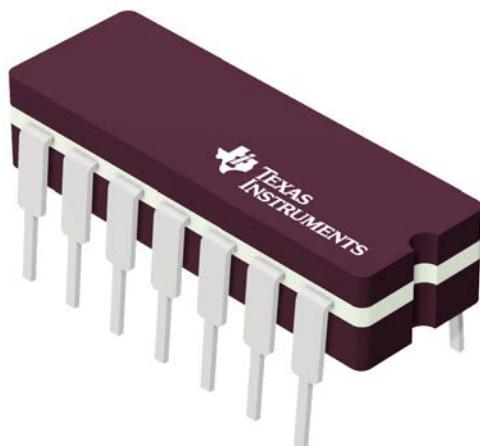
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

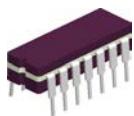
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

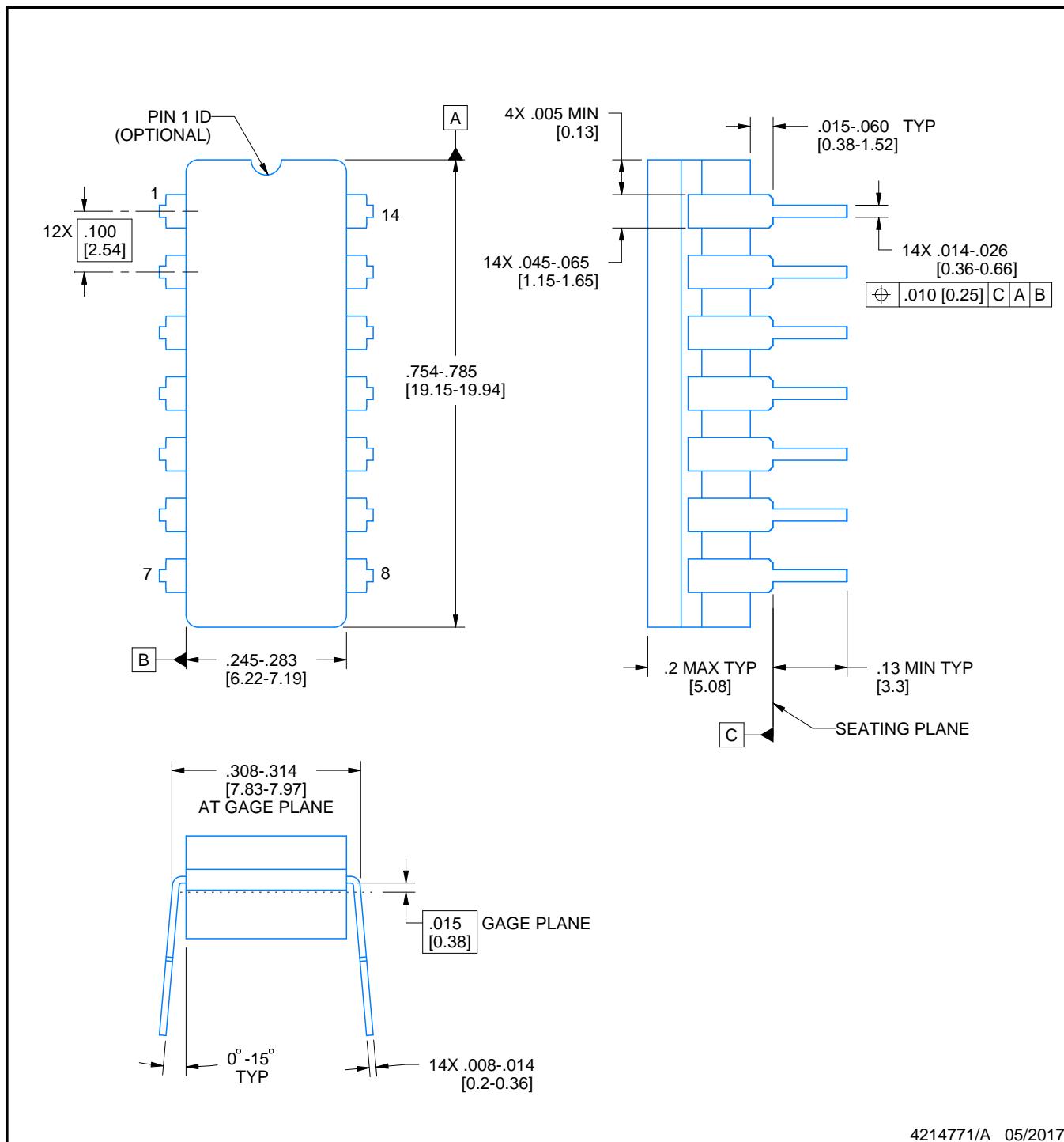


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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## NOTES:

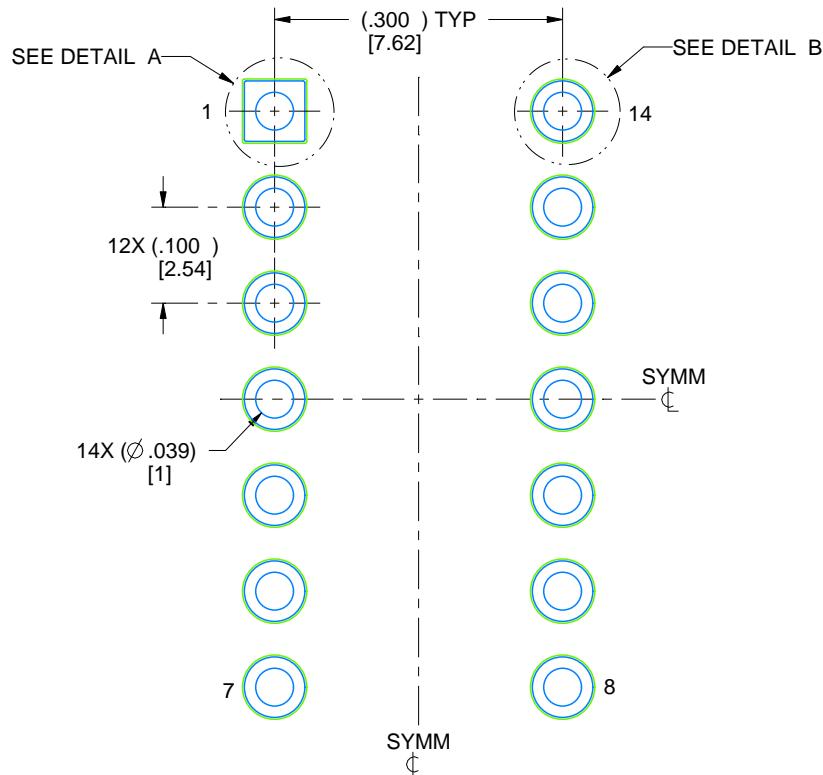
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

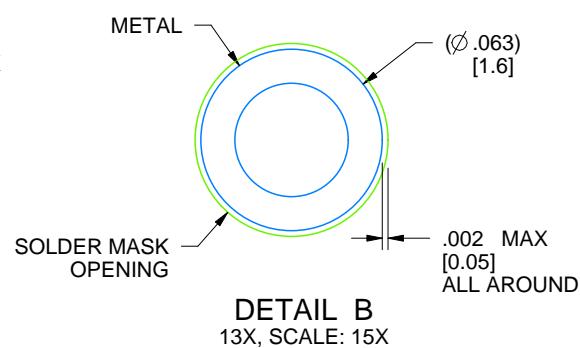
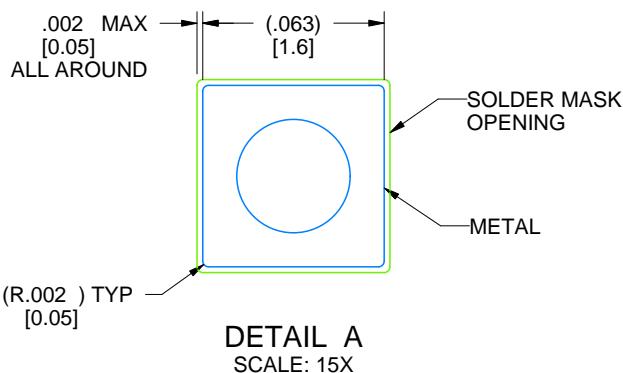
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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