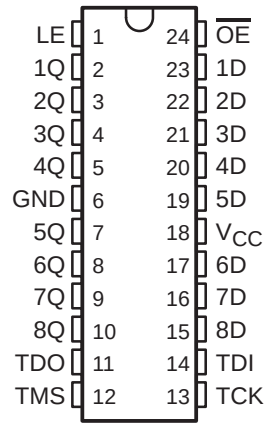
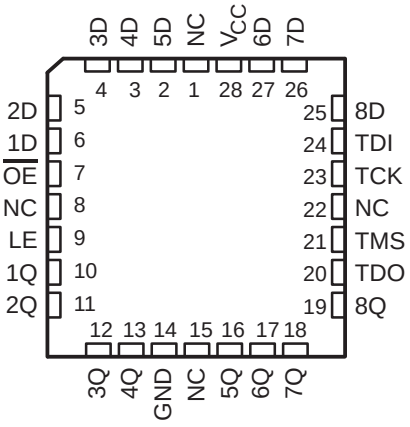
- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Octal Test-Integrated Circuits**
- **Functionally Equivalent to ’F373 and ’BCT373 in the Normal-Function Mode**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ**
  - **Parallel Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)**

SN54BCT8373A . . . JT PACKAGE
SN74BCT8373A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8373A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’BCT8373A scan test devices with octal D-type latches are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the ’F373 and ’BCT373 octal D-type latches. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal latches.

In the test mode, the normal operation of the SCOPE™ octal latches is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations, as described in IEEE Standard 1149.1-1990.

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description (continued)

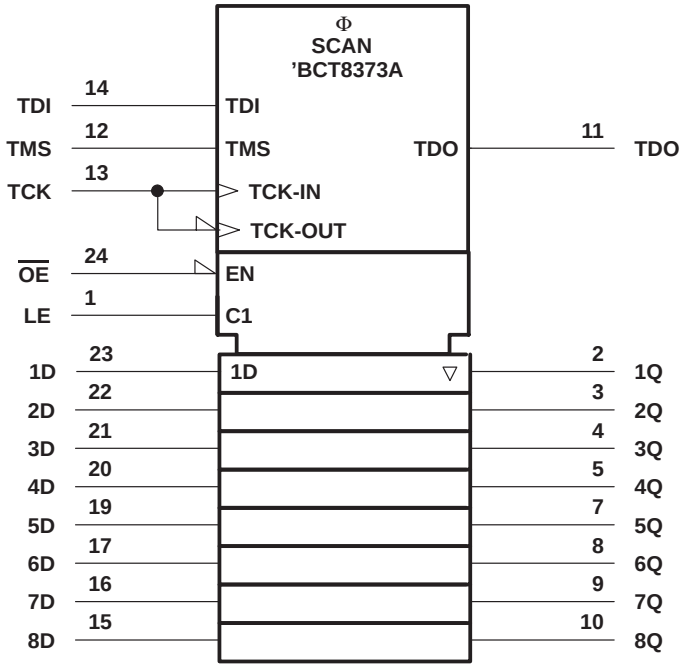
Four dedicated test terminals are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8373A is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74BCT8373A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(normal mode, each latch)

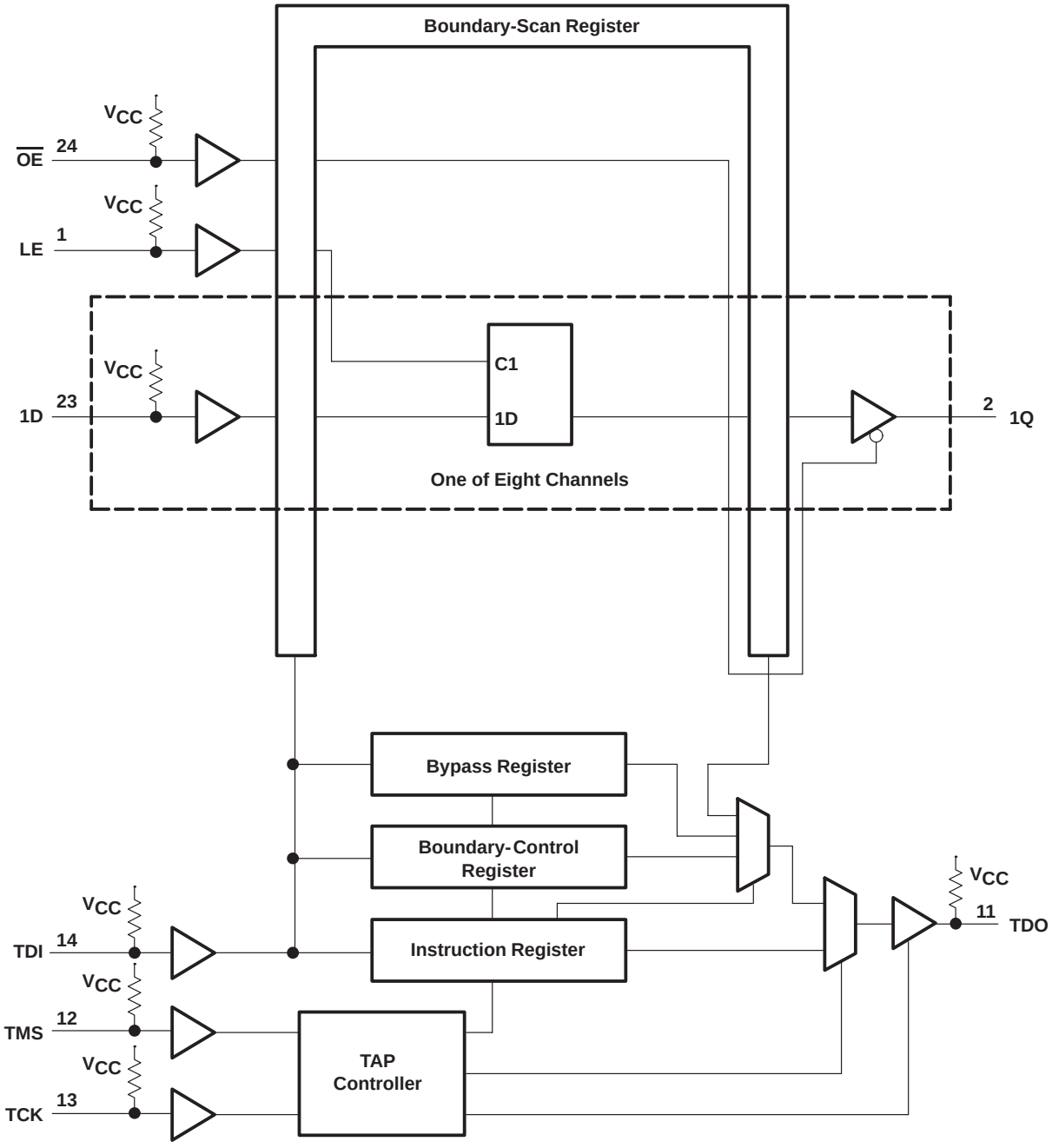
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

functional block diagram



Pin numbers shown are for the DW, JT, and NT packages.

Terminal Functions

TERMINAL NAME	DESCRIPTION
1D–8D	Normal-function data inputs. See function table for normal-mode logic. Internal pullups force these inputs to a high level if left unconnected.
GND	Ground
LE	Normal-function latch-enable input. See function table for normal-mode logic. An internal pullup forces LE to a high level if left unconnected.
$\overline{OE}$	Normal-function output-enable input. See function table for normal-mode logic. An internal pullup forces $\overline{OE}$ to a high level if left unconnected.
1Q–8Q	Normal-function data outputs. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. The TMS pin also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double-high (V_{IHH}), at TMS.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

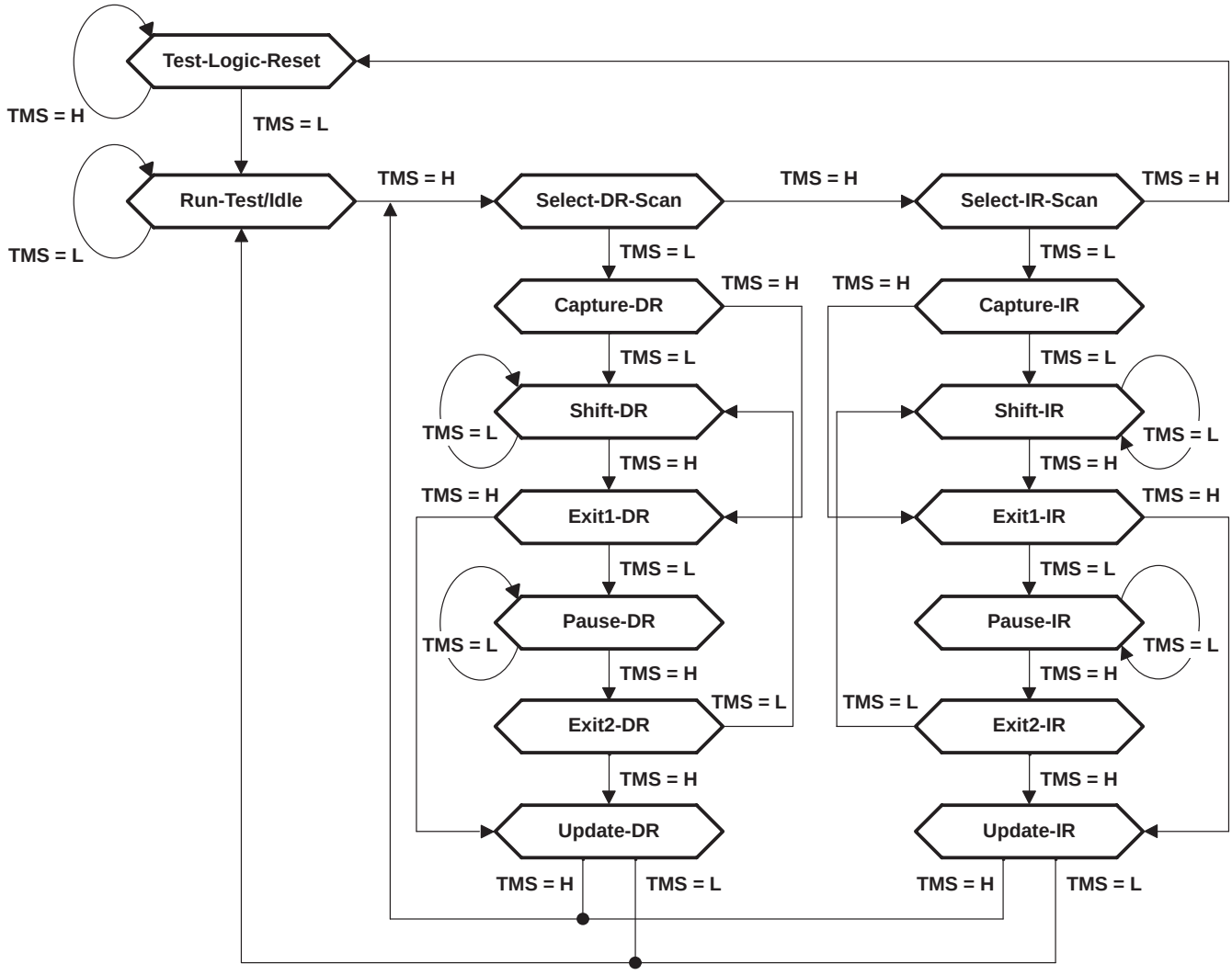


Figure 1. TAP-Controller State Diagram

state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes is to be open circuited.

For the ′BCT8373A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered, following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value, as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the ′BCT8373A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

register overview

With the exception of the bypass register, any test register may be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the ′BCT8373A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

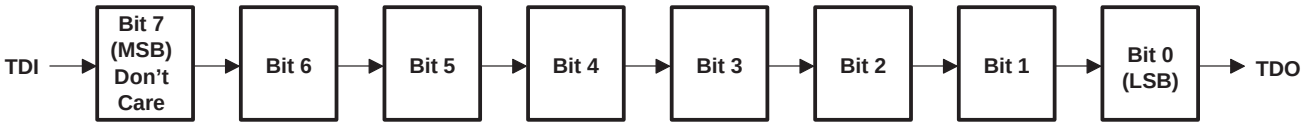


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
17	LE	15	1D	7	1Q
16	$\overline{OE}$	14	2D	6	2Q
–	–	13	3D	5	3Q
–	–	12	4D	4	4Q
–	–	11	5D	3	5Q
–	–	10	6D	2	6Q
–	–	9	7D	1	7Q
–	–	8	8D	0	8Q

boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

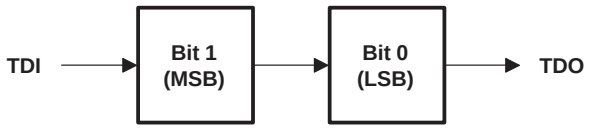


Figure 3. Boundary-Control Register Order of Scan

bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

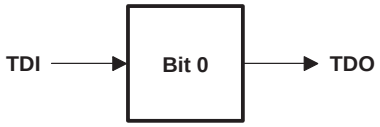


Figure 4. Bypass Register Order of Scan

instruction register opcode description

The instruction register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

Table 2. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST/INTEST	Boundary scan	Boundary scan	Test
X0000001	BYPASS‡	Bypass scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
X0000011	INTEST/EXTEST	Boundary scan	Boundary scan	Test
X0000100	BYPASS‡	Bypass scan	Bypass	Normal
X0000101	BYPASS‡	Bypass scan	Bypass	Normal
X0000110	HIGHZ (TRIBYP)	Control boundary to high impedance	Bypass	Modified test
X0000111	CLAMP (SETBYP)	Control boundary to 1/0	Bypass	Test
X0001000	BYPASS‡	Bypass scan	Bypass	Normal
X0001001	RUNT	Boundary run test	Bypass	Test
X0001010	READBN	Boundary read	Boundary scan	Normal
X0001011	READBT	Boundary read	Boundary scan	Test
X0001100	CELLTST	Boundary self test	Boundary scan	Normal
X0001101	TOPHIP	Boundary toggle outputs	Bypass	Test
X0001110	SCANCN	Boundary-control register scan	Boundary control	Normal
X0001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the ′BCT8373A.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary run test operation in order to specify which test operation is to be executed.

boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 1–0 as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

Table 3. Boundary-Control Register Opcodes

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs (TOPSIP)
01	Pseudo-random pattern generation / 16-bit mode (PRPG)
10	Parallel signature analysis / 16-bit mode (PSA)
11	Simultaneous PSA and PRPG / 8-bit mode (PSA/PRPG)

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSC (bit 16 of the BSR) does control the drive state (active or high impedance) of the device output terminals.

sample inputs / toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data is also updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 illustrates the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

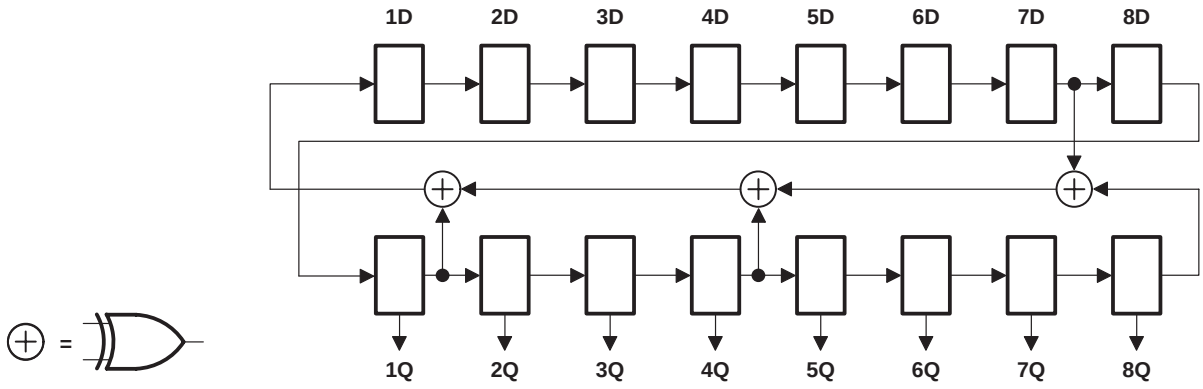


Figure 5. 16-Bit PRPG Configuration

parallel signature analysis (PSA)

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 illustrates the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

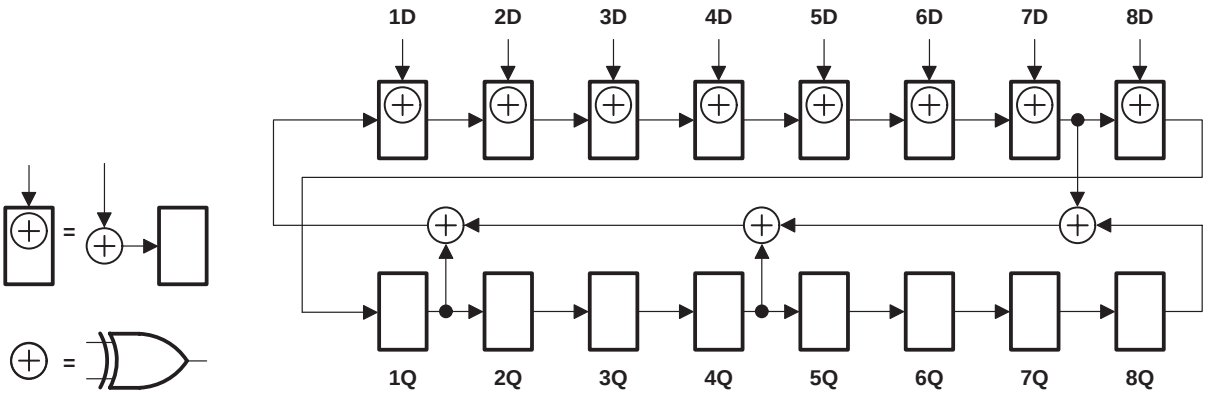


Figure 6. 16-Bit PSA Configuration

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 illustrates the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

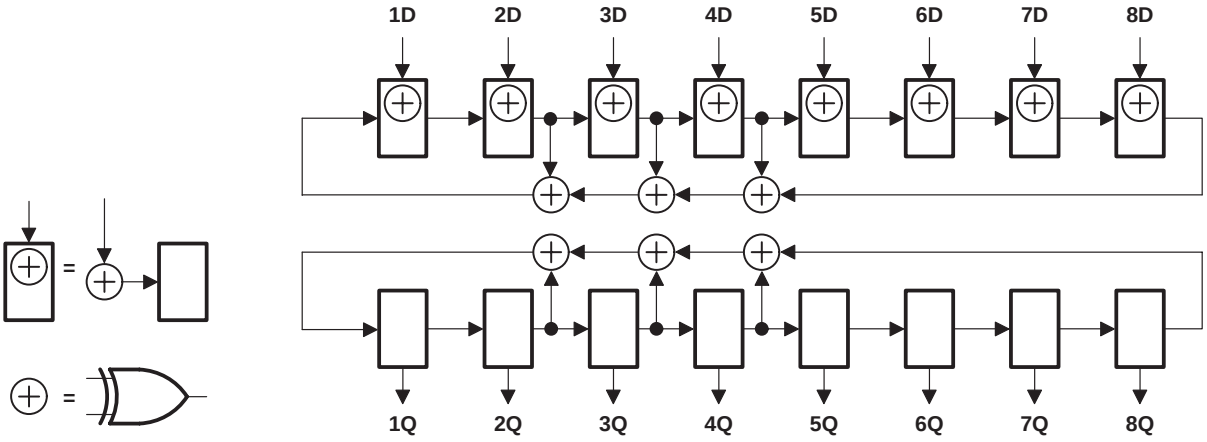


Figure 7. 8-Bit PSA/PRPG Configuration

timing description

All test operations of the ′BCT8373A are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

Table 4. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

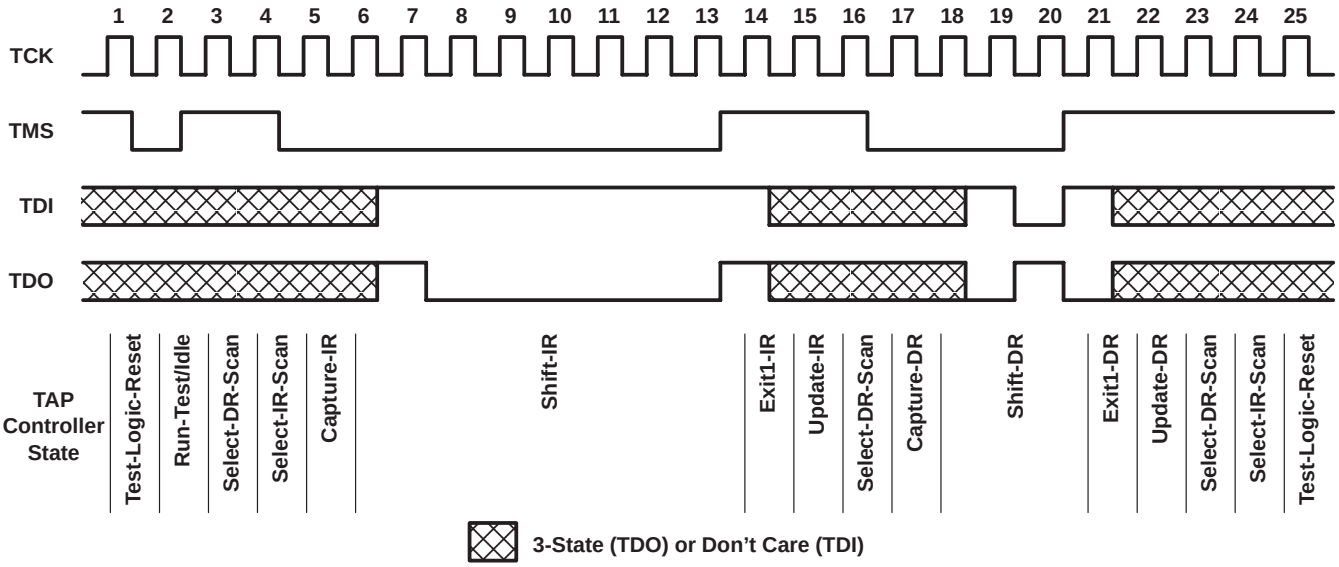


Figure 8. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except TMS (see Note 1) . . . . . –0.5 V to 7 V
TMS (see Note 1) . . . . . –0.5 V to 12 V
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Input clamp current . . . . . –30 mA
Current into any output in the low state: SN54BCT8373A (TDO) . . . . . 40 mA
SN54BCT8373A (Any Q) . . . . . 96 mA
SN74BCT8373A (TDO) . . . . . 48 mA
SN74BCT8373A (Any Q) . . . . . 128 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

			SN54BCT8373A			SN74BCT8373A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IHH}	Double-high-level input voltage	TMS	10		12	10		12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	TDO			–3			–3	mA
		Any Q			–12			–15	
I_{OL}	Low-level output current	TDO			20			24	mA
		Any Q			48			64	
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54BCT8373A			SN74BCT8373A			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	Any Q	V_{CC} = 4.75 V,	I_{OH} = –3 mA		2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V	I_{OH} = –3 mA		2.4	3.4		2.4	3.4		
			I_{OH} = –12 mA		2	3.2					
			I_{OH} = –15 mA					2	3.1		
	TDO	V_{CC} = 4.75 V,	I_{OH} = –1 mA		2.7	3.4		2.7	3.4		
		V_{CC} = 4.5 V	I_{OH} = –1 mA		2.5	3.4		2.5	3.4		
			I_{OH} = –3 mA		2.4	3.3		2.4	3.3		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.38	0.55				V
			I_{OL} = 64 mA						0.42	0.55	
	TDO	V_{CC} = 4.5 V	I_{OL} = 20 mA			0.3	0.5				
			I_{OL} = 24 mA						0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V		–1	–35	–100	–1	–35	–100	µA
I_{IHH}	TMS	V_{CC} = 5.5 V,	V_I = 10 V				1			1	mA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.5 V		–30	–70	–200	–30	–70	–200	µA
I_{OZH}	Any Q	V_{CC} = 5.5 V,	V_O = 2.7 V				50			50	µA
	TDO				–1	–35	–100	–1	–35	–100	
I_{OZL}	Any Q	V_{CC} = 5.5 V,	V_O = 0.5 V				–50			–50	µA
	TDO				–30	–70	–200	–30	–70	–200	
I_{OZPU}		V_{CC} = 0 to 2 V,	V_O = 0.5 V or 2.7 V				±250			±250	µA
I_{OZPD}		V_{CC} = 2 V to 0,	V_O = 0.5 V or 2.7 V				±250			±250	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±250			±250	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0		–100		–225	–100		–225	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open	Outputs high		3.5	7.5		3.5	7.5	mA
				Outputs low		35	52		35	52	
				Outputs disabled		1.5	3.5		1.5	3.5	
C_i		V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			10			10		pF
C_o		V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)

			V_{CC} = 5 V, T_A = 25°C		SN54BCT8373A		SN74BCT8373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	LE high	5		5		5		ns
t_{su}	Setup time	Data before LE↓	3		3		3		ns
t_h	Hold time	Data after LE↓	2		2		2		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

			V_{CC} = 5 V, T_A = 25°C		SN54BCT8373A		SN74BCT8373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	0	20	MHz
t_w	Pulse duration	TCK high or low	25		25		25		ns
		TMS double high	50*		50*		50		
t_{su}	Setup time	Any D before TCK↑	6		6		6		ns
		LE or $\overline{OE}$ before TCK↑	6		6		6		
		TDI before TCK↑	6		6		6		
		TMS before TCK↑	12		12		12		
t_h	Hold time	Any D after TCK↑	4.5		4.5		4.5		ns
		LE or $\overline{OE}$ after TCK↑	4.5		4.5		4.5		
		TDI after TCK↑	4.5		4.5		4.5		
		TMS after TCK↑	0		0		0		
t_d	Delay time	Power up to TCK↑	100*		100*		100		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

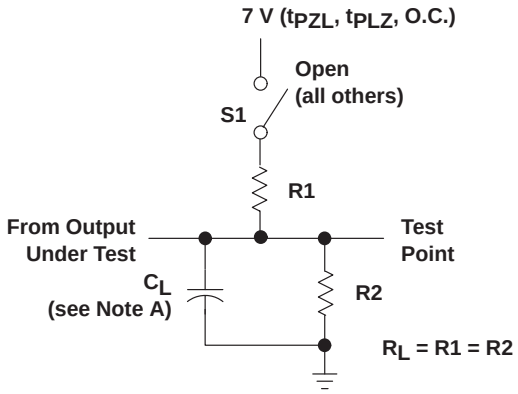
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT8373A		SN74BCT8373A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	6.5	8.5	3	10.5	3	9.5	ns
t_{PHL}			3	6.2	8	3	10.5	3	9.5	
t_{PLH}	LE	Q	3	6.8	9	3	11	3	10	ns
t_{PHL}			3	6.7	8.5	3	11	3	10	
t_{PZH}	OE	Q	3	6.5	8.5	3	10.5	3	10	ns
t_{PZL}			3.5	7.5	9.5	3.5	11.5	3.5	11	
t_{PHZ}	$\overline{OE}$	Q	3	6.1	8	3	10	3	9	ns
t_{PLZ}			2.5	5.8	7.5	2.5	9.5	2.5	8.5	

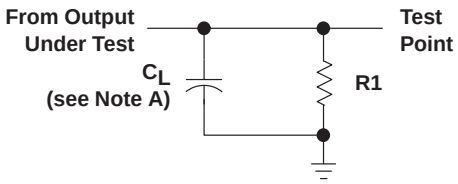
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT8373A		SN74BCT8373A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			20			20		20		MHz
t_{PLH}	TCK↓	Q	6	13	15.5	6	21.5	6	20	ns
t_{PHL}			6	12.5	15.5	6	21.5	6	20	ns
t_{PLH}	TCK↓	TDO	3.5	7.6	10.5	3.5	14	3.5	13	ns
t_{PHL}			3.5	8	10.5	3.5	13	3.5	12	
t_{PLH}	TCK↑	Q	7.5	16.5	20	7.5	28	7.5	24	ns
t_{PHL}			7.5	17	21	7.5	29	7.5	25	
t_{PZH}	TCK↓	Q	6.5	14	17	6.5	24	6.5	21	ns
t_{PZL}			7	15	20	7	26	7	23	
t_{PZH}	TCK↓	TDO	3.5	7.6	10.5	3.5	11.5	3.5	11	ns
t_{PZL}			4	8.5	11	4	13.5	4	12.5	
t_{PZH}	TCK↑	Q	8	18	22	8	30	8	27	ns
t_{PZL}			8	19	25	8	32	8	29	
t_{PHZ}	TCK↓	Q	6	14	18	6	24	6	22	ns
t_{PLZ}			6	14	17	6	23	6	21	
t_{PHZ}	TCK↓	TDO	3	8	11.5	3	13	3	12.5	ns
t_{PLZ}			3	7.5	10	3	13	3	12	
t_{PHZ}	TCK↑	Q	8	18.5	22	8	31	8	27	ns
t_{PLZ}			8	18.5	22	8	31	8	27	

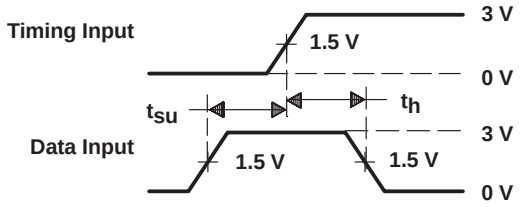
PARAMETER MEASUREMENT INFORMATION



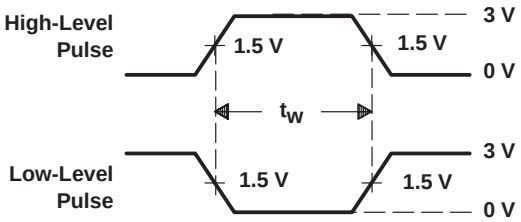
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



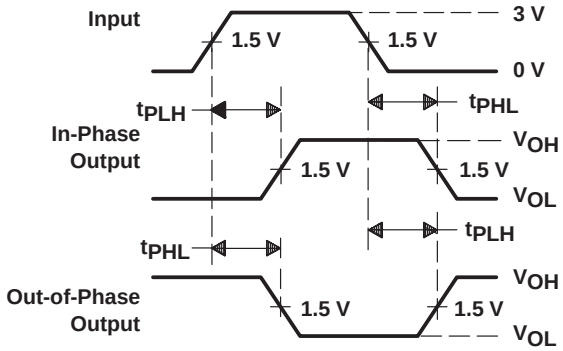
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



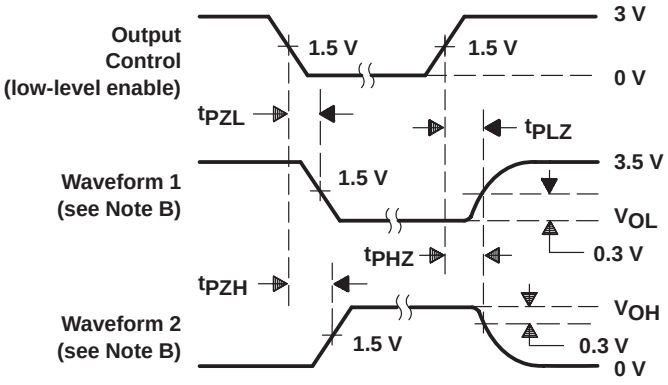
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 9. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9172501M3A	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501M3A SNJ54BCT 8373AFK
5962-9172501MLA	Active	Production	CDIP (JT) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501MLA SNJ54BCT8373AJT
SN74BCT8373ADW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT8373A
SN74BCT8373ADW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT8373A
SNJ54BCT8373AFK	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501M3A SNJ54BCT 8373AFK
SNJ54BCT8373AFK.A	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501M3A SNJ54BCT 8373AFK
SNJ54BCT8373AJT	Active	Production	CDIP (JT) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501MLA SNJ54BCT8373AJT
SNJ54BCT8373AJT.A	Active	Production	CDIP (JT) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9172501MLA SNJ54BCT8373AJT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

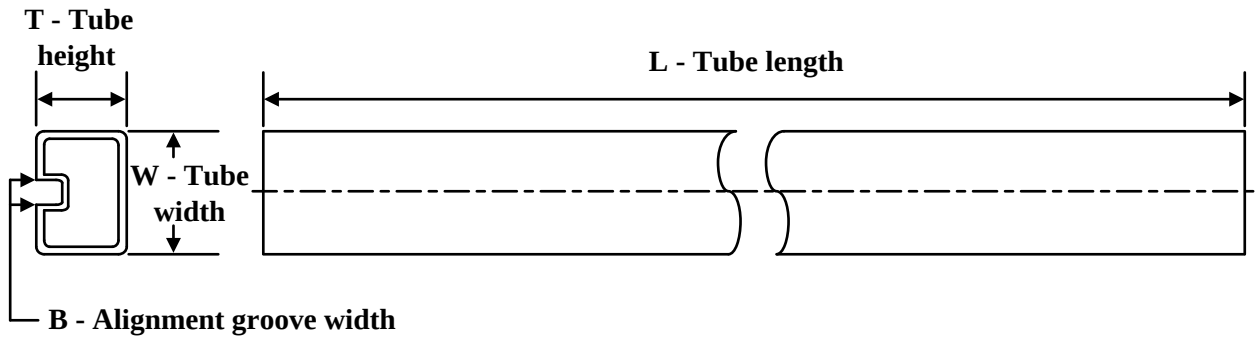
OTHER QUALIFIED VERSIONS OF SN54BCT8373A, SN74BCT8373A :

- Catalog : SN74BCT8373A
- Military : SN54BCT8373A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



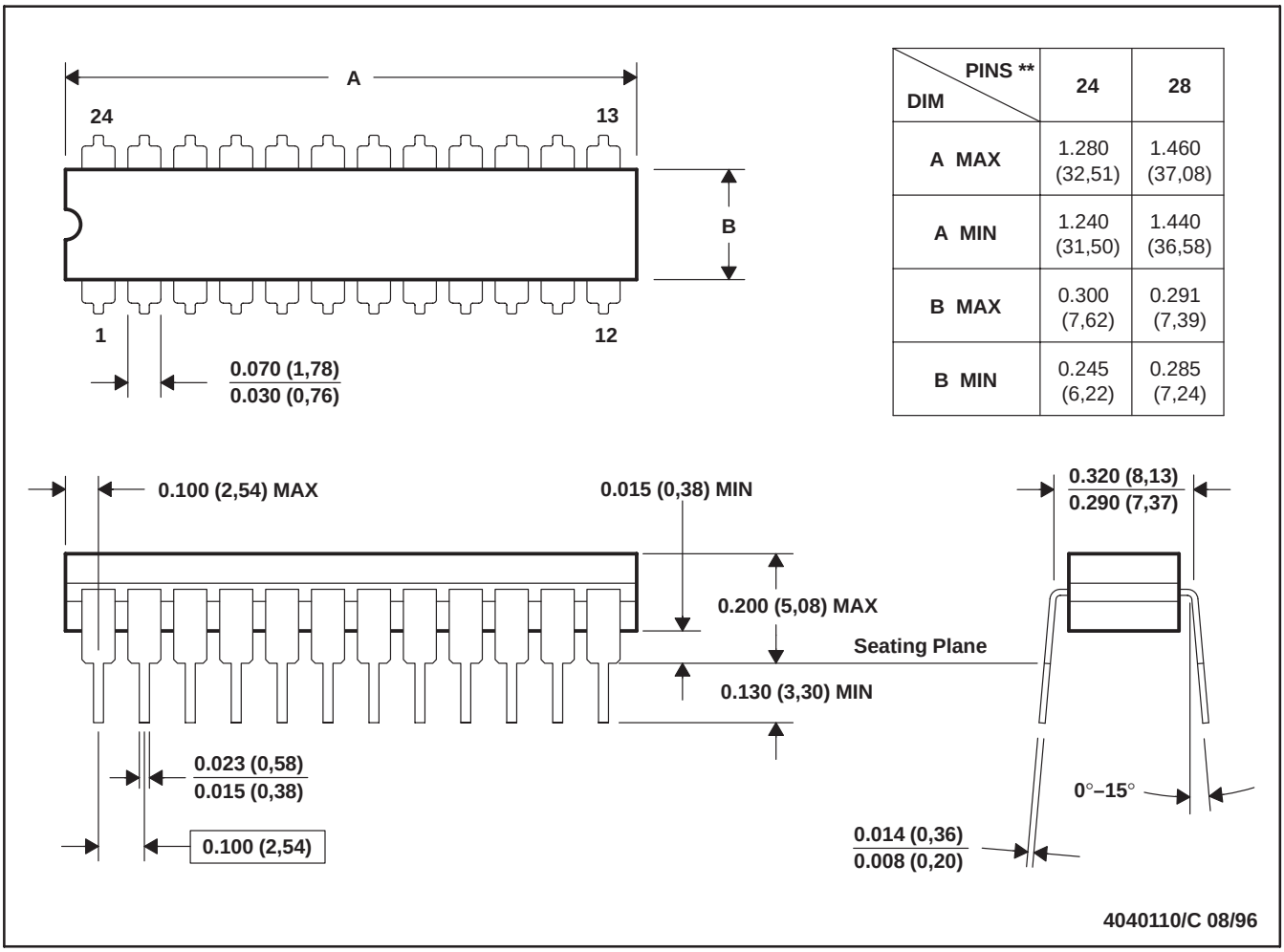
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74BCT8373ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74BCT8373ADW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN

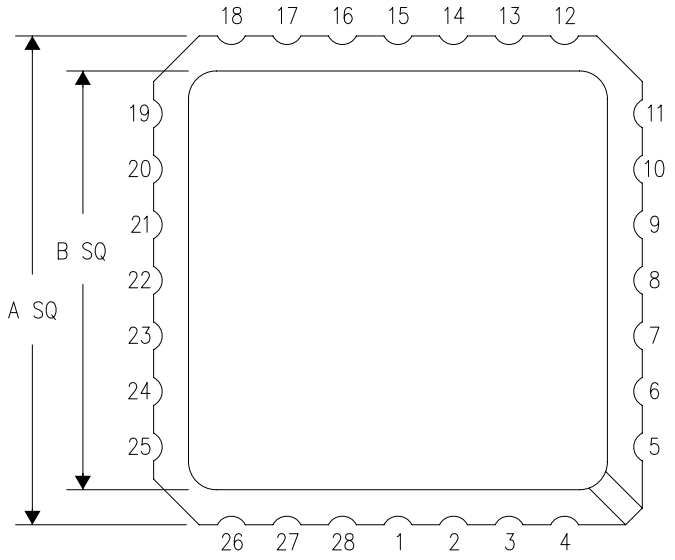


DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

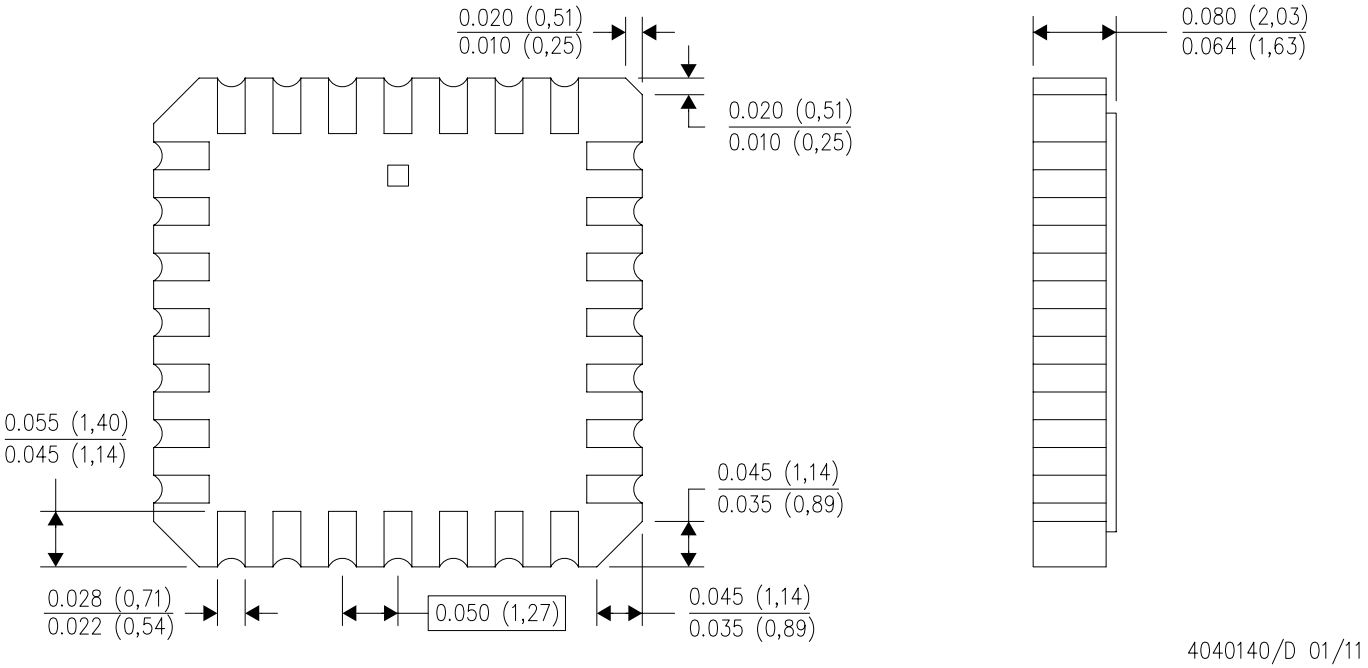
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



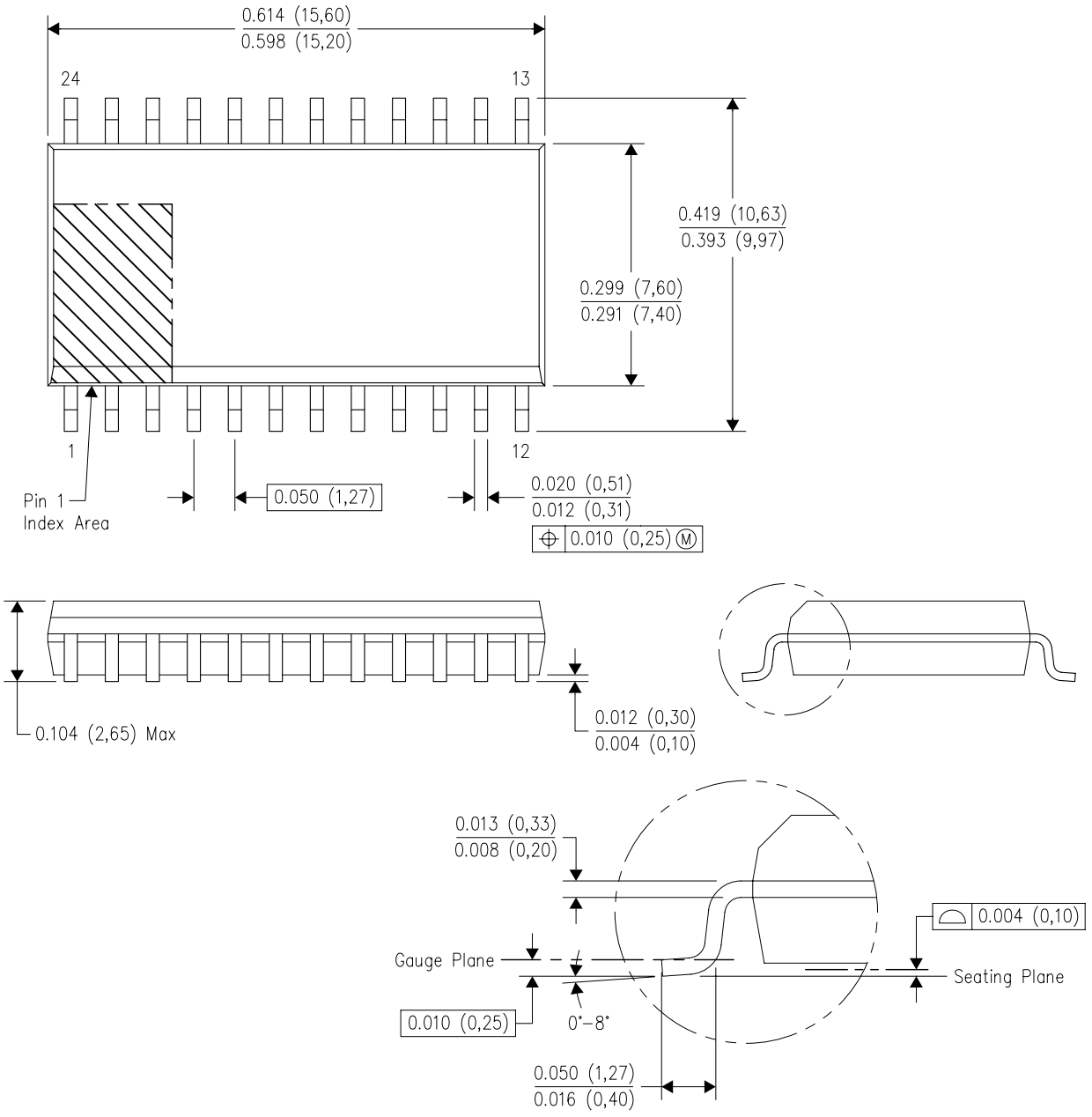
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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