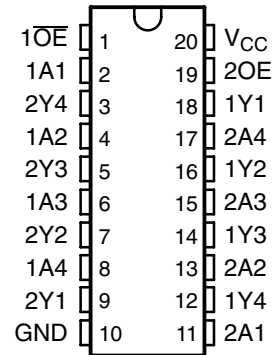


SN74BCT757 OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

SCBS041D – NOVEMBER 1989 – REVISED NOVEMBER 1993

- BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

DW OR N PACKAGE
(TOP VIEW)



description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. This device provides complementary output-enable (OE and \overline{OE}) inputs and noninverting outputs.

The SN74BCT757 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

| INPUTS | | OUTPUT |
|------------------|----|--------|
| $\overline{1OE}$ | 1A | 1Y |
| H | X | H |
| L | L | L |
| L | H | H |

| INPUTS | | OUTPUT |
|--------|----|--------|
| 2OE | 2A | 2Y |
| L | X | H |
| H | L | L |
| H | H | H |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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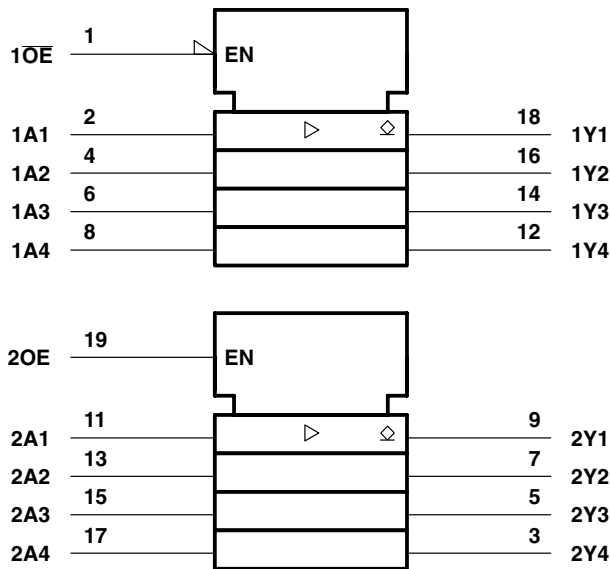
SN74BCT757

OCTAL BUFFER/DRIVER

WITH OPEN-COLLECTOR OUTPUTS

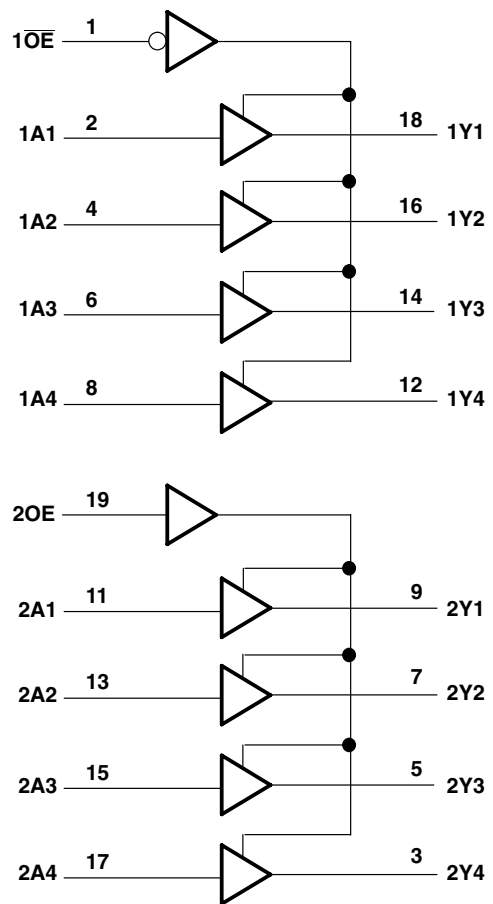
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|--------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I | -0.5 V to 7 V |
| Input current range, I_I | -30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state, V_O | -0.5 V to 5.5 V |
| Voltage range applied to any output in the high state, V_O | -0.5 V to V_{CC} |
| Current into any output in the low state, I_O | 128 mA |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| V_{OH} | High-level output voltage | | | 5.5 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OL} | Low-level output current | | | 64 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

NOTE 1: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------|---------------------------|--|---------------------------------|------|------|------|
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OL} | $V_{CC} = 4.5\text{ V}$, | $I_{OL} = 64\text{ mA}$ | | 0.42 | 0.55 | V |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.5\text{ V}$ | | | -1 | mA |
| I_{OH} | $V_{CC} = 4.5\text{ V}$, | $V_{OH} = 5.5\text{ V}$ | | | 0.1 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, | Outputs open | Outputs high | | 34 | mA |
| | | | Outputs low | | 77 | |
| | | | OE and \overline{OE} inactive | | 10 | |
| C_i | $V_{CC} = 5\text{ V}$, | $V_I = 2.5\text{ V}$ or 0.5 V | | 6 | | pF |
| C_o | $V_{CC} = 5\text{ V}$, | $V_O = 2.5\text{ V}$ or 0.5 V | | 4 | | pF |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-----------|------------------|-------------|---|------|------|------|------|------|
| | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | 6.9 | 8.3 | 9.6 | 6.6 | 10.1 | ns |
| t_{PHL} | | | 2.4 | 4.2 | 6 | 2 | 6.6 | |
| t_{PLH} | 2OE | Y | 11 | 14.8 | 17.9 | 10.8 | 19.7 | ns |
| t_{PHL} | | | 2.9 | 4.6 | 6.2 | 2.6 | 6.9 | |
| t_{PLH} | $1\overline{OE}$ | Y | 11.4 | 13.9 | 16.1 | 10 | 18 | ns |
| t_{PHL} | | | 4.4 | 6.1 | 7.8 | 4 | 8.5 | |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74BCT757DW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT757 |
| SN74BCT757DW.A | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | BCT757 |
| SN74BCT757N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74BCT757N |
| SN74BCT757N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74BCT757N |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74BCT757DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74BCT757DW.A | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74BCT757N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74BCT757N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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