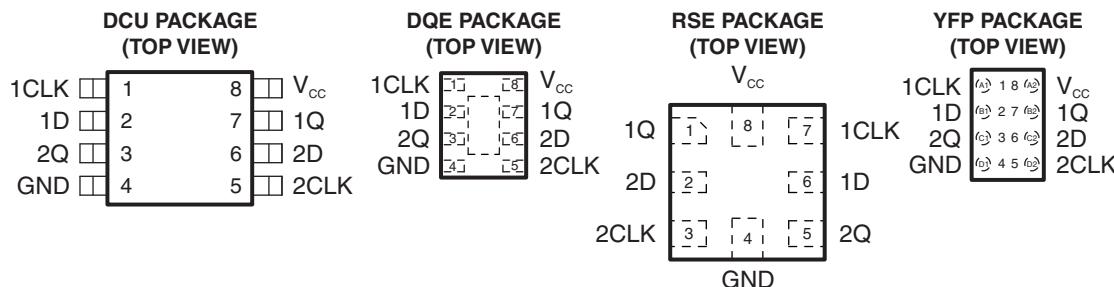


LOW-POWER DUAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP

Check for Samples: [SN74AUP2G79](#)

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{cc} = 0.9 \mu A$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 3 \text{ pF}$ Typ at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot <10% of V_{cc}
- I_{off} Supports Partial-Power-Down Mode Operation
- Wide Operating V_{cc} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{cc} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).

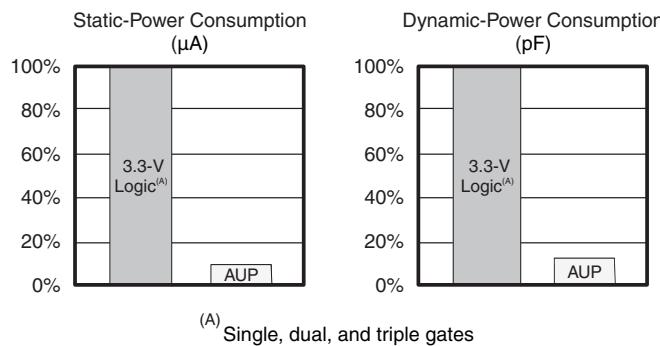
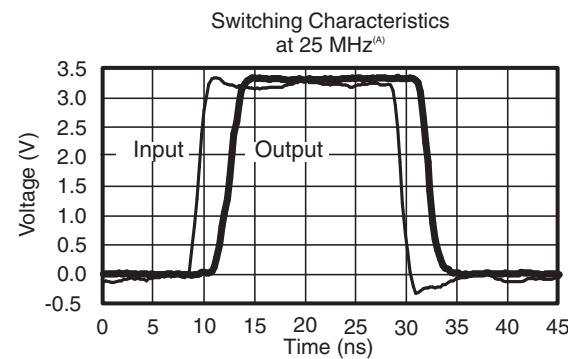


Figure 1. AUP – The Lowest-Power Family



(A) SN74AUP2Gxx data at $C_L = 15 \text{ pF}$.

Figure 2. Excellent Signal Integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. NanoStar is a trademark of Texas Instruments.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoStar™ – WLCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G79YFPR _ _ H W _
	uQFN – DQE	Reel of 5000	SN74AUP2G79DQER PT
	QFN – RSE	Reel of 5000	SN74AUP2G79RSER PT
	SSOP – DCU	Reel of 3000	SN74AUP2G79DCUR H79_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

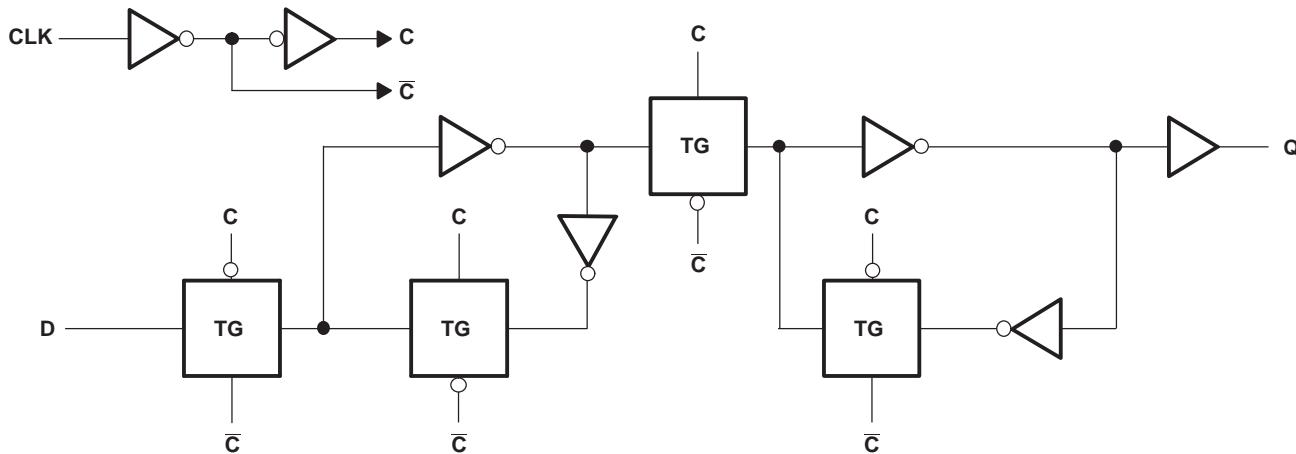
(3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q ₀
H	X	Q ₀

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Pin numbers shown are for the DCU and DQE packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
I_O	Continuous output current		±20	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCU package	220	°C/W
		DQE package	261	
		RSE package	253	
		YFP package	132	
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8 \text{ V}$	V_{CC}	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8 \text{ V}$	0	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.9	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8 \text{ V}$	-20	μA
		$V_{CC} = 1.1 \text{ V}$	-1.1	
		$V_{CC} = 1.4 \text{ V}$	-1.7	
		$V_{CC} = 1.65 \text{ V}$	-1.9	
		$V_{CC} = 2.3 \text{ V}$	-3.1	
		$V_{CC} = 3 \text{ V}$	-4	
I_{OL}	Low-level output current	$V_{CC} = 0.8 \text{ V}$	20	μA
		$V_{CC} = 1.1 \text{ V}$	1.1	
		$V_{CC} = 1.4 \text{ V}$	1.7	
		$V_{CC} = 1.65 \text{ V}$	1.9	
		$V_{CC} = 2.3 \text{ V}$	3.1	
		$V_{CC} = 3 \text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	200	ns/V
T_A	Operating free-air temperature		-40	85 °C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 µA	0.8 V to 3.6 V	V _{CC} – 0.1		V _{CC} – 0.1			V
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}			
	I _{OH} = -1.7 mA	1.4 V	1.11		1.03			
	I _{OH} = -1.9 mA	1.65 V	1.32		1.3			
	I _{OH} = -2.3 mA	2.3 V	2.05		1.97			
	I _{OH} = -3.1 mA		1.9		1.85			
	I _{OH} = -2.7 mA	3 V	2.72		2.67			
	I _{OH} = -4 mA		2.6		2.55			
V _{OL}	I _{OL} = 20 µA	0.8 V to 3.6 V		0.1		0.1		V
	I _{OL} = 1.1 mA	1.1 V		0.3 × V _{CC}		0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V		0.31		0.37		
	I _{OL} = 1.9 mA	1.65 V		0.31		0.35		
	I _{OL} = 2.3 mA	2.3 V		0.31		0.33		
	I _{OL} = 3.1 mA			0.44		0.45		
	I _{OL} = 2.7 mA	3 V		0.31		0.33		
	I _{OL} = 4 mA			0.44		0.45		
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	µA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.2		0.6	µA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V		0.2		0.6	µA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V		0.5		0.9	µA
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V		40		50	µA
C _i		V _I = V _{CC} or GND	0 V		1.5			pF
			3.6 V		1.5			
C _o		V _O = GND	0 V		3			pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

		V _{cc}	T _A = 25°C	T _A = -40°C to 85°C	UNIT
			TYP	MIN MAX	
f _{clock}	Clock frequency	0.8 V		20	MHz
		1.2 V ± 0.1 V		80	
		1.5 V ± 0.1 V		100	
		1.8 V ± 0.15 V		140	
		2.5 V ± 0.2 V		210	
		3.3 V ± 0.3 V		260	
t _w	Pulse duration, CLK high or low	0.8 V		4.8	ns
		1.2 V ± 0.1 V		2.2	
		1.5 V ± 0.1 V		1.5	
		1.8 V ± 0.15 V		1.6	
		2.5 V ± 0.2 V		1.7	
		3.3 V ± 0.3 V		1.9	
t _{su}	Setup time before CLK↑	Data high	0.8 V	2.9	ns
			1.2 V ± 0.1 V	1.4	
			1.5 V ± 0.1 V	1	
			1.8 V ± 0.15 V	0.9	
			2.5 V ± 0.2 V	0.7	
			3.3 V ± 0.3 V	0.6	
		Data low	0.8 V	3.5	
			1.2 V ± 0.1 V	1.8	
			1.5 V ± 0.1 V	1.2	
			1.8 V ± 0.15 V	1.1	
			2.5 V ± 0.2 V	1	
			3.3 V ± 0.3 V	1	
t _h	Hold time, data after CLK↑	0.8 V	0	0	ns
		1.2 V ± 0.1 V		0	
		1.5 V ± 0.1 V		0	
		1.8 V ± 0.15 V		0	
		2.5 V ± 0.2 V		0	
		3.3 V ± 0.3 V		0	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		93		90		MHz
			1.2 V ± 0.1 V		199		220		
			1.5 V ± 0.1 V		250		230		
			1.8 V ± 0.15 V		271		240		
			2.5 V ± 0.2 V		280		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		15.9				ns
			1.2 V ± 0.1 V	3.7	6.9	11	2.6	13.1	
			1.5 V ± 0.1 V	3	4.8	7.6	2	8.8	
			1.8 V ± 0.15 V	2.4	3.8	6.1	1.5	7.1	
			2.5 V ± 0.2 V	1.8	2.7	4.4	1.1	5	
			3.3 V ± 0.3 V	1.5	2.1	3.6	0.9	4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		62		50		MHz
			1.2 V ± 0.1 V		147		160		
			1.5 V ± 0.1 V		189		200		
			1.8 V ± 0.15 V		180		240		
			2.5 V ± 0.2 V		260		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		18				ns
			1.2 V ± 0.1 V	4.3	7.8	12.3	3.2	14.4	
			1.5 V ± 0.1 V	3.5	5.5	8.4	2.5	9.8	
			1.8 V ± 0.15 V	2.8	4.4	6.8	1.9	8	
			2.5 V ± 0.2 V	2.2	3.2	5	1.5	5.7	
			3.3 V ± 0.3 V	1.8	2.6	4.1	1.3	4.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		48		30		MHz
			1.2 V ± 0.1 V		112		120		
			1.5 V ± 0.1 V		151		160		
			1.8 V ± 0.15 V		194		220		
			2.5 V ± 0.2 V		248		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		20.3				ns
			1.2 V ± 0.1 V	5	8.7	13.6	3.9	15.6	
			1.5 V ± 0.1 V	4.1	6.3	9.3	3.1	10.7	
			1.8 V ± 0.15 V	3.3	4	7.6	2.4	8.7	
			2.5 V ± 0.2 V	2.6	3.6	5.5	1.9	6.3	
			3.3 V ± 0.3 V	2.2	3	4.5	1.6	5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

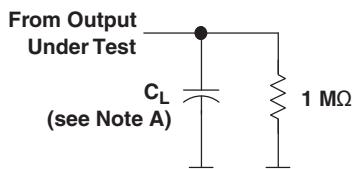
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		24		20		MHz
			1.2 V ± 0.1 V		72		80		
			1.5 V ± 0.1 V		100		100		
			1.8 V ± 0.15 V		127		140		
			2.5 V ± 0.2 V		185		210		
			3.3 V ± 0.3 V		266		260		
t_{pd}	CLK	Q	0.8 V		27.2				ns
			1.2 V ± 0.1 V	7	11.5	17.3	5.9	24	
			1.5 V ± 0.1 V	5.7	8.3	13.3	4.6	15.9	
			1.8 V ± 0.15 V	4.7	6.7	11.3	3.8	13	
			2.5 V ± 0.2 V	3.7	4.9	7.8	2.9	9	
			3.3 V ± 0.3 V	3.2	4.1	6.3	2.6	7.2	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

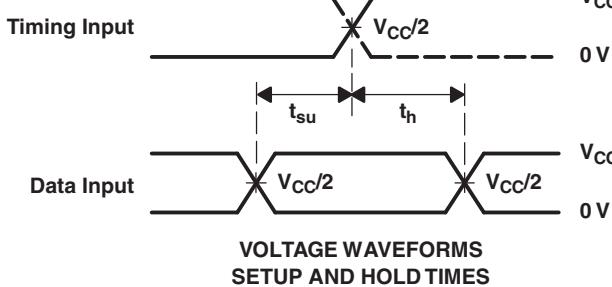
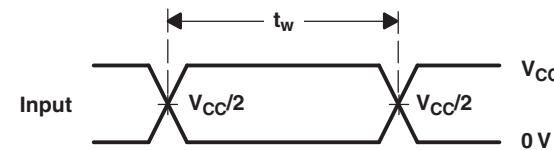
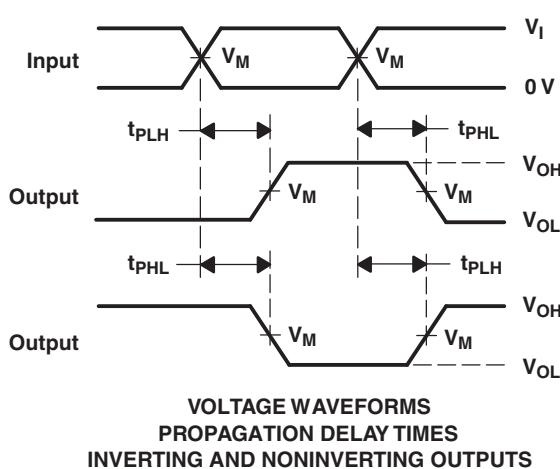
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	2.5	pF
		1.2 V ± 0.1 V	2.5	
		1.5 V ± 0.1 V	2.5	
		1.8 V ± 0.15 V	2.5	
		2.5 V ± 0.2 V	3	
		3.3 V ± 0.3 V	3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

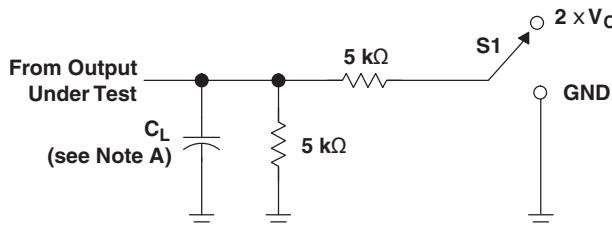
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$
C_L V_M V_I	5, 10, 15, 30 pF $V_{CC}/2$ V_{CC}					



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, for propagation delays $t_f/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_f/t_f = 1.2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

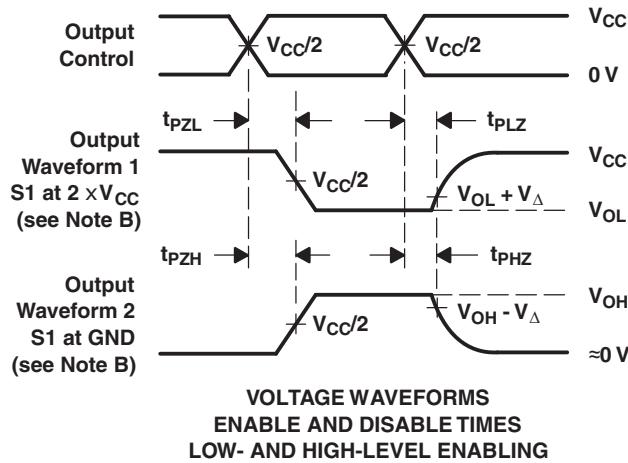
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	2 x V _{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision B (March 2010) to Revision C	Page
• Added clock high to FUNCTION TABLE.	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP2G79DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R
SN74AUP2G79DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R
SN74AUP2G79DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R
SN74AUP2G79DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R
SN74AUP2G79DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PT
SN74AUP2G79DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PT
SN74AUP2G79RSER	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PT
SN74AUP2G79RSER.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

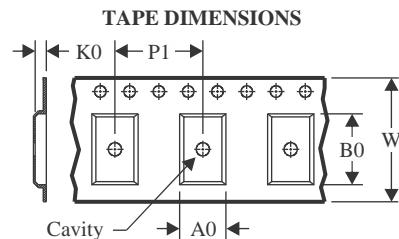
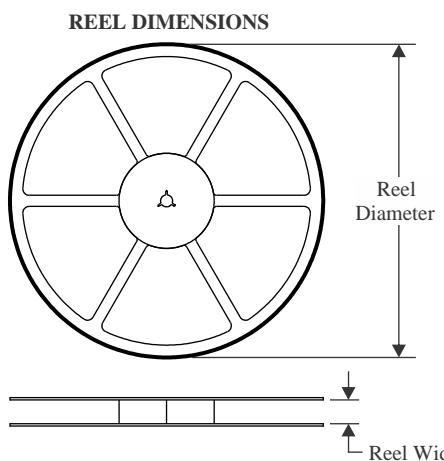
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

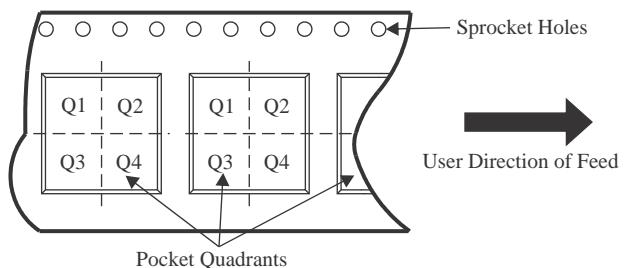
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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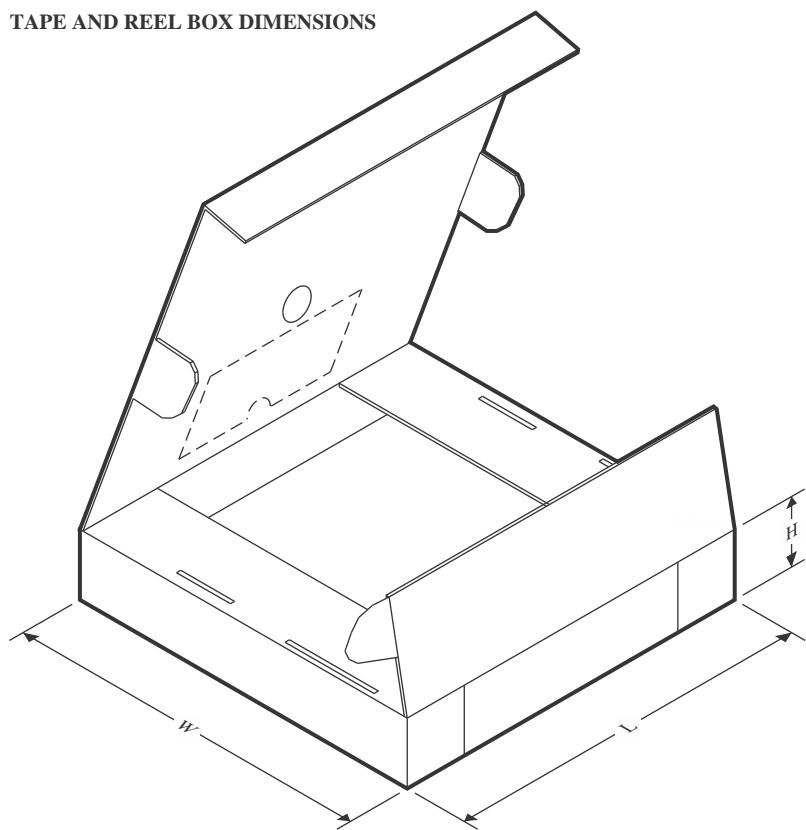
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G79DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G79DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G79DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G79RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G79DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G79DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G79DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G79RSER	UQFN	RSE	8	5000	202.0	201.0	28.0

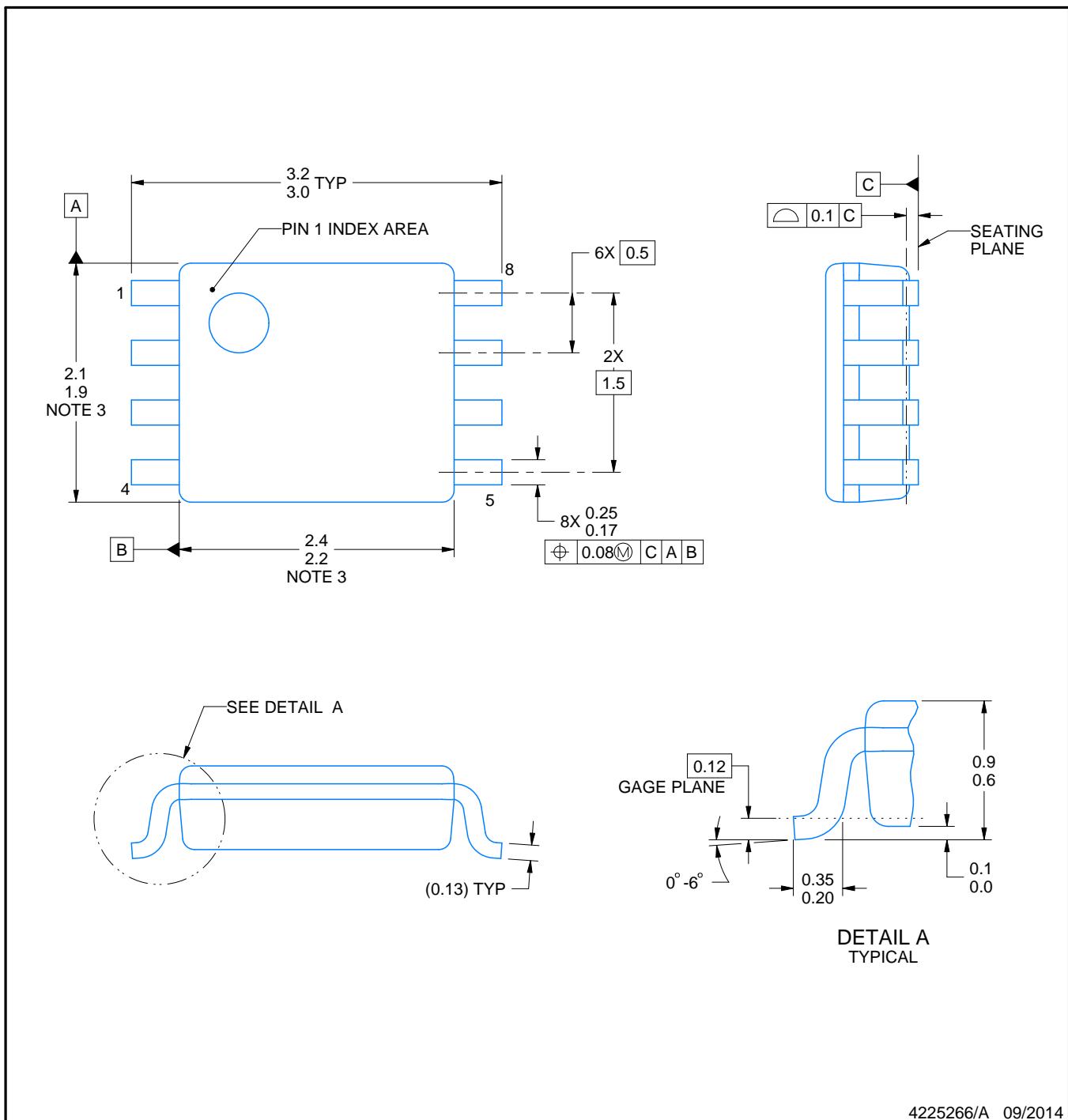
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



NOTES:

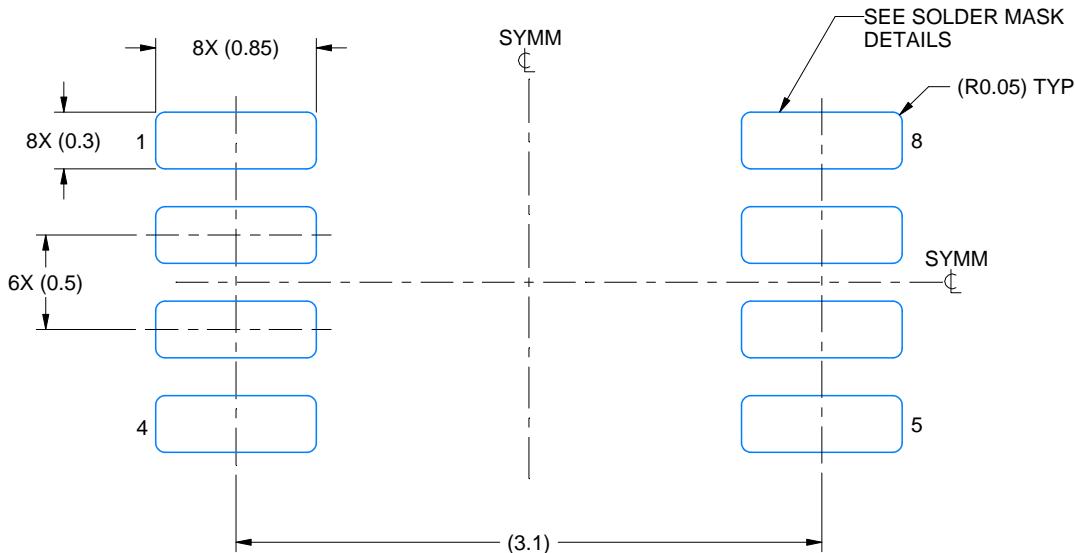
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

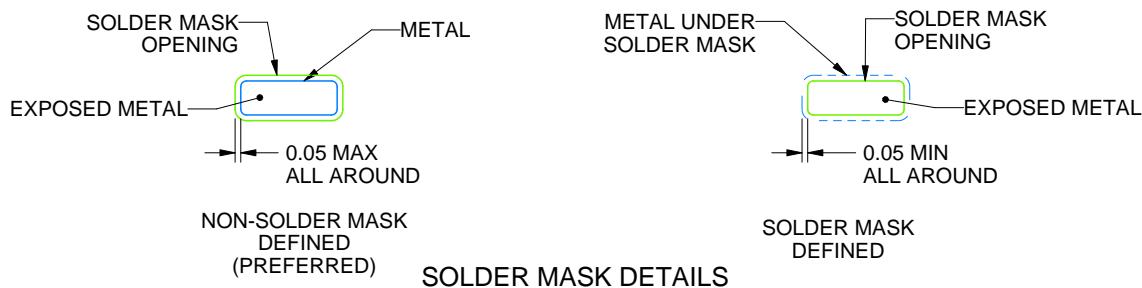
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

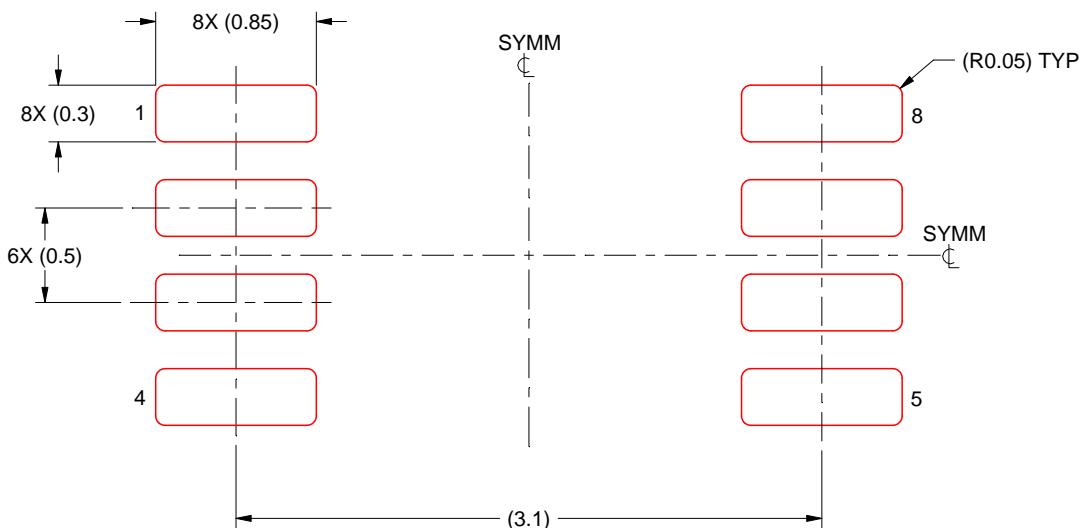
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

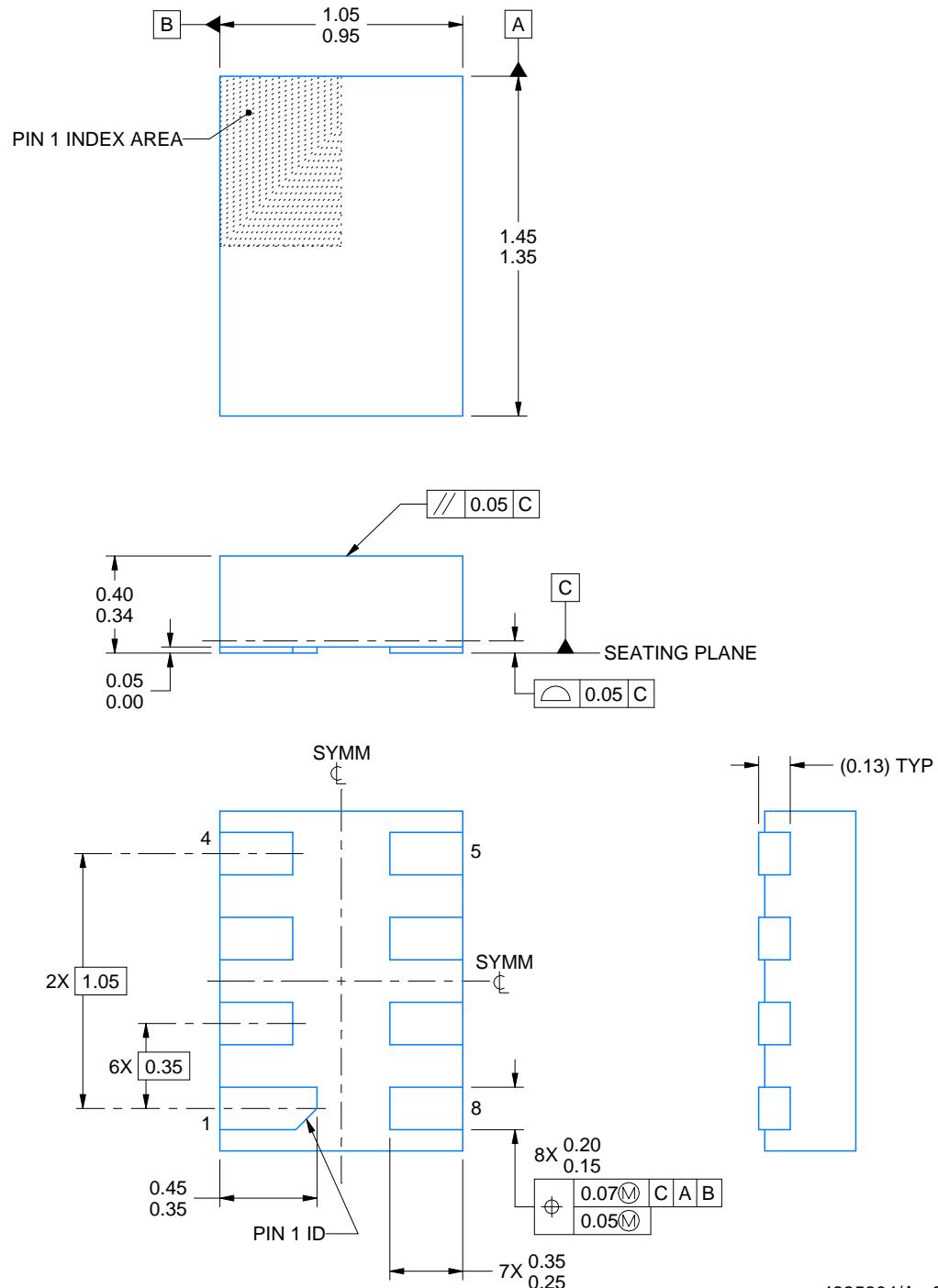
PACKAGE OUTLINE

DQE0008A



X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4225204/A 08/2019

NOTES:

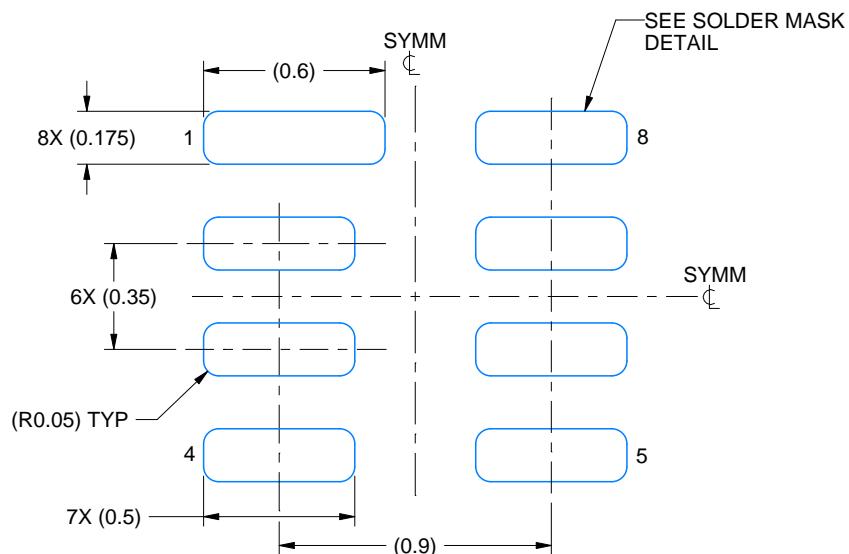
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

EXAMPLE BOARD LAYOUT

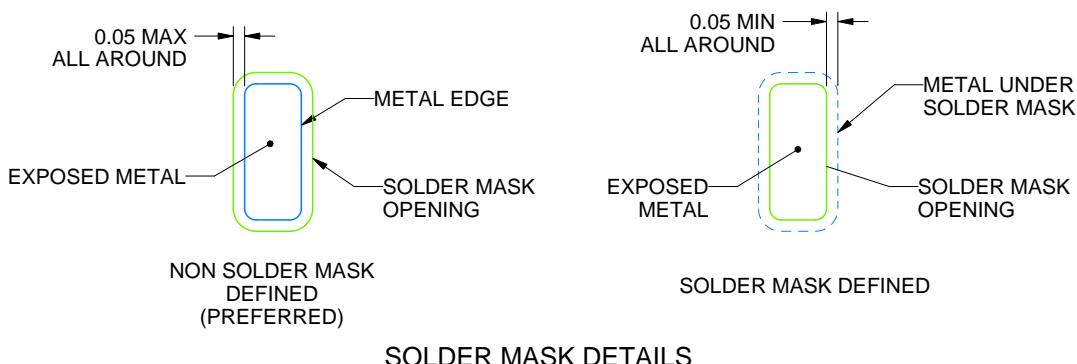
DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



4225204/A 08/2019

NOTES: (continued)

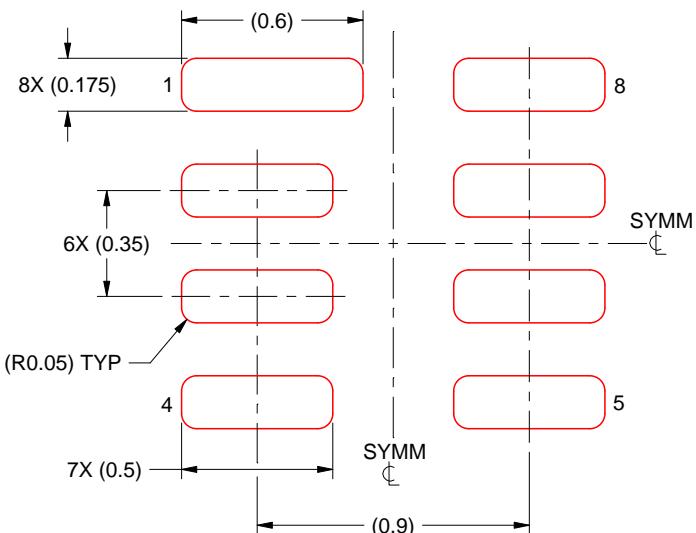
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

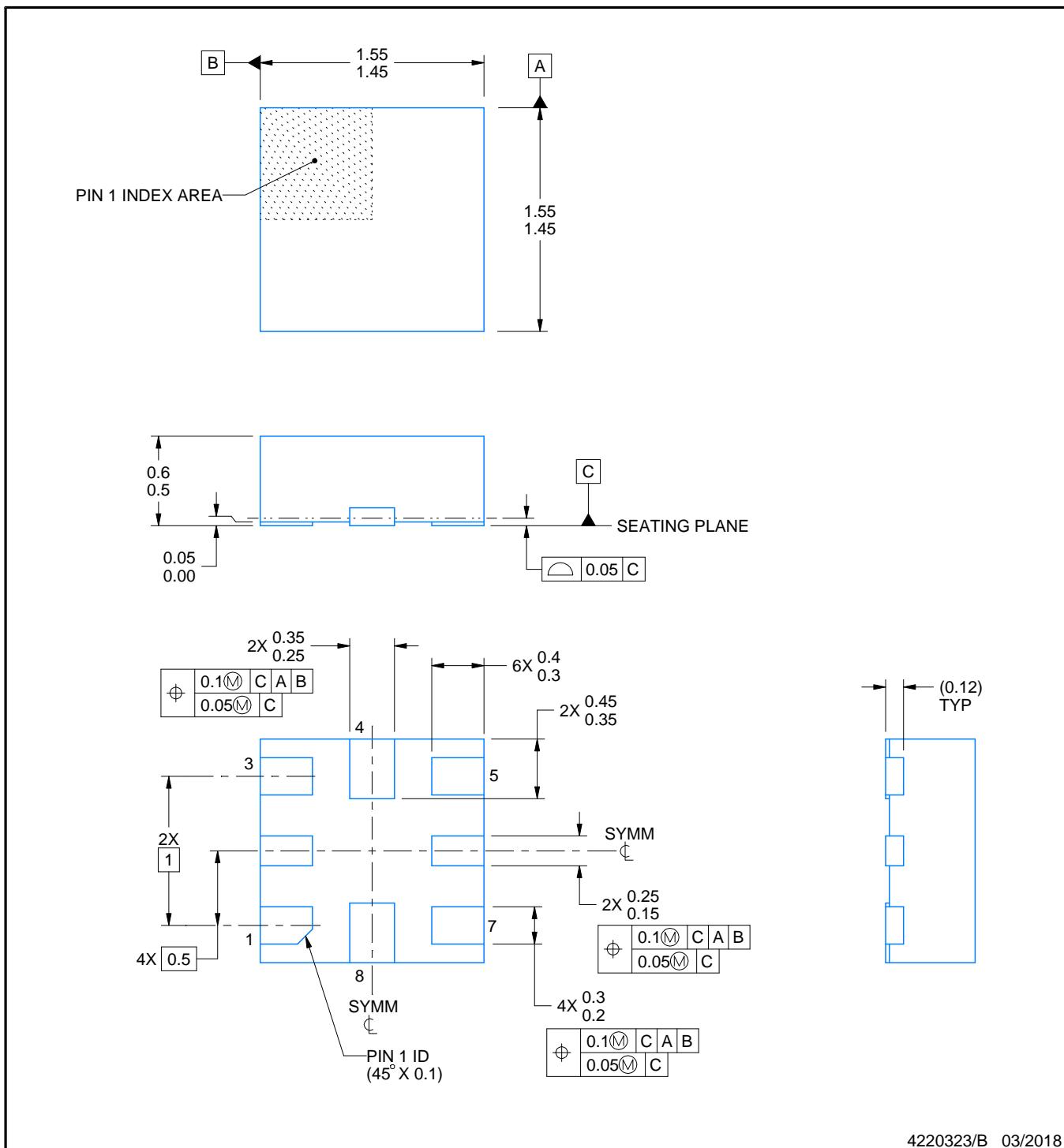
PACKAGE OUTLINE

RSE0008A



UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4220323/B 03/2018

NOTES:

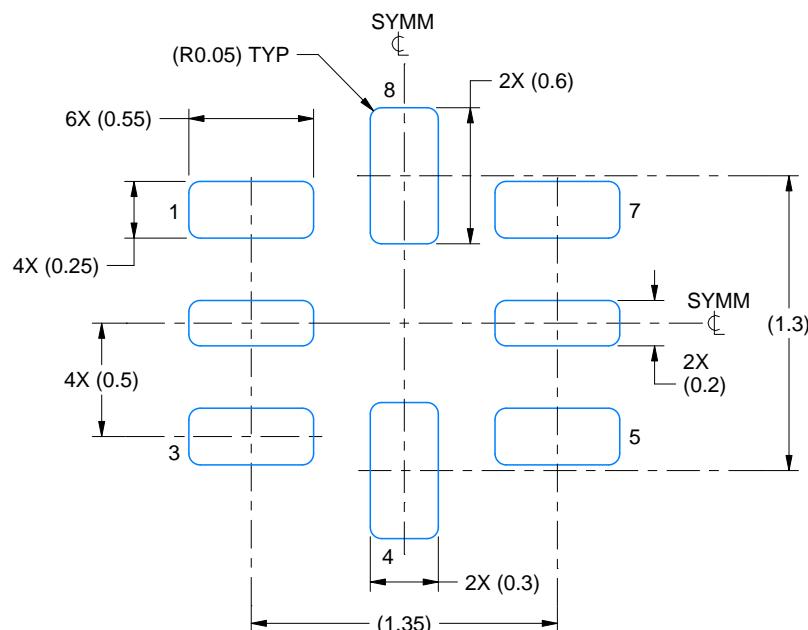
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

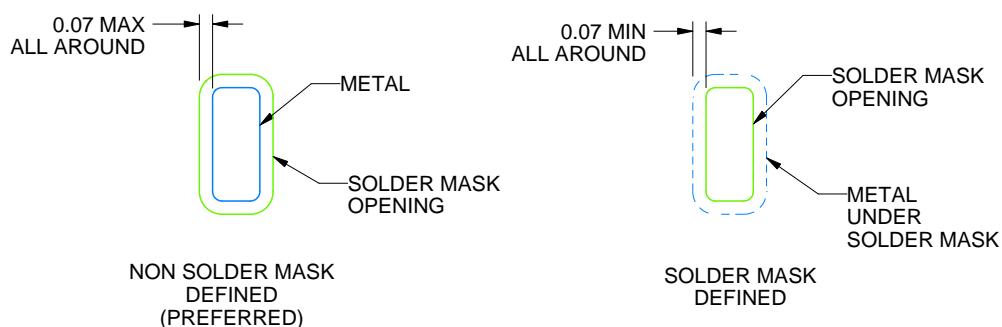
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

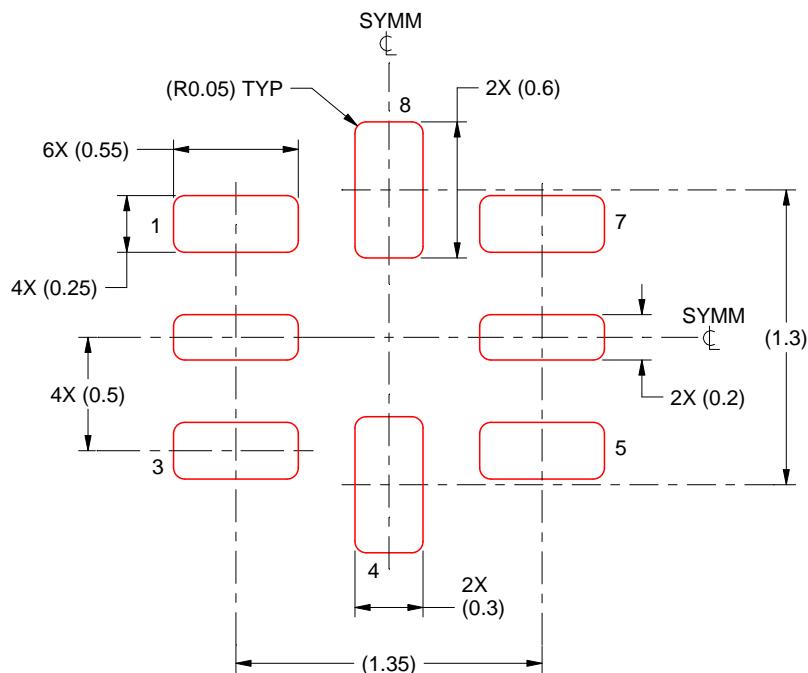
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X**

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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