- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **High Drive (–32/64 mA at 3.3-V V_{CC})**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

SN54ALVTH16245 . . . WD PACKAGE
SN74ALVTH16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$

description

The 'ALVTH16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.2 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
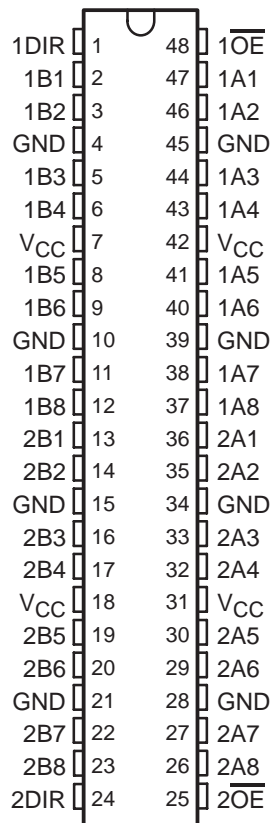
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

SN74ALVTH16245 . . . GQL PACKAGE
(TOP VIEW)
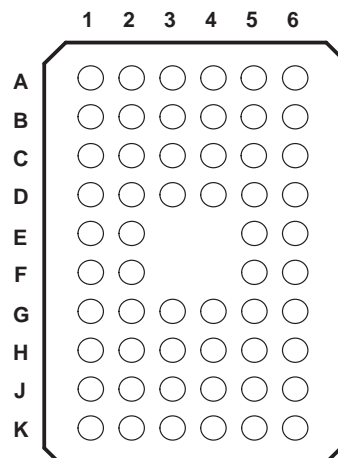
terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{\text{OE}}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V$_{CC}$	V$_{CC}$	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V$_{CC}$	V$_{CC}$	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{\text{OE}}$

NC – No internal connection

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tape and reel	SN74ALVTH16245DLR	ALVTH16245
	TSSOP – DGG	Tape and reel	SN74ALVTH16245GR	ALVTH16245
	TVSOP – DGV	Tape and reel	SN74ALVTH16245VR	VT245
	VFBGA – GQL	Tape and reel	SN74ALVTH16245QR	
–55°C to 125°C	CFP – WD	Tube	SNJ54ALVTH16245WD	SNJ54ALVTH16245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
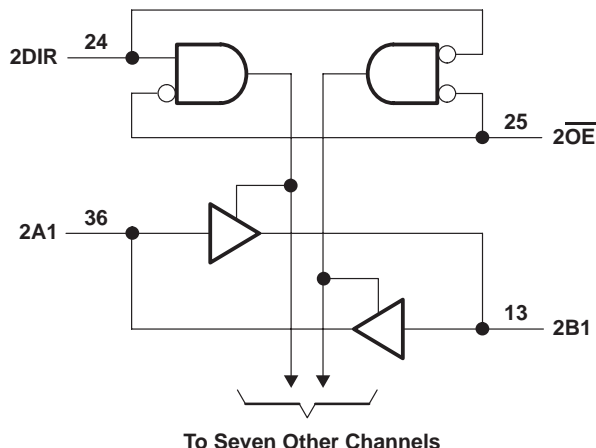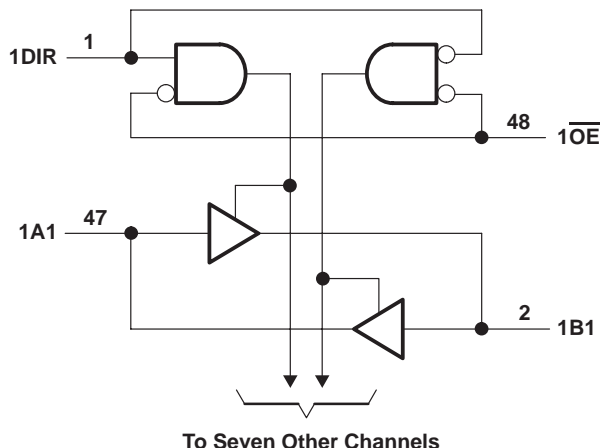
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)

Pin numbers shown are for the DGG, DGV, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	....	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	....	−0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	....	−0.5 V to 7 V
Output current in the low state, I_O: SN54ALVTH16245	....	96 mA
SN74ALVTH16245	....	128 mA
Output current in the high state, I_O: SN54ALVTH16245	....	−48 mA
SN74ALVTH16245	....	−64 mA
Input clamp current, I_{IK} ($V_I < 0$)	....	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	....	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	....	70°C/W
DGV package	....	58°C/W
DL package	....	63°C/W
GQL package	....	42°C/W
Storage temperature range, T_{stg}	....	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2.   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions, V_{CC} = 2.5 V $\pm$ 0.2 V (see Note 3)

			SN54ALVTH16245			SN74ALVTH16245			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage		1.7			1.7			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				−6			−8	mA
I_{OL}	Low-level output current				6			8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, V_{CC} = 3.3 V $\pm$ 0.3 V (see Note 3)

			SN54ALVTH16245			SN74ALVTH16245			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				−24			−32	mA
I_{OL}	Low-level output current				24			32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16245			SN74ALVTH16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.3 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.3 V to 2.7 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.3 V	I_{OH} = −6 mA	1.8						
			I_{OH} = −8 mA				1.8			
V_{OL}		V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 2.3 V	I_{OL} = 6 mA			0.4				
			I_{OL} = 8 mA						0.4	
			I_{OL} = 18 mA			0.5				
			I_{OL} = 24 mA						0.5	
I_I	Control inputs	V_{CC} = 2.7 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 2.7 V,	V_I = 5.5 V			10			10	
	A or B ports	V_{CC} = 2.7 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 2.3 V,	V_I = 0.7 V		115			115		µA
I_{BHH}§		V_{CC} = 2.3 V,	V_I = 1.7 V		−10			−10		µA
I_{BHLO}¶		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	300			300			µA
I_{BHHO}#		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	−300			−300			µA
I_{EX}‖		V_{CC} = 2.3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$★		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{CC}		V_{CC} = 2.7 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.04	0.1		0.04	0.1	mA
			Outputs low		2.3	4.5		2.3	4.5	
			Outputs disabled		0.04	0.1		0.04	0.1	
C_i		V_{CC} = 2.5 V,	V_I = 2.5 V or 0		3.5			3.5		pF
C_{io}		V_{CC} = 2.5 V,	V_O = 2.5 V or 0		8			8		pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
¶ An external driver must source at least I_{BHLO} to switch this node from low to high.
# An external driver must sink at least I_{BHHO} to switch this node from high to low.
‖ Current into an output in the high state when $V_O > V_{CC}$
★ High-impedance state during power up or power down

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16245			SN74ALVTH16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V	I_{OL} = 16 mA						0.4	
			I_{OL} = 24 mA			0.5				
			I_{OL} = 32 mA						0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 3 V,	V_I = 0.8 V	75			75			µA
I_{BHH}§		V_{CC} = 3 V,	V_I = 2 V	−75			−75			µA
I_{BHLO}¶		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	500			500			µA
I_{BHHO}#		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	−500			−500			µA
I_{EX}‖		V_{CC} = 3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$⋆		$V_{CC} \leq$ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.07	0.1		0.07	0.1	mA
			Outputs low		3.2	5		3.2	5	
			Outputs disabled		0.07	0.1		0.07	0.1	
ΔI_{CC}□		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_{CC} = 3.3 V,	V_I = 3.3 V or 0		3.5			3.5		pF
C_{io}		V_{CC} = 3.3 V,	V_O = 3.3 V or 0		8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

‖ Current into an output in the high state when V_O > V_{CC}

⋆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16245		SN74ALVTH16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	3.6	0.5	3.6	ns
t_{PHL}			0.5	3.4	0.5	3.4	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.9	1.5	4.9	ns
t_{PZL}			1	4	1	4	
t_{PHZ}	$\overline{OE}$	A or B	1.5	4.9	1.5	4.9	ns
t_{PLZ}			1	4.2	1	4.2	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16245		SN74ALVTH16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	3.1	0.5	3.1	ns
t_{PHL}			0.5	2.9	0.5	2.9	
t_{PZH}	$\overline{OE}$	A or B	1	4.2	1	4.2	ns
t_{PZL}			1	3.5	1	3.5	
t_{PHZ}	$\overline{OE}$	A or B	1.5	5.3	1.5	5.3	ns
t_{PLZ}			1.5	5	1.5	5	

skew

t_{ps} (pin or transition skew), t_{ps} = |t_{PHL} − t_{PHL}|

	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
	TYP	TYP	
t_{ps}max	438	118	ps

t_{OST} = |$t_{p\Phi m}$ − $t_{p\Phi n}$|, where Φ is any edge transition (high to low or low to high) measured between any two outputs (m or n) within any given device (see Note 4)

		V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
		TYP	TYP	
t_{OST}	A–B	227	248	ps
	B–A	223	243	

NOTE 4: One output switching, T_A = 25°C

t_{OSHL}/t_{OSLH} (common edge skew), t_{OSHL} = |t_{PHL}max − t_{PHL}min| (output skew for low-to-high transitions), and t_{OSLH} = |t_{PLH}max − t_{PLH}min| (output skew for high-to-low transitions) (see Note 4)

		V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
		TYP	TYP	
t_{OSLH}	A–B	210	145	ps
t_{OSHL}		243	351	
t_{OSLH}	B–A	207	136	ps
t_{OSHL}		238	350	

NOTE 4: One output switching, T_A = 25°C

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
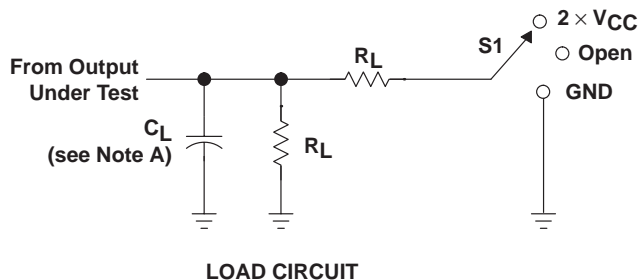
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
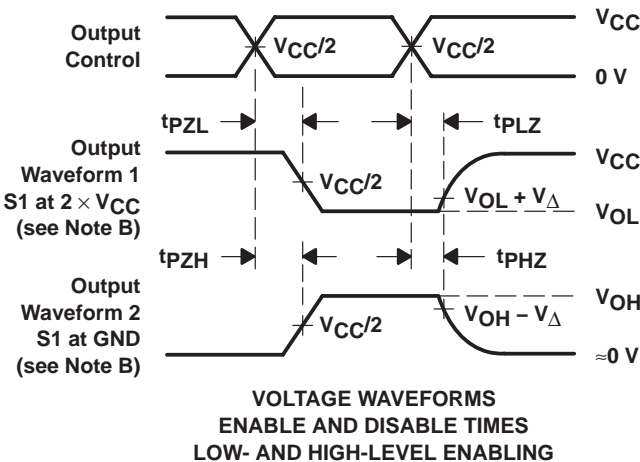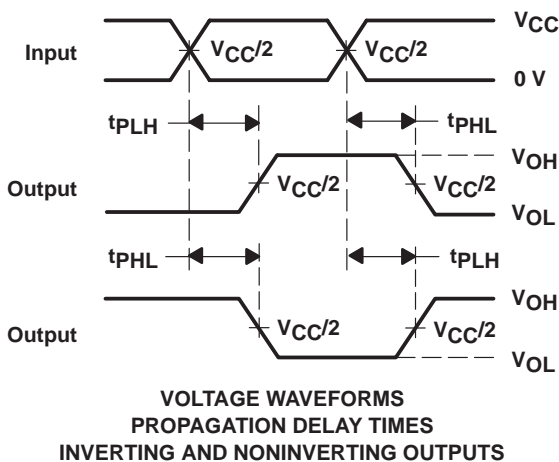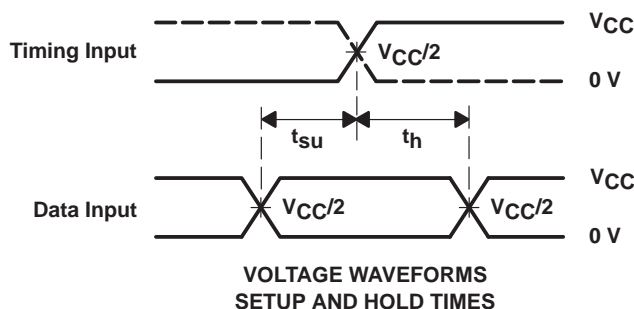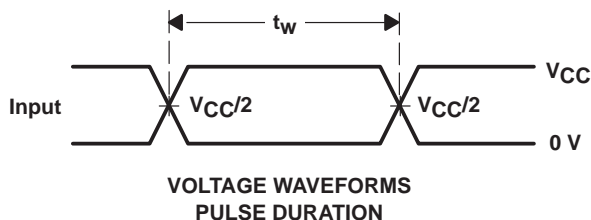
NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
      D. The outputs are measured one at a time with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.
      G. t_{PLH} and t_{PHL} are the same as t_{pd}.
      H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVTH16245VR	Obsolete	Production	TVSOP (DGV) | 48	-	-	Call TI	Call TI	-40 to 85	VT245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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