

SN74ALB16244

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS647D – AUGUST 1995 – REVISED JANUARY 2001

- Member of Texas Instruments' Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot
- Industry Standard '16244 Pinout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity-gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

$\overline{1OE}$	1	48	$\overline{2OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$\overline{4OE}$	24	25	$\overline{3OE}$

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ALB16244DL	ALB16244
		Tape and reel	SN74ALB16244DLR	
	TSSOP – DGG	Tape and reel	SN74ALB16244DGGR	ALB16244
	TVSOP – DGV	Tape and reel	SN74ALB16244DGVR	AV244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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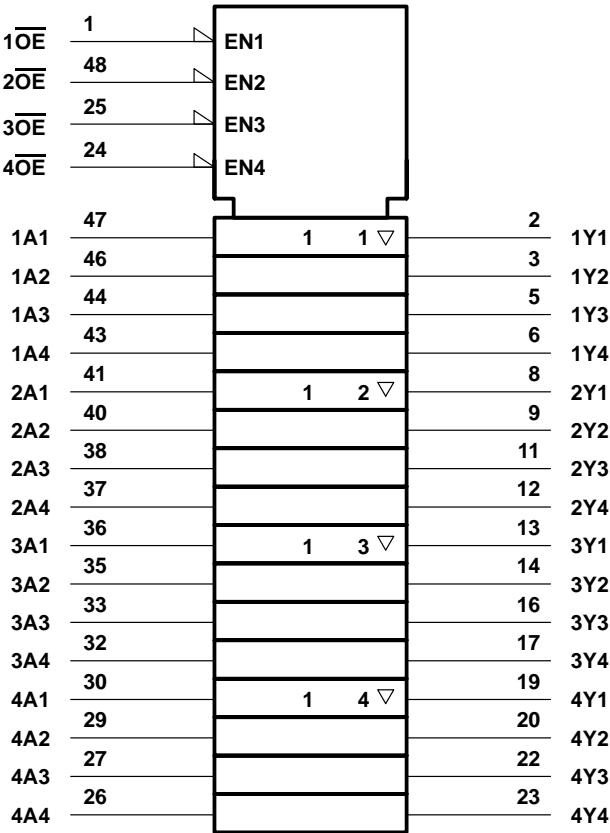
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
I_{OH}^{\dagger}	High-level output current		-25	mA
I_{OL}^{\dagger}	Low-level output current		25	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
T_A	Operating free-air temperature	-40	85	°C

[†] See Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V _{IK}	Data inputs	V _{CC} = 3 V	I _I = 18 mA		3.6		V _{CC} –1.2	V
			I _I = –18 mA		–0.9 –1.2			
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND			±10		μA	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	$\overline{\text{OE}}$ low	0.4	0.6	mA	
				$\overline{\text{OE}}$ high	25		μA	
			V _I = 0	$\overline{\text{OE}}$ low	–0.8	–1	mA	
				$\overline{\text{OE}}$ high	–60		μA	
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V			0.6	20	μA	
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V			–0.1	–50	μA	
I _{CC} /buffer		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND			3.7	5.6	mA	
I _{CCZ}		V _{CC} = 3.6 V, Control inputs = V _{CC} or GND			0.8		mA	
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} –0.6 V, Other inputs at V _{CC} or GND			600		μA	
C _i		V _I = 3 V or 0			4.5		pF	
C _O		V _O = 3 V or 0			5.5		pF	

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

^{\S} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			UNIT
			MIN	TYP [‡]	MAX	
t_{pd}	A	Y	0.6	1.3	2	ns
t_{en}	\overline{OE}	Y	1.3	2.5	4.7	ns
t_{dis}	\overline{OE}	Y	1.8	2.8	4.2	ns

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

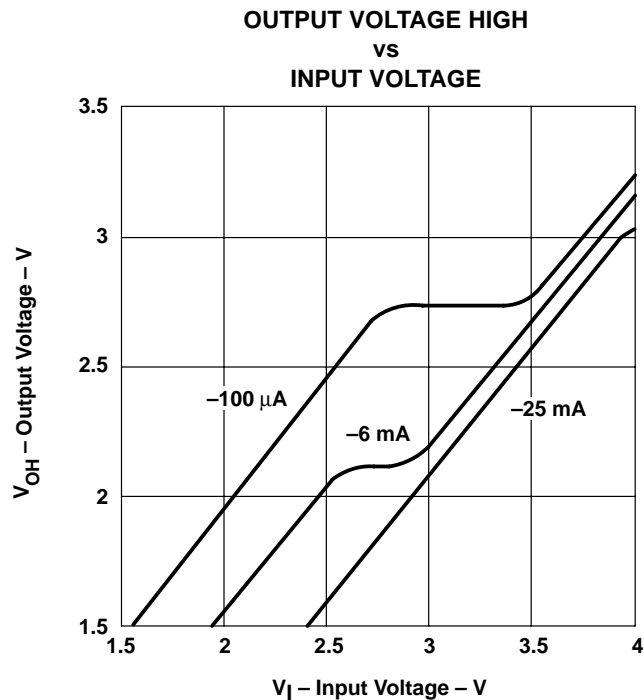


Figure 1. V_{OH} Over Recommended Free-Air Temperature Range

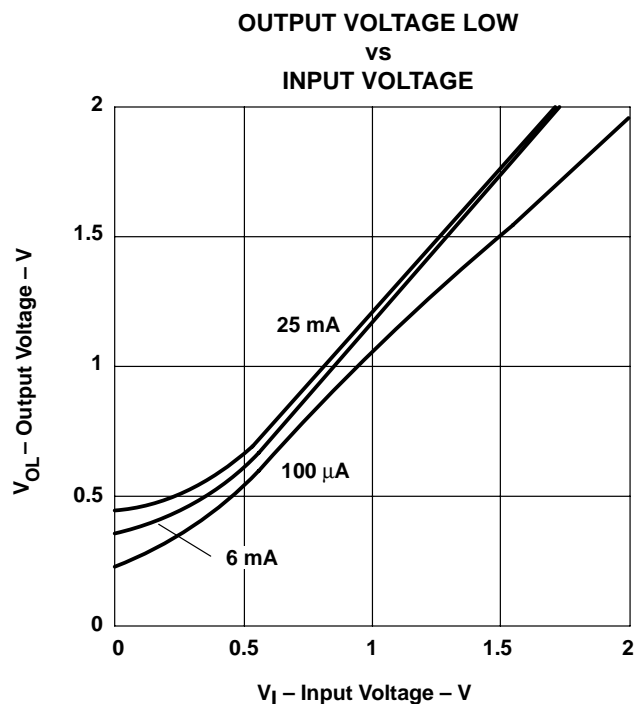


Figure 2. V_{OL} Over Recommended Free-Air Temperature Range

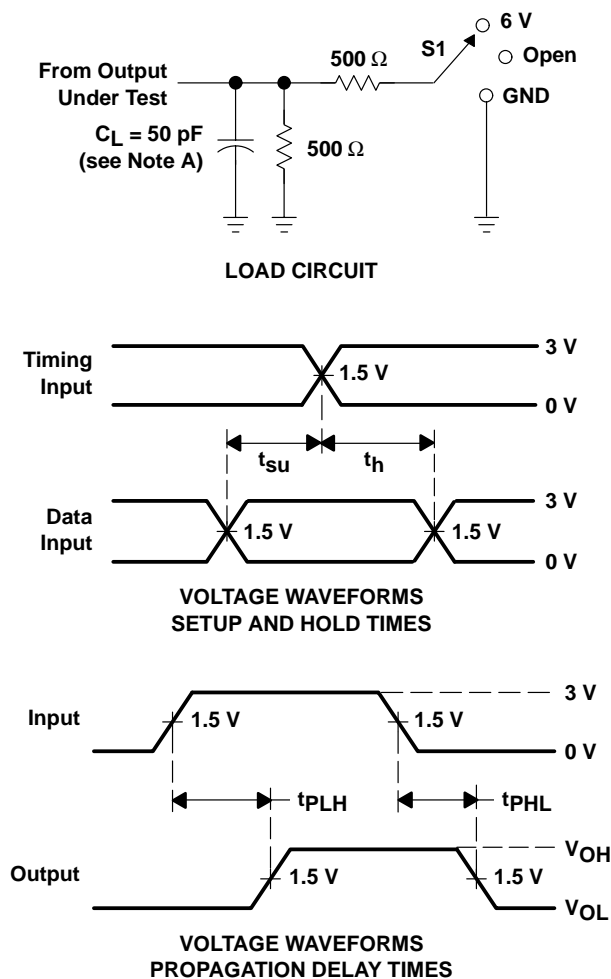
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16-BIT BUFFER/DRIVER

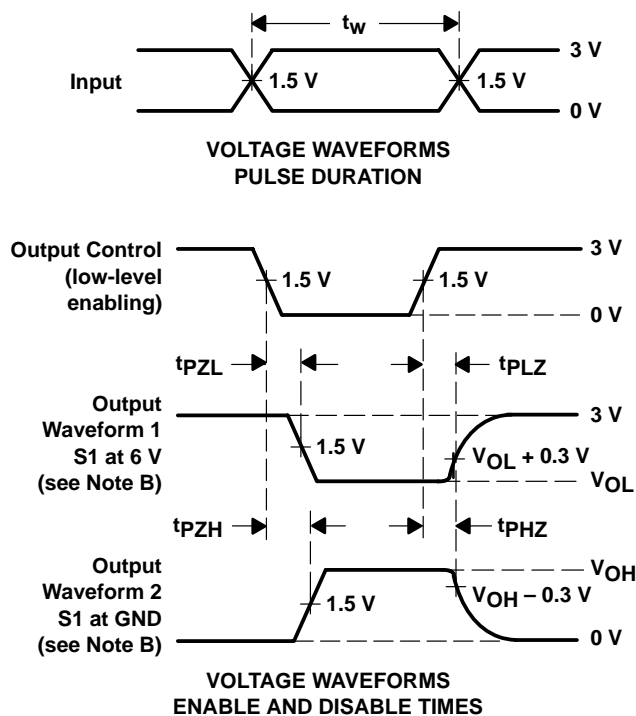
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALB16244DGGR	Obsolete	Production	TSSOP (DGG) 48	-	-	Call TI	Call TI	-40 to 85	ALB16244
SN74ALB16244DL	Obsolete	Production	SSOP (DL) 48	-	-	Call TI	Call TI	-40 to 85	ALB16244
SN74ALB16244DLR	Obsolete	Production	SSOP (DL) 48	-	-	Call TI	Call TI	-40 to 85	ALB16244

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

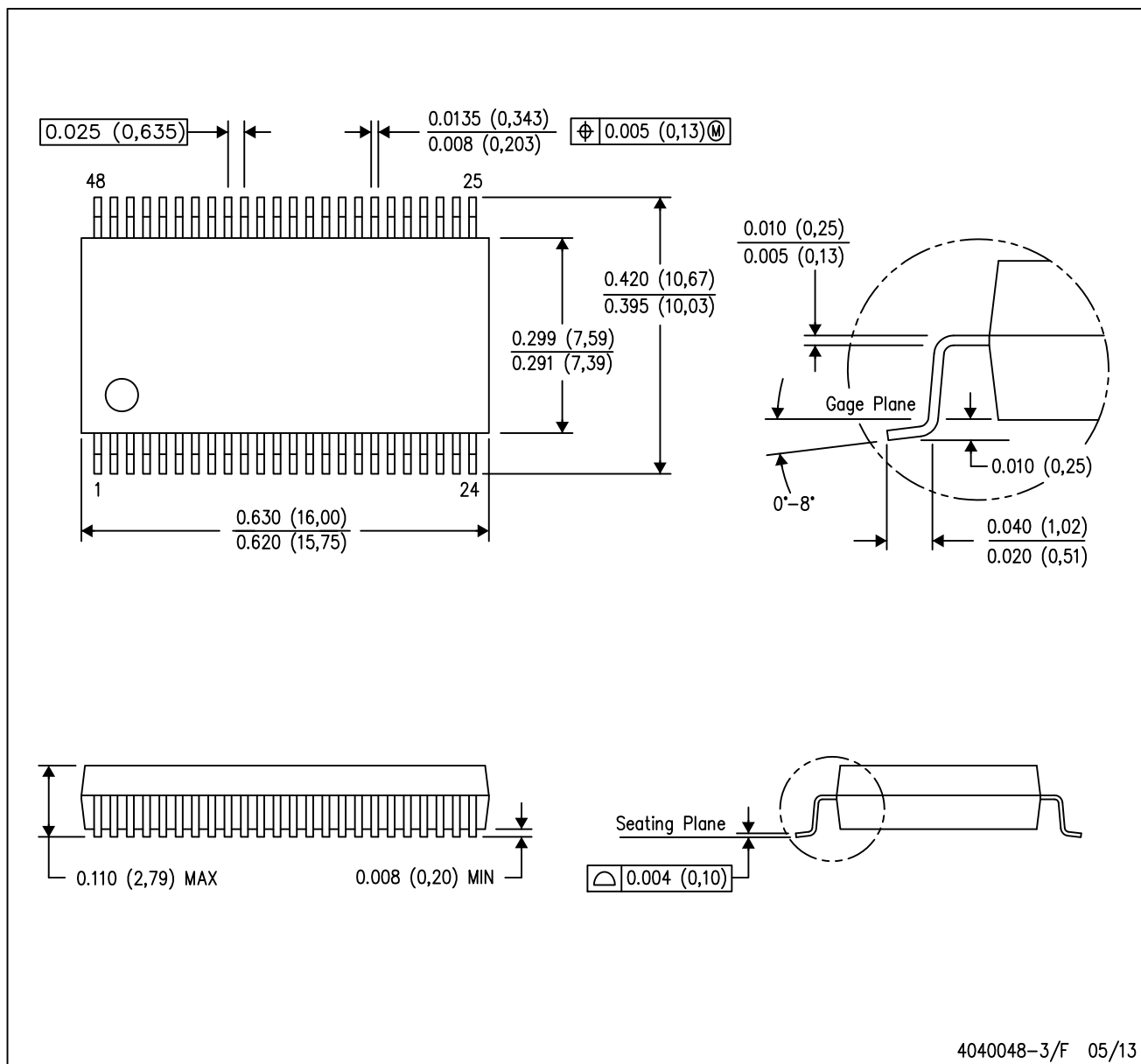
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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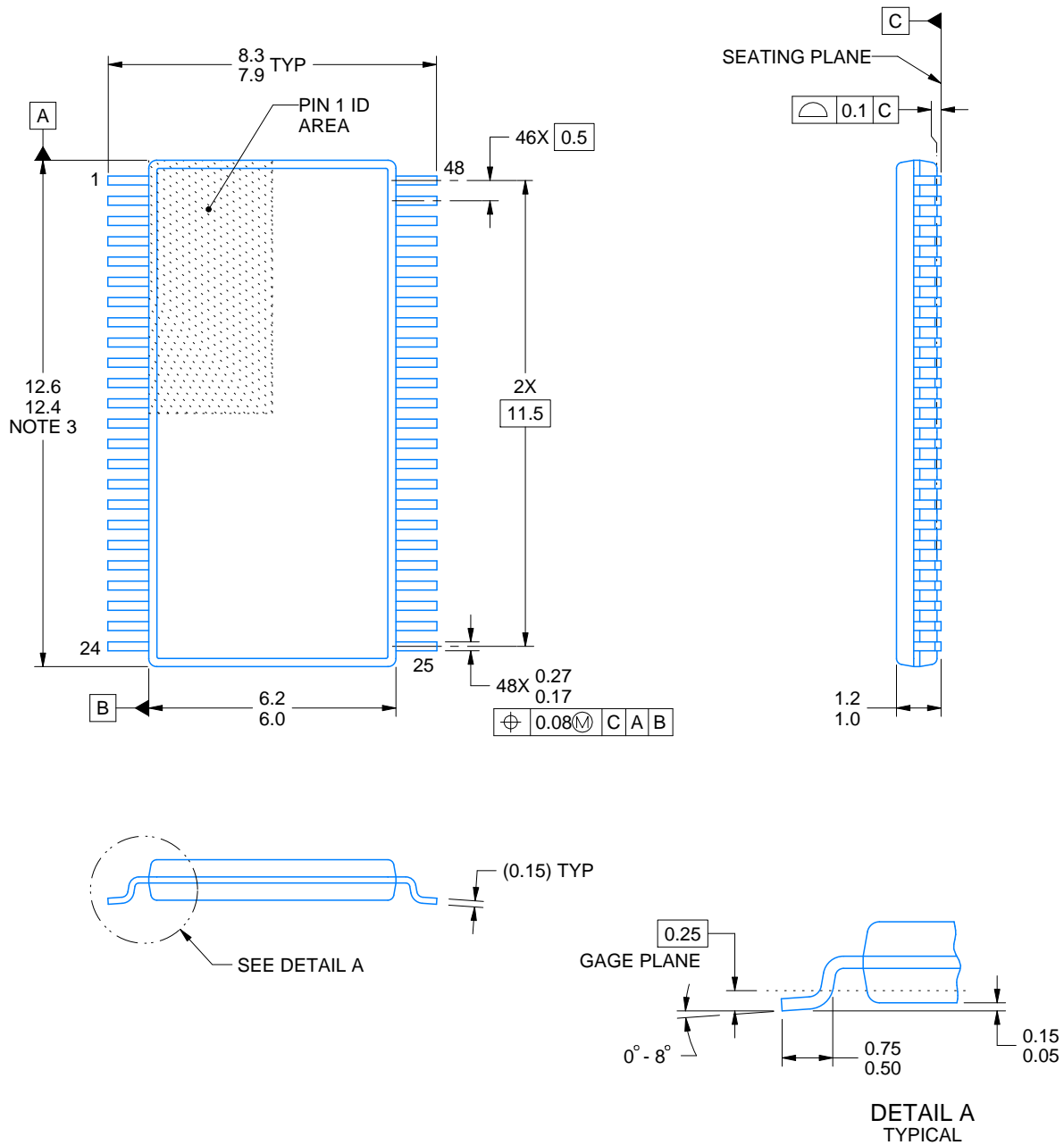
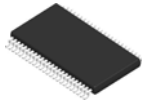
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DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

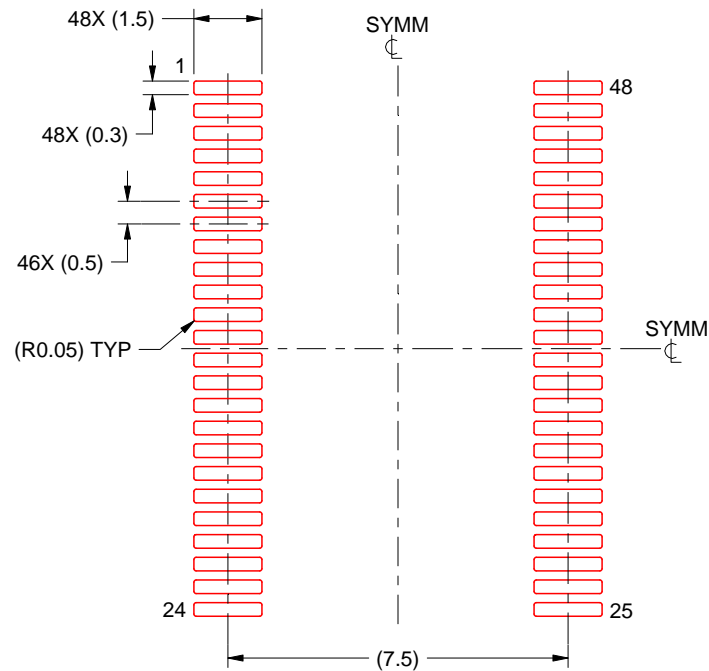
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2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
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 D. Falls within JEDEC MO-153

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