

SN74AHC4066 四路双边模拟开关

1 特性

- 1V 至 5.5V V_{CC} 运行
- 所有端口上均支持以混合模式电压运行
- 高开关输出电压比
- 低开关间串扰
- 单独的开关控制
- 极低输入电流
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求：
 - 2000V 人体放电模型 (A114-A)
 - 200V 机器放电模型 (A115-A)
 - 1000V 组件充电模式 (C101)

2 应用

- 模拟信号开关或多路复用：
 - 信号门控、调制器、静噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用
 - [音频和视频信号路由](#)
- 传输门逻辑实施
- 模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
- 电机转速控制
- [电池充电器](#)
- [直流/直流转换器](#)

3 说明

这款四路硅栅 CMOS 模拟开关专为在 1V 至 5.5V V_{CC} 下运行而设计，

能够处理模拟和数字信号。每个开关允许在任意方向传输振幅高达 5.5V (峰值) 的信号。

每个开关部分都有自己的启用输入控制 (C)。应用到 C 上的一个高电平电压开启相关开关部分。

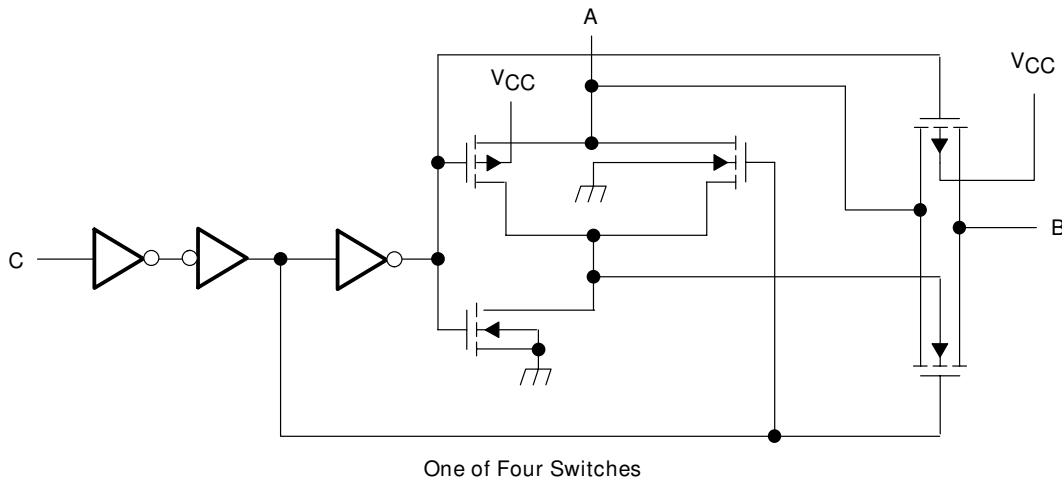
应用包括用于模数和数模转换系统的信号选通、斩波、调制或者解调 (modem)，以及信号复用。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN74AHC4066	D (SOIC, 14)	8.65mm x 6mm
	PW (TSSOP, 14)	5mm x 6.4mm
	RGY (VQFN, 14)	3.5mm x 3.5mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



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4 Pin Configuration and Functions

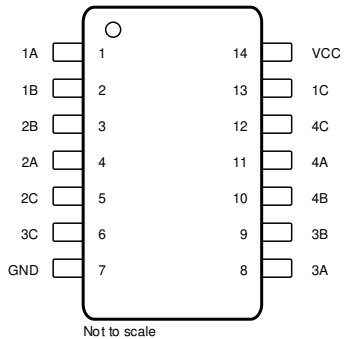


图 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

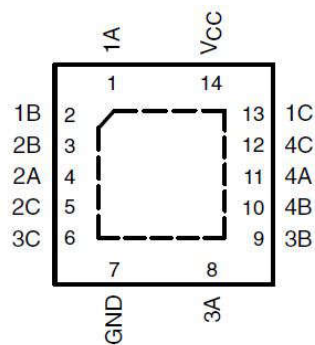


图 4-2. RGY Package, 14-Pin QFN (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I/O	Switch 1 input/output
1B	2	I/O	Switch 1 output/input
2B	3	I/O	Switch 2 output/input
2A	4	I/O	Switch 2 input/output
2C	5	I	Switch 2 control
3C	6	I	Switch 3 control
GND	7	—	Ground
3A	8	I/O	Switch 3 input/output
3B	9	I/O	Switch 3 output/input
4B	10	I/O	Switch 4 output/input
4A	11	I/O	Switch 4 input/output
4C	12	I	Switch 4 control
1C	13	I	Switch 1 control

表 4-1. Pin Functions (续)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{CC}	14	—	Power

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	- 0.5	7	V
V _I	Input voltage range	- 0.5	7	V
V _{IO}	Switch I/O voltage range	- 0.5 to V _{CC}	+0.5	V
I _{IK}	Control-input clamp current	V _I < 0	-20	mA
I _I	I/O port diode current	V _I < 0 or V _{IO} > V _{CC}	±50	mA
	On-state switch current	V _{IO} = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature	- 60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground unless otherwise specified.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. CDM value for N package only.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC4066			UNIT
		D	PW	RGY	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	127.7	150.6	91.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽²⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1 (1)	5.5	V
V _{IH}	High-level input voltage, control inputs	V _{CC} = 2V	1.5	V
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.7	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.7	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage, control inputs	V _{CC} = 2V	0.5	V
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.3	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.3	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.3	
V _I	Control input voltage	0	5.5	V
V _{I/O}	Input/output voltage	0	V _{CC}	V
Δt/Δv	Input transition rise and fall time	V _{CC} = 2.3V to 2.7V	200	ns/V
		V _{CC} = 3V to 3.6V	100	
		V _{CC} = 4.5V to 5.5V	20	
T _A	Operating free-air temperature	– 40	85	°C

- (1) With supply voltages at or below 2V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.
- (2) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

5.5 Electrical Characteristics

T_A = – 40 to +85 °C unless otherwise specified.

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
r _{on}	On-state switch resistance	I _T = – 1mA, V _I = 0 to V _{CC} , V _C = V _{IH} (see 图 6-1)	2.3V	38	180		225	Ω
			3V	29	150		190	
			4.5V	21	75		100	
r _{on(p)}	Peak on-state resistance	I _T = – 1mA V _I = V _{CC} to GND V _C = V _{IH}	2.3V	143	500		600	Ω
			3V	57	180		225	
			4.5V	31	100		125	
Δ r _{on}	Difference in on-state resistance between switches	I _T = – 1mA V _I = V _{CC} to GND V _C = V _{IH}	2.3V	6	30		40	Ω
			3V	3	20		30	
			4.5V	2	15		20	
I _{IH} I _{IL}	Control input current	V _C = 0 or V _{CC}	5.5		±0.1		±1	μA
I _{s(off)}	Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see 图 6-2)	5.5V		±0.1		±1	μA

5.5 Electrical Characteristics (续)

$T_A = -40$ to $+85$ °C unless otherwise specified.

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$I_{S(on)}$	On-state switch leakage current $V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see 图 6-3)	5.5V			± 0.1		± 1	μA
I_{CC}	Supply current $V_I = V_{CC}$ or GND	5.5V					20	μA
C_{iC}	Control input capacitance			1.5				pF
C_{iO}	Switch input/output capacitance			5.5				pF
C_F	Feed-through capacitance			0.5				pF

5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH} , t_{PHL}	A or B	B or A	$C_L = 50\text{pF}$ (see 图 6-4)		1.2	10		16	ns
t_{PZH} , t_{PZL}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-5)		3.3	15		20	ns
t_{PLZ} , t_{PHZ}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-5)		6	15		23	ns
t_{PLZ} , t_{PHZ}	A or B	B or A	$C_L = 50\text{pF}$ (see 图 6-6)		2.6	12		18	ns
t_{PLZ} , t_{PHZ}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-8)		4.2	25		32	ns
t_{PLZ} , t_{PHZ}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-8)		9.6	25		32	ns

5.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH} , t_{PHL}	A or B	B or A	$C_L = 50\text{pF}$ (see 图 6-4)		0.8	6		10	ns
t_{PZH} , t_{PZL}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-5)		2.3	11		15	ns
t_{PLZ} , t_{PHZ}	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$, (see 图 6-5)		4.5	11		15	ns
t_{PLZ} , t_{PHZ}	A or B	B or A	$C_L = 50\text{pF}$ (see 图 6-6)		1.5	9		12	ns

5.7 Switching Characteristics (续)

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLZ} , t_{PHZ} Switch turn-on time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-8)		3	18		22	ns
t_{PLZ} , t_{PHZ} Switch turn-off time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-8)		7.2	18		22	ns

5.8 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH} , t_{PHL} Propagation delay time	A or B	B or A	$C_L = 50pF$ (see 图 6-4)		0.3	4		7	ns
t_{PZH} , t_{PZL} Switch turn-on time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-5)		1.6	7		10	ns
t_{PLZ} , t_{PHZ} Switch turn-off time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-5)		3.2	7		10	ns
t_{PLZ} , t_{PHZ} Propagation delay time	A or B	B or A	$C_L = 50pF$ (see 图 6-6)		0.6	6		8	ns
t_{PLZ} , t_{PHZ} Switch turn-on time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-8)		2.1	12		16	ns
t_{PLZ} , t_{PHZ} Switch turn-off time	C	A or B	$C_L = 50pF$ $R_L = 1k\Omega$, (see 图 6-8)		5.1	12		16	ns

5.9 Analog Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ C$			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	$C_L = 50pF$, $R_L = 600\Omega$ $f_{in} = 1MHz$ (sine wave) $20\log_{10}(V_O/V_I) = -3$ dB (see 图 6-4)	2.3V		60		MHz
				3V		75		
				4.5V		100		
Crosstalk (between any switches)	A or B	B or A	$C_L = 50pF$, $R_L = 600\Omega$ $f_{in} = 1MHz$ (sine wave) (see 图 6-4)	2.3V		-45		dB
				3V		-45		
				4.5V		-45		
Crosstalk (control input to signal output)	C	A or B	$C_L = 50pF$, $R_L = 600\Omega$, $f_{in} =$ $1MHz$ (sine wave) (see 图 6-4)	2.3V		15		mV
				3V		20		
				4.5V		50		
Feed-through attenuation (switch off)	A or B	B or A	$C_L = 50pF$, $R_L = 600\Omega$, $f_{in} =$ $1MHz$ (sine wave) (see 图 6-4)	2.3V		-40		dB
				3V		-40		
				4.5V		-40		

5.9 Analog Switching Characteristics (续)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
					MIN	TYP	MAX	
Sine-wave distortion	A or B	B or A	C _L = 50pF, R _L = 10kΩ, f _{in} = 1kHz (sine wave) (see 图 6-4)	V _I = 2V _{p-p} 2.3V		0.1		%
				V _I = 2.5V _{p-p} 3V		0.1		
				V _I = 4V _{p-p} 4.5V		0.1		

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50pF, f = 10MHz	4.5	pF

6 Parameter Measurement Information

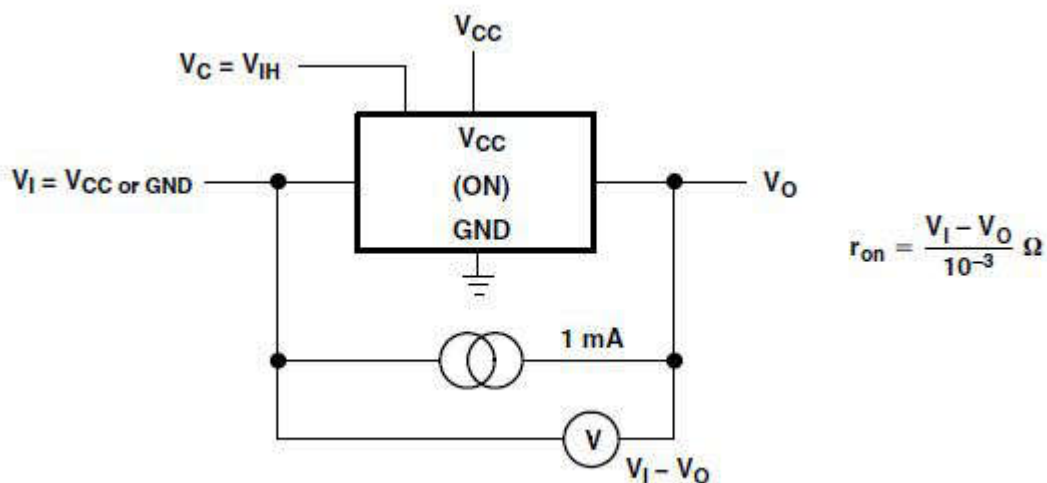


图 6-1. ON-State Resistance Test Circuit

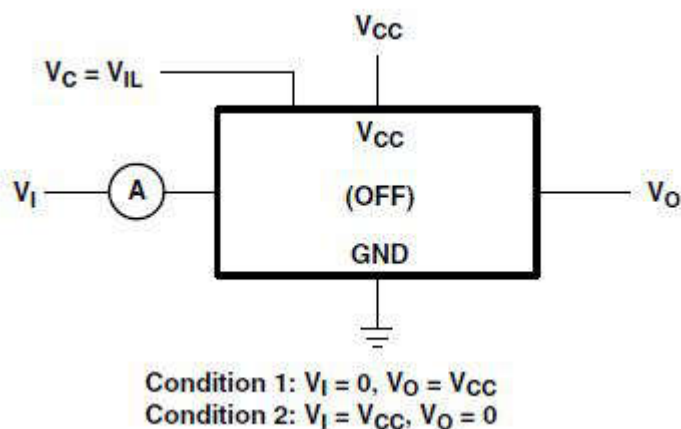


图 6-2. OFF-State Switch Leakage-Current Test Circuit

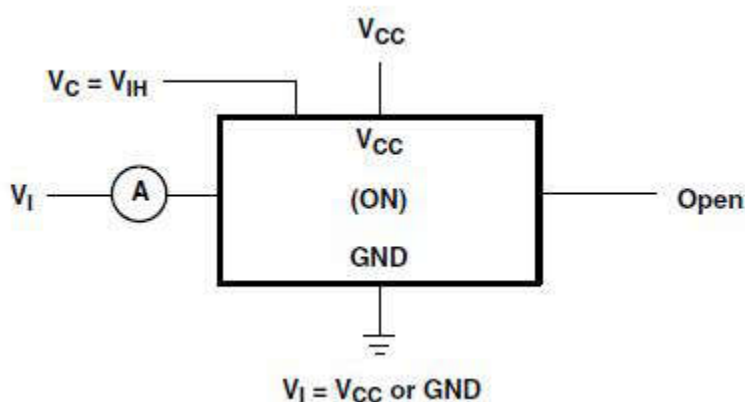


图 6-3. ON-State Leakage-Current Test Circuit

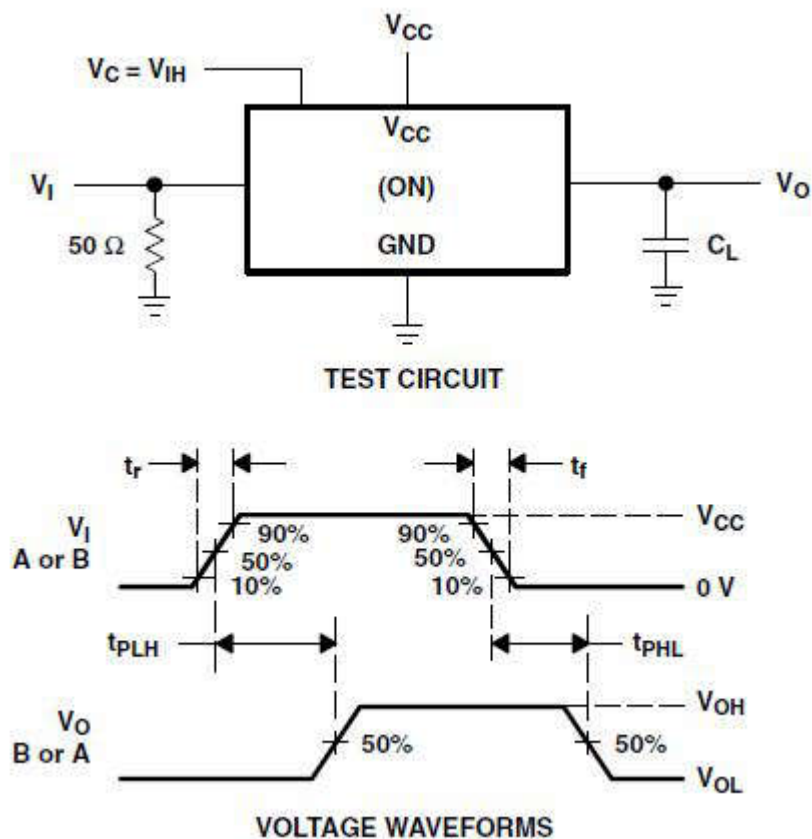
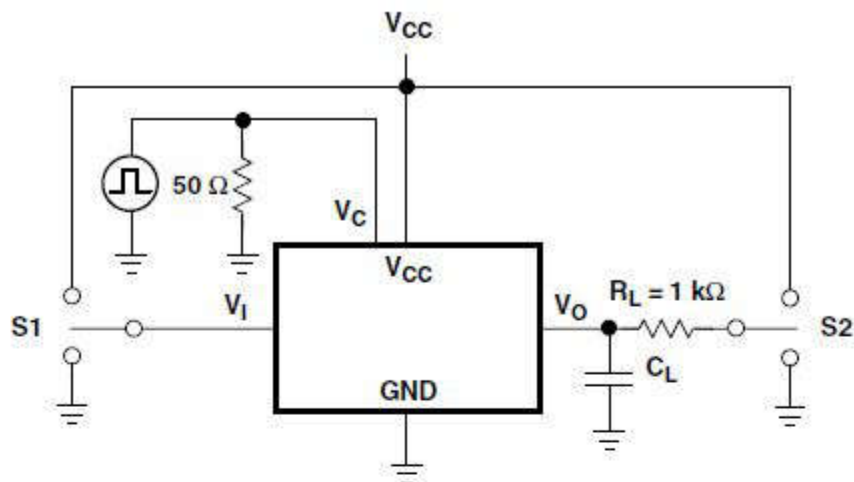
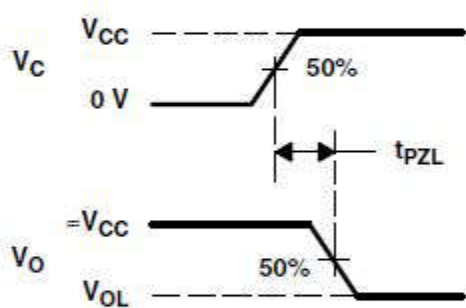


图 6-4. Propagation Delay Time, Signal Input to Signal Output

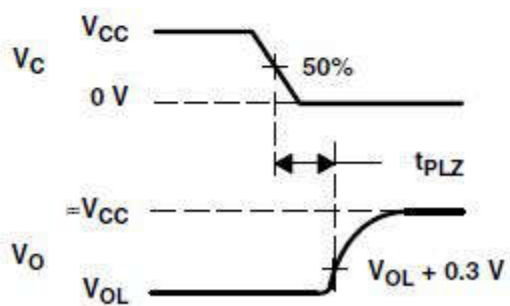
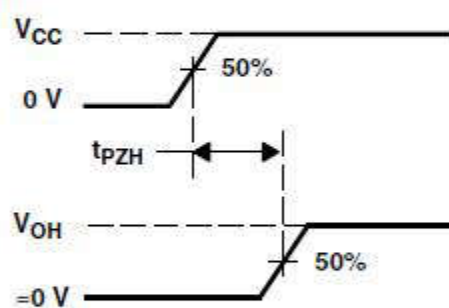


TEST CIRCUIT

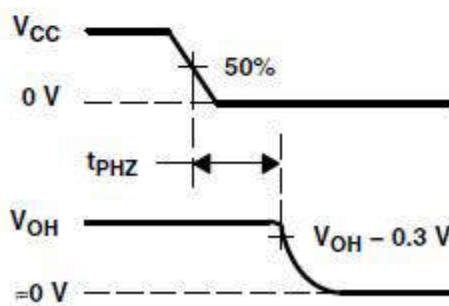
TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



(t_{PZL} , t_{PZH})



(t_{PLZ} , t_{PHZ})



VOLTAGE WAVEFORMS

图 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

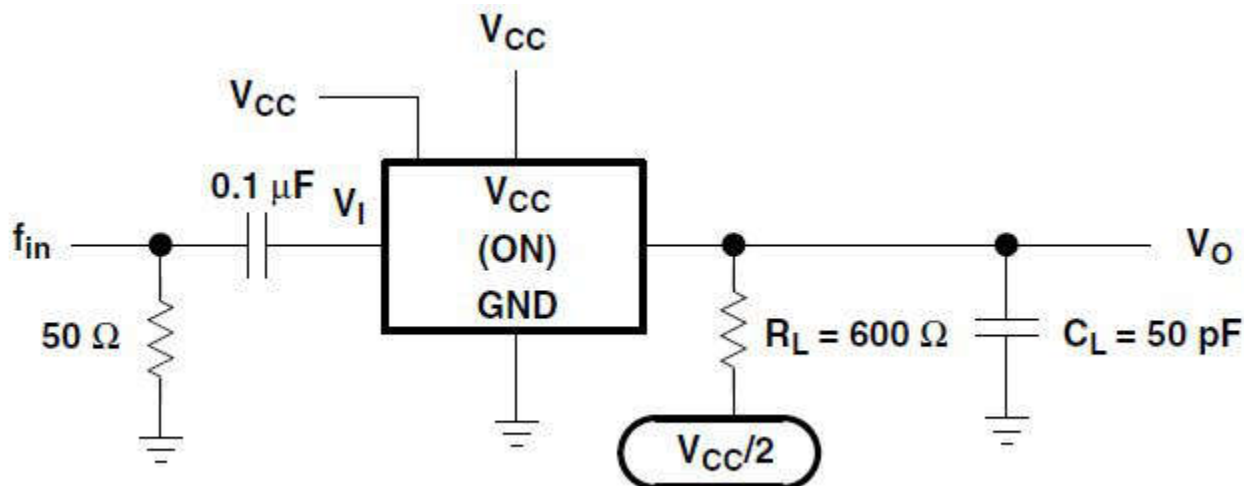


图 6-6. Frequency Response (Switch On)

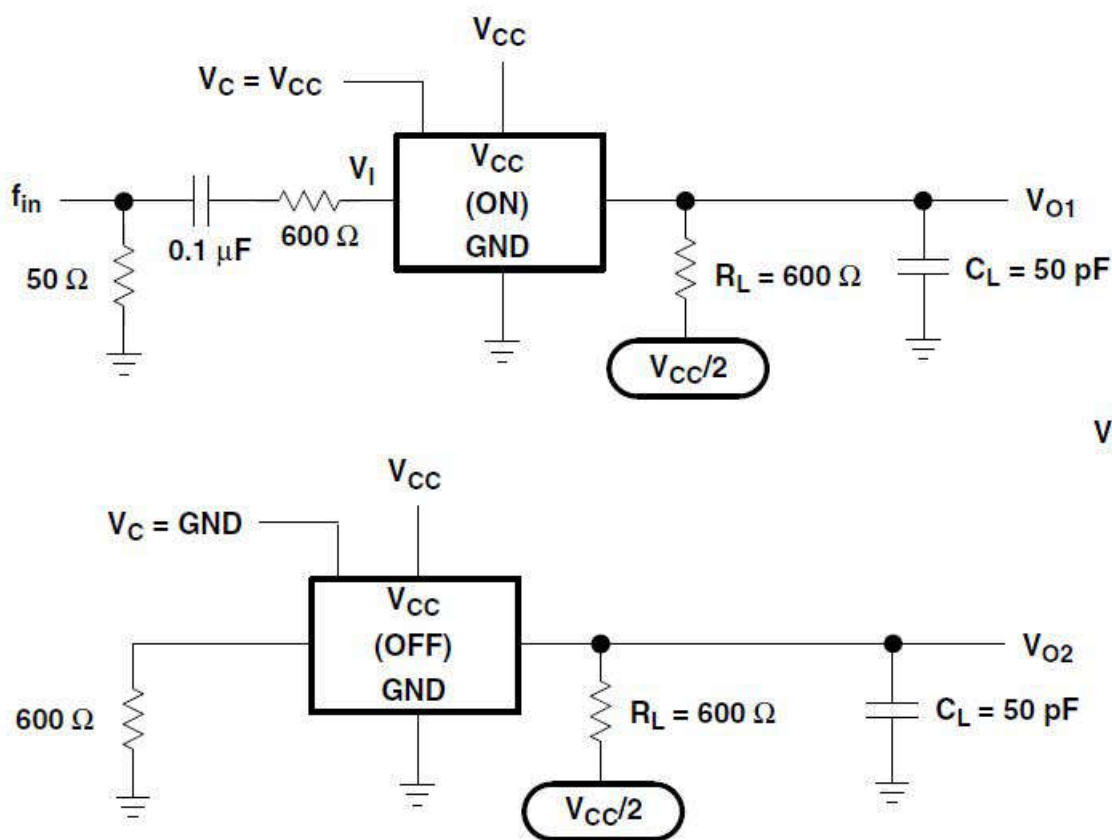


图 6-7. Crosstalk Between Any Two Switches

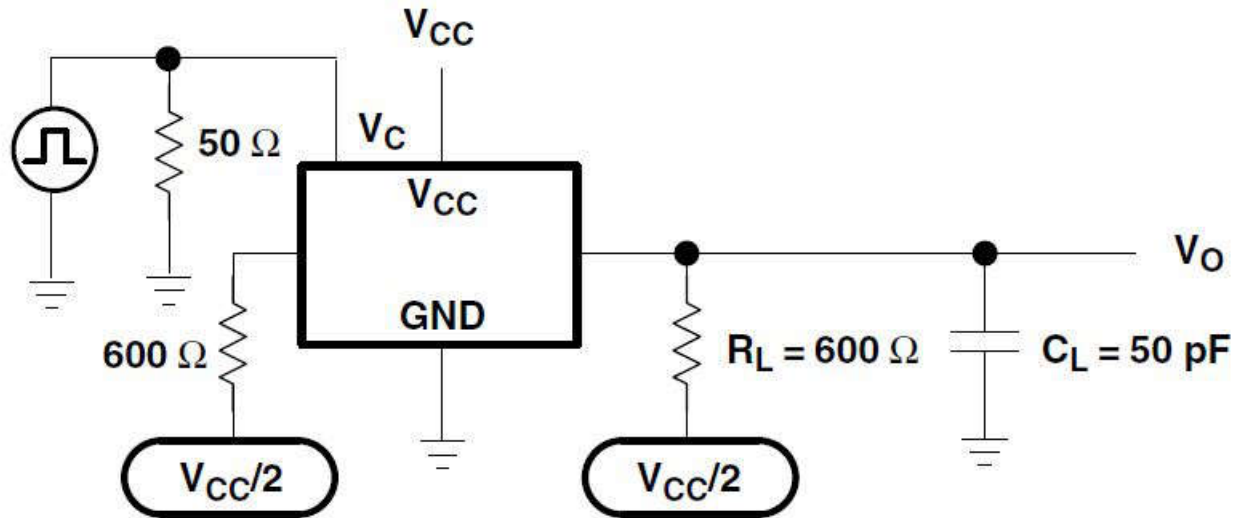


图 6-8. Crosstalk (Control Input - Switch Output)

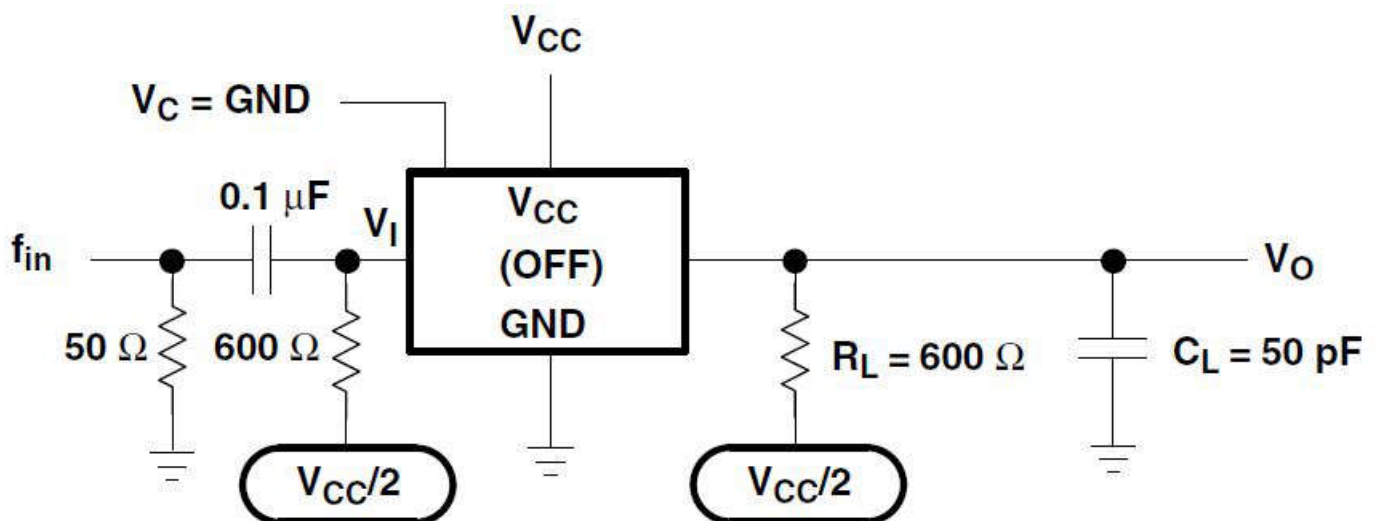


图 6-9. Feed-Through Attenuation (Switch Off)

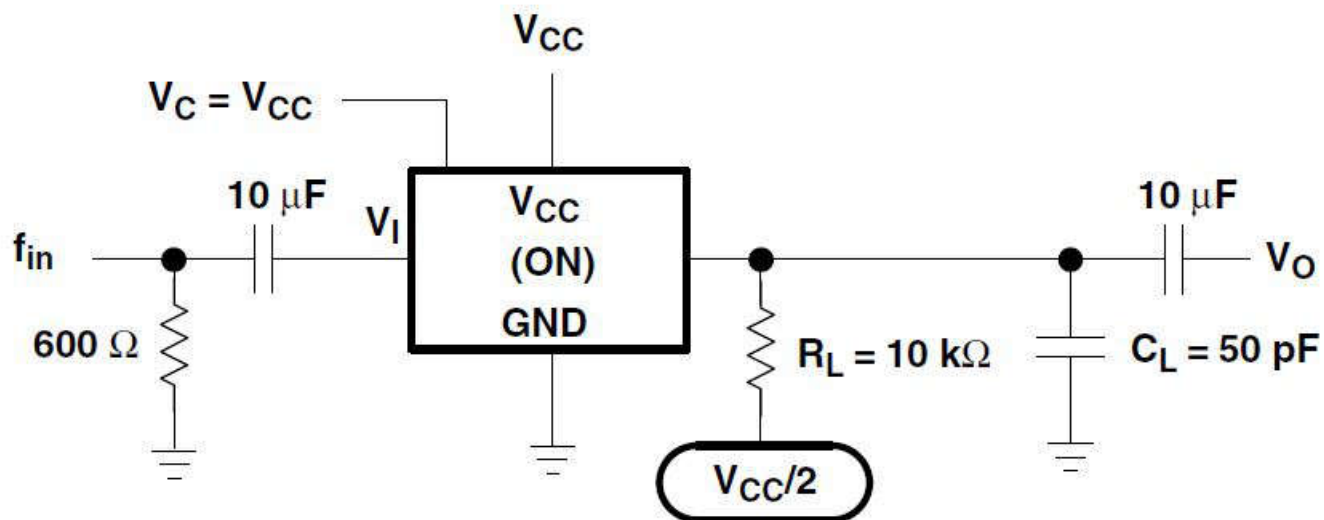


图 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SN74AHC4066 device is a silicon-gate CMOS quadruple analog switch designed for 1V to 6V VCC operation. It is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device.

7.2 Functional Block Diagram

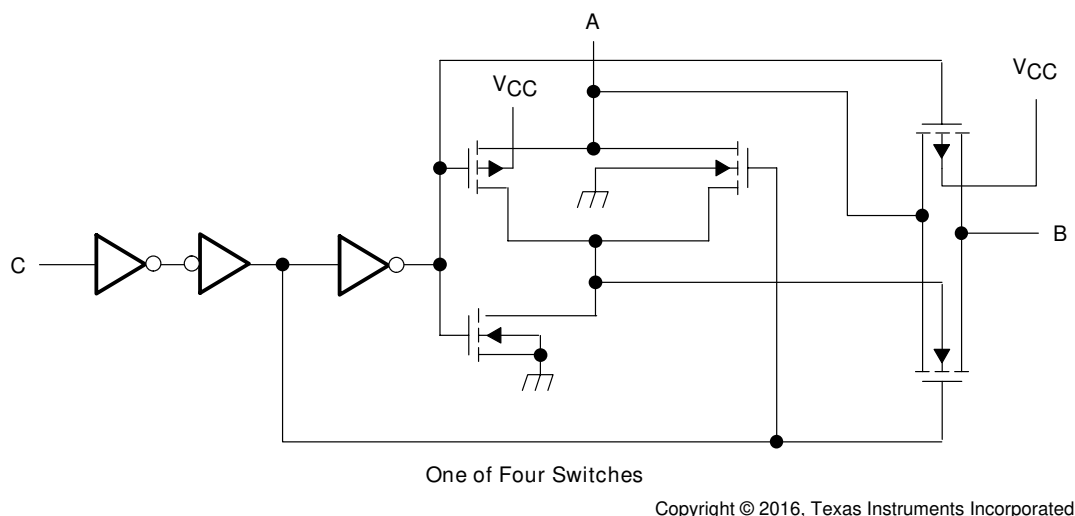


图 7-1. Logic Diagram, Each Switch (Positive Logic)

7.3 Device Functional Modes

表 7-1 lists the functions for the SN74AHC4066 device.

表 7-1. Function Table
(Each Switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application notes](#)

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2003) to Revision A (February 2024)	Page
• 将数据表更新为仅包含 <i>D</i> 、 <i>PW</i> 或 <i>RGY</i> 封装.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated the <i>Thermal Information</i>	4
• Updated V _{CC} operation from: 2V - 5.5V to: 1V - 5.5V.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC4066D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AHC4066
SN74AHC4066DBR	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066DBR.A	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066DGVR	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066DGVR.A	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066
SN74AHC4066DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066
SN74AHC4066N	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC4066N
SN74AHC4066N.A	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC4066N
SN74AHC4066NSR	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066
SN74AHC4066NSR.A	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066
SN74AHC4066PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	HA4066
SN74AHC4066PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066
SN74AHC4066RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA4066
SN74AHC4066RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA4066

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

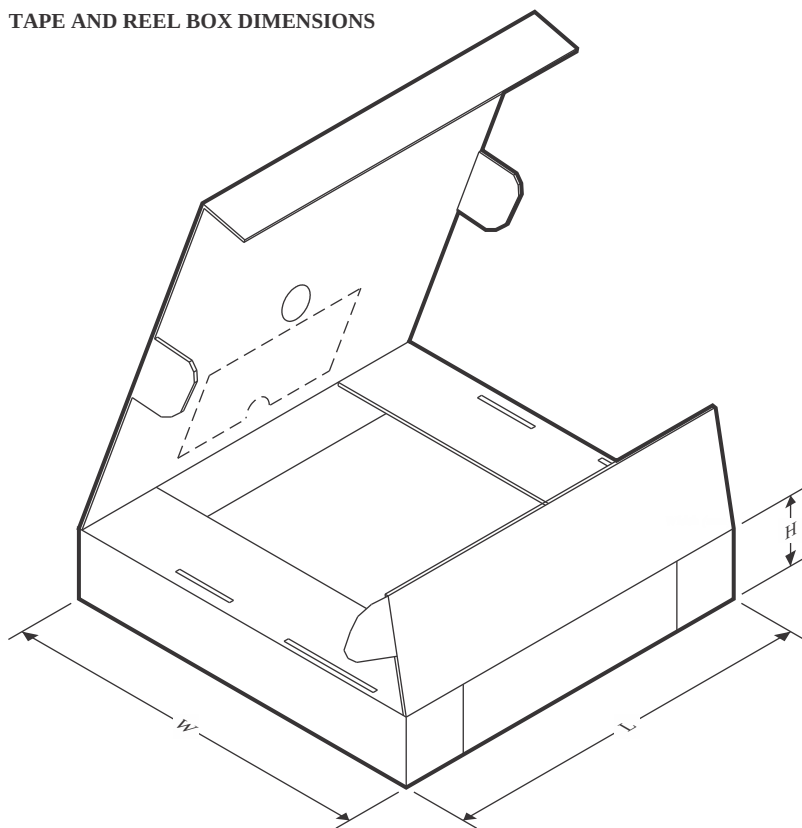
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC4066DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC4066DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC4066NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC4066RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC4066DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC4066DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC4066DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC4066NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC4066PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC4066RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC4066N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC4066N.A	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

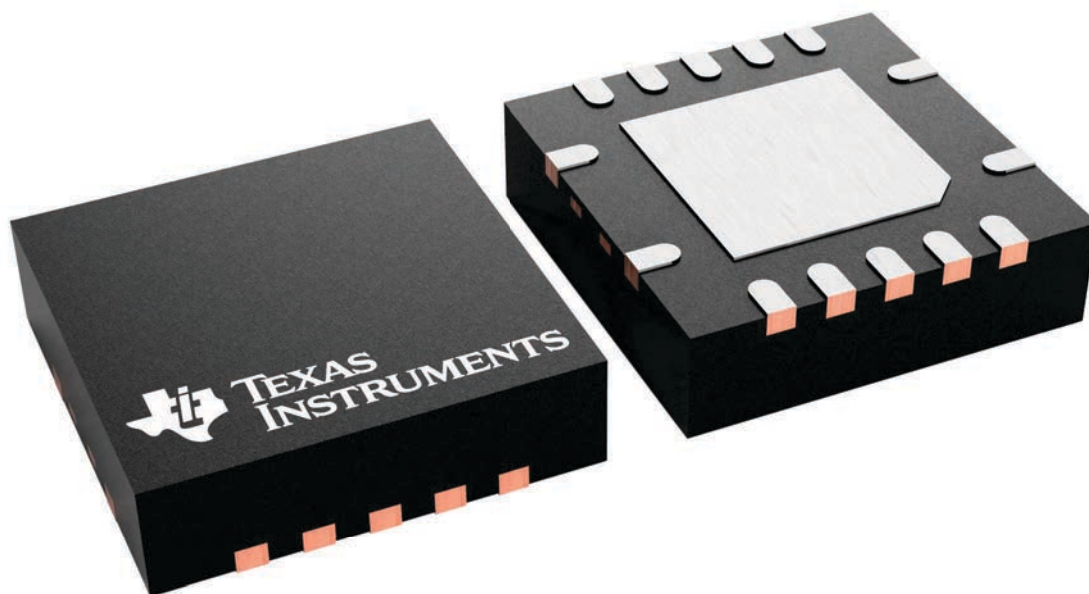
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

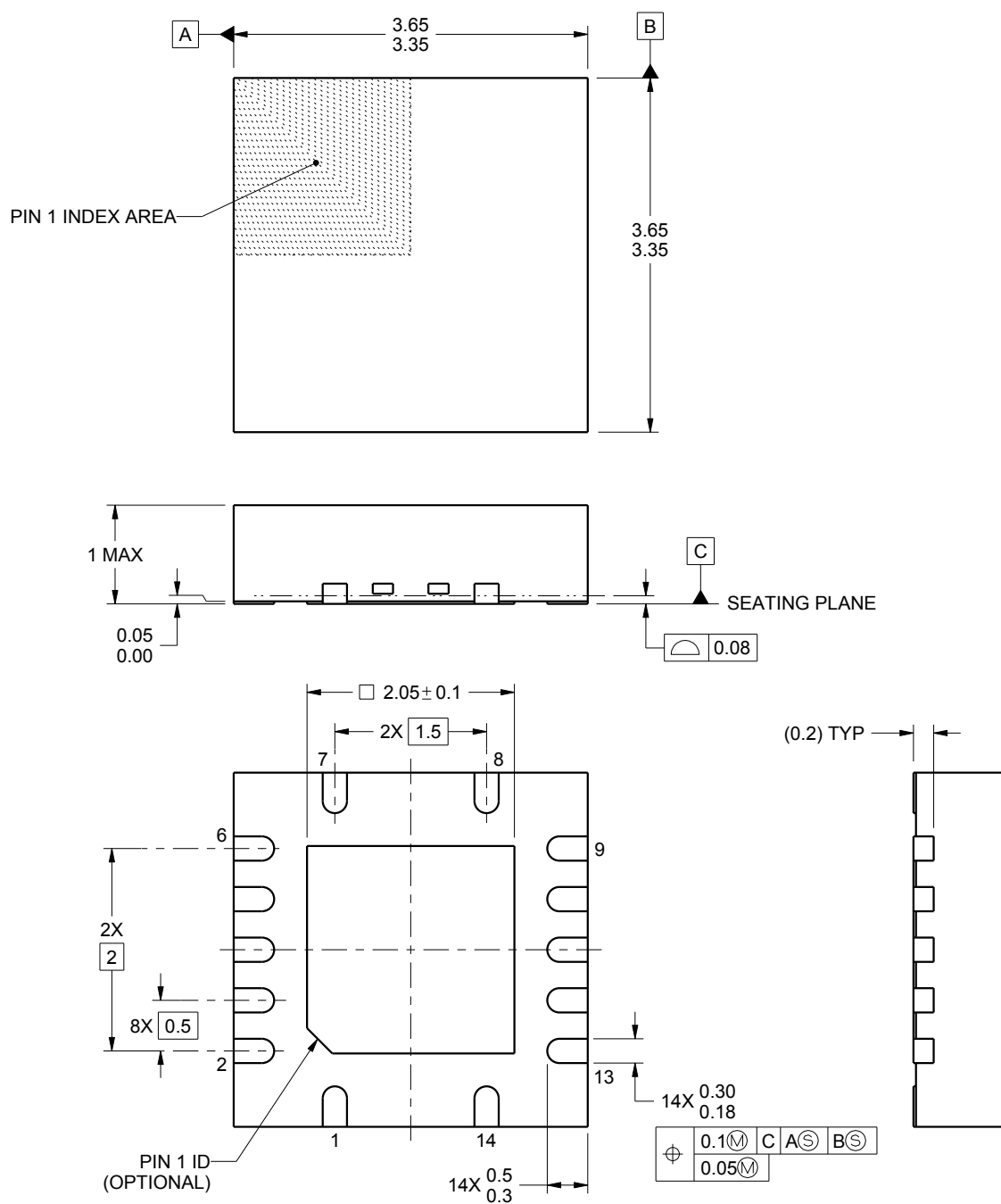


4231541/A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

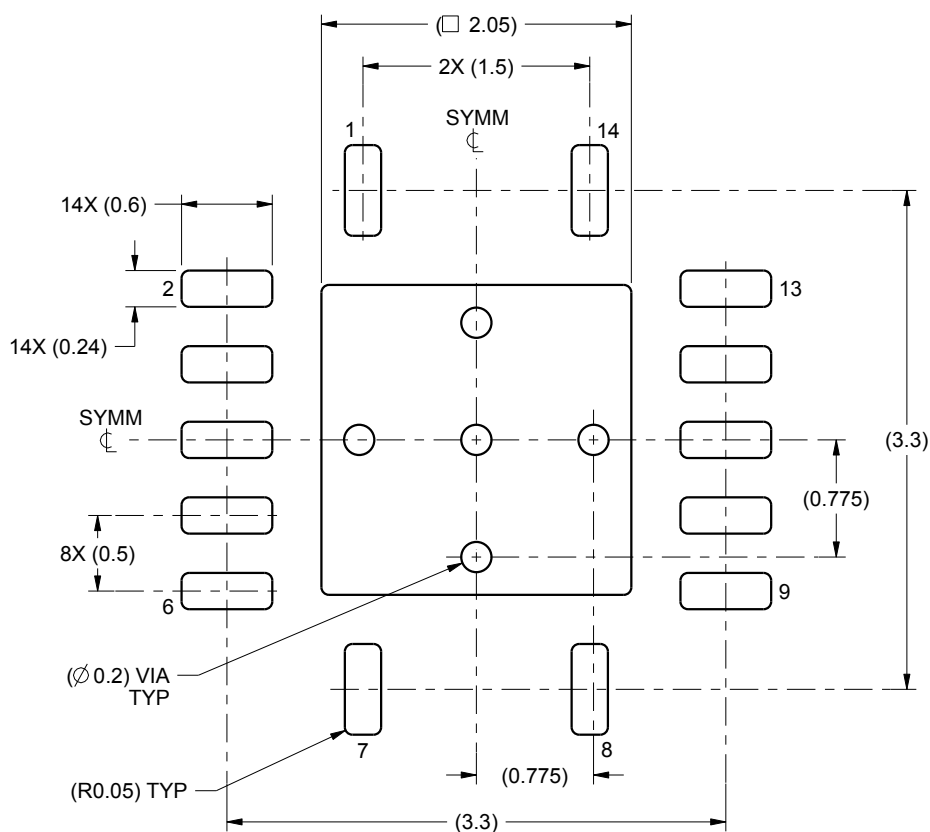
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

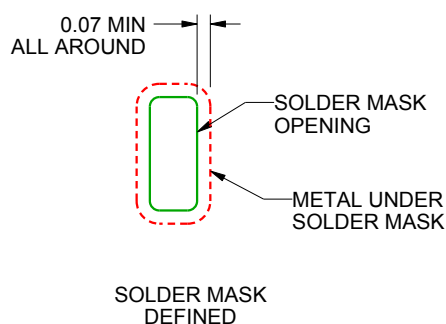
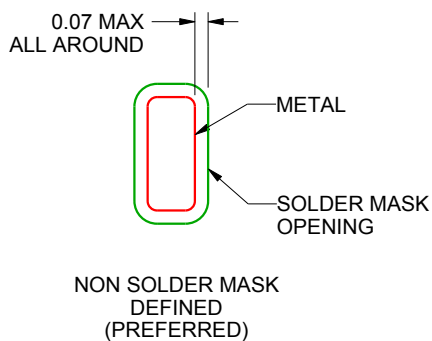
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

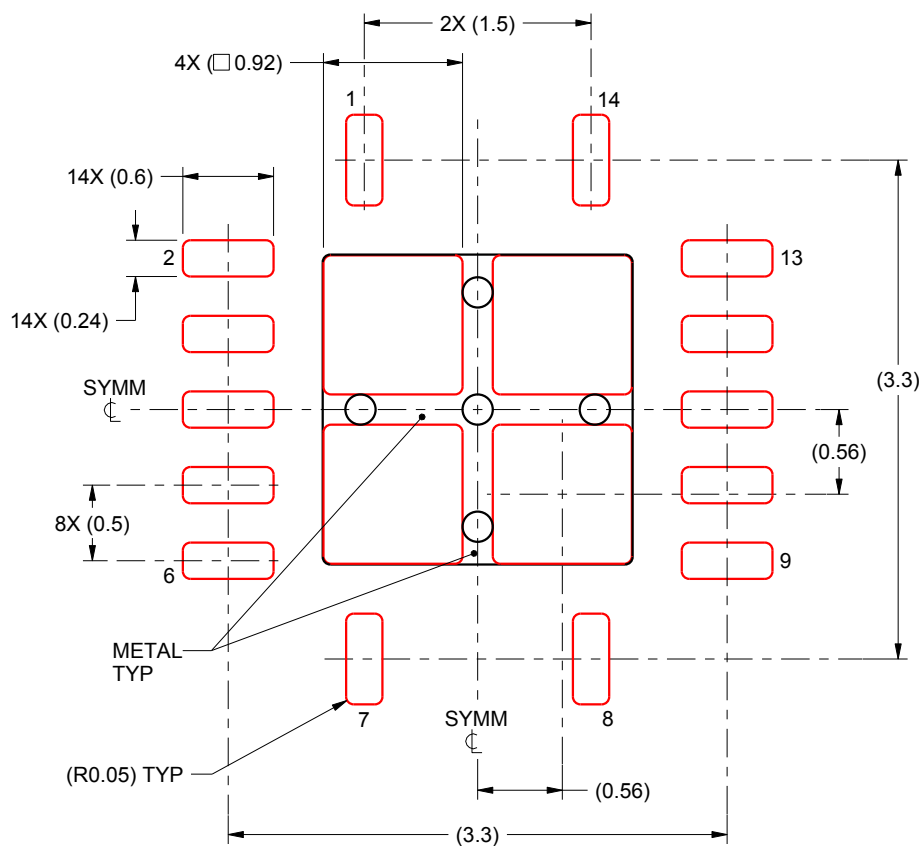
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



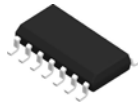
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

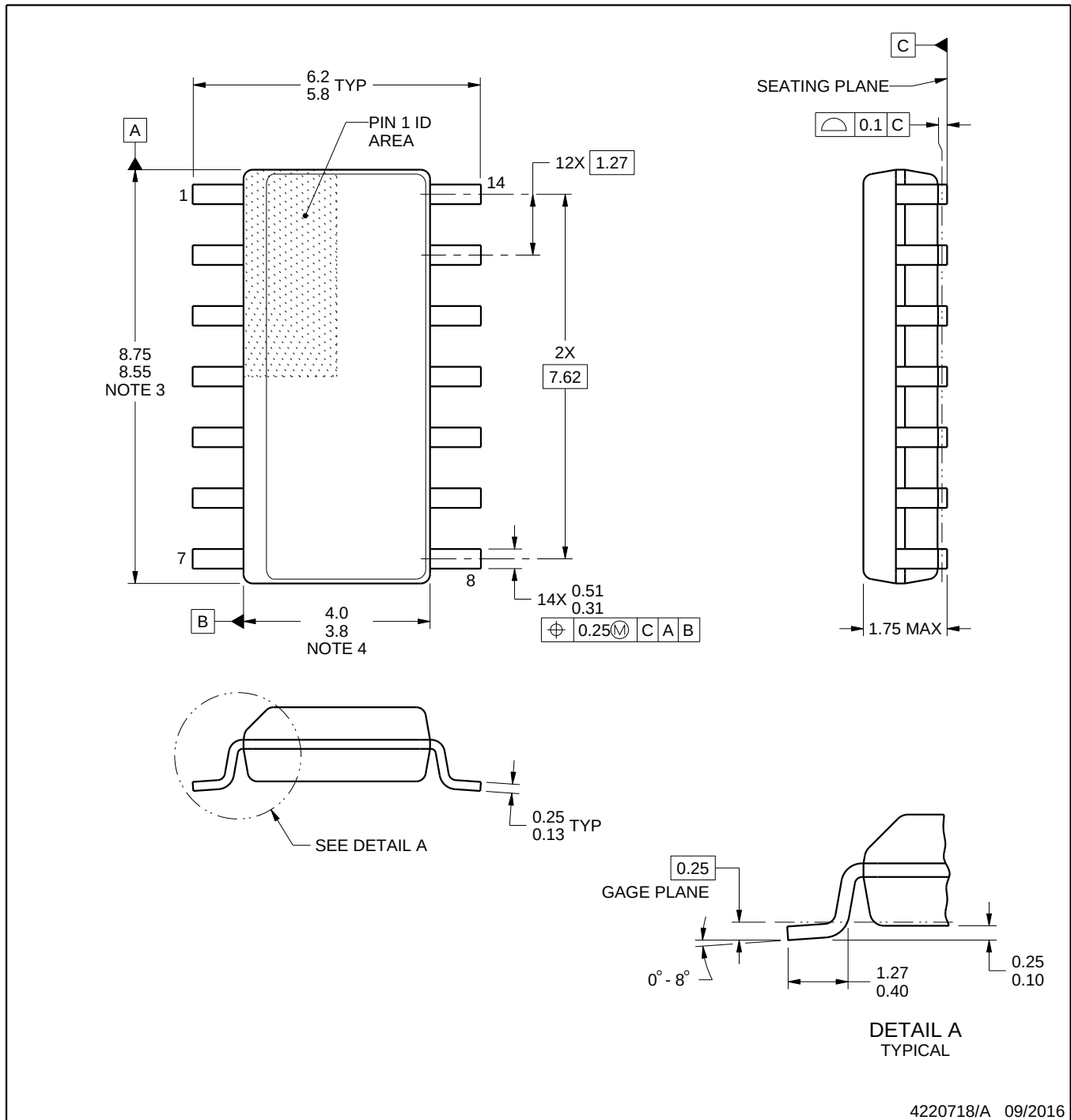
4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

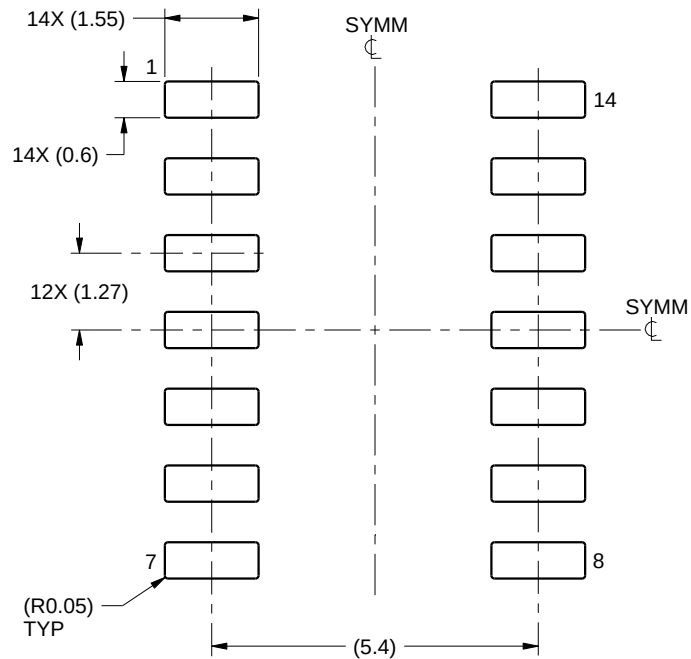
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

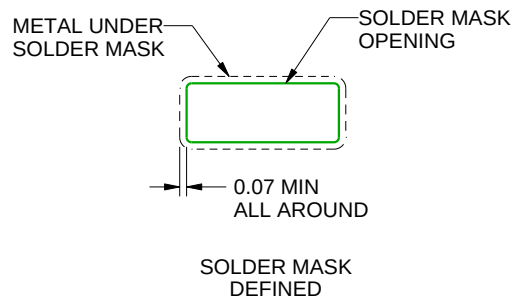
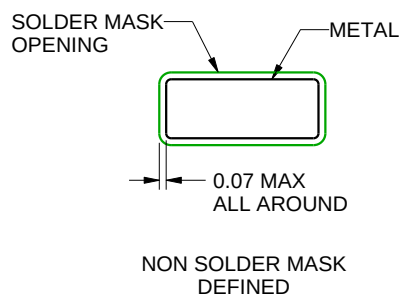
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

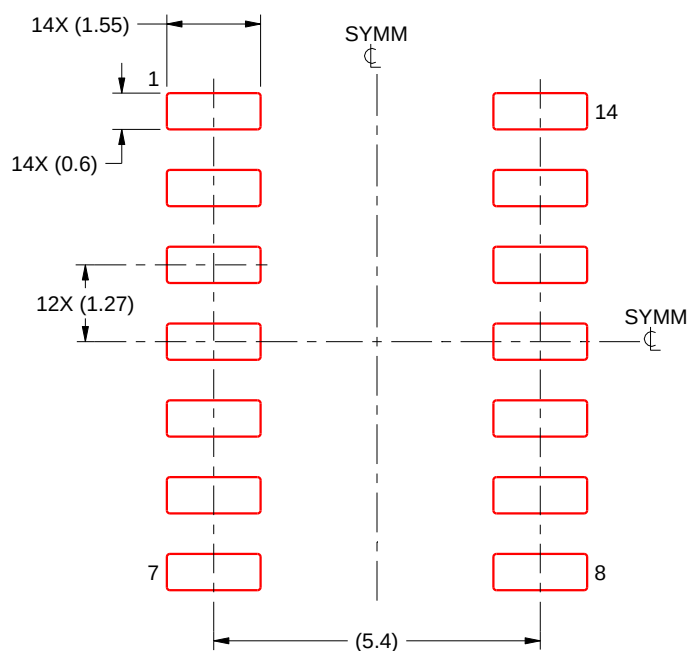
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

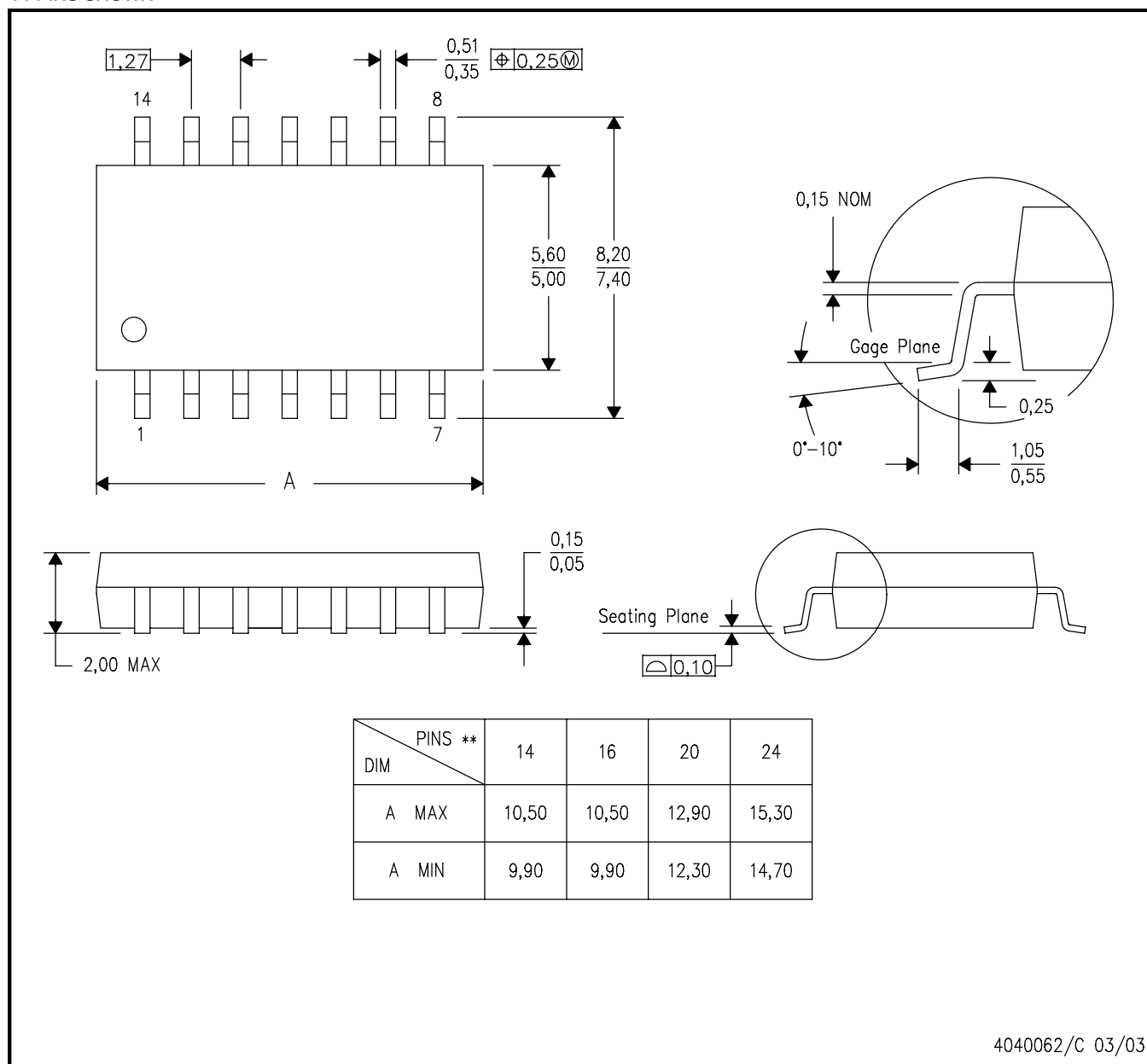
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

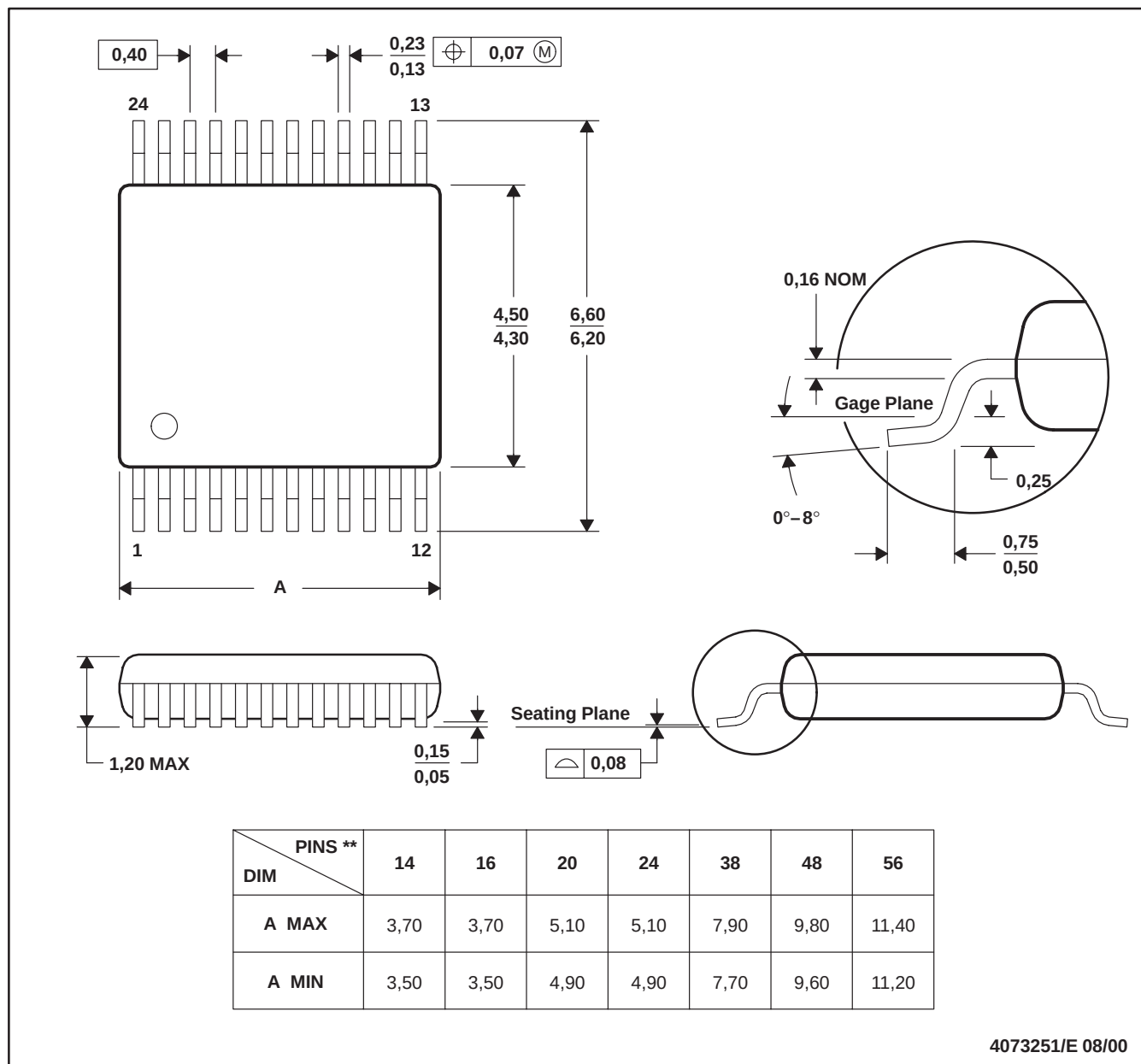


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

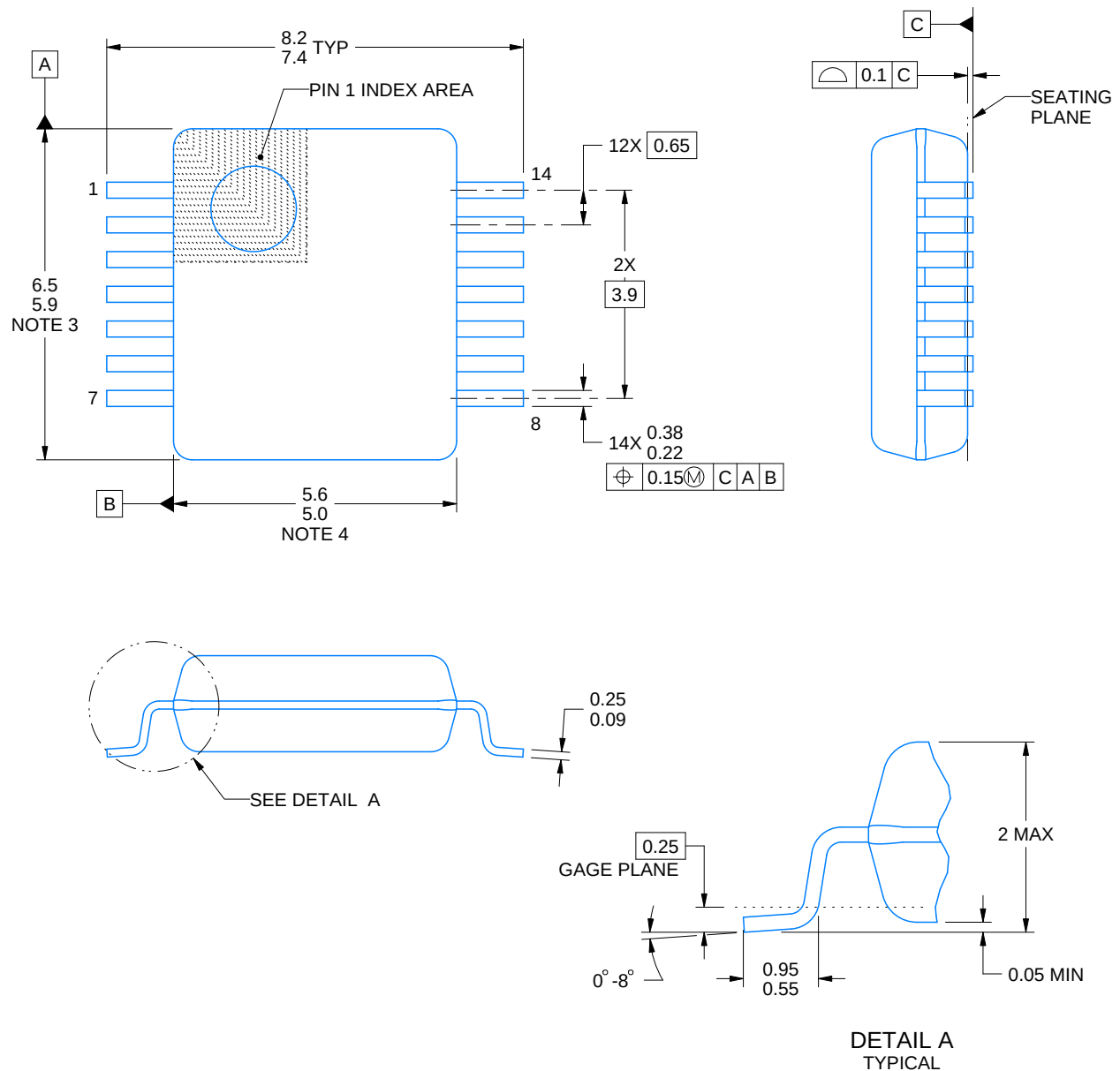
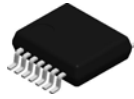
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

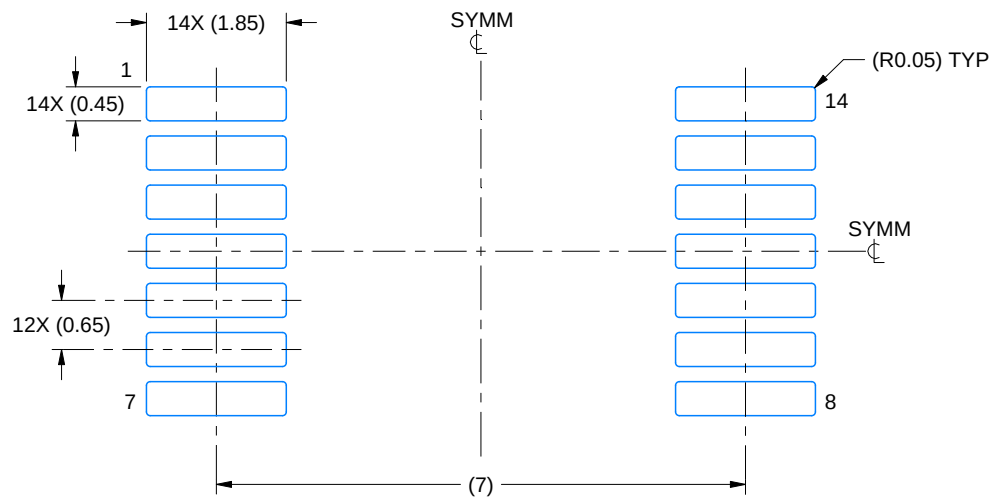
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

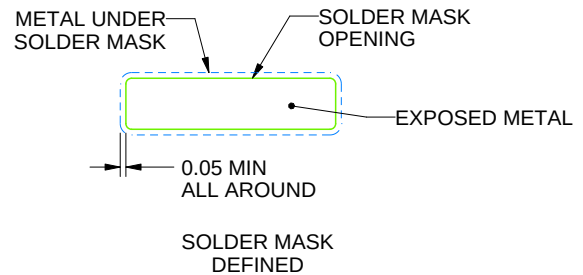
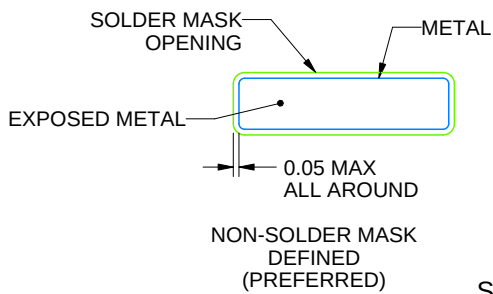
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

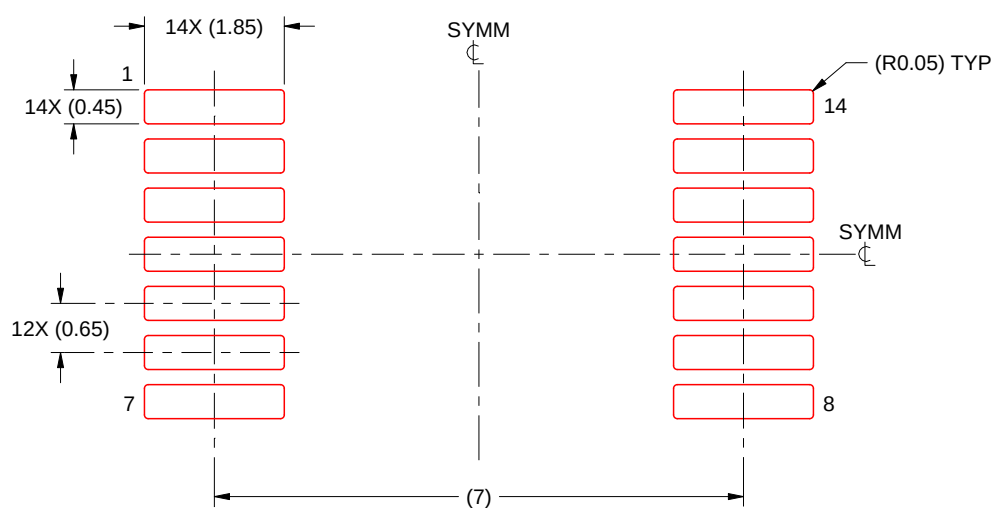
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

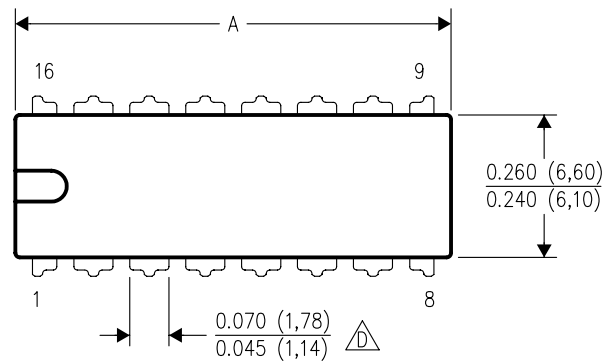
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

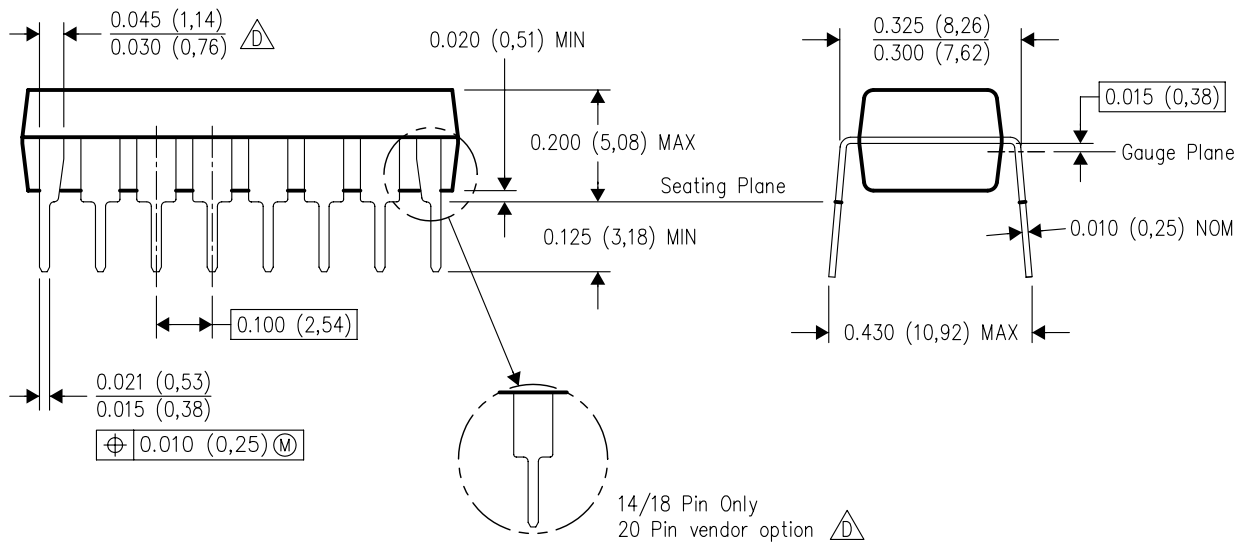
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



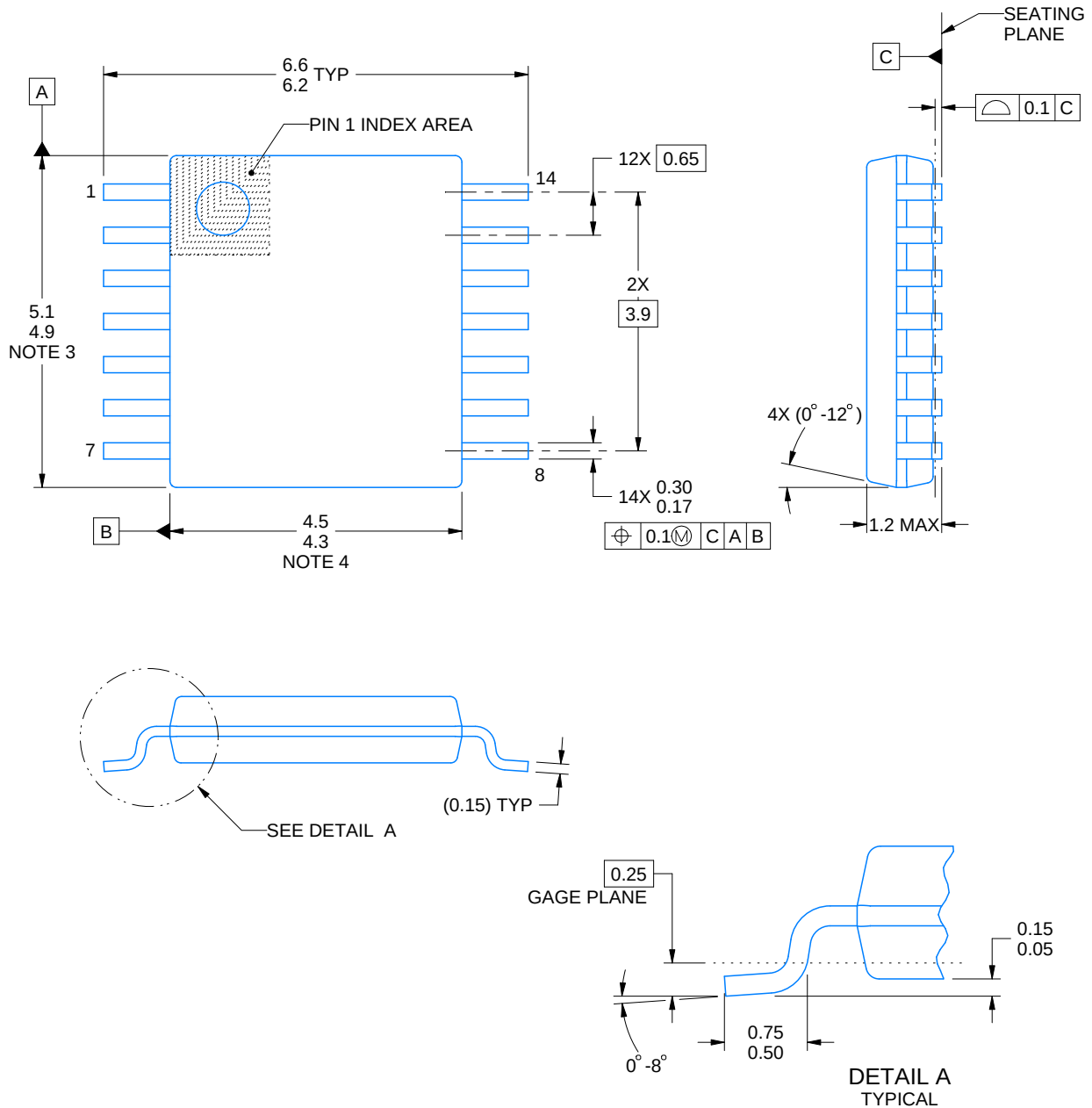
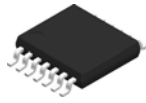
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

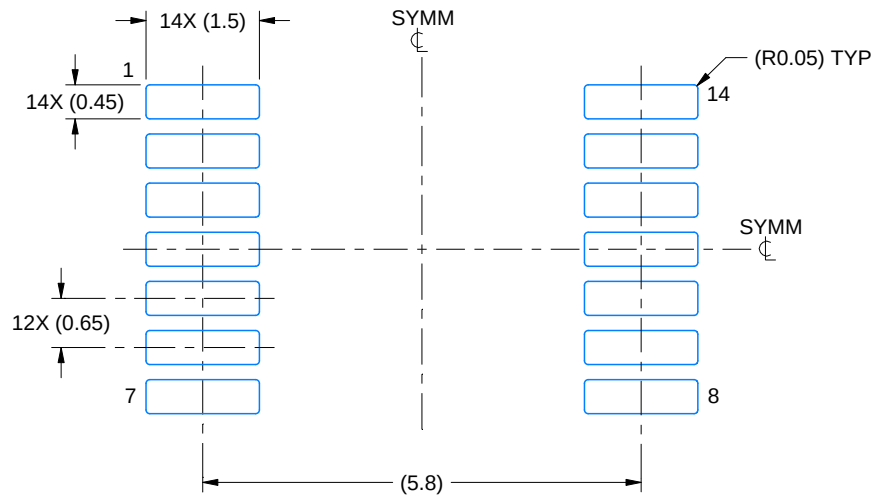
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

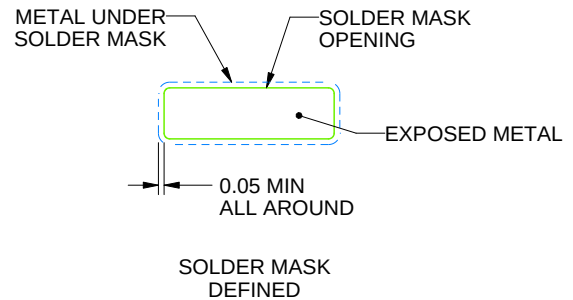
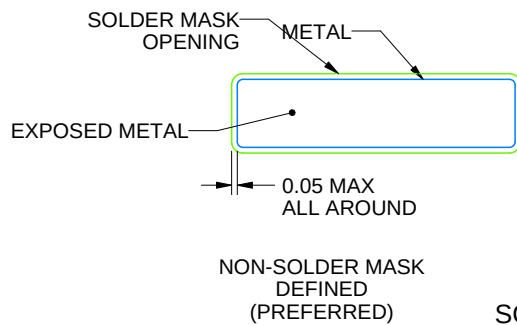
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

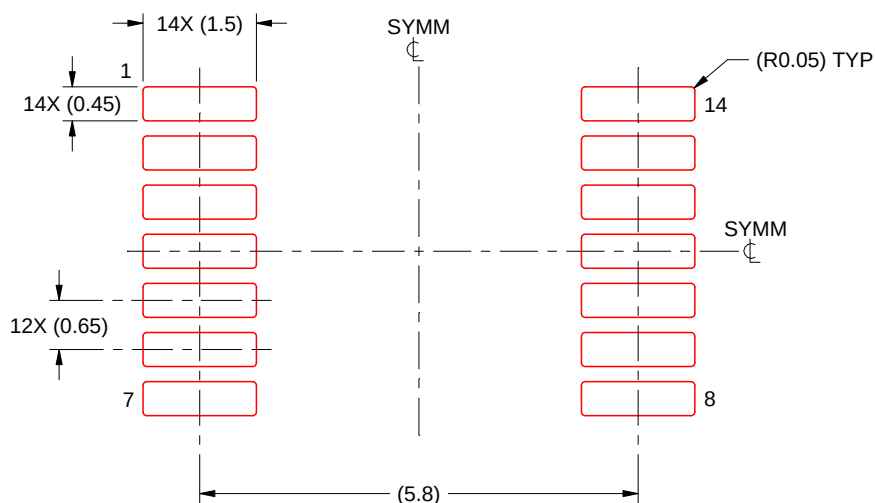
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月