

SN54AHC16240, SN74AHC16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS326G – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

description

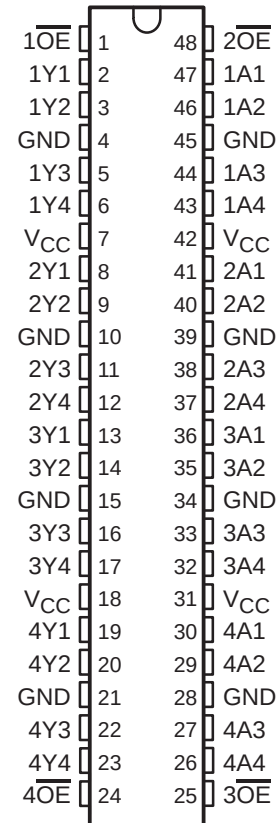
The 'AHC16240 devices are 16-bit buffers and line drivers designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. They provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16240 is characterized for operation from -40°C to 85°C .

SN54AHC16240 . . . WD PACKAGE
SN74AHC16240 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z



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**TEXAS
INSTRUMENTS**

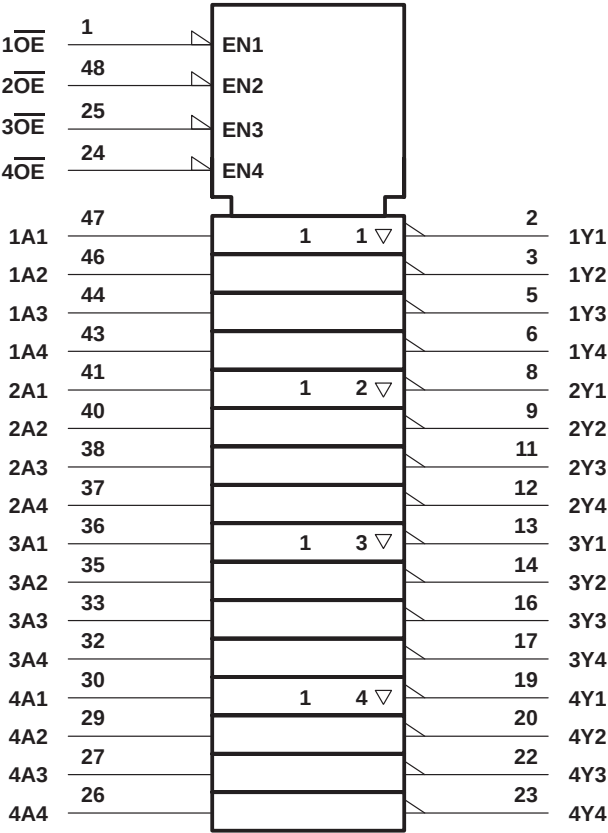
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SN54AHC16240, SN74AHC16240
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

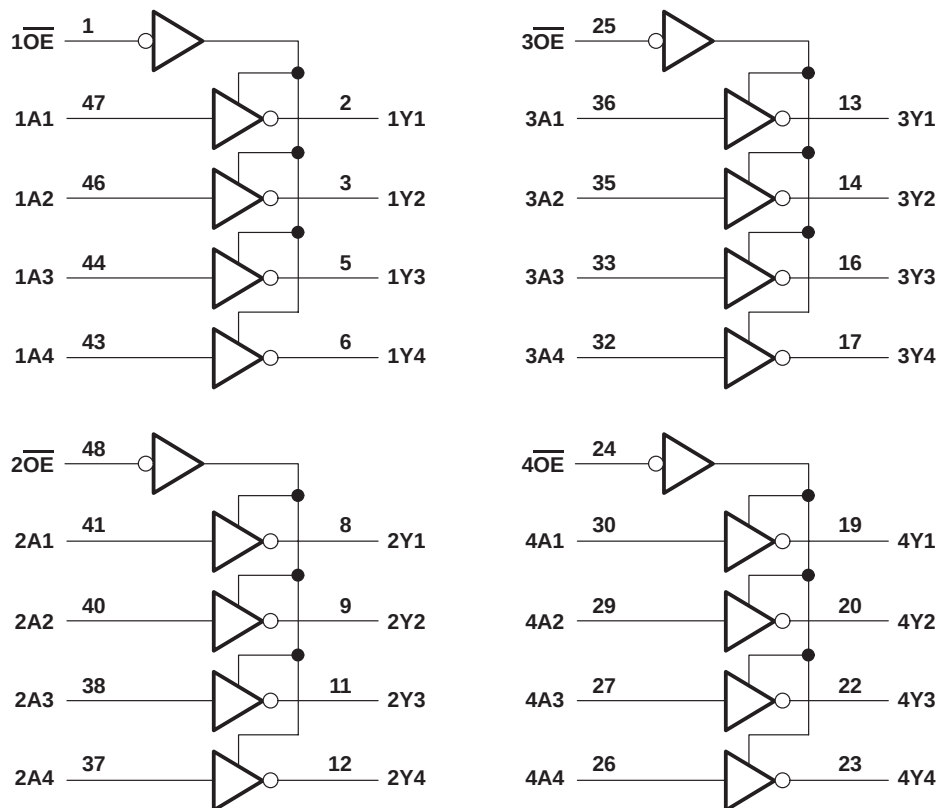
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through each V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN54AHC16240, SN74AHC16240

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54AHC16240		SN74AHC16240		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 3 V	0.9		0.9		
		V _{CC} = 5.5 V	1.65		1.65		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 3.3 ± 0.3 V	−4		−4		mA
		V _{CC} = 5 ± 0.5 V	−8		−8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 3.3 ± 0.3 V	4		4		mA
		V _{CC} = 5 ± 0.5 V	8		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 ± 0.3 V	100		100		ns/V
		V _{CC} = 5 ± 0.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^{\circ}\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.5		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	0 V to 5.5 V			± 0.1		$\pm 1^*$		± 1	μA
I_{OZ}	$V_O = V_{CC}$ or GND, V_I (OE) = V_{IL} or V_{IH}	5.5 V			± 0.25		± 2.5		± 2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_O	$V_O = V_{CC}$ or GND	5 V		3.5						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0\text{ V}$.

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SN54AHC16240, SN74AHC16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5.3*	8.4*		1*	10*	1	10	ns
t_{PHL}				5.3*	8.4*		1*	10*	1	10	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	6.6*	10.6*		1*	12.5*	1	12.5	ns
t_{PZL}				6.6*	10.6*		1*	12.5*	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	7.8*	11.5*		1*	12.5*	1	12.5	ns
t_{PLZ}				7.8*	11.5*		1*	12.5*	1	12.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	7.8	11.9*		1	13.5	1	13.5	ns
t_{PHL}				7.8	11.9		1	13.5	1	13.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	9.1	14.1		1	16	1	16	ns
t_{PZL}				9.1	14.1		1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	10.3	14		1	16	1	16	ns
t_{PLZ}				10.3	14		1	16	1	16	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5**					1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.6*	6*		1*	7*	1	6.5	ns
t_{PHL}				3.6*	6*		1*	7*	1	6.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.7*	7.3*		1*	8.5*	1	8.5	ns
t_{PZL}				4.7*	7.3*		1*	8.5*	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5.2*	7.2*		1*	8.5*	1	8.5	ns
t_{PLZ}				5.2*	7.2*		1*	8.5*	1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.1	8		1	9	1	8.5	ns
t_{PHL}				5.1	8		1	9	1	8.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.2	9.3		1	10.5	1	10.5	ns
t_{PZL}				6.2	9.3		1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.7	9.2		1	10.5	1	10.5	ns
t_{PLZ}				6.7	9.2		1	10.5	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1**					1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC16240			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

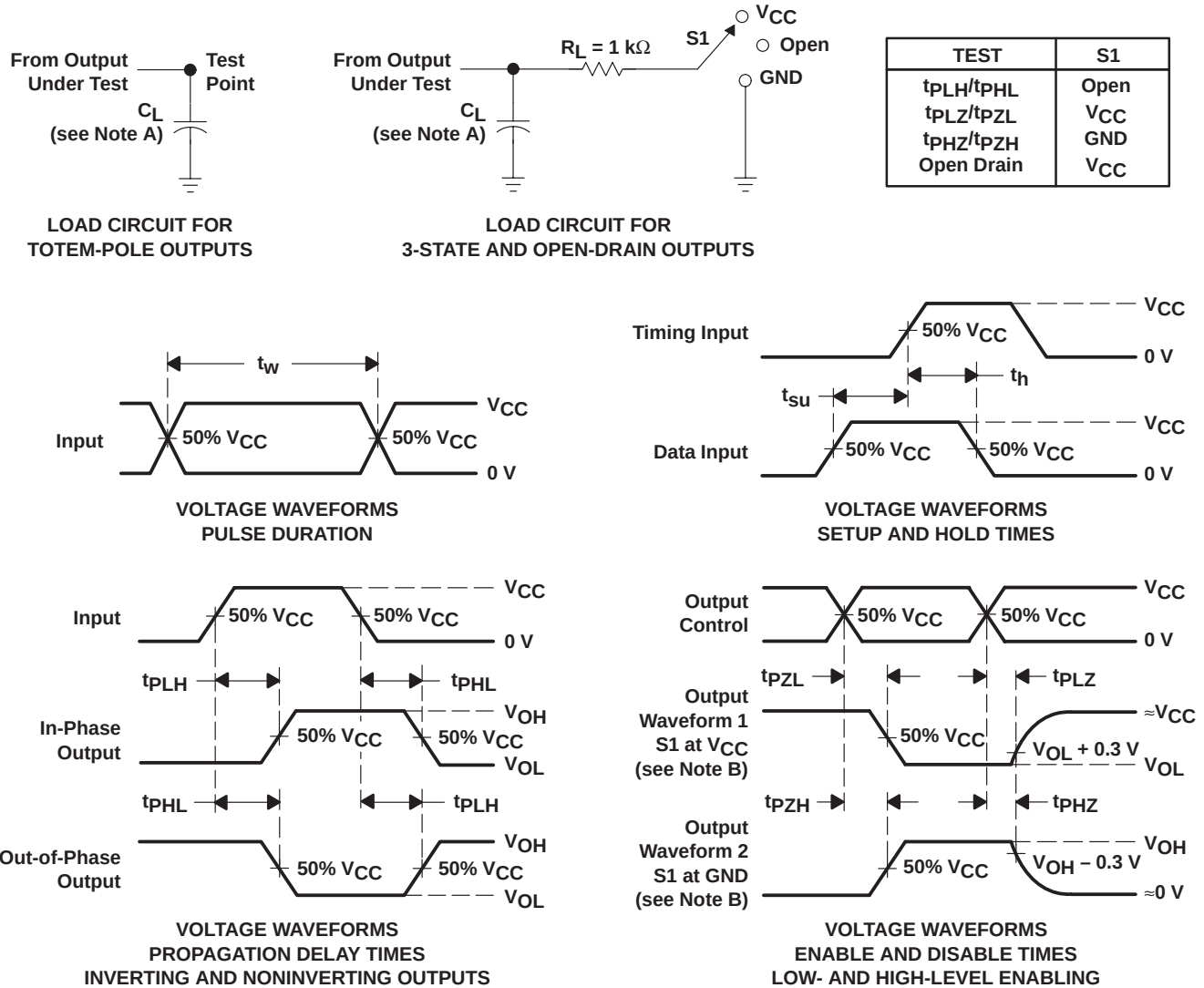
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC16240DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240
SN74AHC16240DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240
SN74AHC16240DGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE240
SN74AHC16240DGVR.A	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE240
SN74AHC16240DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240
SN74AHC16240DL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

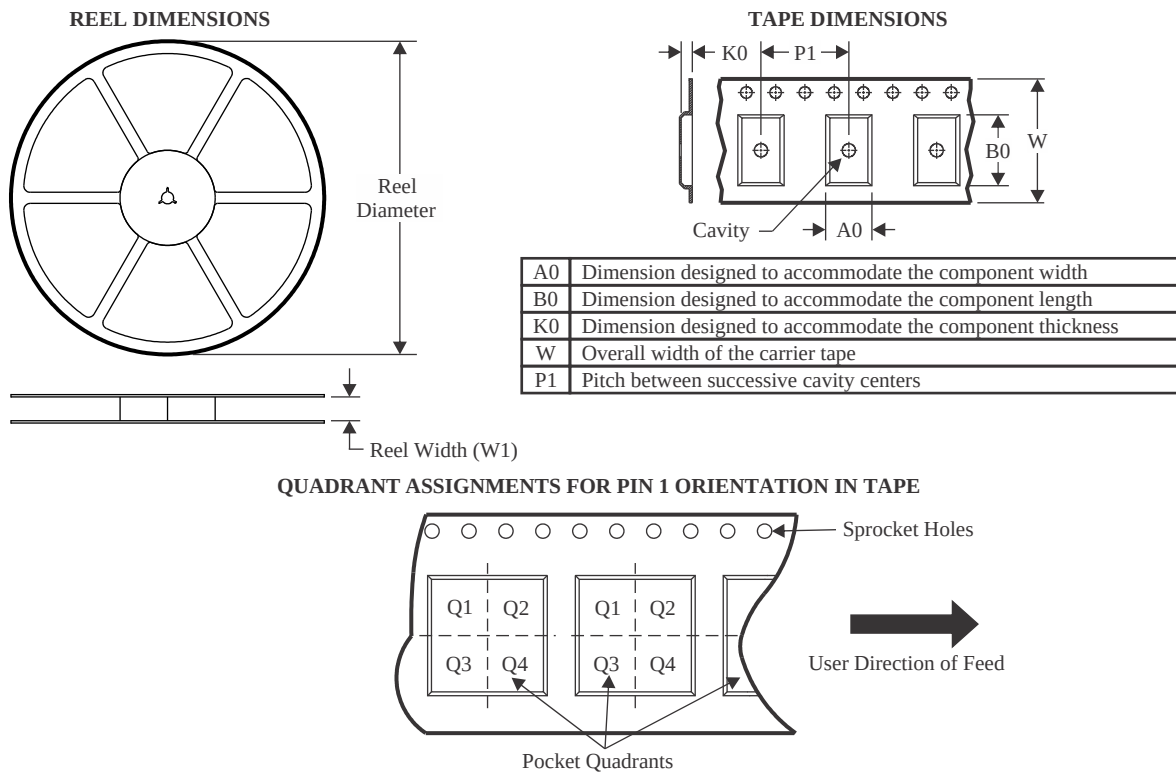
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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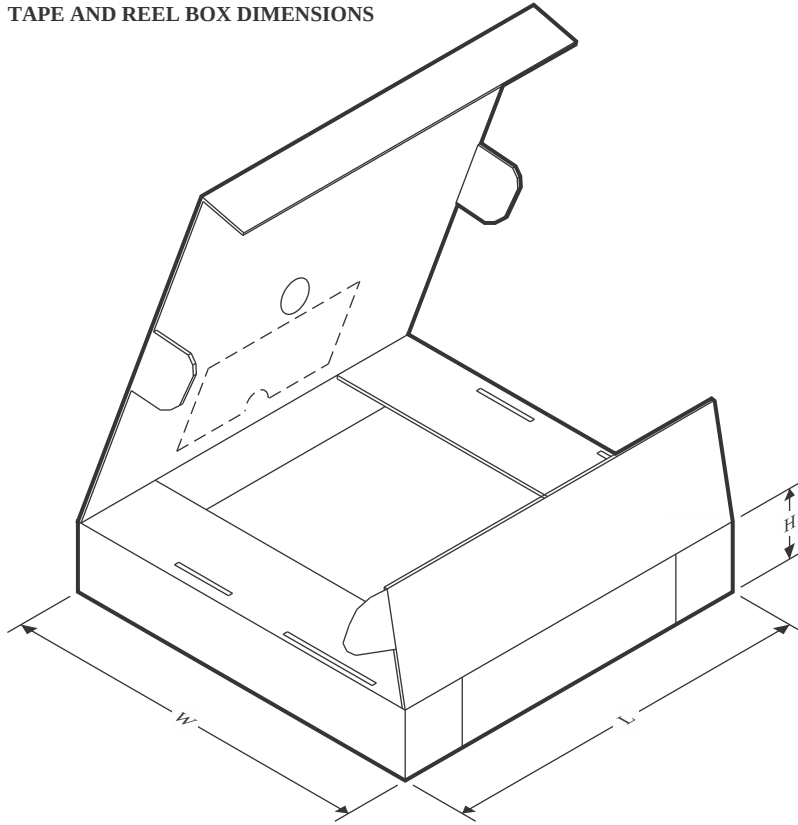
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16240DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AHC16240DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

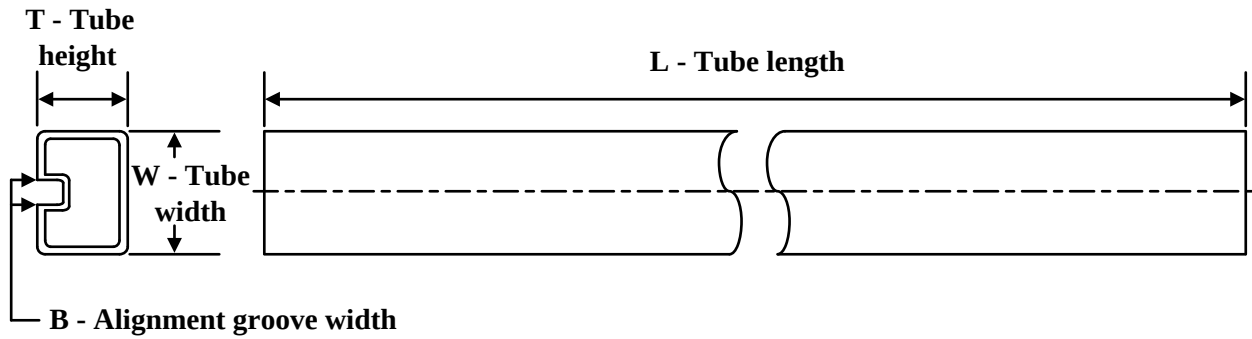
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16240DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AHC16240DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0

TUBE

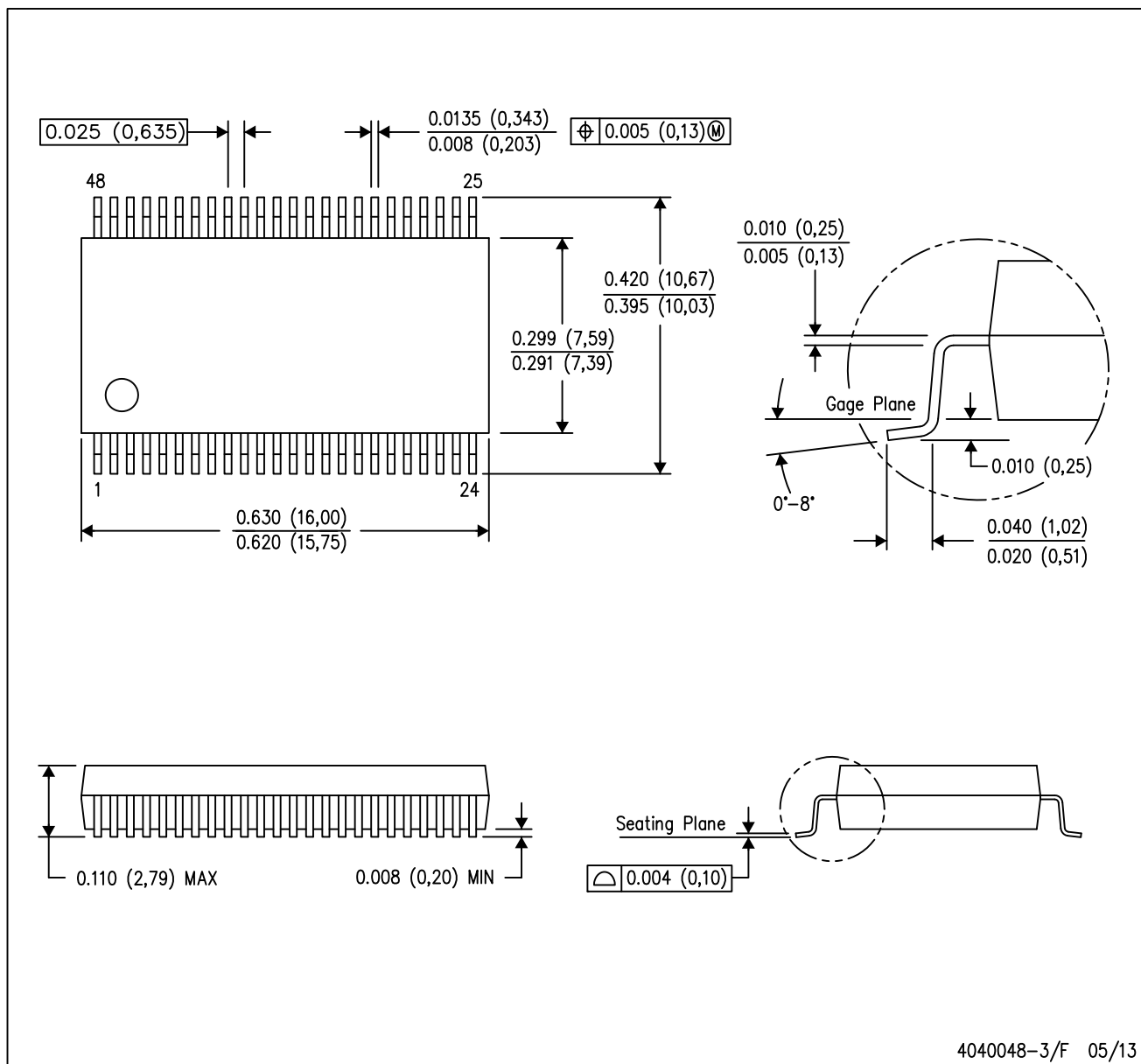


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC16240DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74AHC16240DL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

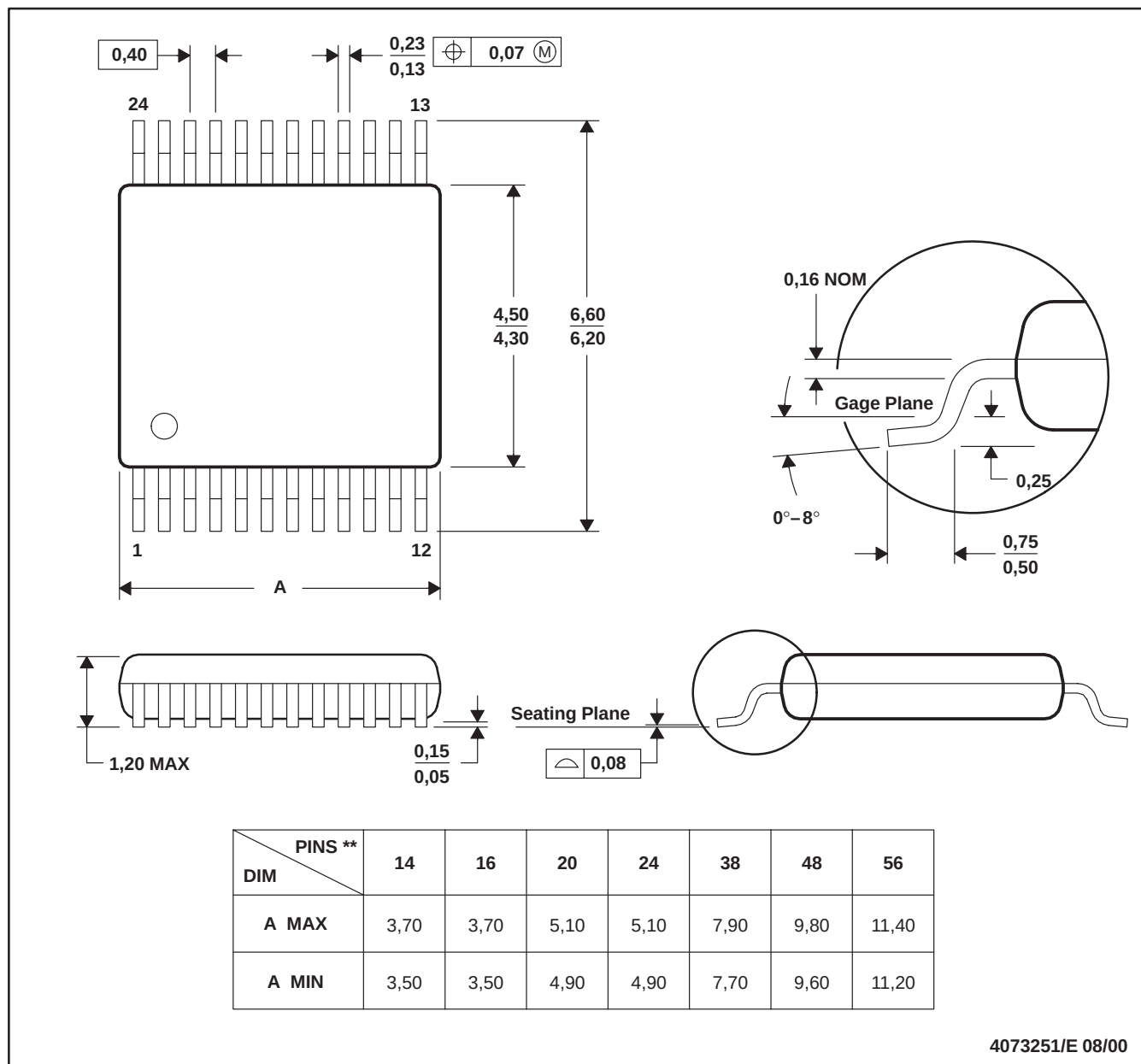


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

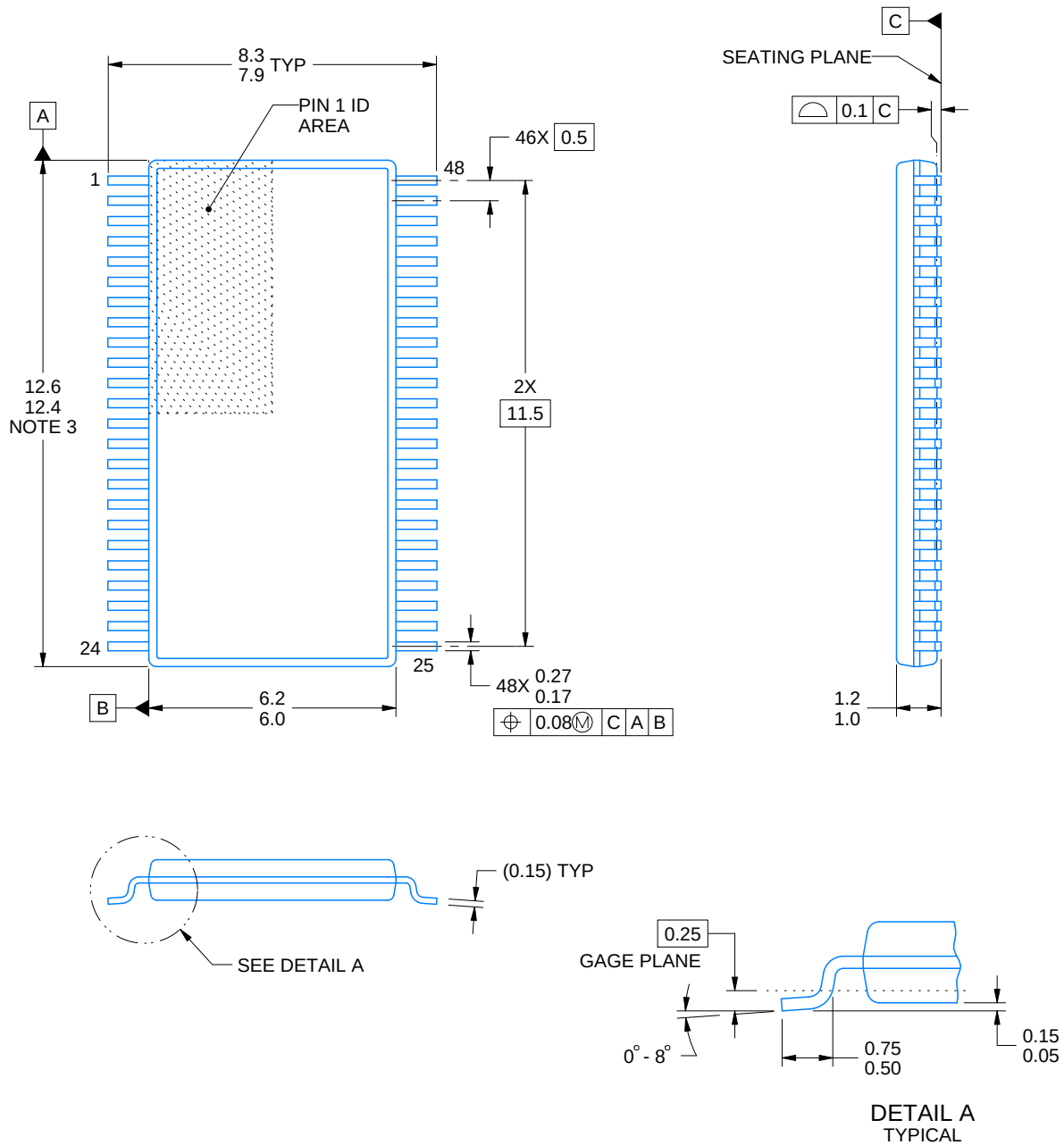
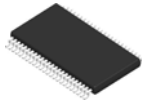
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

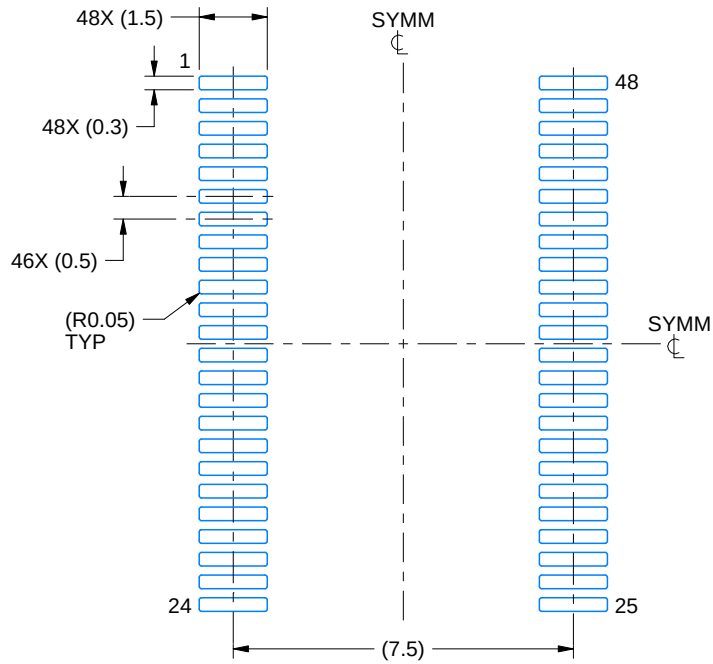
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

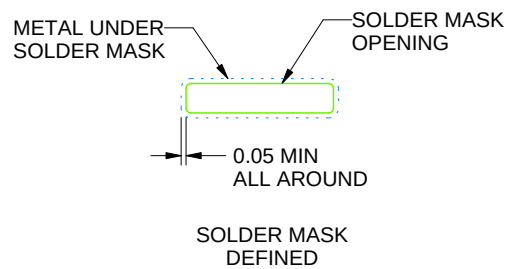
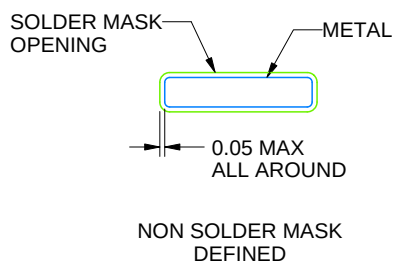
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

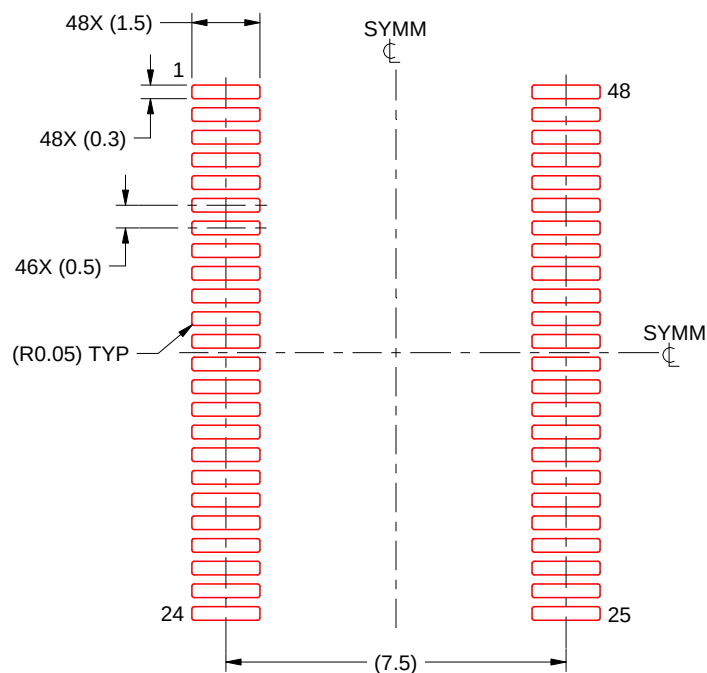
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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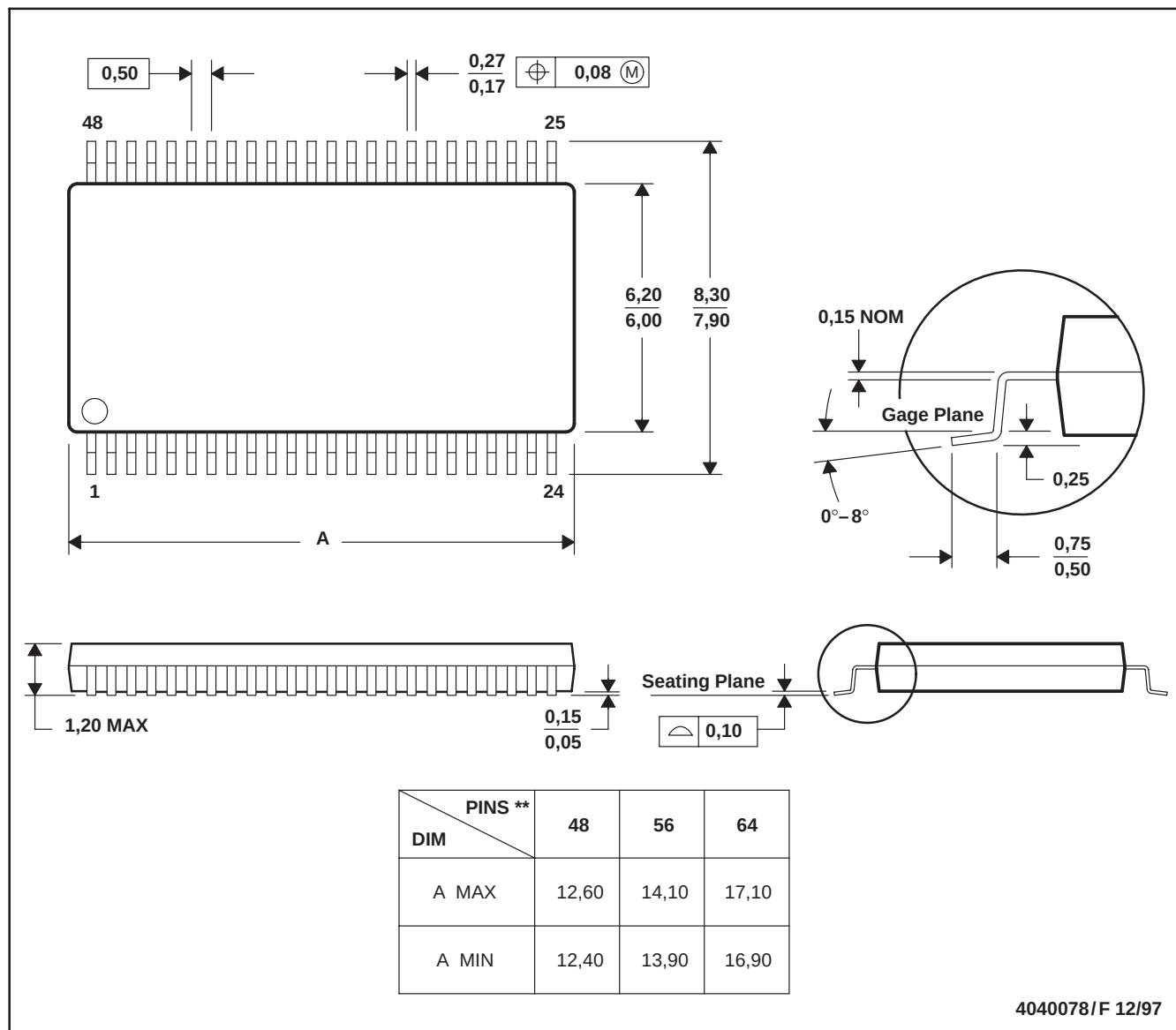
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Last updated 10/2025