TEXAS INSTRUMENTS
SN54ACT240, SN74ACT240
ZHCSS61G – JUNE 1995 – REVISED MARCH 2024

SNx4ACT240 具有三态输出的八通道缓冲器或驱动器

1 特性

- 工作电压范围为 4.5V 至 5.5V V_{CC}
- 输入电压高达 5.5V
- 5V 时,t_{pd} 最大值为 8.5ns
- 输入与 TTL 兼容

2 应用

- 手持终端：智能手机
- 网络交换机
- 健康与健身/可穿戴设备

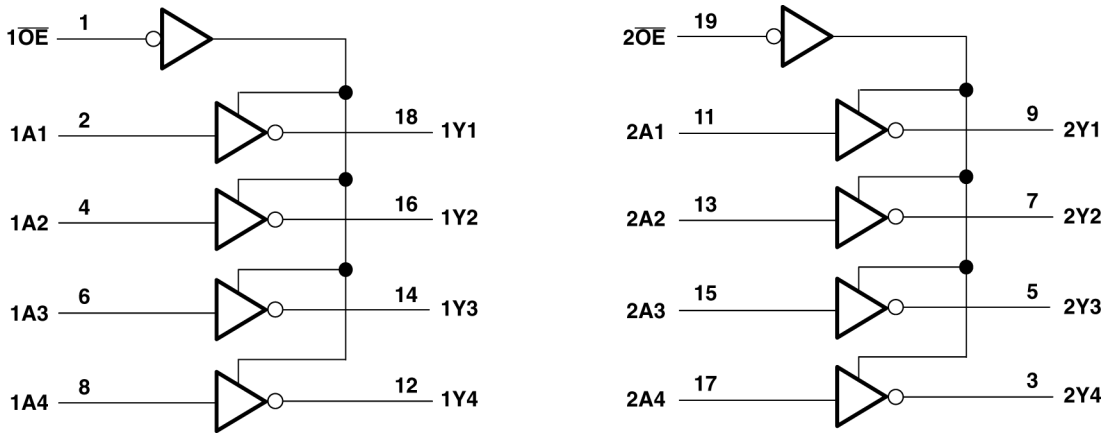
3 说明

这些八通道缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线用接收器和发送器的性能和密度。

封装信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SN74ACT240	N（PDIP，20）	24.33mm × 9.4mm	24.33mm × 6.35mm
	DGS（VSSOP，20）	5.1mm × 4.9mm	5.1mm × 3mm
	DW（SOIC，20）	12.8mm × 10.3mm	12.80mm × 7.50mm
	NS（SOP，20）	12.6mm × 7.8mm	12.6mm × 5.3mm
	DB（SSOP，20）	7.2mm × 7.8mm	7.2mm × 5.3mm
	PW（TSSOP，20）	6.5mm × 6.4mm	6.5mm × 4.4mm
	RKS（VQFN，20）	4.5mm × 2.5mm	4.5mm × 2.5mm

(1) 有关更多信息，请参阅第 10 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

内容

4 引脚配置和功能

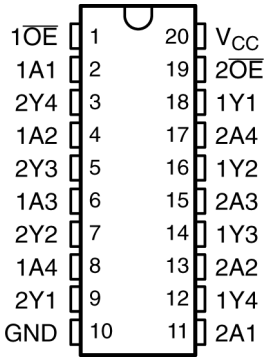


图 4-1. SN54ACT240 J 或 W 封装；SN74ACT240 DB、DGS、DW、N、NS 或 PW 封装（顶视图）

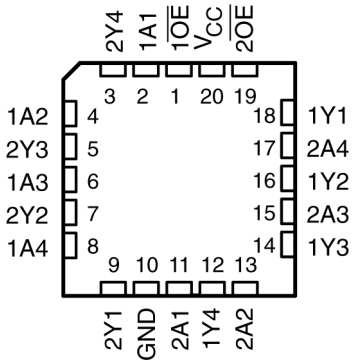


图 4-2. SN54ACT240 FK 封装（顶视图）

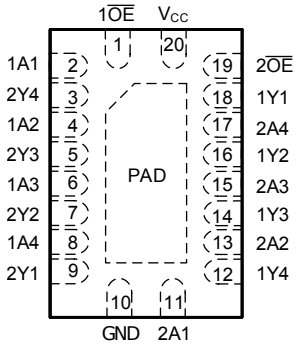


图 4-3. SNx4ACT240 VQFN 封装（顶视图）

表 4-1. 引脚功能

引脚		类型[1]	说明
名称	编号		
1OE	1	I	输出使能 1
1A1	2	I	1A1 输入
2Y4	3	O	2Y4 输出
1A2	4	I	1A2 输入
2Y3	5	O	2Y3 输出
1A3	6	I	1A3 输入
2Y2	7	O	2Y2 输出
1A4	8	I	1A4 输入
2Y1	9	O	2Y1 输出
GND	10	—	接地引脚
2A1	11	I	2A1 输入
1Y4	12	O	1Y4 输出
2A2	13	I	2A2 输入
1Y3	14	O	1Y3 输出
2A3	15	I	2A3 输入
1Y2	16	O	1Y2 输出
2A4	17	I	2A4 输入

表 4-1. 引脚功能（续）

引脚		类型(1)	说明
名称	编号		
1Y1	18	O	1Y1 输出
$2\overline{OE}$	19	I	输出使能 2
VCC	20	—	电源引脚
散热焊盘(2)		—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源。

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出
(2) 仅限 RKS 封装

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I (2)	输入电压范围		- 0.5	V_{CC}+0.5	V
V_O (2)	输出电压范围		- 0.5	V_{CC}+0.5	V
I_{IK}	输入钳位电流	（V_I < 0 或 V_I > V_{CC}）		±20	mA
I_{OK}	输出钳位电流	（V_O < 0 或 V_O > V_{CC}）		±20	mA
I_O	持续输出电流	（V_O = 0 或 V_{CC}）		±50	mA
	通过 V_{CC} 或 GND 的持续电流			±200	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 超出*绝对最大额定值*下列出的压力可能会对器件造成永久损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在*建议的工作条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		SN54ACT240		SN74ACT240		单位
		最小值	最大值	最小值	最大值	
V_{CC}	电源电压	4.5	5.5		5.5	V
V_{IH}	高电平输入电压	2				V
V_{IL}	低电平输入电压		0.8		0.8	V
V_I	输入电压	0	V_{CC}		V_{CC}	V
V_O	输出电压	0	V_{CC}		V_{CC}	V
I_{OH}	高电平输出电流		-24		-24	mA
I_{OL}	低电平输出电流		24		24	mA
$\Delta t/\Delta v$	输入转换上升或下降速率		8		8	ns/V
T_A	自然通风条件下的工作温度范围	-55	125		85	°C

(1) 器件所有的未使用输入必须被保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢变化或悬空的影响*，文献编号 SCBA004。

5.3 热性能信息

热指标(1)		DB (SSOP)	DGS (VSSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	RKS (VQFN)	单位
		20 引脚							
$R_{\theta JA}$	结至环境热阻(2)	70	123.5	101.2	69	60	126.2	68	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标*应用报告 SPRA953。
(2) 封装热阻抗根据 JESD 51-7 计算。

5.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件		V_{CC}	T_A = 25°C			SN54ACT240		SN74ACT240		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA		4.5V	4.4	4.49		4.4		4.4		V
			5.5V	5.4	5.49		5.4		5.4		
	I_{OH}=-24mA		4.5V	3.86			3.7		3.76		
			5.5V	4.86			4.7		4.76		
	I_{OH} = – 50mA(1)		5.5V				3.85				
	I_{OH} = – 75mA(1)		5.5V						3.85		
V_{OL}	I_{OL} = 50μA		4.5V		0.001	0.1		0.1		0.1	V
			5.5V		0.001	0.1		0.1		0.1	
	I_{OL}=24mA		4.5V			0.36		0.5		0.44	
			5.5V			0.36		0.5		0.44	
	I_{OL} = 50mA(1)		5.5V					1.65			
	I_{OL} = 75mA(1)		5.5V							1.65	
I_{OZ}	V_O = V_{CC} 或 GND		5.5V			±0.25		±5		±2.5	μA
I_I	V_I=V_{CC} 或 GND		5.5V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，	I_O = 0	5.5V			4		80		40	μA
ΔI_{CC} (2)	一个输入电压为 3.4V，其他输入电压为 GND 或 V_{CC}		5.5V		0.6			1.6		1.5	mA
C_i	V_I=V_{CC} 或 GND		5V		2.5						pF
C_O	V_I=V_{CC} 或 GND		5V		8						pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 2ms。
(2) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

5.5 开关特性

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅负载电路和电压波形）

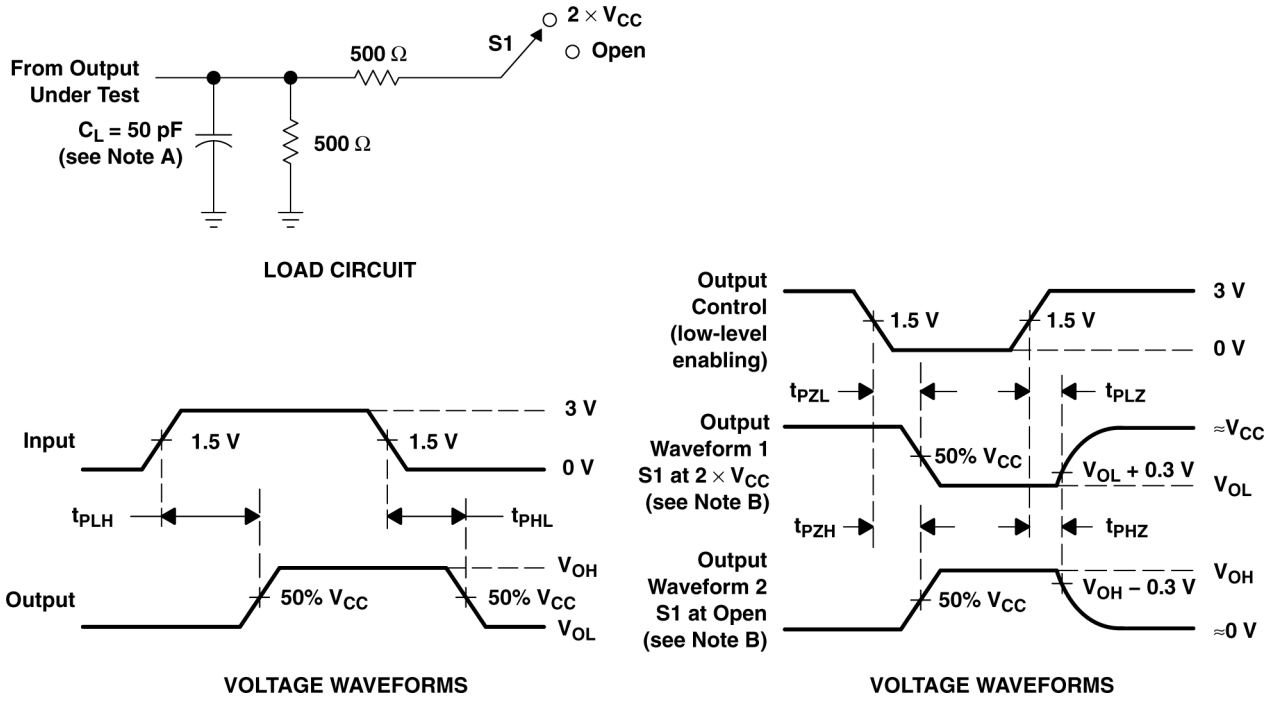
参数	从（输入）	到（输出）	T_A = 25°C			SN54ACT240		SN74ACT240		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A	Y	1.5	6	8.5	1	9.5	1.5	9.5	ns
t_{PHL}			1.5	5.5	7.5	1	9	1.5	8.5	
t_{PZH}	$\overline{OE}$	Y	1.5	7	8.5	1	10	1	9.5	ns
t_{PZL}			2	7	9.5	1	11.5	1.5	10.5	
t_{PHZ}	$\overline{OE}$	Y	2	8	9.5	1	11	2	10.5	ns
t_{PLZ}			2.5	6.5	10	1	11.5	2	10.5	

5.6 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件	典型值	单位
C_{pd}	每个缓冲器/驱动器的功率耗散电容	C_L = 50pF， f = 1MHz	45	pF

6 参数测量信息



A. C_L 包括探头和夹具电容。

B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。

C. 所有输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50 Ω，t_r ≤ 2.5ns，t_f ≤ 2.5ns。

D. 一次测量一个输出，每次测量一个输入转换。

图 6-1. 负载电路和电压波形

测试	S1
t_{PLH}/t_{PHL}	开路
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	开路

7 详细说明

7.1 概述

SNx4ACT240 器件配置为两个具有独立输出使能 ($\overline{OE}$) 输入的 4 位缓冲器或驱动器。当 $\overline{OE}$ 为低电平时，该器件将来自 A 输入的反相数据传递到 Y 输出。当 $\overline{OE}$ 为高电平时，输出处于高阻态。

要在上电或断电期间将器件置于高阻抗状态，应通过一个上拉电阻器将 $\overline{OE}$ 连接至 V_{CC}；该电阻器的最小值由驱动器的电流灌入能力决定。

7.2 功能方框图

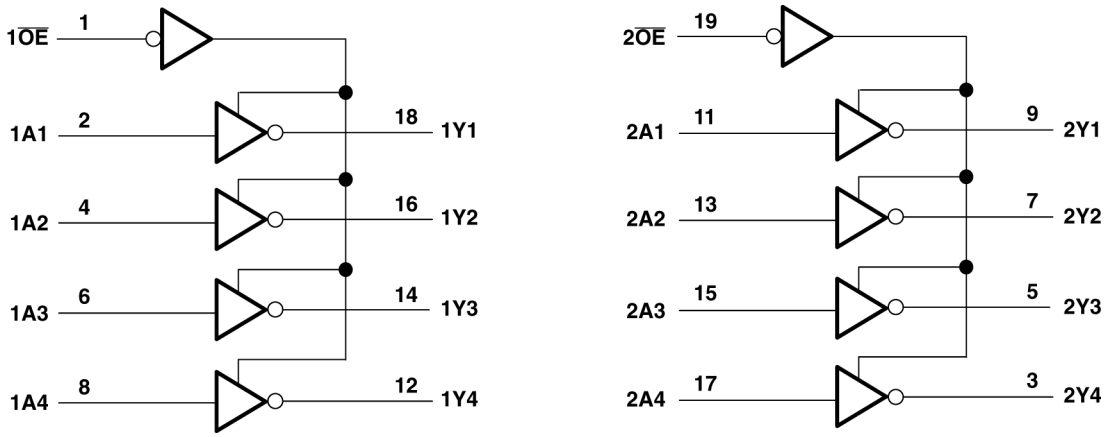


图 7-1. 逻辑图（正逻辑）

7.3 特性说明

7.3.1 平衡 CMOS 推挽式输出

该器件包括平衡 CMOS 推挽输出。术语*平衡*表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动的电流比此器件能够承受的电流更大，而不会损坏器件。务必限制器件的输出功率，以避免因过流而损坏器件。必须始终遵守*绝对最大额定值*中规定的电气和热限值。

未使用的推挽 CMOS 输出必须保持断开状态。

7.4 器件功能模式

表 7-1. 功能表（每个缓冲器）

输入		输出
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (November 2023) to Revision G (March 2024)	Page
• 向*器件信息* 表、*引脚配置和功能* 部分和*热性能信息* 表中添加了 DGS 和 PW 封装	1
• 向*器件信息* 表中添加了本体尺寸	1

Changes from Revision E (November 2023) to Revision F (March 2024)	Page
• 更新了 R θ JA 值：DW = 58 至 101.2，PW = 83 至 126.2，所有值均以 °C/W 为单位	5

10 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8775901M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901M2A SNJ54ACT240FK
5962-8775901MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MRA SNJ54ACT240J
5962-8775901MSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MSA SNJ54ACT240W
SN74ACT240DBR	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240DBR.A	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T240
SN74ACT240DGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T240
SN74ACT240DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT240
SN74ACT240DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT240
SN74ACT240N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT240N
SN74ACT240N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT240N
SN74ACT240NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT240
SN74ACT240NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT240
SN74ACT240PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	AD240
SN74ACT240PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240PWRG4	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240PWRG4.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD240
SN74ACT240RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ACT240
SN74ACT240RKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ACT240
SNJ54ACT240FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901M2A SNJ54ACT240FK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ACT240FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901M2A SNJ54ACT 240FK
SNJ54ACT240J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MR A SNJ54ACT240J
SNJ54ACT240J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MR A SNJ54ACT240J
SNJ54ACT240W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MS A SNJ54ACT240W
SNJ54ACT240W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775901MS A SNJ54ACT240W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54ACT240, SN74ACT240 :

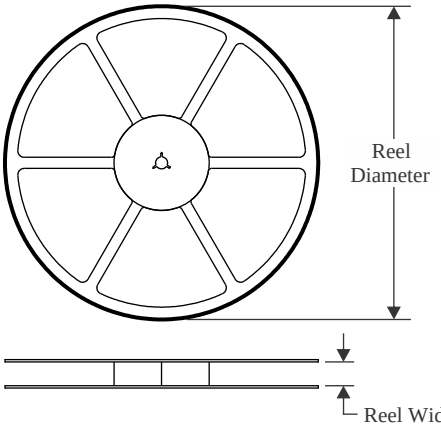
- Catalog : SN74ACT240
- Automotive : SN74ACT240-Q1, SN74ACT240-Q1
- Military : SN54ACT240

NOTE: Qualified Version Definitions:

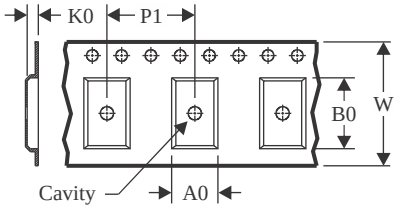
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

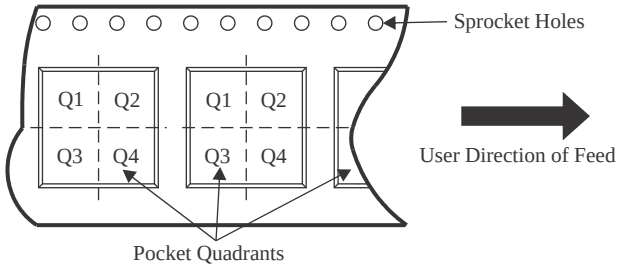


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

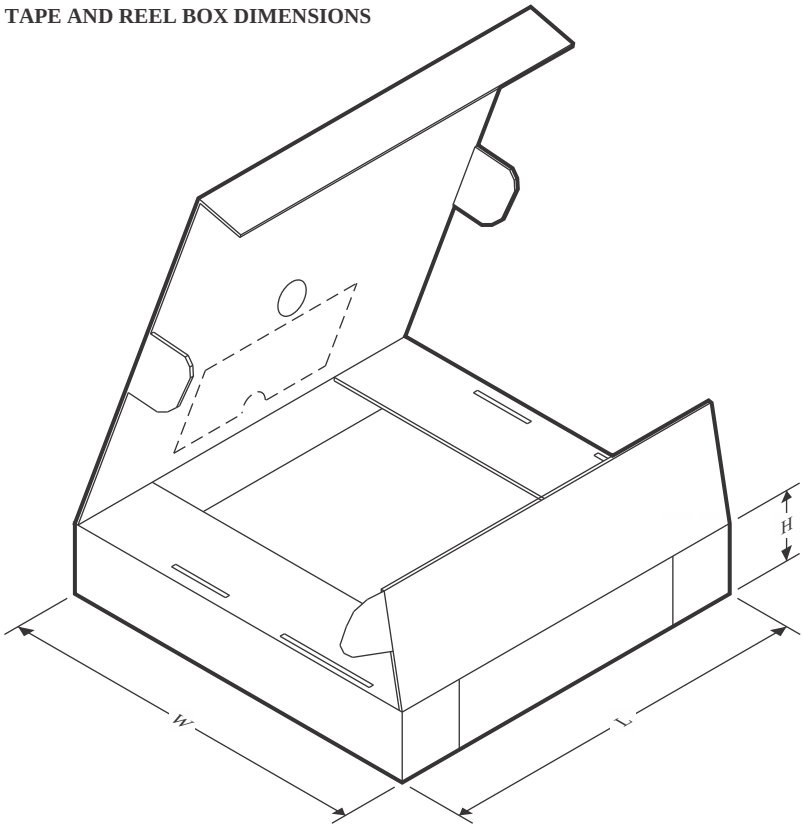
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT240DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74ACT240DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT240PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT240RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

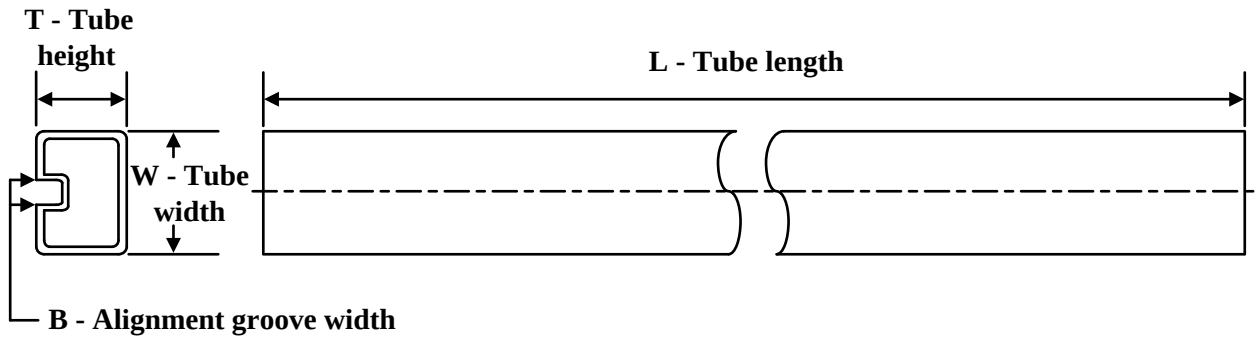
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT240DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ACT240DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74ACT240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT240NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ACT240PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT240PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT240RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

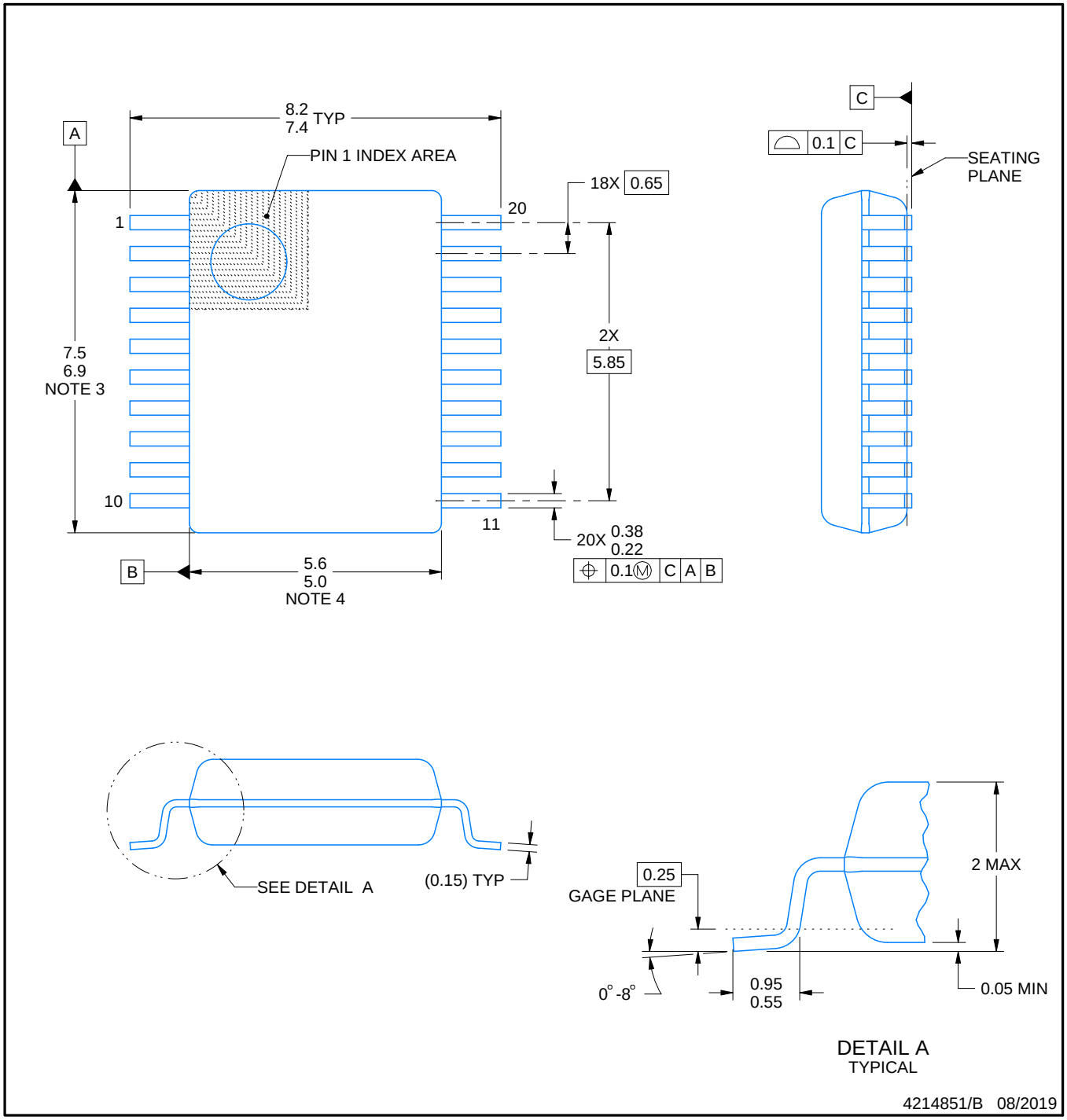
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8775901M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8775901MSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ACT240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT240N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT240FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT240W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ACT240W.A	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

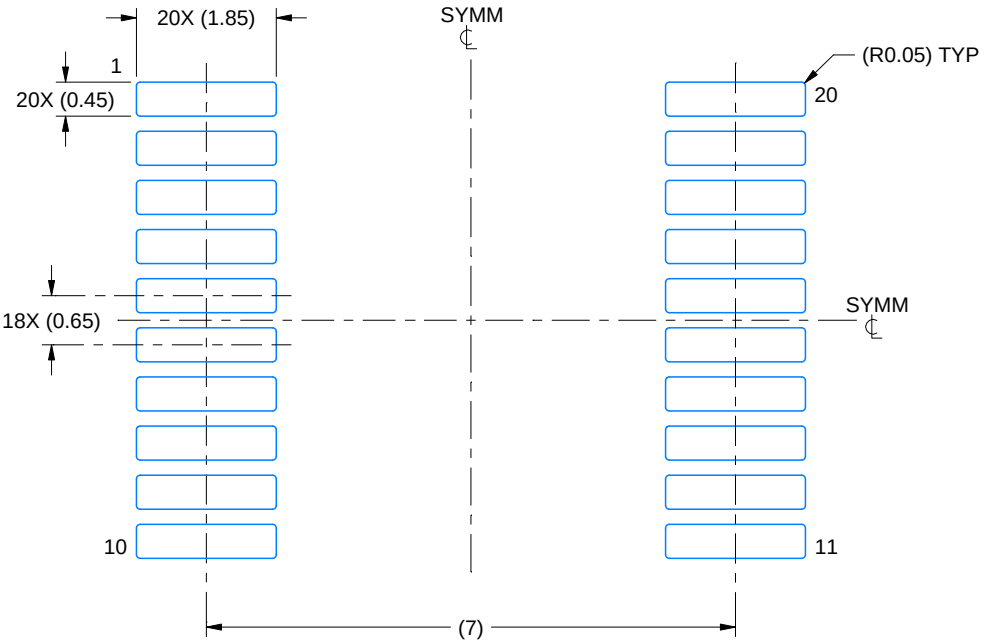
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

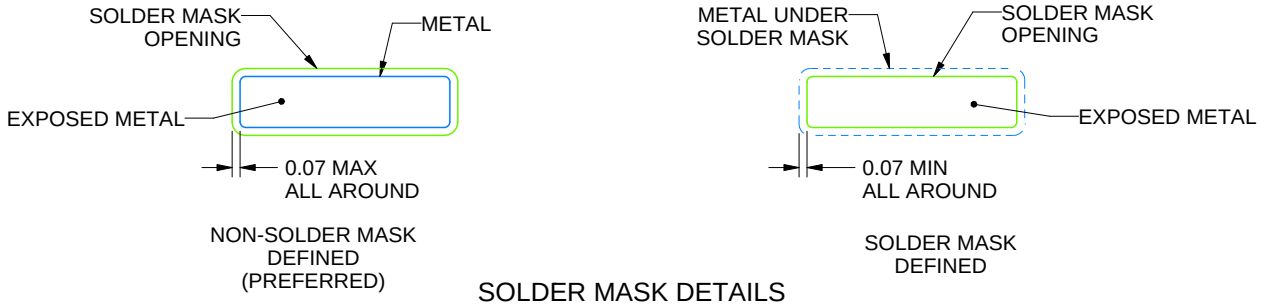


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

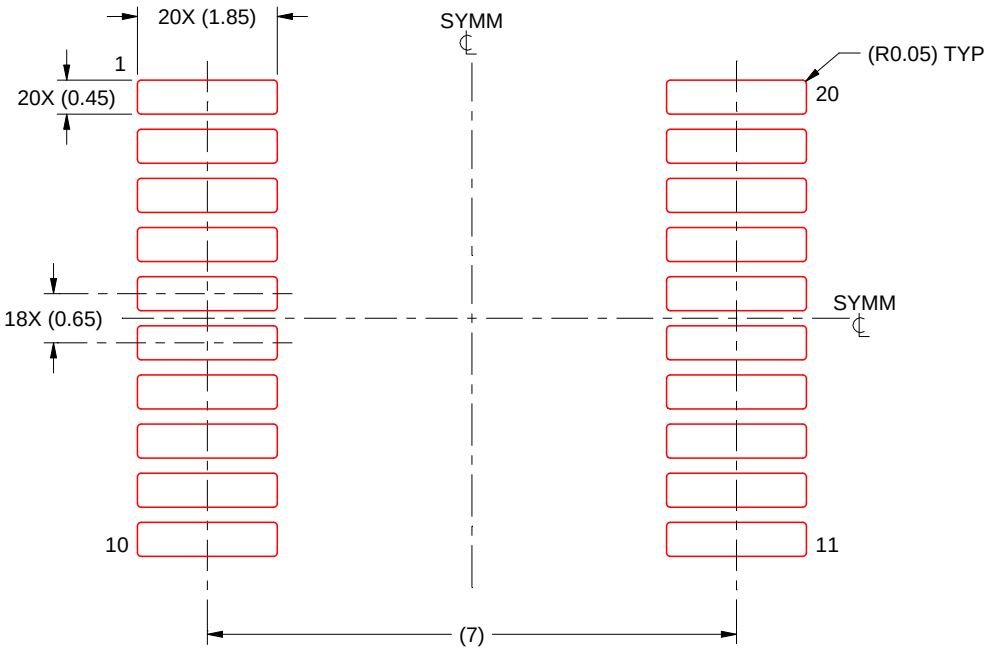
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

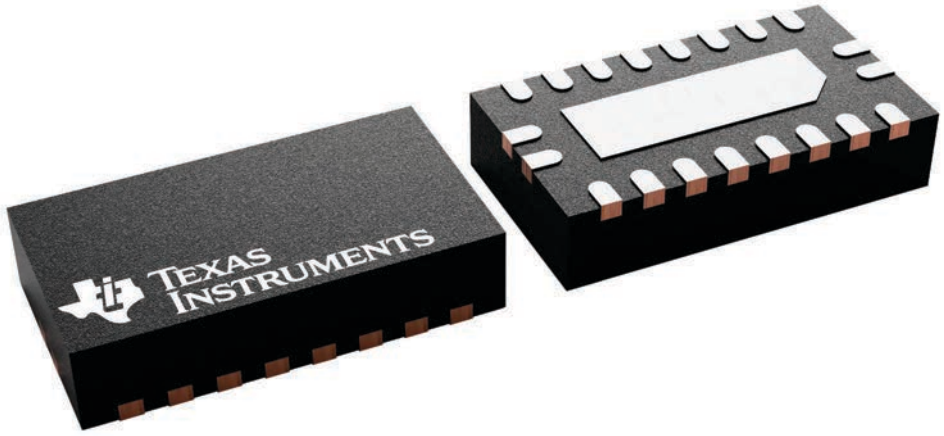
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

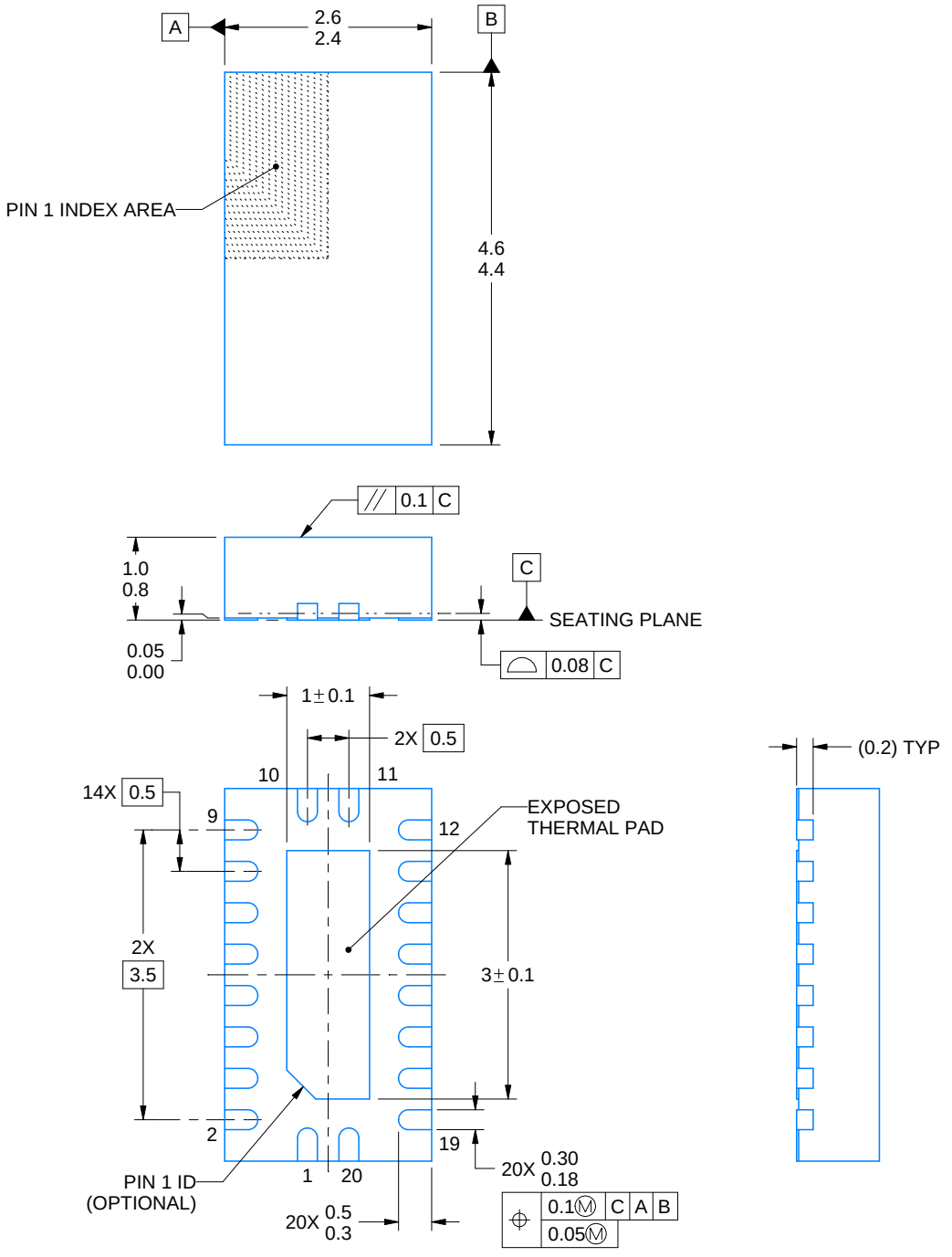


PACKAGE OUTLINE

RKS0020A

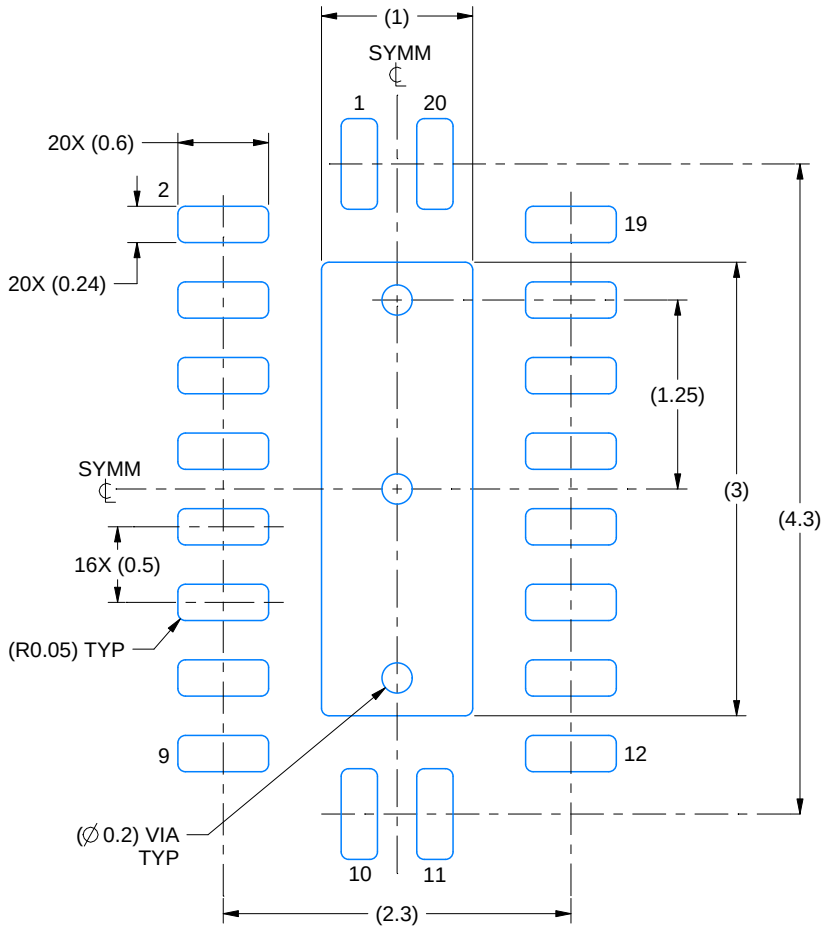
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

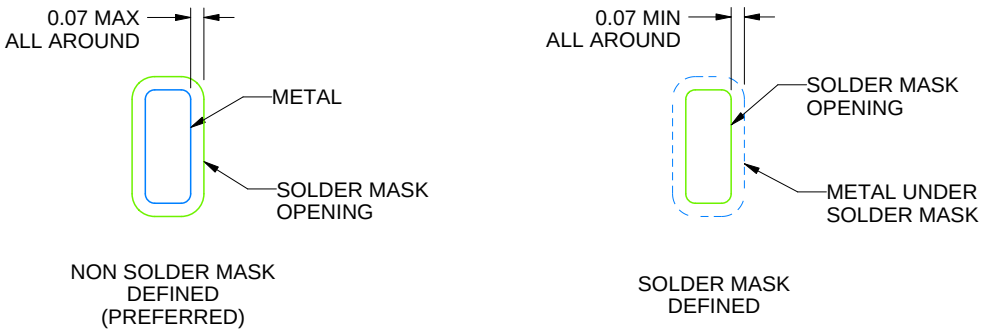


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

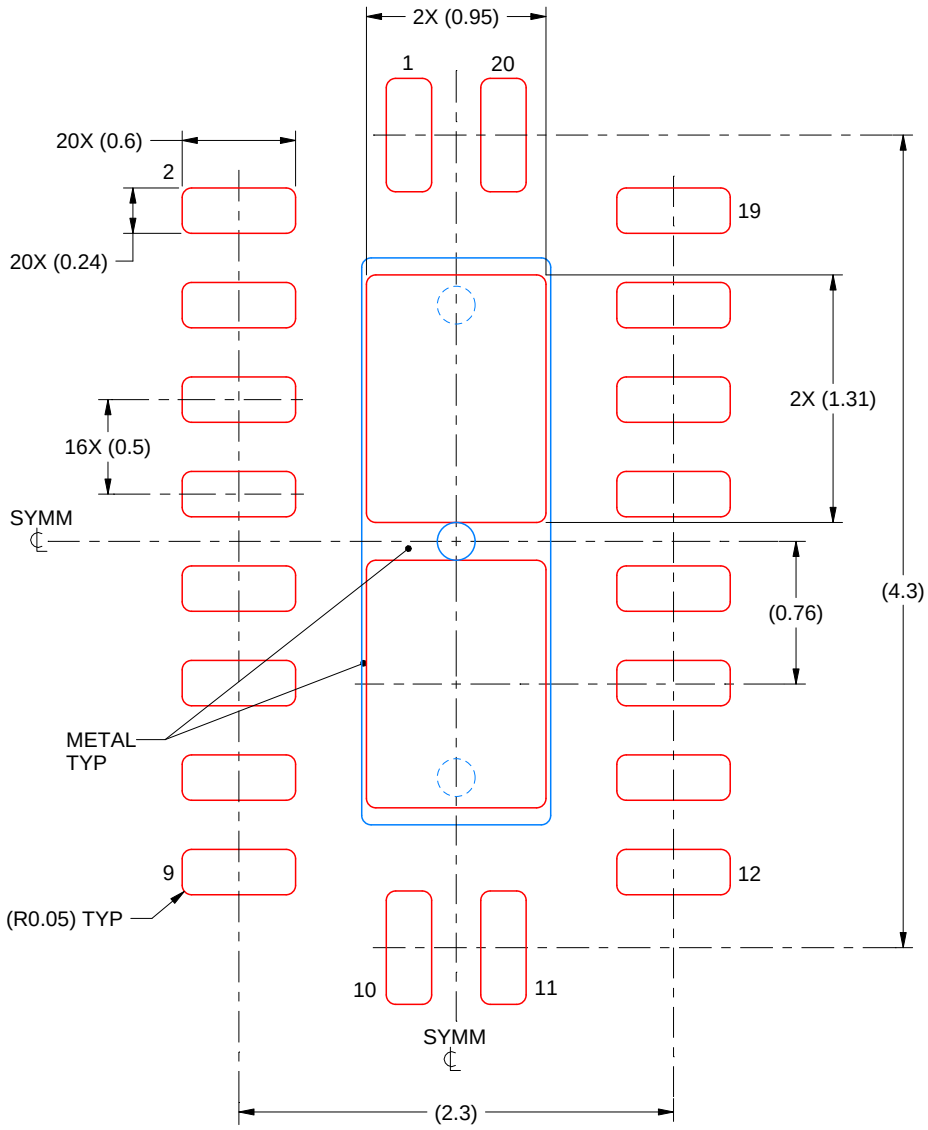


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

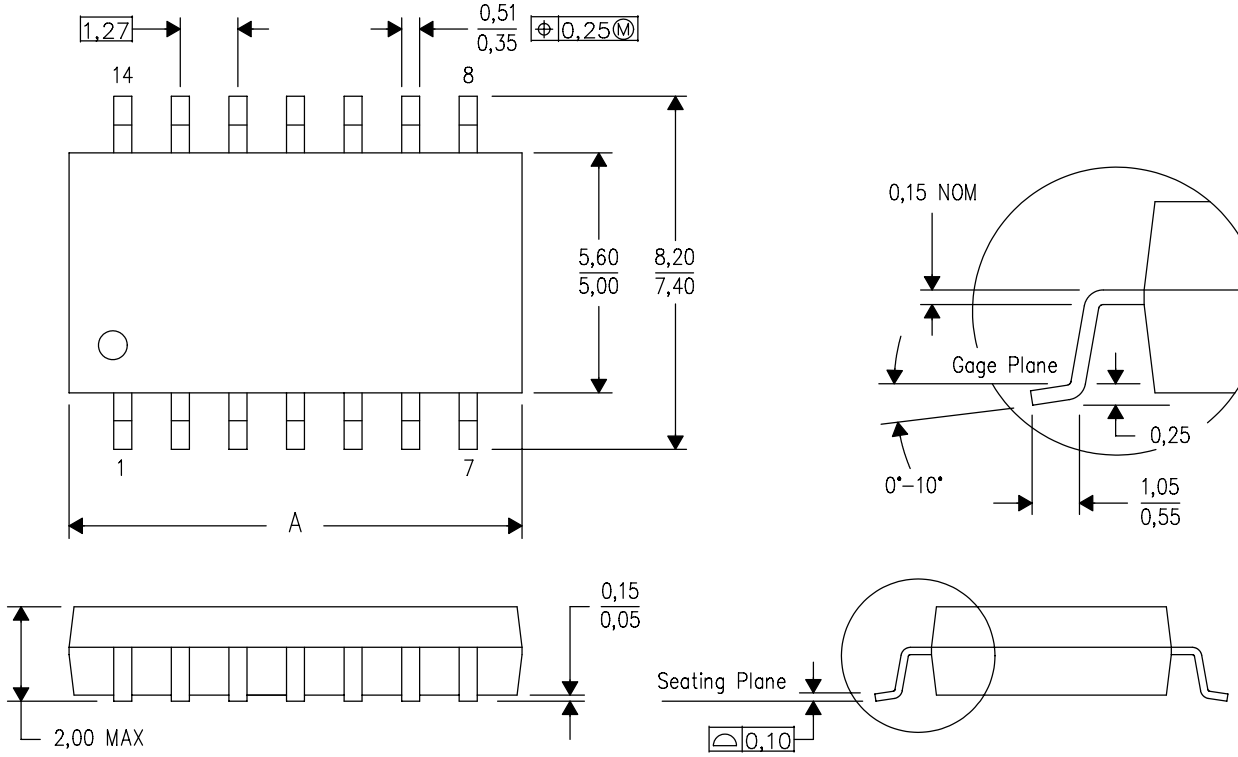
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

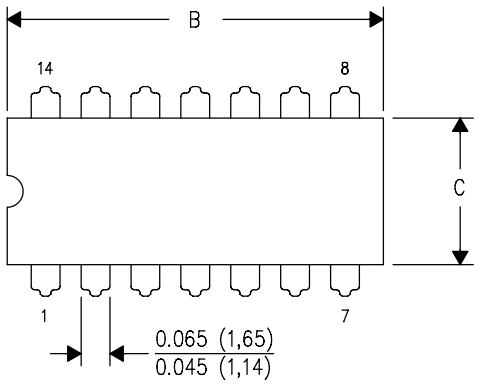
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

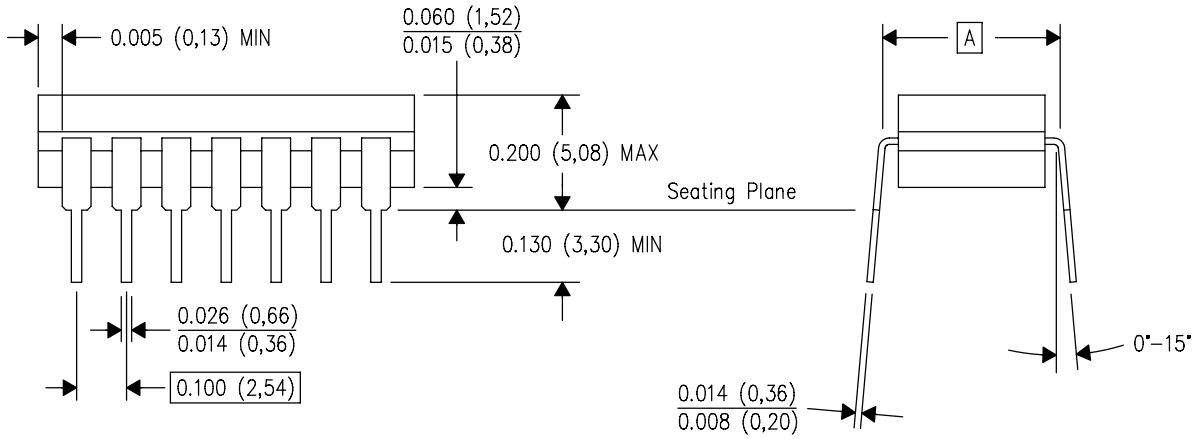
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

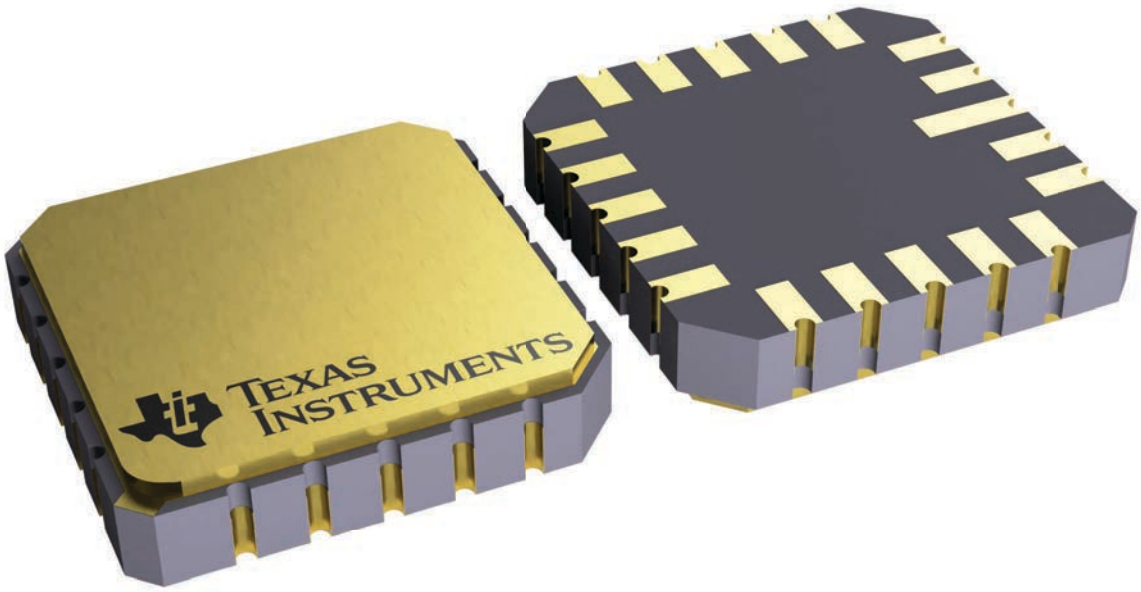
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

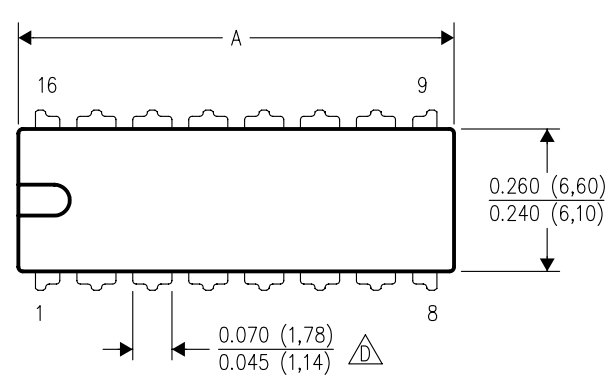


4229370VA\

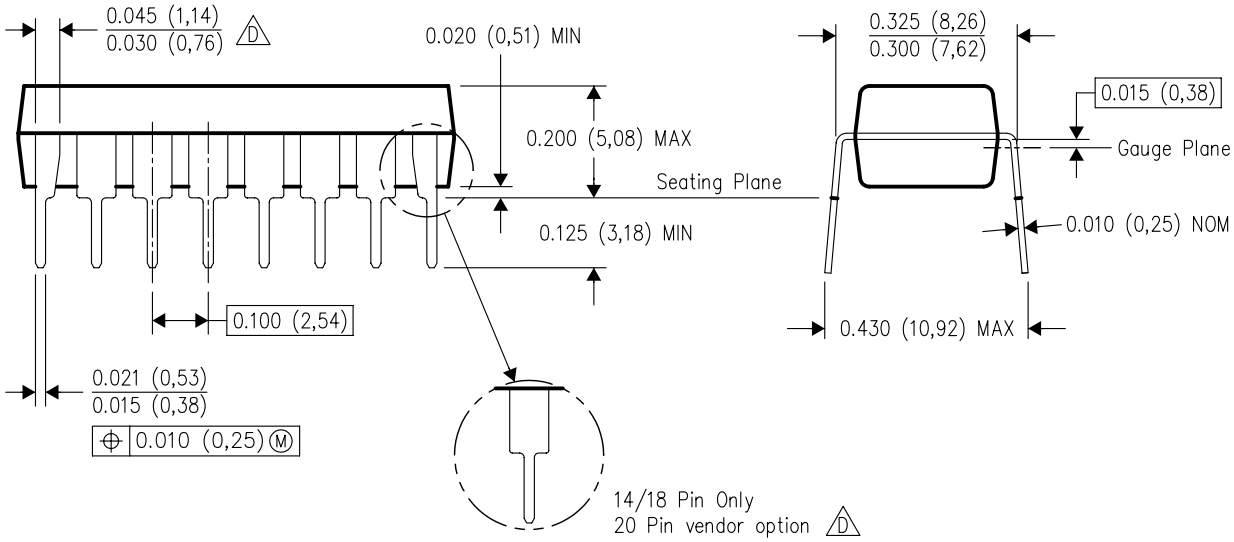
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

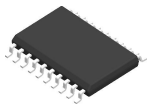


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

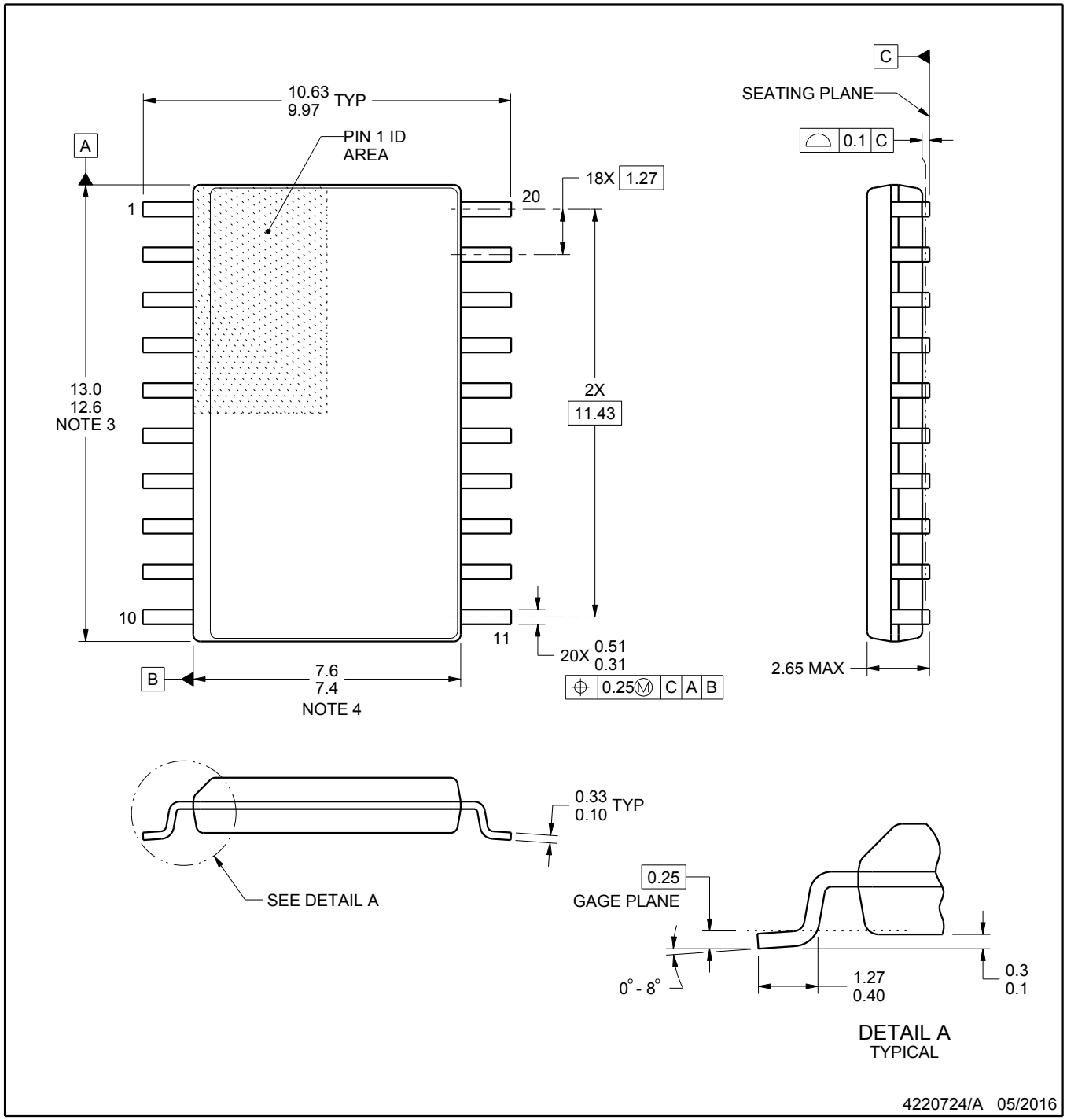


PACKAGE OUTLINE

DW0020A

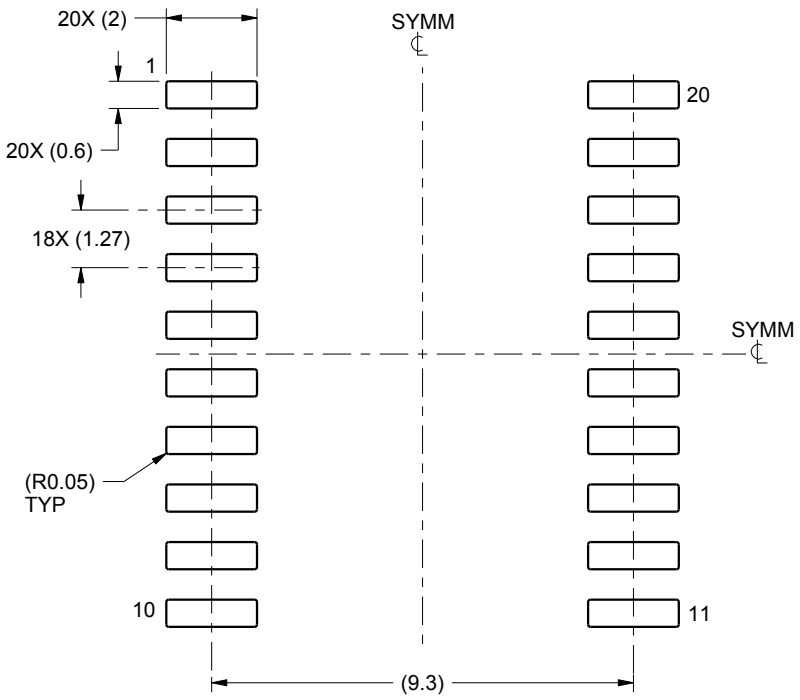
SOIC - 2.65 mm max height

SOIC

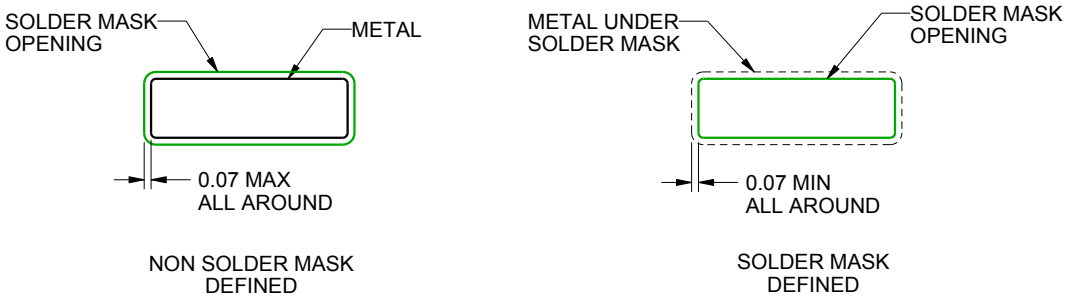


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

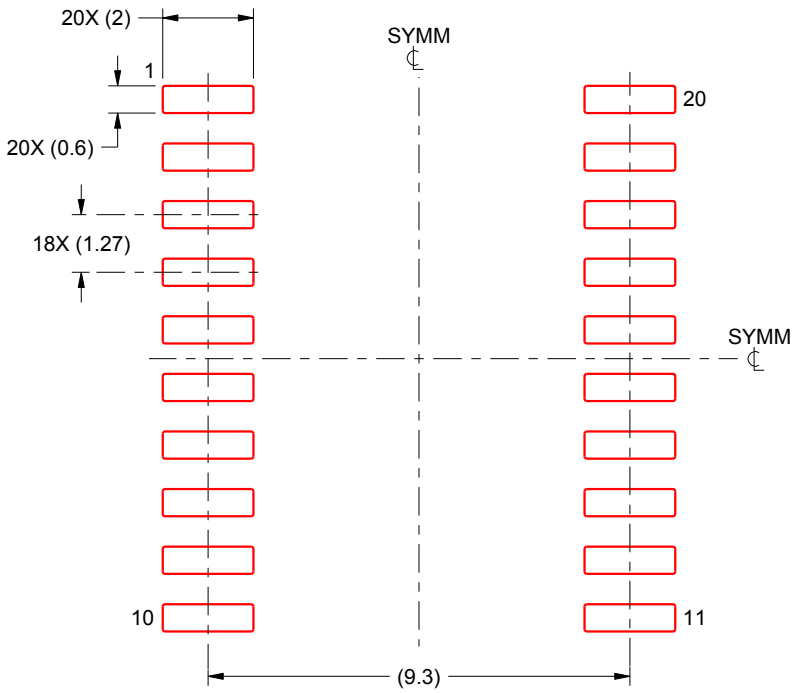


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



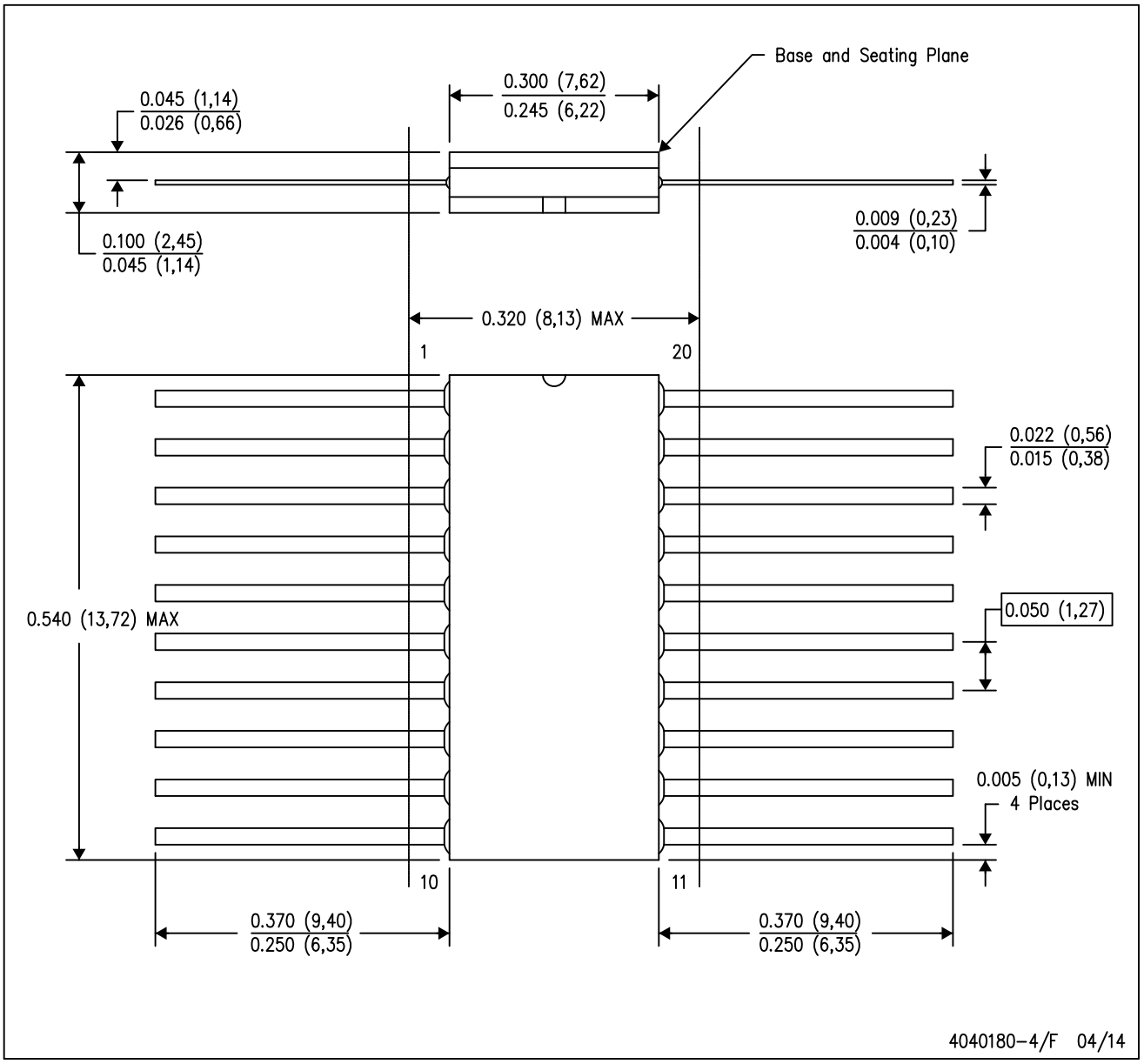
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



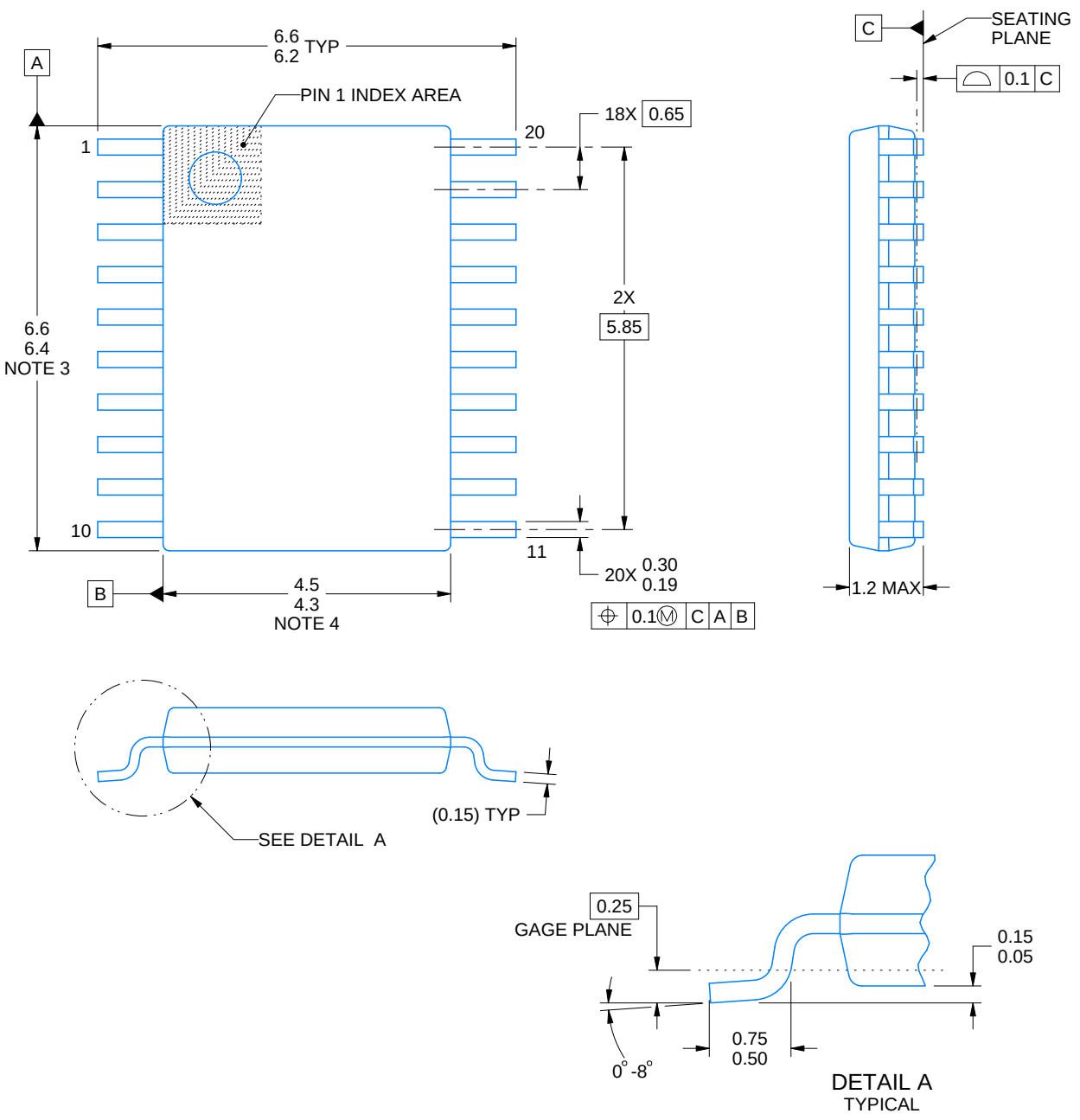
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

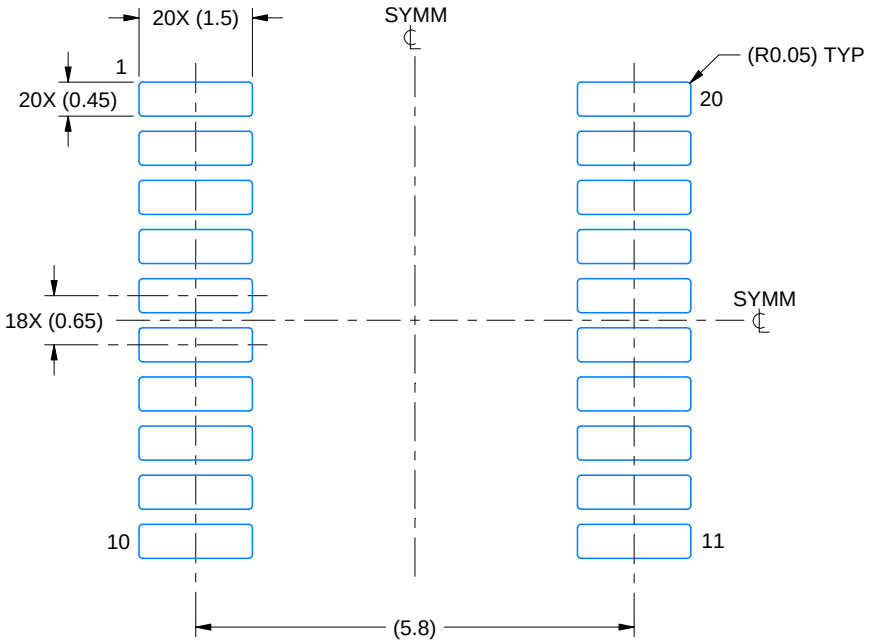
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



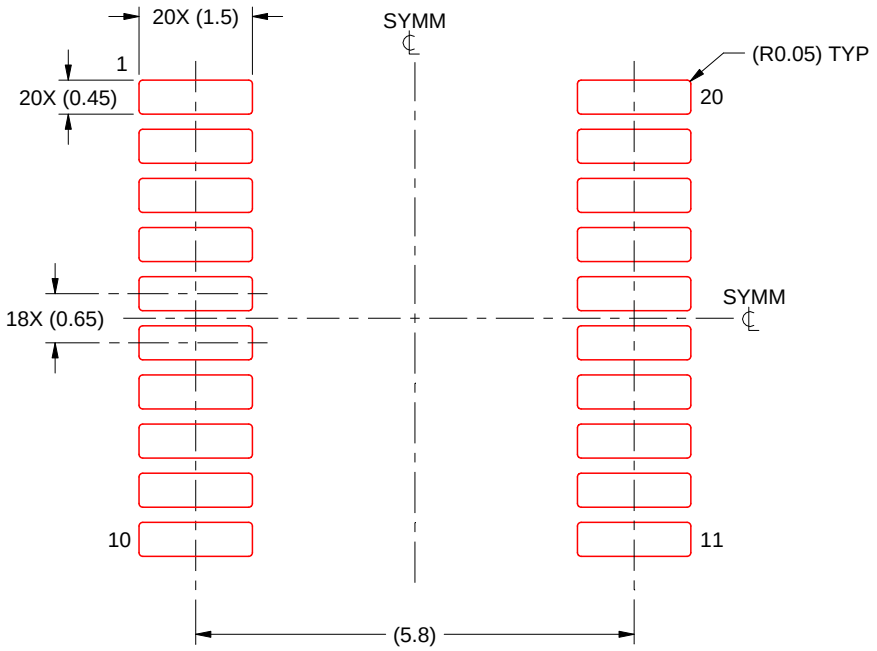
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

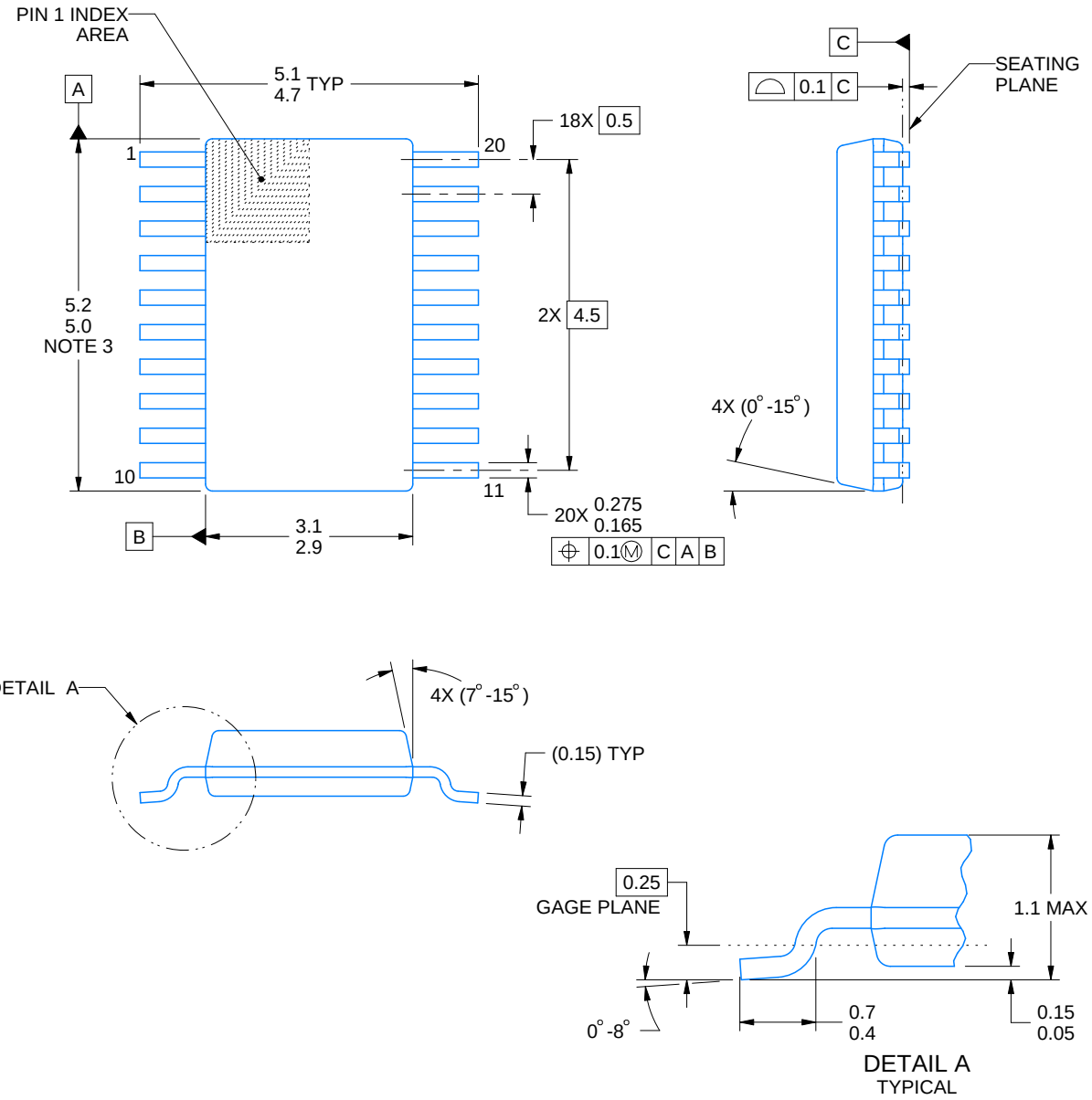
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

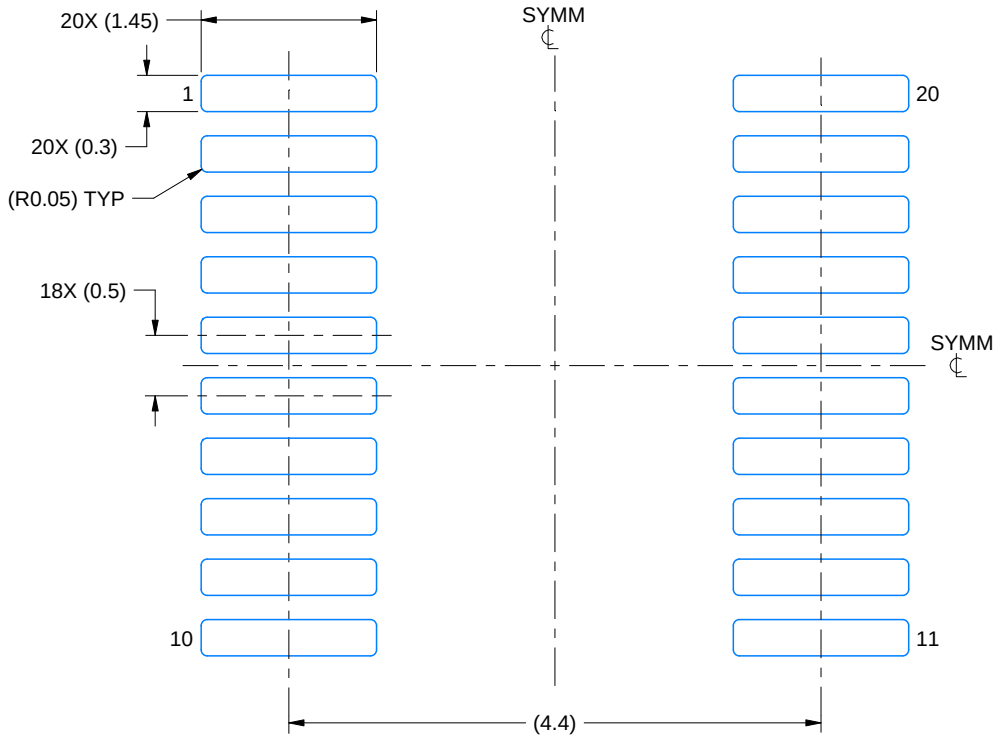
SMALL OUTLINE PACKAGE



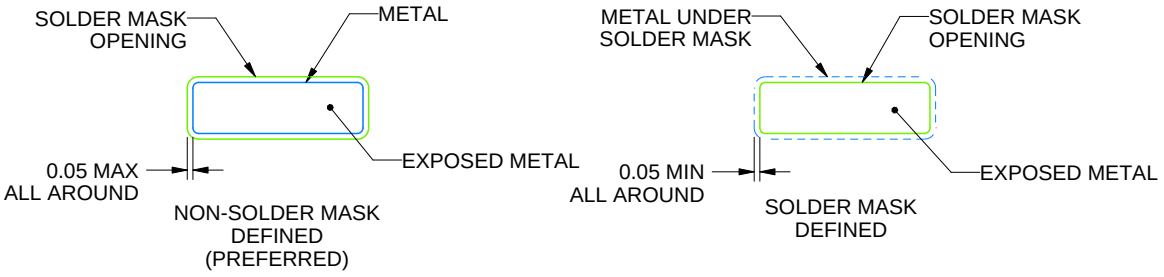
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

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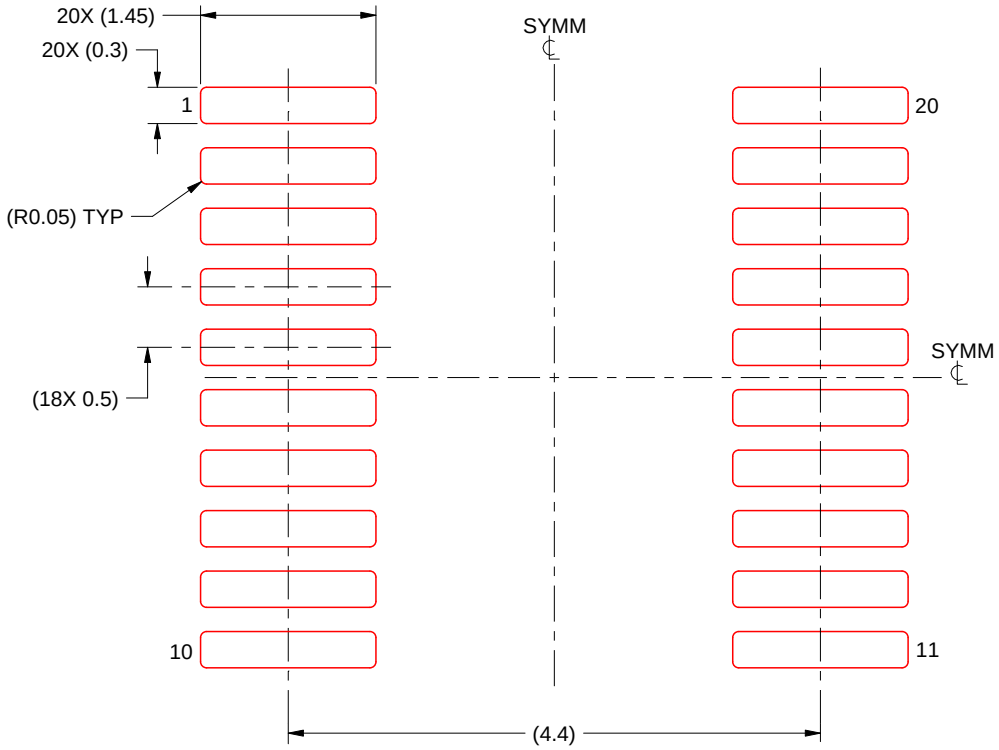
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月