

## SN74ACT10-Q1 汽车类三路 3 输入正与非门

### 1 特性

- 符合汽车应用要求
- 4.5V 至 5.5V  $V_{CC}$  运行
- 输入电压高达 5.5V
- $t_{pd}$  最大值为 9.5ns (5V 时)
- 输入兼容 TTL 电压

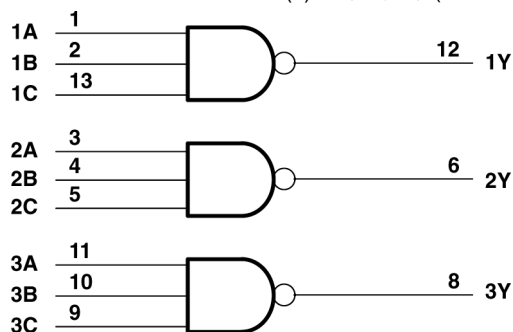
### 2 说明

SN74ACT10 器件包含三个独立 3 输入与非门。该器件以正逻辑执行布尔函数  $Y = A \cdot B \cdot C$  或  $Y = \overline{A + B + C}$ 。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SN74ACT10-Q1	PW ( TSSOP , 14 )	5mm x 6.4mm	5mm x 4.4mm

- 如需了解更多信息，请参阅[机械、封装和可订购信息](#)。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图，每个逻辑门 (正逻辑)



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	<b>7 Application and Implementation</b> .....	<b>8</b>
<b>2 说明</b> .....	<b>1</b>	7.1 Power Supply Recommendations.....	8
<b>3 Pin Configuration and Functions</b> .....	<b>3</b>	7.2 Layout.....	8
<b>4 Specifications</b> .....	<b>4</b>	<b>8 Device and Documentation Support</b> .....	<b>9</b>
4.1 Absolute Maximum Ratings.....	4	8.1 Documentation Support (Analog).....	9
4.2 Recommended Operating Conditions.....	4	8.2 接收文档更新通知.....	9
4.3 Thermal Information.....	4	8.3 支持资源.....	9
4.4 Electrical Characteristics.....	5	8.4 Trademarks.....	9
4.5 Switching Characteristics.....	5	8.5 静电放电警告.....	9
4.6 Operating Characteristics.....	5	8.6 术语表.....	9
<b>5 Parameter Measurement Information</b> .....	<b>6</b>	<b>9 Revision History</b> .....	<b>9</b>
<b>6 Detailed Description</b> .....	<b>7</b>	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	<b>9</b>
6.1 Functional Block Diagram.....	7		
6.2 Device Functional Modes.....	7		

### 3 Pin Configuration and Functions

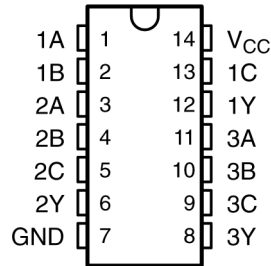


图 3-1. SN74ACT10-Q1 PW Package, 14-PIN TSSOP (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3C	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3A	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V <sub>CC</sub>	14	—	Positive Supply

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$ <sup>(2)</sup>	Input voltage range	-0.5	$V_{CC} + 0.5$	V
$V_O$ <sup>(2)</sup>	Output voltage range	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		$\pm 20$ mA
$I_{OK}$	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		$\pm 20$ mA
$I_O$	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		$\pm 50$ mA
	Continuous current through $V_{CC}$ or GND			$\pm 200$ mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8	ns/V
$T_A$	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74ACT10-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 125°C		T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	4.5V	4.4	4.49		4.4		4.4	V	
		5.5V	5.4	5.49		5.4		5.4		
	I <sub>OH</sub> = -24mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I <sub>OH</sub> = -50mA <sup>(1)</sup>	5.5V				3.85				
I <sub>OH</sub> = -75mA <sup>(1)</sup>	5.5V						3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	4.5V		0.001	0.1		0.1		0.1	
		5.5V		0.001	0.1		0.1		0.1	
	I <sub>OL</sub> = 24mA	4.5V			0.36		0.5		0.44	
		5.5V			0.36		0.5		0.44	
	I <sub>OL</sub> = 50mA <sup>(1)</sup>	5.5V					1.65			
I <sub>OL</sub> = 75mA <sup>(1)</sup>	5.5V							1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5V			±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5V			4		80		40	μA
ΔI <sup>(2)</sup> CC	One input at 3.4V, Other inputs at GND or V <sub>CC</sub>	5.5V		0.6			1.6		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		2.6						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 4.5 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5V ± 0.5V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

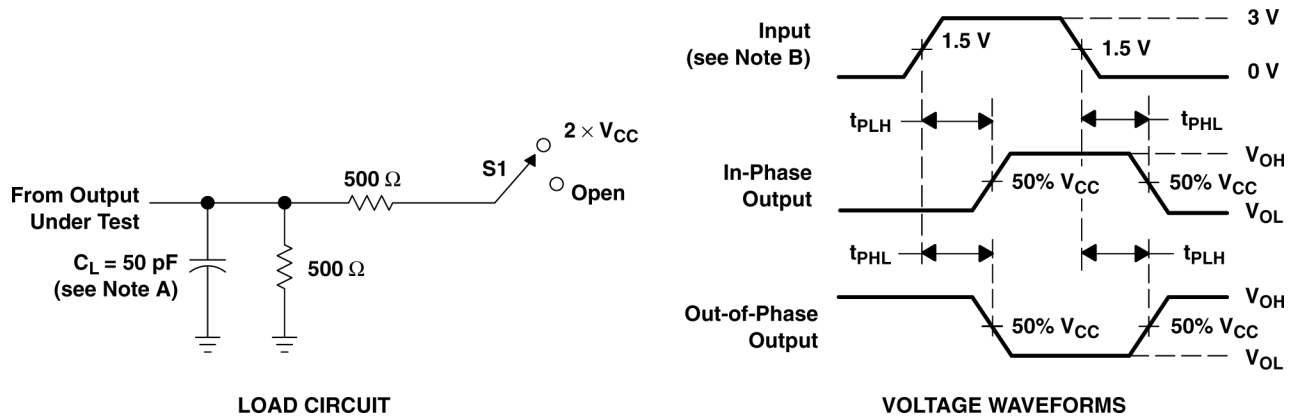
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 125°C		T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Any	Y	1	6.5	9	1	10	1	10	ns
t <sub>PHL</sub>			1	6.5	9	1	9.5	1	9.5	

## 4.6 Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50pF, f = 1 MHz	25	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. The outputs are measured one at a time, with one input transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open

## 6 Detailed Description

### 6.1 Functional Block Diagram

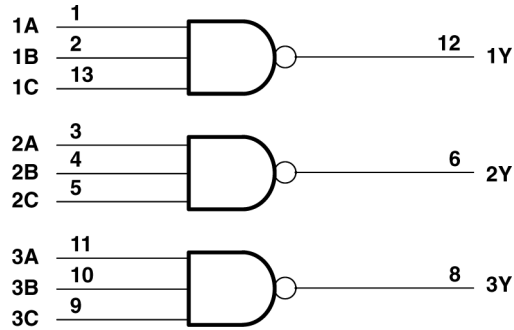


图 6-1. Logic Diagram, Each Gate (Positive Logic)

### 6.2 Device Functional Modes

表 6-1. Function Table (Each Gate)

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

## 7 Application and Implementation

---

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

---

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [节 4.2](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74ACT10-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

#### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (January 2008) to Revision B (July 2024)	Page
• 添加了封装信息表、引脚功能表、热性能信息表、器件功能模式、“应用和实施”部分、器件和文档支持部分以及机械、封装和订购信息部分.....	1
• Updated R <sup>θ</sup> JA values: PW = 113 to 145.7, all values in °C/W.....	4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT10QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT10Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ACT10-Q1 :**

- Catalog : [SN74ACT10](#)
- Military : [SN54ACT10](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024，德州仪器 (TI) 公司