

## SN65MLVD047A 多点 LVDS 四路差分线路驱动器

### 1 特性

- 差分线路驱动器支持  $30\ \Omega$  至  $55\ \Omega$  负载和高达 200Mbps 的数据速率，<sup>1</sup> 时钟频率高达 100MHz
- 支持多点总线架构
- 由 3.3V 单电源供电运行
- 额定运行温度范围为  $-40^{\circ}\text{C}$  至  $85^{\circ}\text{C}$
- 16 引脚 SOIC (JEDEC MS-012) 和 16 引脚 TSSOP (JEDEC MS-153) 封装

### 2 应用

- AdvancedTCA™ (ATCA™) 时钟总线驱动器
- 时钟分配
- 电信、汽车、工业以及其他计算机系统背板或有线多点数据传输
- 蜂窝基站
- 中心局交换和 PBX 交换
- 桥接器和路由器
- 符合 TIA/EIA-485 标准的低功耗、高速短距离替代方案

### 3 说明

SN65MLVD047A 是一款四路线路驱动器，符合 TIA/EIA-899 标准中的多点低电压差分信号 (M-LVDS) 电气特性。与符合 LVDS 标准的器件相比，此 M-LVDS 器件的输出电流有所增加，以便支持双端接传输线和重负载的背板总线应用。背板应用通常需要在总线两端使用阻抗匹配的端接电阻器。由于总线端接以及总线接口器件的容性负载，双端接总线的有效阻抗可低至  $30\ \Omega$ 。SN65MLVD047A 驱动器支持在低至  $30\ \Omega$  的负载下运行。SN65MLVD047A 器件允许在一条总线上存在多个驱动器。SN65MLVD047A 驱动器在禁用或未上电时保持高阻抗。驱动器融合了边沿速率控制功能以支持运行。当从主传输线到接口器件预期有多个总线存根时，M-LVDS 标准允许多达 32 个节点（驱动器和/或接收器）连接到背板中的同一介质。SN65MLVD047A 在所有总线引脚上提供 9kV ESD 保护。

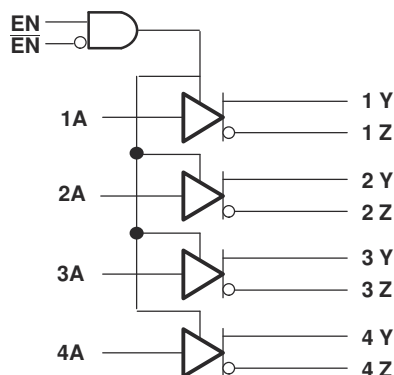
#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
SN65MLVD047A	PW ( TSSOP , 16 )	5mm × 6.4mm
	D ( SOIC , 16 )	9.9mm × 6mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

### LOGIC DIAGRAM (POSITIVE LOGIC)



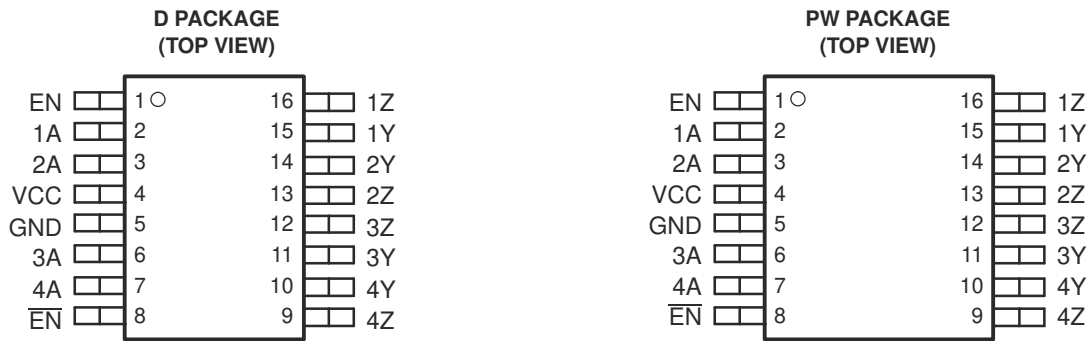
<sup>1</sup> 线路的数据速率是指每秒钟的电压转换次数，单位为 bps (比特每秒)。



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	<b>6 Parameter Measurement Information</b> .....	<b>10</b>
<b>2 应用</b> .....	<b>1</b>	<b>7 Device Functional Modes</b> .....	<b>13</b>
<b>3 说明</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>14</b>
<b>4 Pin Configuration</b> .....	<b>3</b>	8.1 Application Information.....	14
<b>5 Specifications</b> .....	<b>4</b>	<b>9 Device and Documentation Support</b> .....	<b>16</b>
5.1 Absolute Maximum Ratings.....	4	9.1 接收文档更新通知.....	16
5.2 ESD Ratings.....	4	9.2 支持资源.....	16
5.3 Recommended Operating Conditions.....	4	9.3 Trademarks.....	16
5.4 Package Dissipation Ratings.....	4	9.4 静电放电警告.....	16
5.5 Thermal Information.....	5	9.5 术语表.....	16
5.6 Device Electrical Characteristics.....	5	<b>10 Revision History</b> .....	<b>16</b>
5.7 Device Electrical Characteristics.....	6	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>
5.8 Switching Characteristics.....	7		
5.9 Typical Characteristics.....	8		

## 4 Pin Configuration



## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

			MIN	MAX	UNITS
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>		- 0.5	4	V
V <sub>I</sub>	Input voltage range	A, EN, EN̄	- 0.5	4	V
V <sub>O</sub>	Output voltage range	Y, Z	- 1.8	4	V
T <sub>J</sub>	Junction temperature			140	°C
P <sub>D</sub>	Device power dissipation	EN = V <sub>CC</sub> , EN̄ = GND, R <sub>L</sub> = 50Ω, Input 100MHz 50 % duty cycle square wave to 1A:4A, T <sub>A</sub> = 85°C		288.5	mW
T <sub>stg</sub>	Storage Temperature		- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to the circuit ground terminal.

### 5.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Y and Z	±9000	V
			All pins	±4000	
		Charged device model (CDM), per AEC Q100-011 <sup>(2)</sup>	All pins	±1500	
			Machine Model	All pins	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

see 图 6-1

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
V <sub>IH</sub>	High-level input voltage	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	0		0.8	V
	Voltage at any bus terminal (separate or common mode) V <sub>Y</sub> or V <sub>Z</sub>	- 1.4		3.8	V
R <sub>L</sub>	Differential load resistance	30		55	Ω
1/t <sub>UI</sub>	Signaling rate			200	Mbps
	Clock frequency			100	MHz
T <sub>J</sub>	Junction temperature	- 40		125	°C

### 5.4 Package Dissipation Ratings

PACKAGE	PCB JEDEC STANDARD	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C <sup>(1)</sup>	T <sub>A</sub> = 85°C POWER RATING
D(16)	Low-K <sup>(2)</sup>	898mW	7.81mW/°C	429mW
PW(16)	Low-K <sup>(2)</sup>	592mW	5.15mW/°C	283mw
	High-K <sup>(3)</sup>	945mW	8.22mW/°C	452mw

- (1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
- (2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
- (3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## 5.5 Thermal Information

PARAMETER		TEST CONDITIONS		VALUE	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance	Low-K board <sup>(1)</sup> , no airflow	D	128	°C/W
		Low-K board <sup>(1)</sup> , no airflow	PW	194.2	
		Low-K board <sup>(1)</sup> , 150 LFM		146.8	
		Low-K board <sup>(1)</sup> , 250 LFM		133.1	
		High-K board <sup>(2)</sup> , no airflow		121.6	
$\theta_{JB}$	Junction-to-board thermal resistance	High-K board <sup>(2)</sup>	D	51.1	°C/W
			PW	85.3	
$\theta_{JC}$	Junction-to-case thermal resistance		D	45.4	°C/W
			PW	34.7	

- (1) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.  
(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## 5.6 Device Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_{CC}$	Supply current	Driver enabled	EN = $V_{CC}$ , $\overline{EN}$ = GND, $R_L$ = 50 $\Omega$ , All inputs = $V_{CC}$ or GND		59	70	mA
		Driver disabled	EN = GND, $\overline{EN}$ = $V_{CC}$ , $R_L$ = No load, All inputs = $V_{CC}$ or GND		2	4	

- (1) All typical values are at 25°C and with a 3.3V supply voltage.

## 5.7 Device Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX	UNIT
<b>LVTTL (EN, EN, 1A:4A)</b>						
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = 2 V or V <sub>CC</sub>	0		10	μ A
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = GND or 0.8 V	0		10	μ A
C <sub>i</sub>	Input capacitance	V <sub>i</sub> = 0.4 sin(30E6 π t) + 0.5 V <sup>(3)</sup>		5		pF
<b>M-LVDS (1Y/1Z:4Y/4Z)</b>						
V <sub>YZ</sub>	Differential output voltage magnitude		480		650	mV
Δ V <sub>YZ</sub>	Change in differential output voltage magnitude between logic states	See 图 6-2	- 50		50	mV
V <sub>OS(SS)</sub>	Steady-state common-mode output voltage		0.8		1.2	V
ΔV <sub>OS(SS)</sub>	Change in steady-state common-mode output voltage between logic states	See 图 6-3	- 50		50	mV
V <sub>OS(PP)</sub>	Peak-to-peak common-mode output voltage				150	mV
V <sub>Y(OC)</sub>	Maximum steady-state open-circuit output voltage		0		2.4	V
V <sub>Z(OC)</sub>	Maximum steady-state open-circuit output voltage	See 图 6-7	0		2.4	V
V <sub>P(H)</sub>	Voltage overshoot, low-to-high level output	See 图 6-5			1.2 V <sub>SS</sub>	V
V <sub>P(L)</sub>	Voltage overshoot, high-to-low level output		- 0.2 V <sub>SS</sub>			V
I <sub>OS</sub>	Differential short-circuit output current magnitude	See 图 6-4			24	mA
I <sub>OZ</sub>	High-impedance state output current	- 1.4 V ≤ (V <sub>Y</sub> or V <sub>Z</sub> ) ≤ 3.8 V, Other output = 1.2 V	- 15		10	μ A
I <sub>O(OFF)</sub>	Power-off output current	- 1.4 V ≤ (V <sub>Y</sub> or V <sub>Z</sub> ) ≤ 3.8 V, Other output = 1.2 V, V <sub>CC</sub> = 0 V	- 10		10	μ A
C <sub>Y</sub> or C <sub>Z</sub>	Output capacitance	V <sub>Y</sub> or V <sub>Z</sub> = 0.4 sin(30E6 π t) + 0.5 V, <sup>(3)</sup> Other input at 1.2 V, driver disabled		3		pF
C <sub>YZ</sub>	Differential output capacitance	V <sub>YZ</sub> = 0.4 sin(30E6 π t) V, <sup>(3)</sup> Driver disabled			2.5	pF
C <sub>Y/Z</sub>	Output capacitance balance, (C <sub>Y</sub> /C <sub>Z</sub> )		0.99	1.01		

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

## 5.8 Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	See 图 6-5	1	1.5	2.4	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
$t_r$	Differential output signal rise time		1		1.9	ns
$t_f$	Differential output signal fall time		1		1.9	ns
$t_{sk(o)}$	Output skew <sup>(2)</sup>				100	ps
$t_{sk(p)}$	Pulse skew ( $ t_{pHL} - t_{pLH} $ )			22	100	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(3)</sup>				600	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(4)</sup>	All inputs 100 MHz clock input		0.2	1	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter <sup>(4)</sup>	All inputs 100 MHz clock input		5	36	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(4) (5)</sup>	All inputs 200 Mbps 2 <sup>15</sup> -1 PRBS input		46	158	ps
$t_{PZH}$	Enable time, high-impedance-to-high-level output	See 图 6-6			9	ns
$t_{PZL}$	Enable time, high-impedance-to-low-level output				9	ns
$t_{PHZ}$	Disable time, high-level-to-high-impedance output	See 图 6-6			10	ns
$t_{PLZ}$	Disable time, low-level-to-high-impedance output				10	ns

- (1) All typical values are at 25°C and with a 3.3V supply voltage.
- (2)  $t_{sk(o)}$ , output skew is the magnitude of the time difference in propagation delay times between any specified terminals of a device.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (4) Stimulus jitter has been subtracted from the measurements.
- (5) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

### 5.9 Typical Characteristics

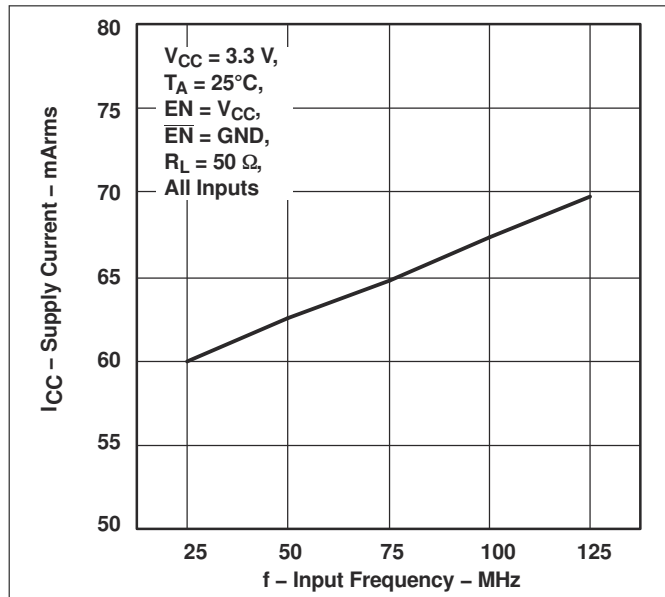


图 5-1. RMS Supply Current vs Input Frequency

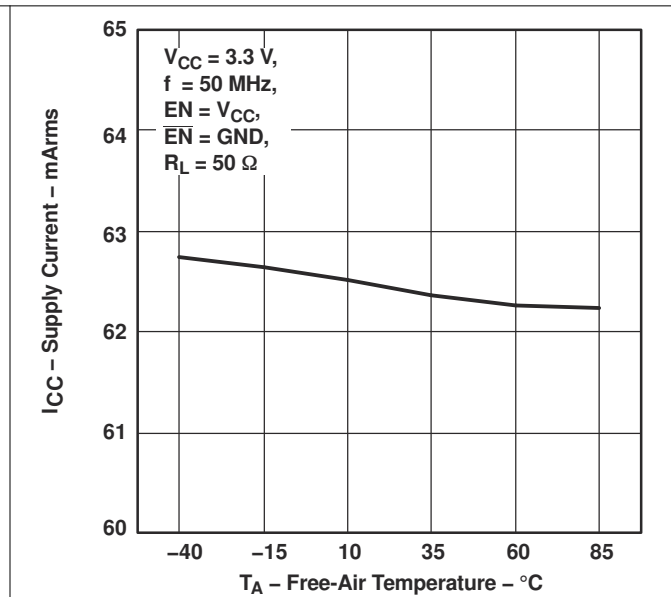


图 5-2. RMS Supply Current vs Free-Air Temperature

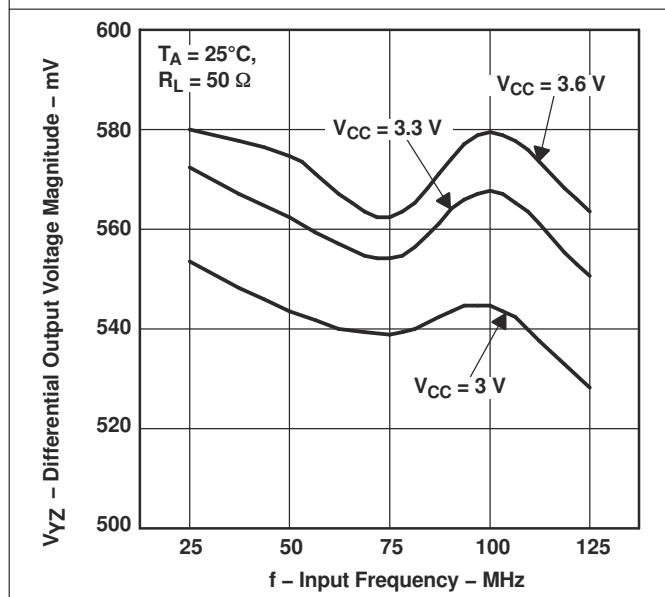


图 5-3. Differential Output Voltage Magnitude vs Input Frequency

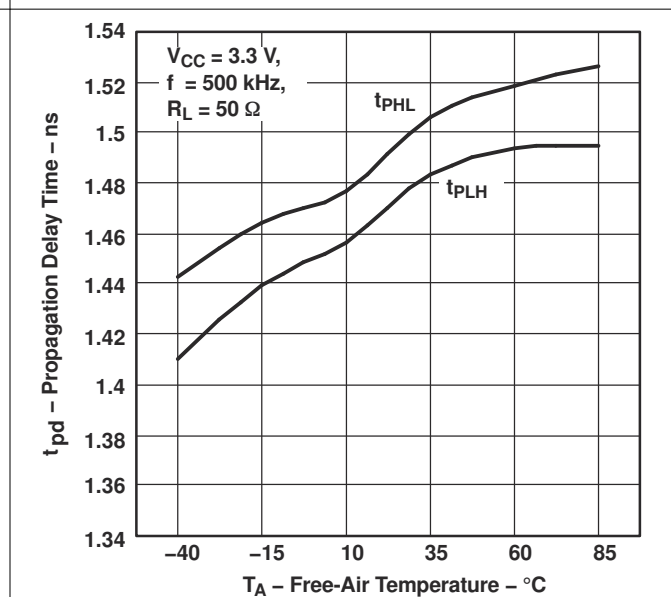


图 5-4. Driver Propagation Delay Time vs Free-Air Temperature



### 5.9 Typical Characteristics (continued)

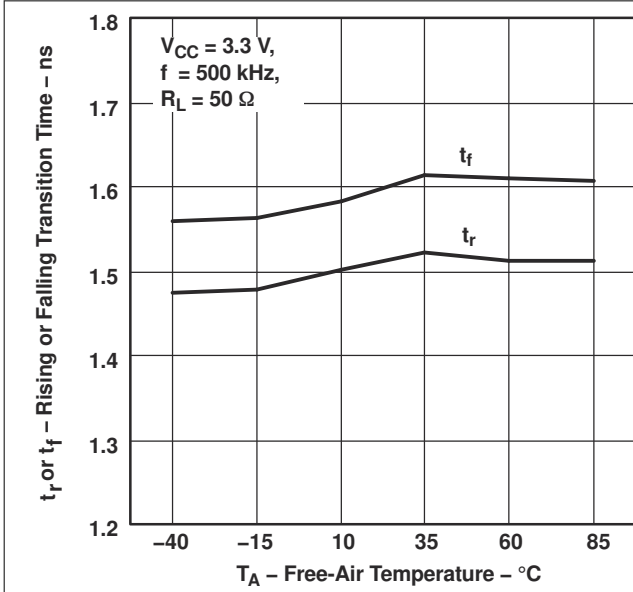


图 5-5. Driver Transition Time vs Free-Air Temperature

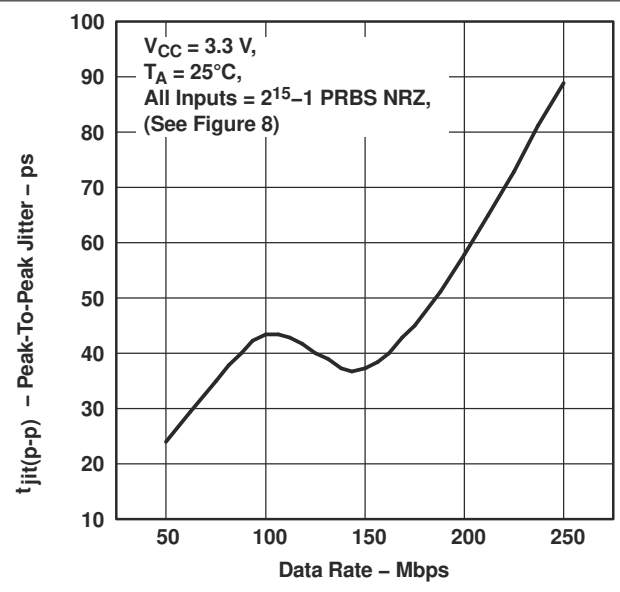


图 5-6. Peak-to-Peak Jitter vs Data Rate

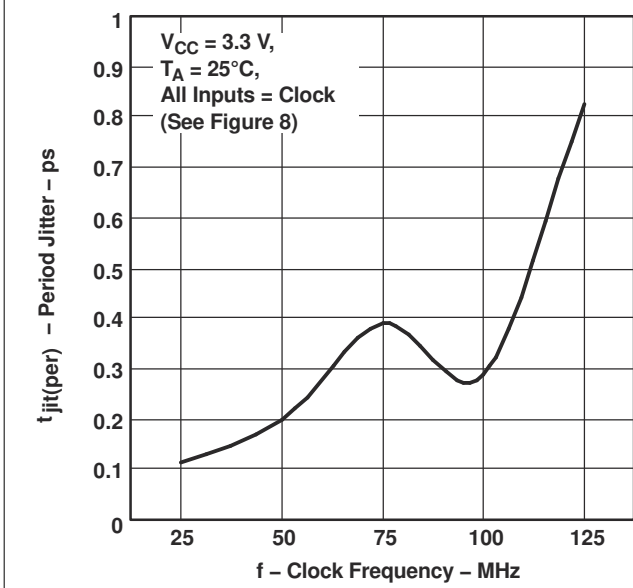


图 5-7. Period Jitter vs Clock Frequency

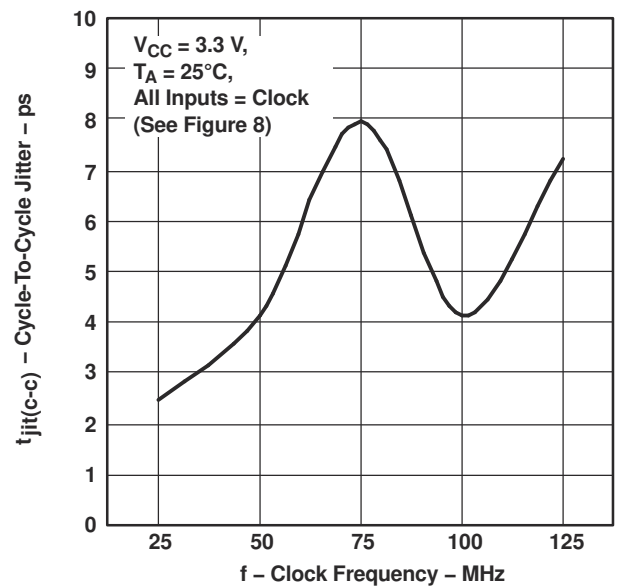


图 5-8. Cycle-to-Cycle Jitter vs Clock Frequency

## 6 Parameter Measurement Information

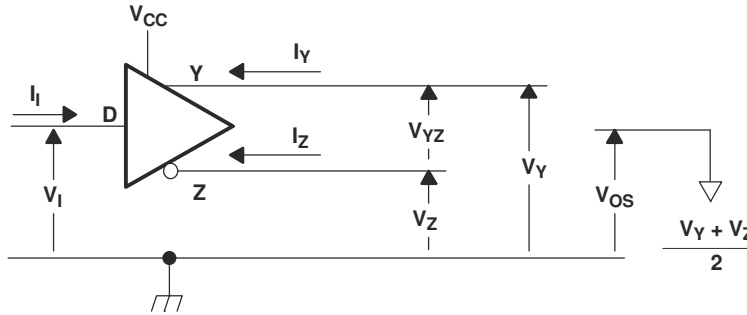
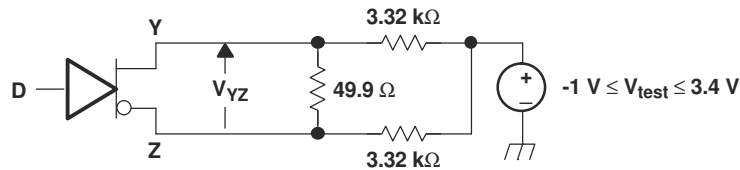
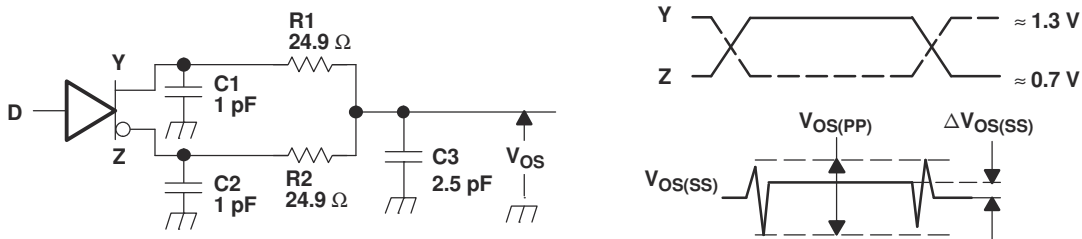


图 6-1. Driver Voltage and Current Definitions



All resistors are 1% tolerance.

图 6-2. Differential Output Voltage Test Circuit



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse frequency = 500kHz, duty cycle =  $50 \pm 5\%$ .
- C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- R1 and R2 are metal film, surface mount,  $\pm 1\%$ , and located within 2 cm of the D.U.T.
- The measurement of  $V_{OS(PP)}$  is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

图 6-3. Test Circuit and Definitions for the Common-Mode Output Voltage

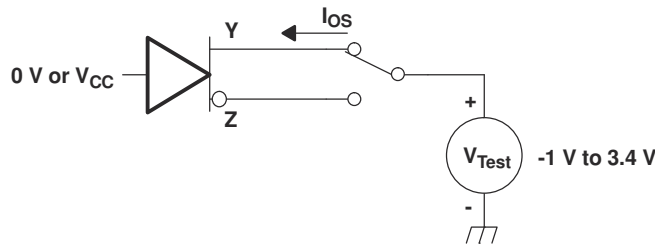
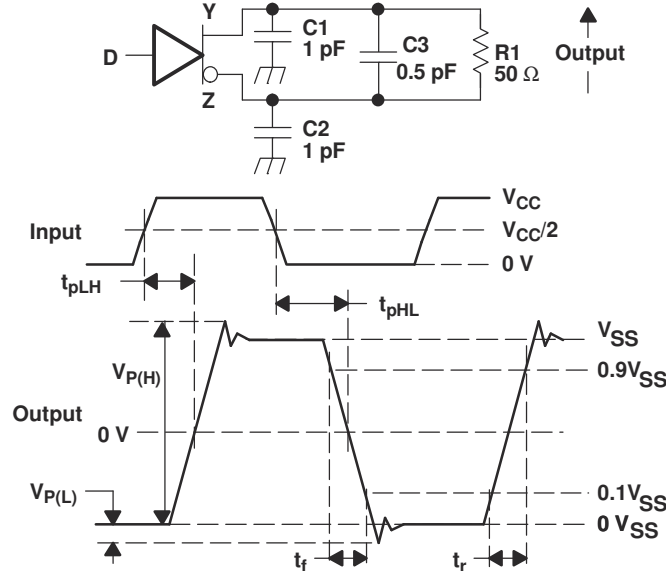
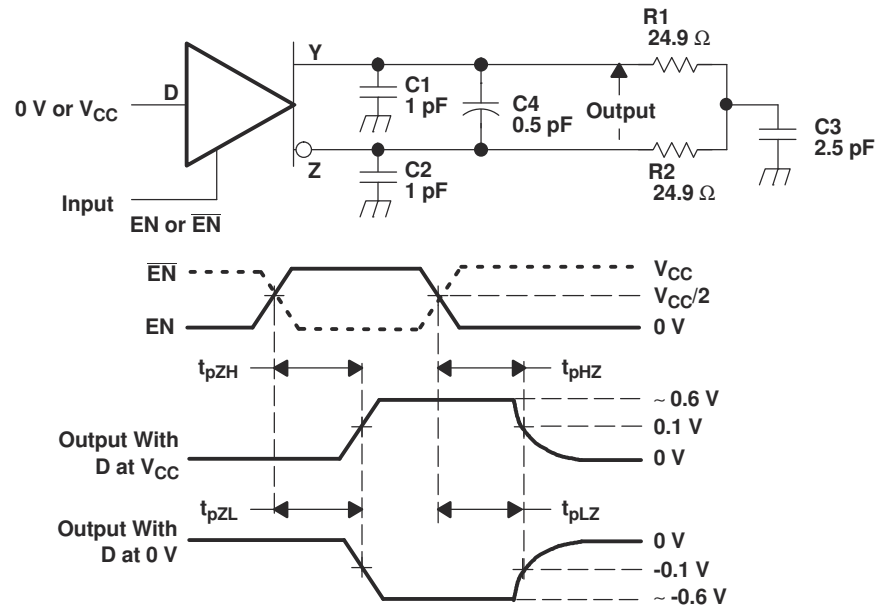


图 6-4. Short-Circuit Test Circuit



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500kHz, duty cycle = 50 ± 5%.
- C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
- R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a -3dB bandwidth of at least 1 GHz.

图 6-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500kHz, duty cycle = 50 ± 5%.
- C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
- R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a -3dB bandwidth of at least 1GHz.

图 6-6. Driver Enable and Disable Time Circuit and Definitions

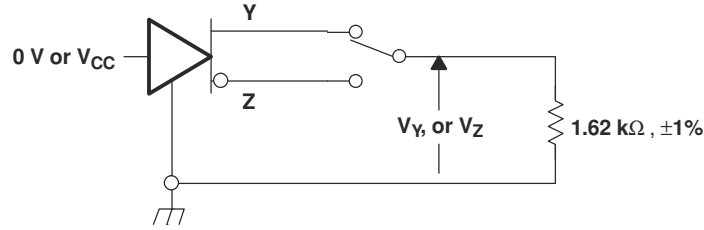
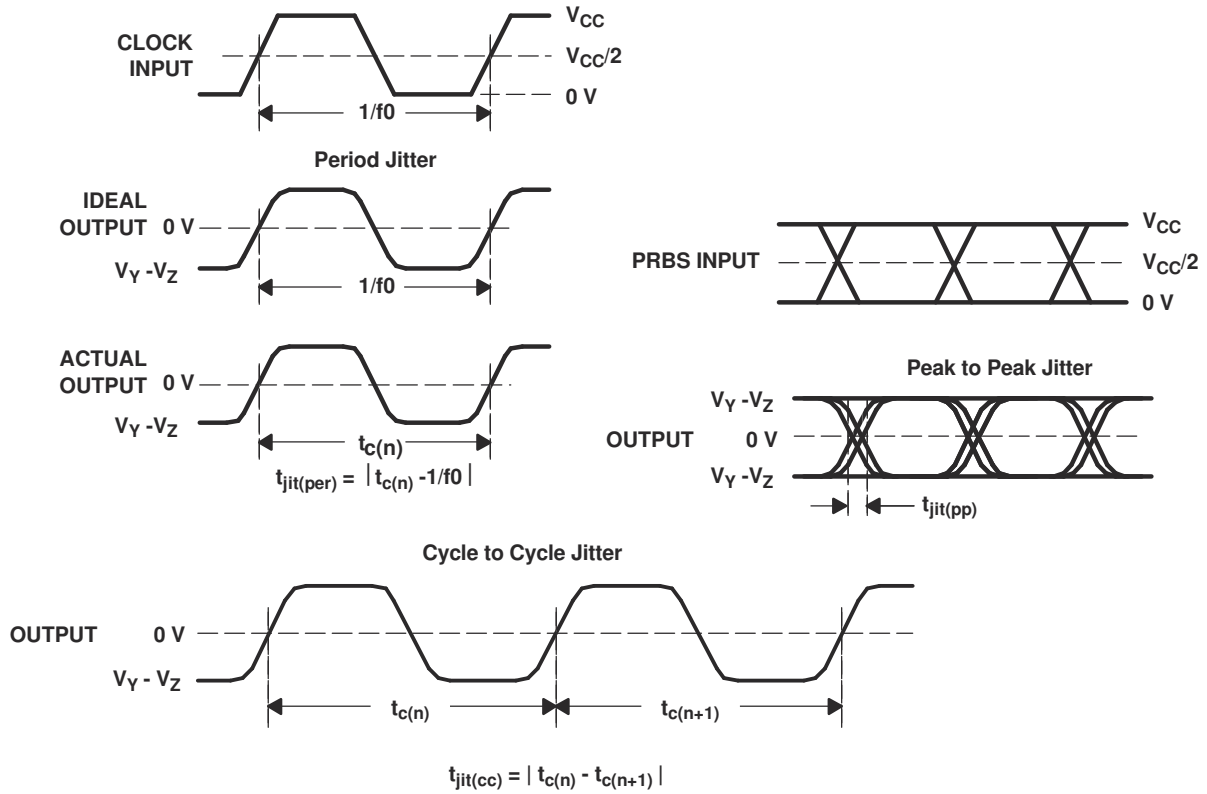


图 6-7. Driver Maximum Steady State Output Voltage



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter and cycle-to-cycle jitter are measured using a 100MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200Mbps 2<sup>15</sup> - 1PRBS input.

图 6-8. Driver Jitter Measurement Waveforms

## 7 Device Functional Modes

表 7-1. Device Function Table

INPUTS <sup>(1)</sup>			OUTPUTS <sup>(1)</sup>	
D	EN	EN	Y	Z
L	H	L	L	H
H	H	L	H	L
OPEN	H	L	L	H
X	L or OPEN	X	Z	Z
X	X	H or OPEN	Z	Z

(1) H = high level, L = low level, Z = high impedance, X = Don't Care

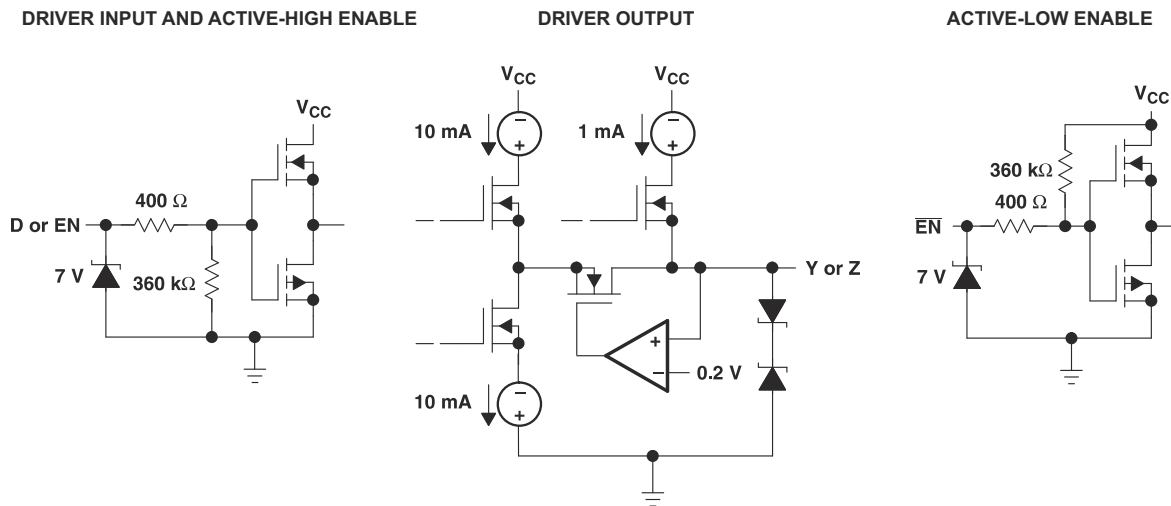


图 7-1. Equivalent Input and Output Schematic Diagrams

## 8 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Synchronization Clock in AdvancedTCA

Advanced Telecommunications Computing Architecture, also known as AdvancedTCA, is an open architecture to meet the needs of the rapidly changing communications network infrastructure. M-LVDS based clocking is recommended by the ATCA.

The ATCA specification includes requirements for three redundant clock signals. An 8KHz and a 19.44MHz clock signal as well as an user-defined clock signal are included in the specification. The SN65MLVD047A quad driver supports distribution of these three ATCA clock signals, supporting operation beyond 100MHz, which is the highest clock frequency included in the ATCA specification. A pair of SN65MLVD047A devices can be used to support the ATCA redundancy requirements.

#### 8.1.2 Multipoint Configuration

The SN65MLVD047A is designed to meet or exceed the requirement of the TIA/EIA-899 (M-LVDS) standard, which allows multipoint communication on a shared bus.

Multipoint is a bus configuration with multiple drivers and receivers present. An example is shown in [图 8-1](#). The figure shows transceivers interfacing to the bus, but a combination of drivers, receivers, and transceivers is also possible. Termination resistors need to be placed on each end of the bus, with the termination resistor value matched to the loaded bus impedance.

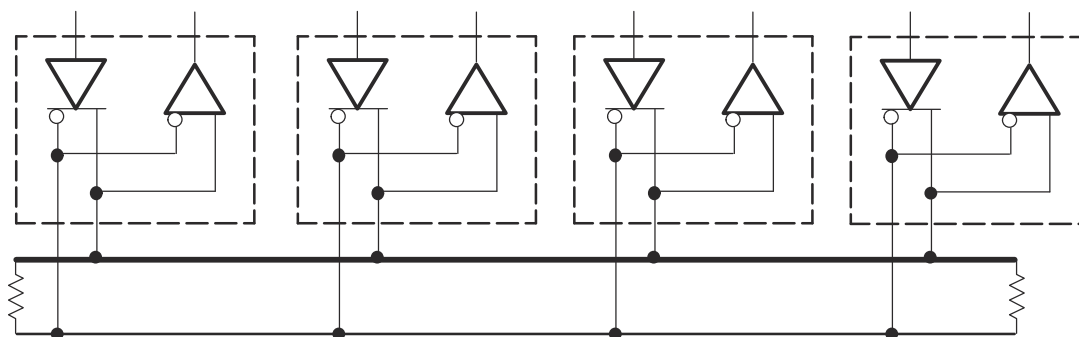


图 8-1. Multipoint Architecture

### 8.1.3 Multidrop Configuration

Multidrop configuration is similar to multipoint configuration, but only one driver is present on the bus. A multidrop system can be configured with the driver at one end of the bus, or in the middle of the bus. When a driver is located at one end, a single termination resistor is located at the far end, close to the last receiver on the bus. Alternatively, the driver can be located in the middle of the bus, to reduce the maximum flight time. With a centrally located driver, termination resistors are located at each end of the bus. In both cases, the termination resistor value should be matched to the loaded bus impedance. 图 8-2 shows examples of both cases.

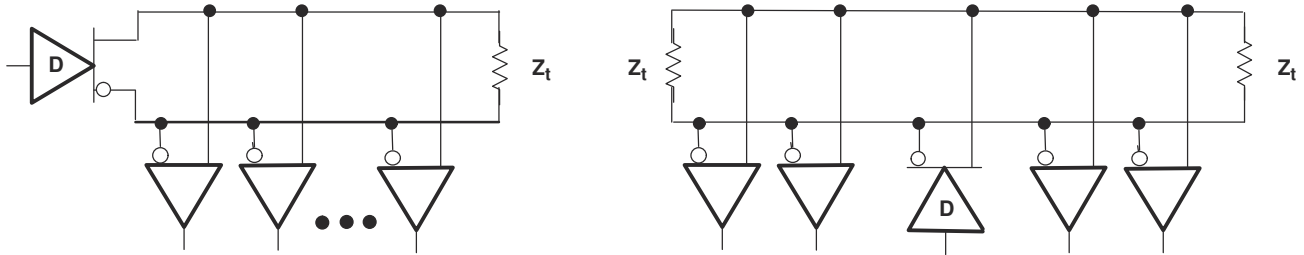


图 8-2. Multidrop Architectures With Different Driver Locations

### 8.1.4 Unused Channel

A 360kΩ pull-down resistor is built in every LVTTTL input. The unused driver inputs should be left floating or connected to ground. The low-level output of an unused enabled driver can oscillate if left floating, and should be connected to ground. If the input is floating or connected to ground, the unused Y (non-inverting) output of an enabled driver should be connected to ground. The unused Z (inverting) should be left floating

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.2 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.3 Trademarks

AdvancedTCA™ and ATCA™ are trademarks of PCI Industrial Computer Manufacturers Group.

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2005) to Revision B (February 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD047AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	<a href="#">Samples</a>
SN65MLVD047ADG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	<a href="#">Samples</a>
SN65MLVD047ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	<a href="#">Samples</a>
SN65MLVD047APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	<a href="#">Samples</a>
SN65MLVD047APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD047ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65MLVD047APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD047ADR	SOIC	D	16	2500	350.0	350.0	43.0
SN65MLVD047APWR	TSSOP	PW	16	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65MLVD047AD	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047ADG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047APW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司