

双通道 USB3.0 转接驱动器 / 均衡器

查询样品: [SN65LVPE502CP](#)

特性

- 单线路 **USB 3.0** 均衡器 / 转接驱动器
- 可选均衡、去加重以及输出摆幅控制
- 集成型端接
- 支持热插拔
- 低工作功耗 (**U0** 状态)
 - **315 mW (TYP)**, $V_{CC} = 3.3V$
- **USB 3.0** 低功耗支持
 - 未检测到连接时功耗为 **7 mW** (典型值)
 - 在 **U2/U3** 模式下进行链接时功耗为 **70 mW** (典型值)
- 优异的抖动与损耗补偿性能:
 - **FR4** 上大于 **40** 英寸的总体 **4 mil** 带状线
- 小型封装 — **24** 引脚 (**4 毫米 x 4 毫米**) **QFN** 封装
- 针对 **ESD** 瞬态的高度保护功能

- **HBM: 5,000 V**
- **CDM: 1,500 V**
- **MM: 200 V**

应用

- 笔记本、台式机、扩展基座、有源线缆、背板与有源线缆

说明

SN65LVPE502CP 是一款支持 5.0Gbps 数据速率的双通道、单线 USB 3.0 转接驱动器与信号调节器。该器件符合 USB 3.0 规范 1.0 版, 可针对 USB 3.0 电源管理模式提供电气空闲调节与低频率周期信号 (LFPS) 支持。

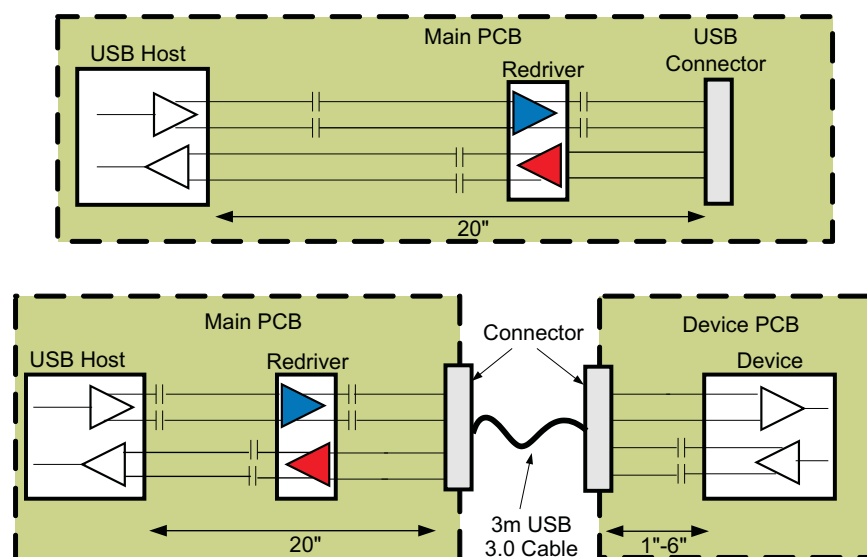


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: [SLLSE79](#)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

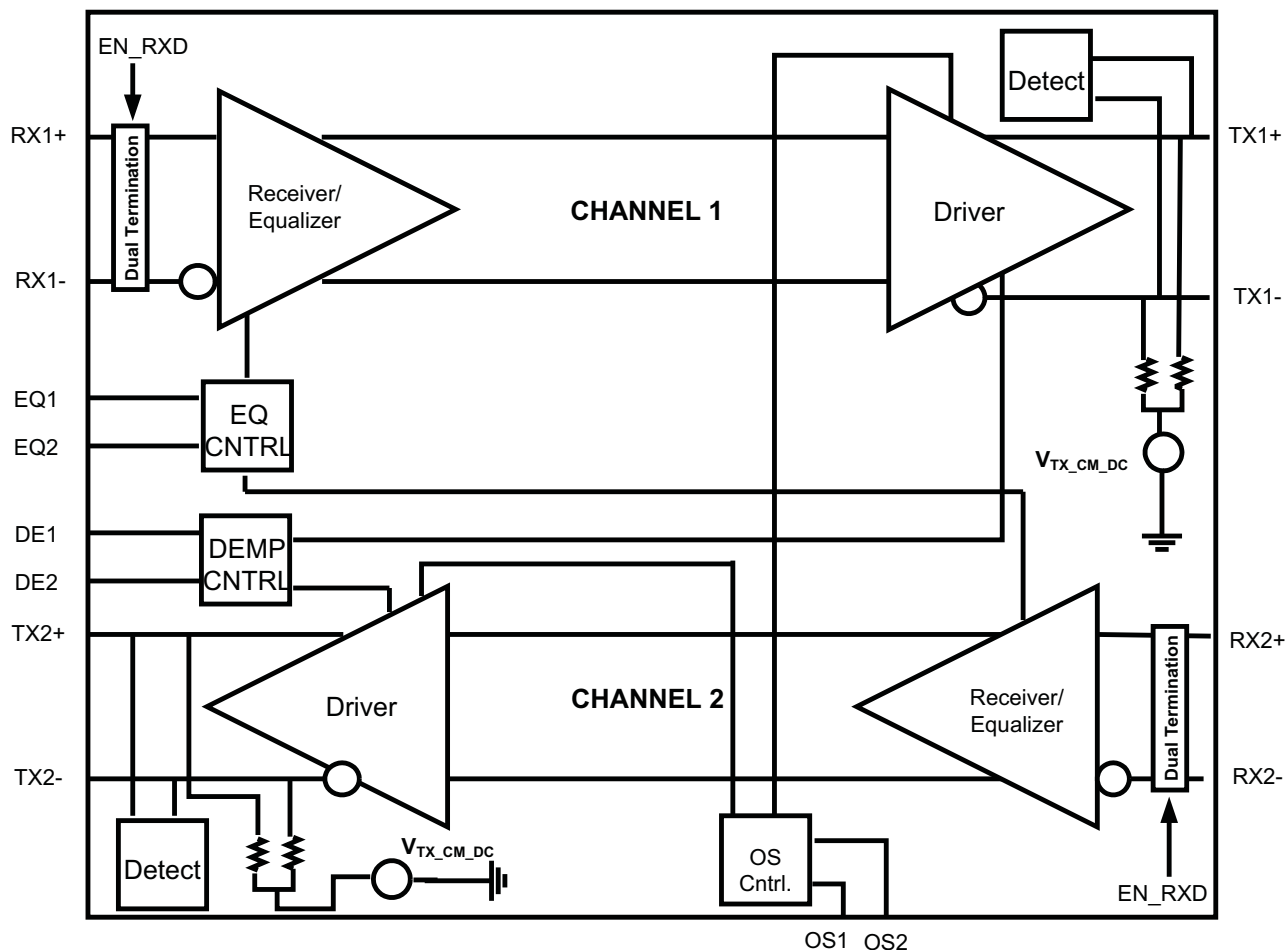


Figure 2. Data Flow Block Diagram

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE
SN65LVPE502CPRGER	502CP	24-pin RGE Reel (Large)
SN65LVPE502CPRGET	502CP	24-pin RGE Reel (Small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range ⁽²⁾	V _{CC}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V _{CC} + 0.5	V
Electrostatic discharge	Human body model ⁽³⁾	±5000		V
	Charged-device model ⁽⁴⁾	±1500		V
	Machine model ⁽⁵⁾	±200		V
Continuous power dissipation		See Thermal Table		

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
- (5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN65LVPE502CP	UNITS
		RGE PACKAGE	
		24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	46	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	42	
θ_{JB}	Junction-to-board thermal resistance	13	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX ⁽¹⁾	UNIT
P _D	Device power dissipation RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V _{ID} = 1000mV _{p-p}		330	450	mW
P _{Slp}	Device power dissipation in sleep mode EN_RXD= GND		0.3	1	mW

- (1) The maximum rating is simulated under 3.6V VCC.

Device Power

The SN65LVPE502CP is designed to operate from a single 3.3V supply.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC}	Supply voltage		3	3.3	3.6	V
C _{COUPLING}	AC Coupling capacitor		75		200	nF
	Operating free-air temperature		0		85	°C
DEVICE PARAMETERS						
I _{CC}	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p	100	120		mA
I _{CC} _{Rx.Detect}		In Rx.Detect mode	2	5		
I _{CC} _{sleep}		EN_RXD = GND	0.01	0.1		
I _{CC} _{U2-U3}		Link in USB low power state	21			
	Maximum data rate				5	Gbps
t _{ENB}	Device enable time	Sleep mode exit time EN_RXD L → H With Rx termination present		100		μs
t _{DIS}	Device disable time	Sleep mode entry time EN_RXD H → L		2		μs
T _{RX.DETECT}	Rx.Detect start event	Power-up time		100		μs
CONTROL LOGIC						
V _{IH}	High level input voltage		1.4	V _{CC}		V
V _{IL}	Low level input voltage		–0.3	0.5		V
V _{HYS}	Input hysteresis		150			mV
I _{IH}	High level input current	OSx, EQx, DEx = V _{CC}		30		μA
		EN_RXD = V _{CC}		1		
		RSVD = V _{CC}		30		
I _{IL}	Low level input current	OSx, EQx, DEx = GND	–30			μA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER AC/DC						
V _{in_diff_P-P}	RX1, RX2 input voltage swing	AC coupled differential RX peak to peak signal	100		1200	mVp-p
V _{CM_RX}	RX1, RX2 common mode voltage			3.3		V
V _{in_COM_P}	RX1, RX2 AC peak common mode voltage	Measured at Rx pins with termination enabled			150	mVP
Z _{DC_RX}	DC common mode impedance		18	26	30	Ω
Z _{diff_RX}	DC differential input impedance		72	80	120	Ω
Z _{RX_High_IMP+}	DC Input high impedance	Device in sleep mode Rx termination not powered measured with respect to GND over 500mV max	50	85		kΩ
V _{RX-LFPS-DETPP}	Low voltage periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output	100		300	mVpp
RL _{RX-DIFF}	Differential return loss	50 MHz – 1.25 GHz	10	11		dB
		1.25 GHz – 2.5 GHz	6	7		
RL _{RX-CM}	Common mode return loss	50 MHz– 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
V _{TxDIFF_TB_P-P}	Differential peak-to-peak output voltage (VID = 800, 1200 mVpp, 5Gbps)	R _L = 100 Ω ±1%, DEX, OSx = NC, Transition Bit	800	1042	1200	mV
		R _L = 100 Ω ±1%, DEX = NC, OSx = GND Transition Bit		908		
		R _L = 100 Ω ±1%, DEX = NC, OSx = VCC Transition Bit		1127		
V _{TxDIFF NTB_P-P}		R _L = 100 Ω ±1%, DEX=NC, OSx = 0,1,NC Non-Transition Bit		1042		mV
		R _L = 100 Ω ±1%, DEX=0 OSx = 0,1,NC Non-Transition Bit		661		
		R _L = 100 Ω ±1%, DEX=1 OSx = 0,1,NC Non-Transition Bit		507		
DE	De-emphasis level OS1,2 = NC (for OS1, 2 = 1 and 0 see Table 2)	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0	–3.0	–3.5	–4.0	
		DE1/DE2 = 1		–6.0		
T _{DE}	De-emphasis width			0.85		UI
Z _{diff_TX}	DC differential impedance		72	90	120	Ω
Z _{CM_TX}	DC common mode impedance	Measured w.r.t to AC ground over 0-500mV	18	23	30	Ω
RL _{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	9	10		dB
		f = 1.25 GHz – 2.5 GHz	6	7		
RL _{CM_TX}	Common mode return loss	f = 50 MHz – 2.5 GHz	11	12		dB
I _{TX_SC}	TX short circuit current	TX± shorted to GND			60	mA
V _{TX_CM_DC}	Transmitter DC common-mode voltage		2.0	2.6	3.0	V
V _{TX_CM_AC_Active}	TX AC common mode voltage active			30	100	mVpp
V _{TX_idle_diff-AC-pp}	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mVpp
V _{TX_CM_DeltaU1-U0}	Absolute delta of DC CM voltage during active and idle states			35	200	mV
V _{TX_idle_diff-DC}	DC Electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V _{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t _R , t _F	Output rise/fall time	20%–80% of differential voltage measured 1" from the output pin	30	65		ps
t _{RF_MM}	Output rise/fall time mismatch	20%–80% of differential voltage measured 1" from the output pin		1.5	20	ps
T _{diff_LH} , T _{diff_HL}	Differential propagation delay	De-Emphasis = –3.5 dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		305	370	ps
t _{idleEntry} , t _{idleExit}	Idle entry and exit times	See Figure 4		4	6	ns
C _{TX}	Tx input capacitance to GND	At 2.5 GHz		1.25		pF

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EQUALIZATION					
$T_{TX-EYE}^{(1)(2)}$ Total jitter (Tj) at point A	Device setting: OS1 = L, DE1 = -6 dB, EQ1 = 7 dB		0.23	0.5	UI ⁽³⁾ p-p
$DJ_{TX}^{(2)}$ Deterministic jitter (Dj)			0.14	0.3	
$RJ_{TX}^{(2)(4)}$ Random jitter (Rj)			0.08	0.2	
$T_{TX-EYE}^{(1)(2)}$ Total jitter (Tj) at point B	Device setting: OS2 = H, DE2 = -6 dB, EQ2 = 7dB		0.15	0.5	UI ⁽³⁾ p-p
$DJ_{TX}^{(2)}$ Deterministic jitter (Dj)			0.07	0.3	
$RJ_{TX}^{(2)(4)}$ Random jitter (Rj)			0.08	0.2	

(1) Includes RJ at 10^{-12} BER

(2) Deterministic jitter measured with K28.5 pattern, Random jitter measured with K28.5 pattern at the ends of reference channel in [Figure 6](#), VID=1000mVpp, 5Gbps, -3.5dB DE from source

(3) UI = 200ps

(4) Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER

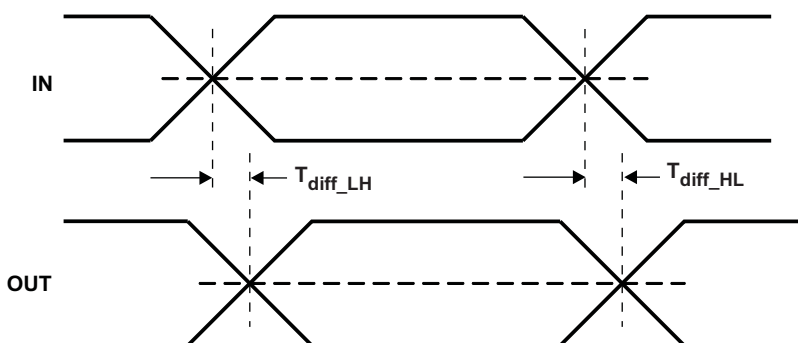


Figure 3. Propagation Delay

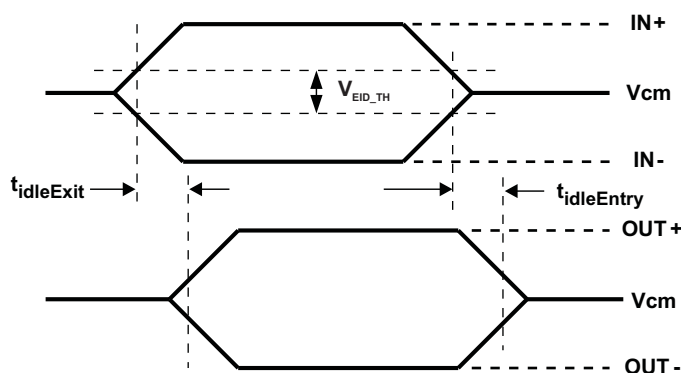


Figure 4. Electrical Idle Mode Exit and Entry Delay

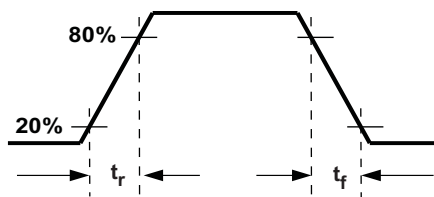


Figure 5. Output Rise and Fall Times

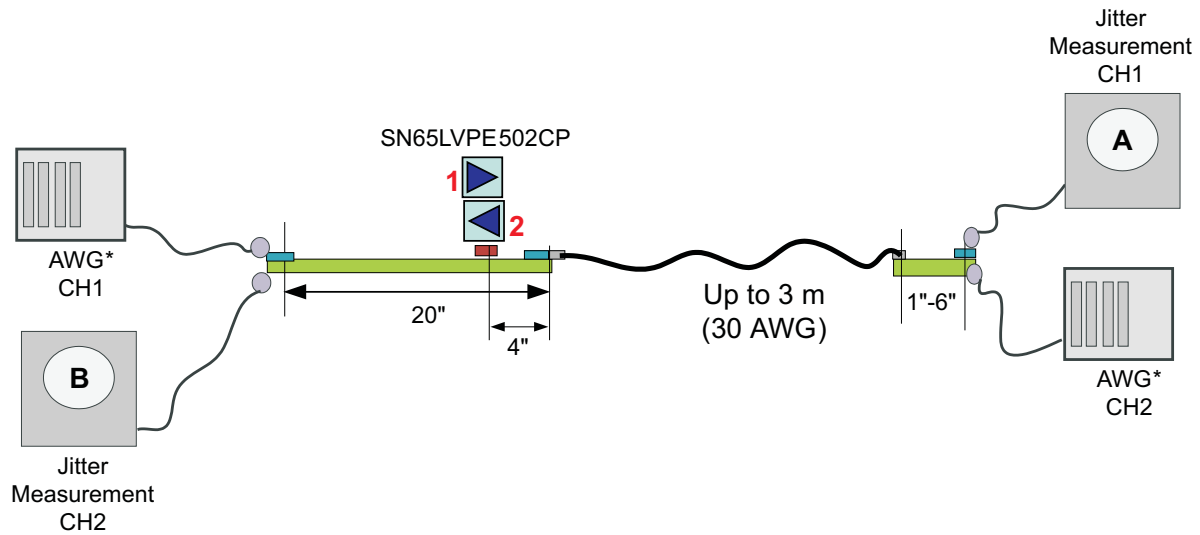


Figure 6. Jitter Measurement Setup

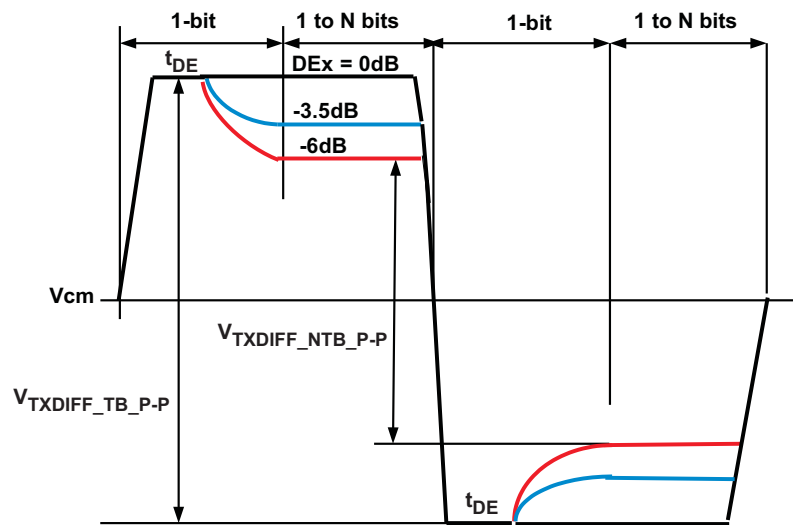
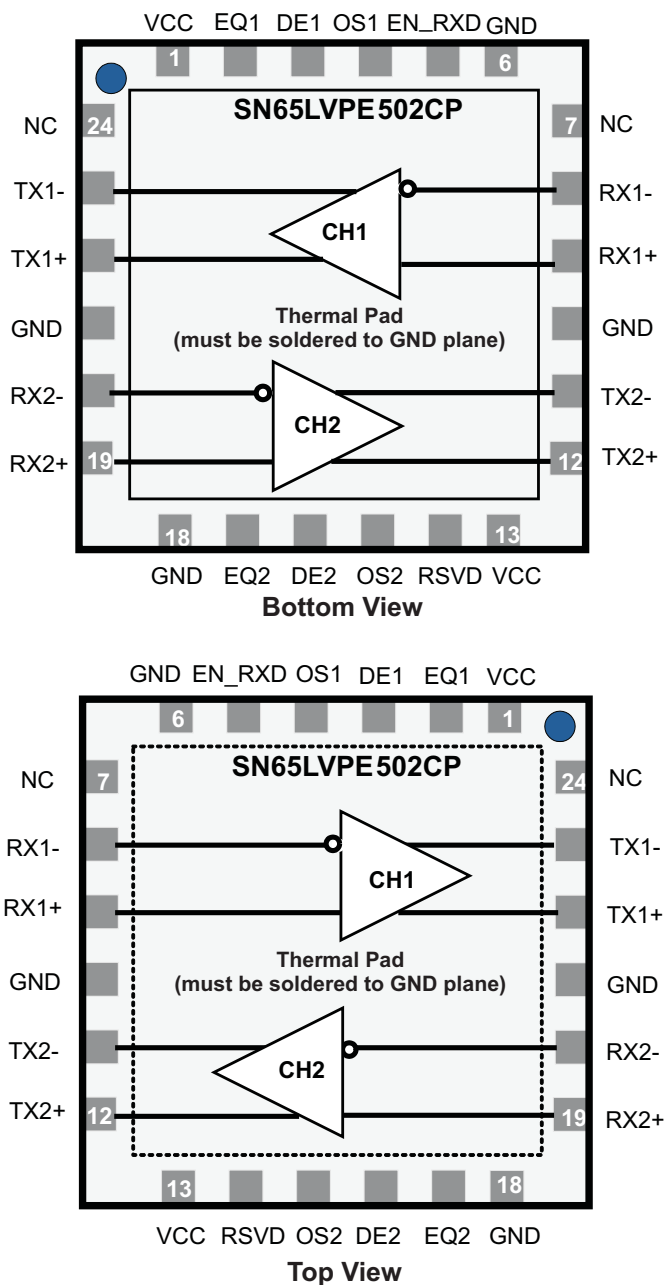


Figure 7. Output De-Emphasis Levels OSx = NC

DEVICE INFORMATION**Figure 8. Flow-Through Pin-Out****Table 1. Pin Functions**

PIN		I/O Type	Description
Number	Name		
HIGH SPEED DIFFERENTIAL I/O PINS			
8	RX1–	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit.
9	RX1+	I, CML	
20	RX2–	I, CML	
19	RX2+	I, CML	

Table 1. Pin Functions (continued)

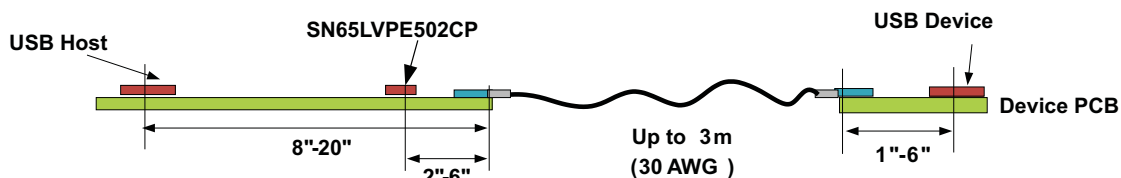
PIN		I/O Type	Description
Number	Name		
23	TX1–	O, VML	Non-inverting and inverting VML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors.
22	TX1+	O, VML	
11	TX2–	O, VML	
12	TX2+	O, VML	
DEVICE CONTROL PIN			
5	EN_RXD	I, LVCMOS	Sets device operation modes per Table 2 . Internally pulled to VCC
14	RSVD	I, LVCMOS	RSVD, internally pulled to GND. Can be left as No-connect.
7, 24	NC	No-connect	Pads are not internally connected
EQ CONTROL PINS ⁽¹⁾			
3, 16	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per Table 2 . Internally tied to Vcc/2
2, 17	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH 1 and CH 2 per Table 2 . Internally tied to Vcc/2
4, 15	OS1, OS2	I, LVCMOS	Selects output amplitude for CH 1 and CH 2 per Table 2 . Internally tied to Vcc/2
POWER PINS			
1,13	VCC	Power	Positive supply should be 3.3V ± 10%
6, 10, 18, 21	GND	Power	Supply ground

(1) Internally biased to Vcc/2 with >200kΩ pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be < 1 μA otherwise drive to Vcc/2 to assert mid-level state

Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OS _x ⁽¹⁾	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQ _x ⁽¹⁾	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DE _x ⁽¹⁾	OS _x ⁽¹⁾ = NC	OS _x ⁽¹⁾ = 0	OS _x ⁽¹⁾ = 1
NC (default)	0 dB	0 dB	0 dB
0	–3.5 dB	–2.2 dB	–4.4 dB
1	–6.0 dB	–5.2 dB	–6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION		
1 (default)	Normal Operation		
0	Sleep Mode		

(1) Where x = Channel 1 or Channel 2



NOTE: For more detailed placement example of redriver see typical eye diagrams and jitter plots at end of data sheet.

Figure 9. Redriver Placement Example

DETAILED DESCRIPTION

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE502CP is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE502CP provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in [Table 2](#).

Low Power Modes

Device supports three low power modes as described below

1. Sleep Mode

Initiated anytime EN_RXD undergoes a high to low transition and stays low or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2μs, device exits sleep mode to Rx.Detect mode after EN_RXD is driven to Vcc, exit time is 100μs max.

2. RX Detect Mode--When no remote device is connected

Anytime LVPE502CP detects a break in link (i.e. when upstream device is disconnected) or after power-up fails to find a remote device, LVPE502CP goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is <10mW (TYP) or less than 5% of its normal operating power. This feature is very useful in saving system power in mobile applications like notebook PC where battery life is critical.

Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

3. U2/U3 Mode

With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes link is in electrical idle state. LVPE502CP will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signal activity (LFPS) is detected.

Receiver Detection

At Power Up or Reset

After power-up or anytime EN_RXD is toggled, RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel

- The TX and RX terminations are switched to Z_{DIFF_TX} , Z_{DIFF_RX} respectively.

If no receiver is detected on one or both channels

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or device is put in sleep mode

During U2/U3 Link State

Rx detection is also performed periodically when link is in U2/U3 states. However in these states during Rx detection, input termination is not automatically disabled before performing Rx.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power-up RX.Detect state.

Electrical Idle Support

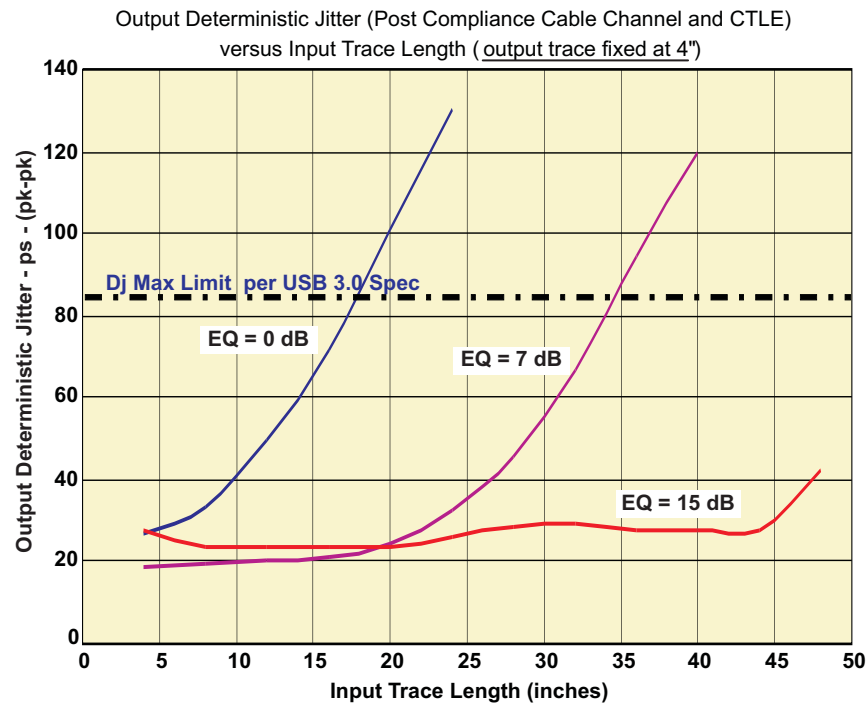
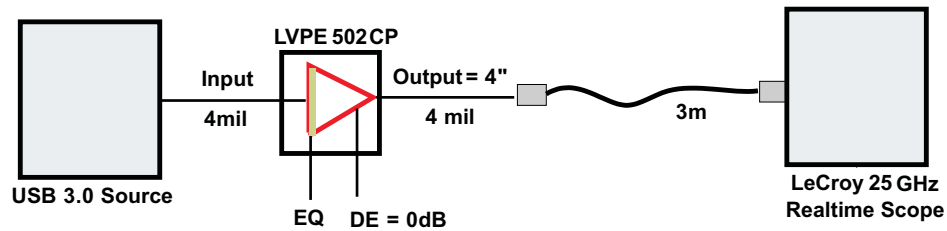
Electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. LVPE502CP detects an electrical idle state when RX± voltage at the device pin falls below VRX_LFPS_DIFFp-p min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds VRX_LFPS_DIFFp-p max normal operation is restored and output start passing input signal. Electrical idle exit and entry time is speccified at < 6ns.

TYPICAL EYE DIAGRAM AND PERFORMANCE CURVES

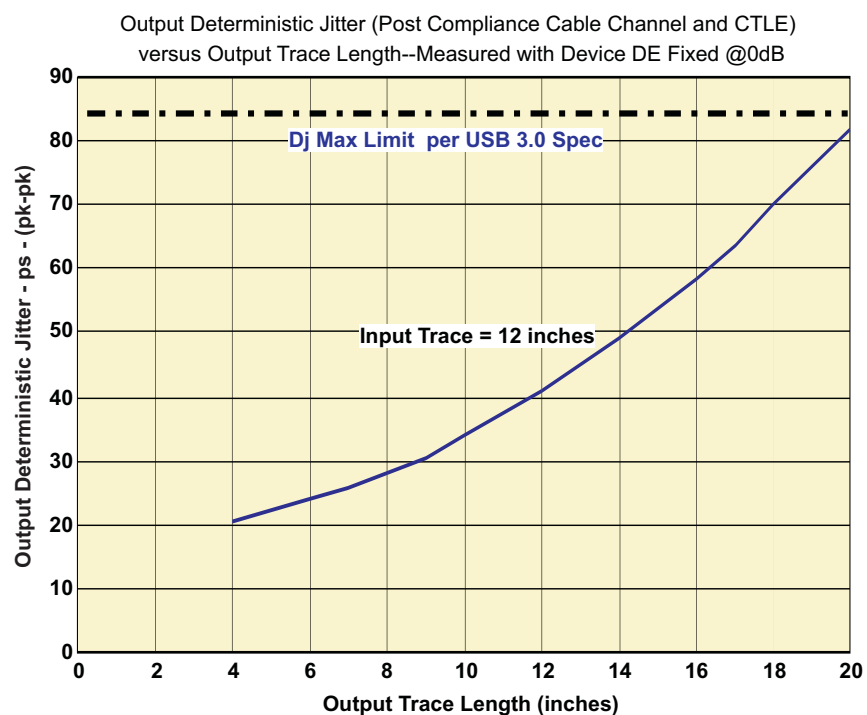
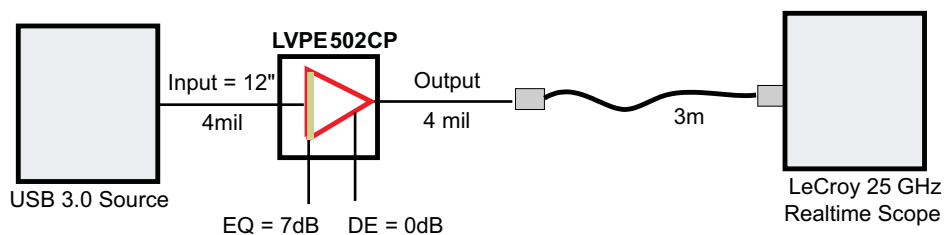
Measurement equipment details:

- Generator (source) LeCroy PERT3,
- Signal: 5Gbps, 1000mVp-p, 3.5 dB De-Emphasis
- Tj and Dj measurements based on CP0 (USB 3 compliance pattern) which is D0.0 or logical idle with SKP sequences removed
- Rj measurements based on CP1 or D10.2 symbol containing alternating 0s and 1s at Nyquist frequency
- Oscilloscope (Sink) LeCroy 25GHz Real Time Oscilloscope
- LeCroy QualiPHY software used to measure jitter and collect compliance eye diagrams

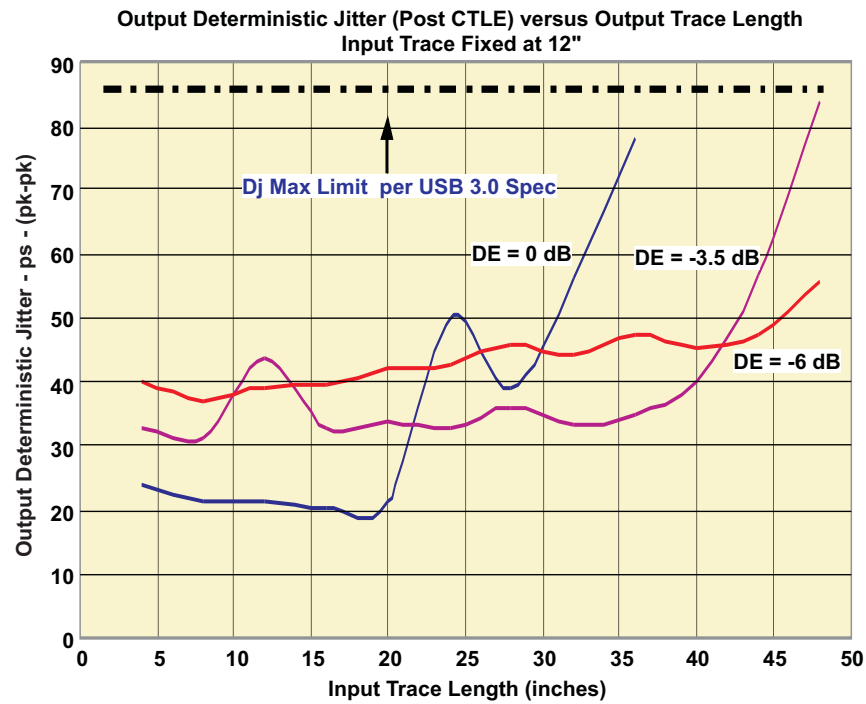
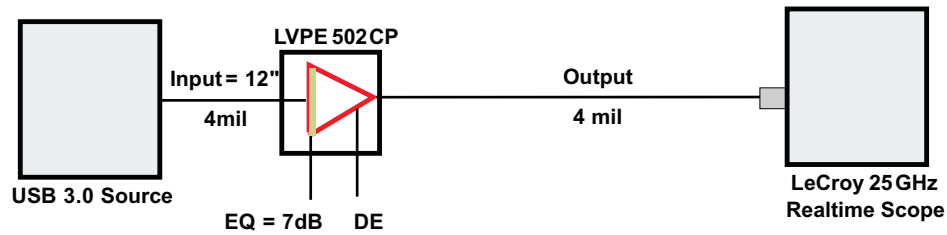
Device Operating Conditions: VCC = 3.3 V, Temp = 25°C, EQx/DEx/OSx set to their default value when not mentioned

PLOT #1 FIXED OUTPUT TRACE +3m USB 3 CABLE WITH VARIABLE INPUT TRACE

PLOT #2 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and +3m USB 3.0 CABLE



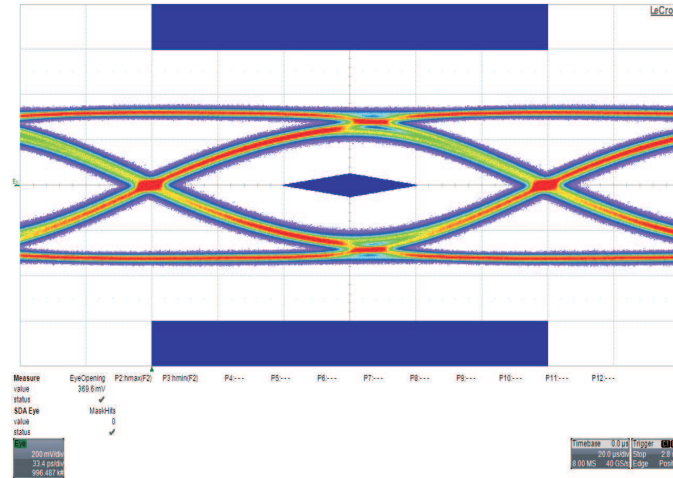
PLOT #3 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and (No Cable)



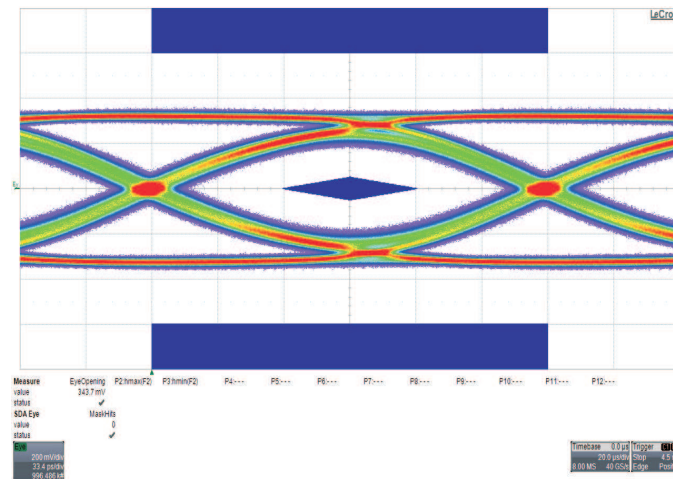
USB 3.0 MASK EYE DIAGRAM TEST

CASE I FIXED OUTPUT AND VARIABLE INPUT TRACE

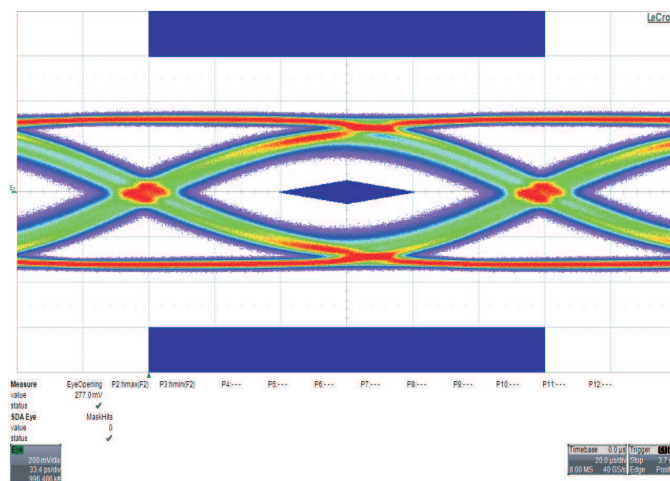
DE= 0dB, EQ = 0dB, Input = 4", Output = 4" + 3m Cable



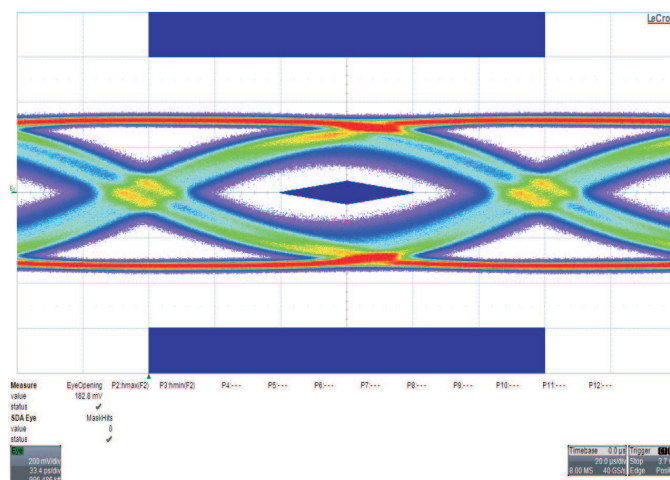
DE= 0dB, EQ = 0dB, Input = 8", Output = 4" + 3m Cable



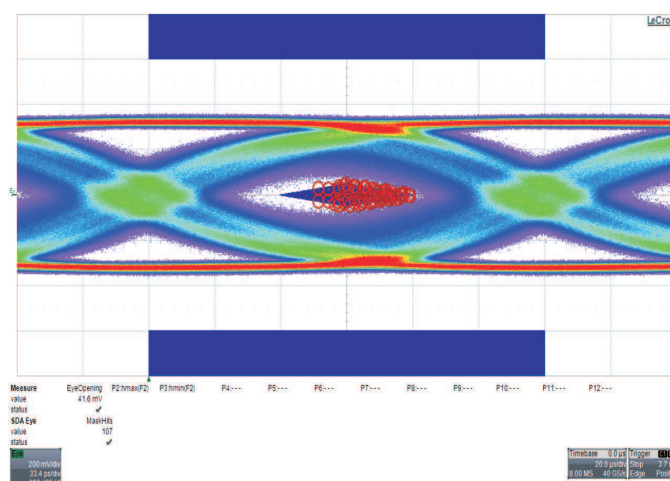
DE= 0dB, EQ = 0dB, Input = 12", Output = 4" + 3m Cable



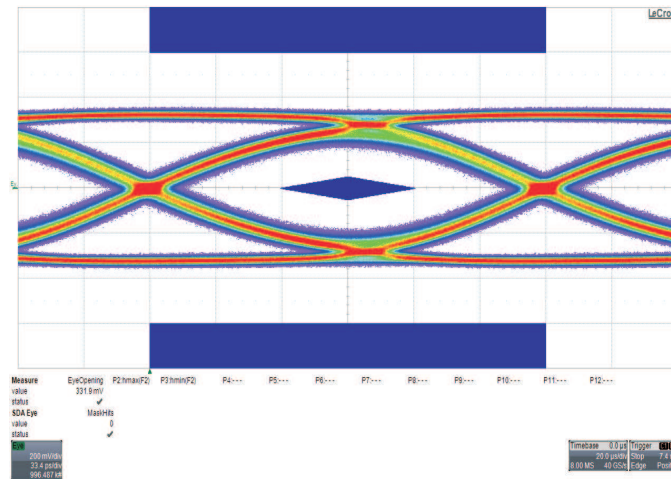
DE= 0dB, EQ = 0dB, Input = 16", Output = 4" + 3m Cable



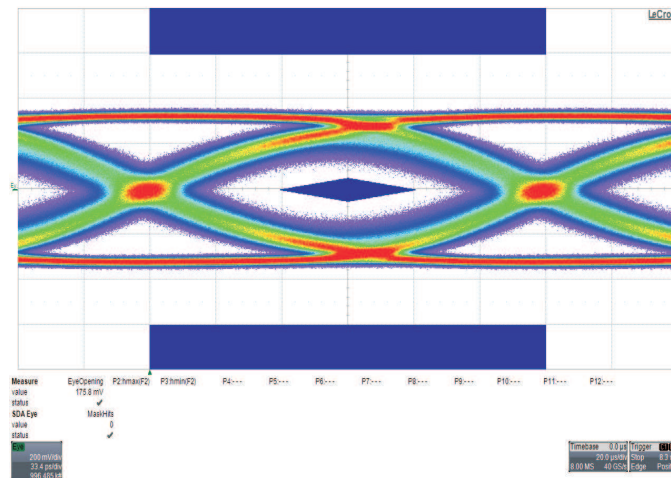
DE= 0dB, EQ = 0dB, Input = 20", Output = 4" + 3m Cable



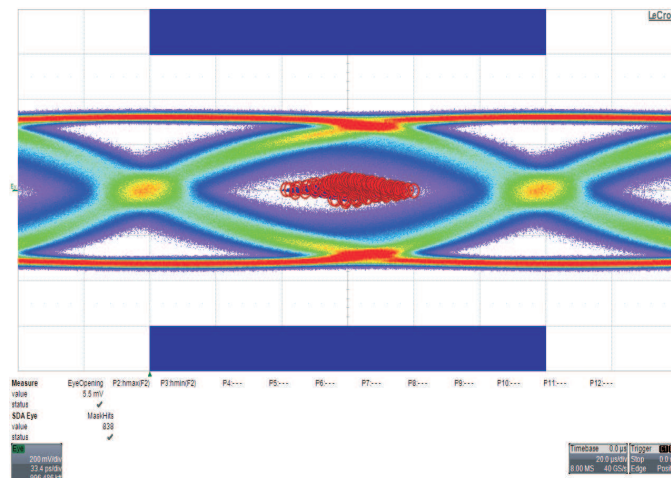
DE= 0dB, EQ = 7dB, Input = 24", Output = 4" + 3m Cable



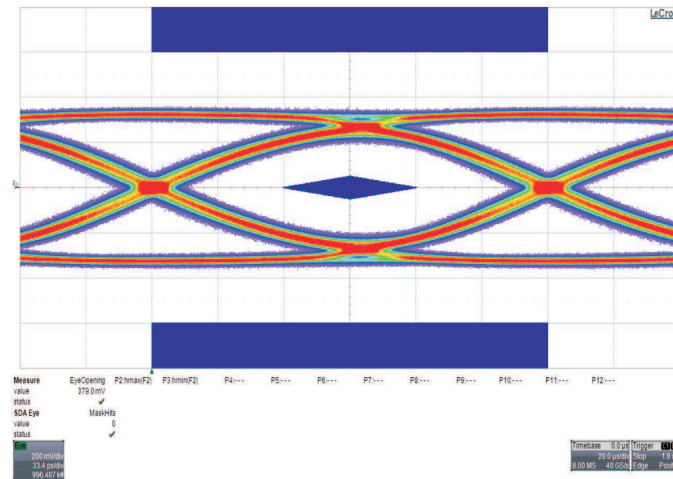
DE= 0dB, EQ = 7dB, Input = 32", Output = 4" + 3m Cable



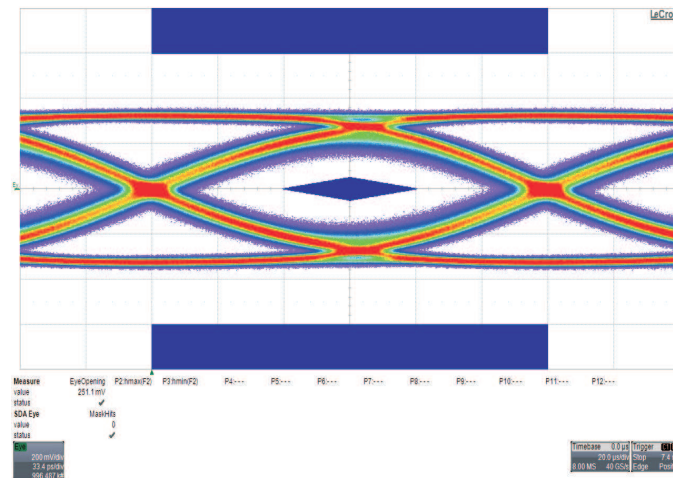
DE= 0dB, EQ = 7dB, Input = 36", Output = 4" + 3m Cable



DE= 0dB, EQ = 15dB, Input = 36", Output = 4" + 3m Cable

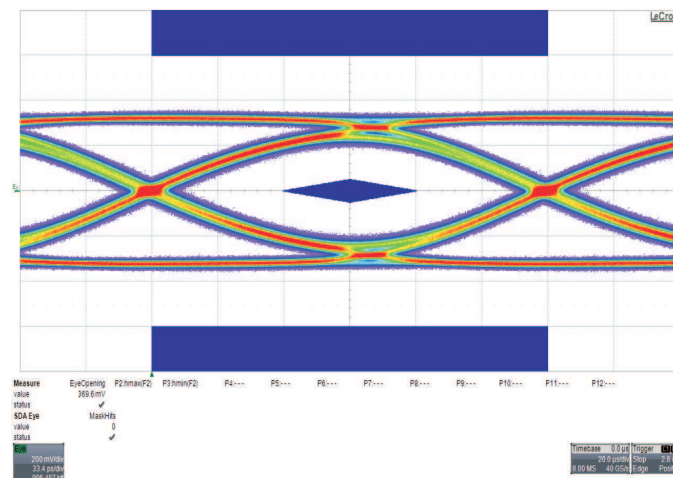


DE= 0dB, EQ = 15dB, Input = 48", Output = 4" + 3m Cable

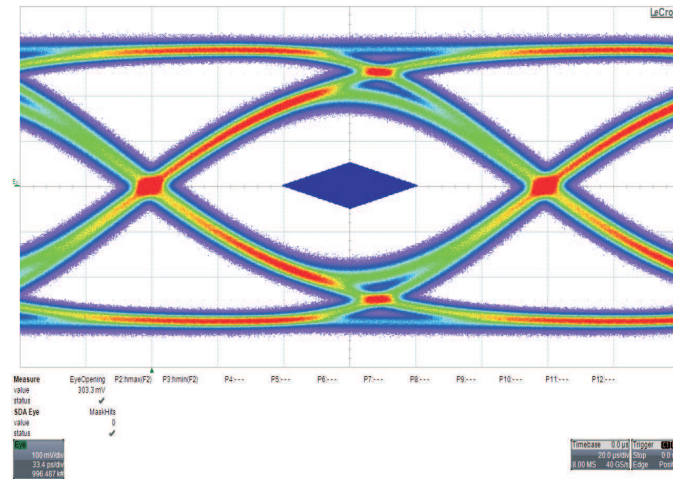


CASE II FIXED INPUT AND VARIABLE OUTPUT TRACE+ 3m CABLE

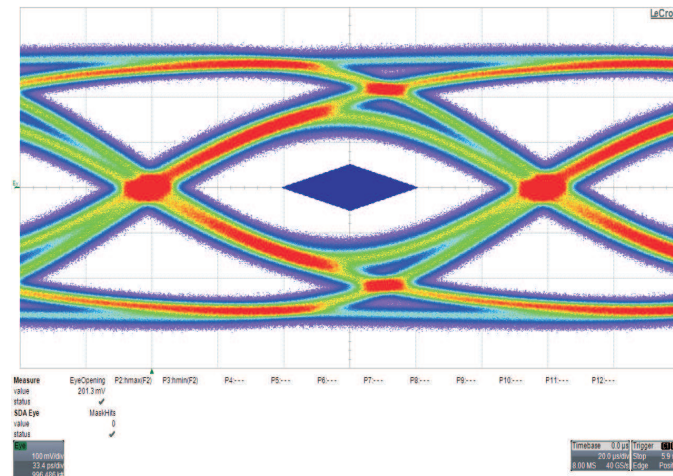
DE= 0dB, EQ = 7dB, Input = 12", Output = 4" + 3m Cable



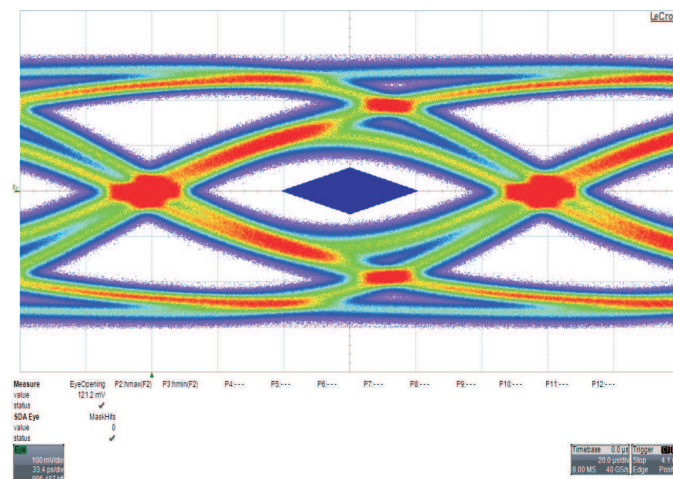
DE= 0dB, EQ = 7dB, Input = 12", Output = 8" + 3m Cable



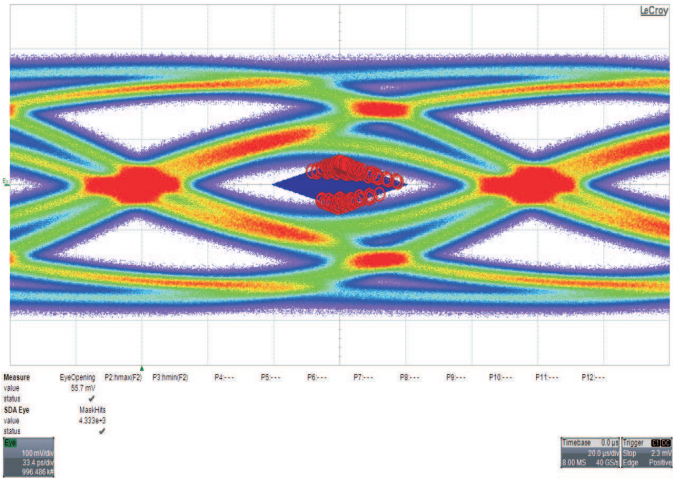
DE= 0dB, EQ = 7dB, Input = 12", Output = 12" + 3m Cable



DE= 0dB, EQ = 7dB, Input = 12", Output = 16" + 3m Cable

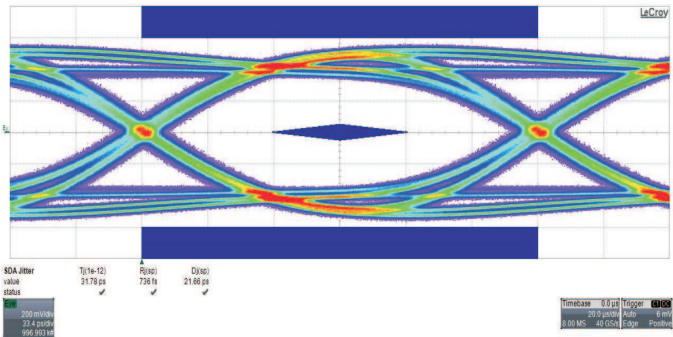


DE= 0dB, EQ = 7dB, Input = 12", Output = 20" + 3m Cable

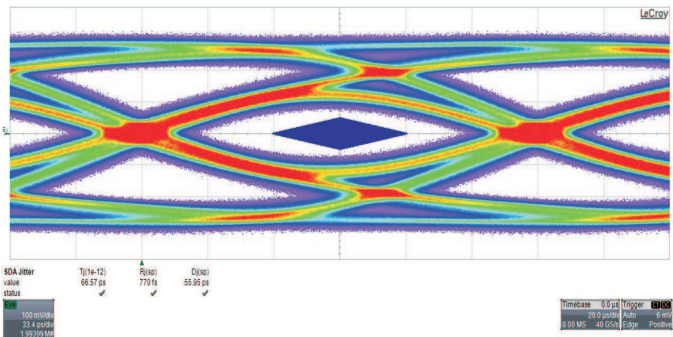


CASE III FIXED INPUT AND VARIABLE OUTPUT TRACE (No Cable)

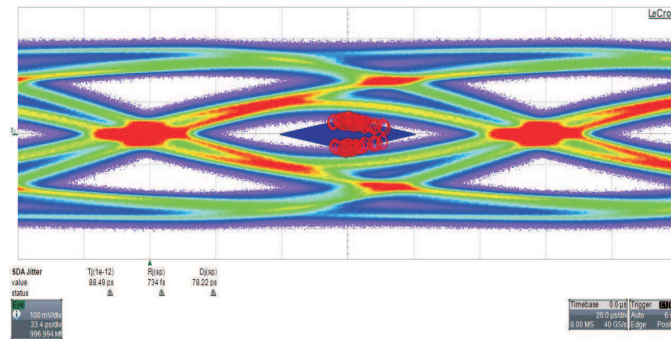
DE= 0dB, EQ = 7dB, Input = 12", Output = 8"



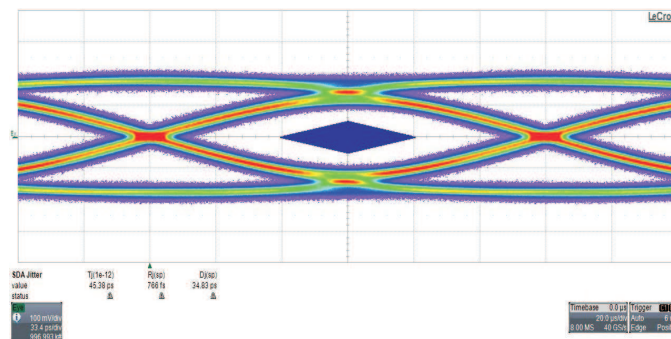
DE= 0dB, EQ = 7dB, Input = 12", Output = 32"



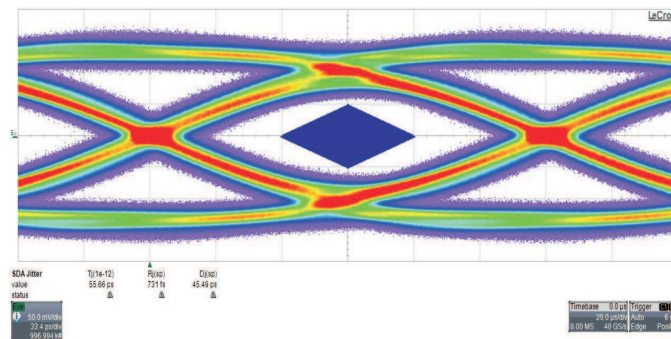
DE= 0dB, EQ = 7dB, Input = 12", Output = 36"



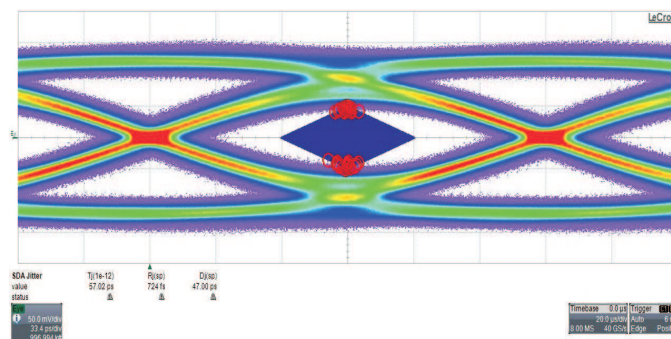
DE= -3.5dB, EQ = 7dB, Input = 12", Output = 36"



DE= -6.0dB, EQ = 7dB, Input = 12", Output = 40"



DE= -6.0dB, EQ = 7dB, Input = 12", Output = 44"



REVISION HISTORY

Changes from Original (March 2011) to Revision A	Page
• Changed the Block Diagram label From: CM/EN_RXD To: EN_RXD	2
• Changed From: CM To: RSVD in the THERMAL CHARACTERISTICS table Test Conditions	3
• Changed From: CM To: RSVD in the RECOMMENDED OPERATING CONDITIONS table Test Conditions	4
• Changed pin name From: CM To: RSVD in the Flow-Through Pin-Out illustration	8
• Changed pin name and description From: CM To: RSVD in the Pin Functions table	9
• Deleted CM and Device Functions columns from the Control Pins Settings of Table 2	9
• Deleted the USB Compliance Mode section	11
Changes from Revision A (September 2011) to Revision B	Page
• Changed the I/O type for the TX pins (11, 12, 22, 23) From: O, CML To: O, VML	9
• Changed the pin Description for the TX pins (11, 12, 22, 23) From: Non-inverting and inverting CML differential output for CH 1 and CH 2 To: Non-inverting and inverting VML differential output for CH 1 and CH 2	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVPE502CPRGER	NRND	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP
SN65LVPE502CPRGER.B	NRND	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP
SN65LVPE502CPRGET	NRND	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP
SN65LVPE502CPRGET.B	NRND	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

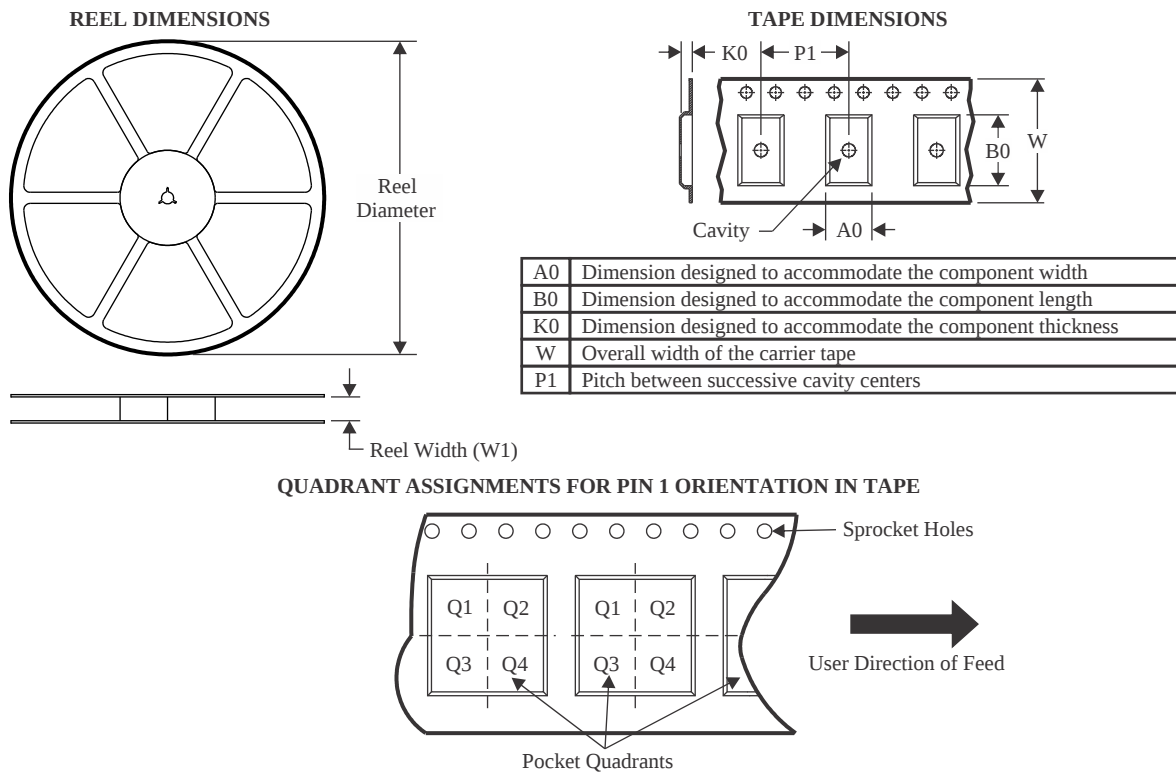
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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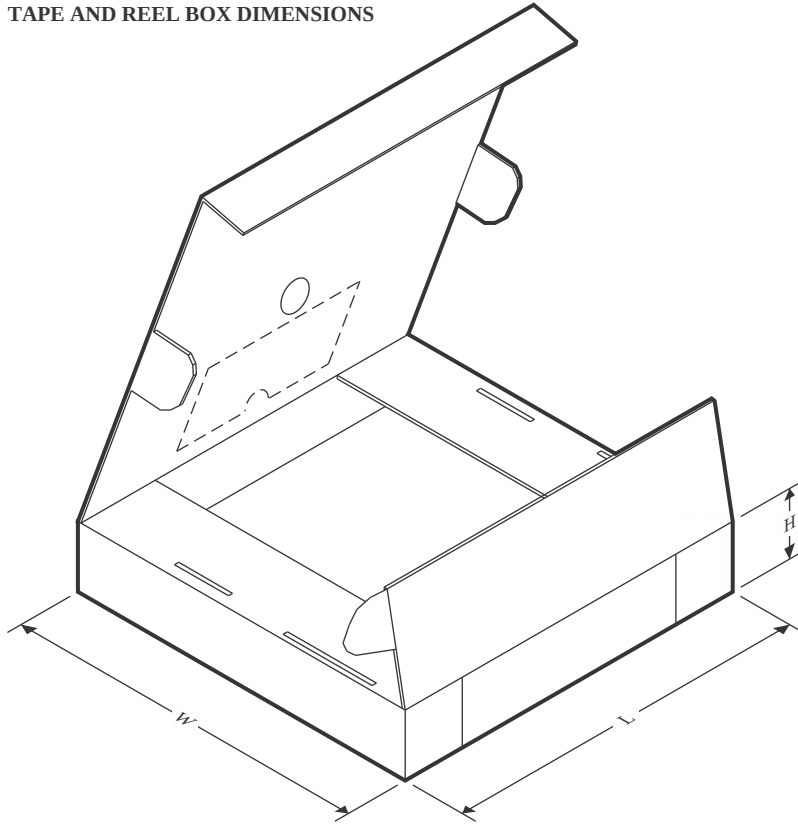
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE502CPRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE502CPRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

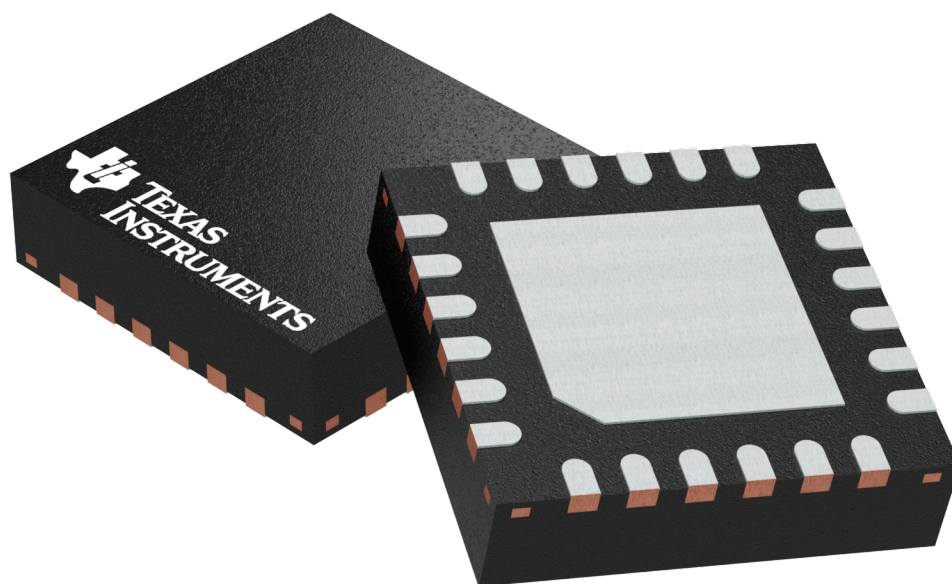
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE502CPRGER	VQFN	RGE	24	3000	353.0	353.0	32.0
SN65LVPE502CPRGET	VQFN	RGE	24	250	213.0	191.0	35.0

RGE 24

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

VQFN - 1 mm max height

The drawing illustrates the mechanical specifications for a 24-pin connector housing. It includes three views: a top view, a front view, and a side view.

Top View: Shows the overall dimensions of the housing. The width is 4.1 (3.9) and the height is 4.1 (3.9). A shaded area in the top-left corner is labeled "PIN 1 INDEX AREA". A feature control frame at the bottom center specifies a circular runout of 0.1 (M) C A B and a circular runout of 0.05 (M) C.

Front View: Shows the front of the housing with 24 pins. The top edge has a maximum thickness of 1. The bottom edge has a thickness of 0.05 (0.00). The pins are spaced at 2X 2.5. The pin height is 2.1 ± 0.1. The pin width is 0.08 (C). The pin pitch is 0.08 (C). The pin ID (optional) is 0.05 (M) C. The pin ID (optional) is 0.05 (M) C. The pin ID (optional) is 0.05 (M) C.

Side View: Shows the side of the housing with a typical thickness of 0.2. The side view shows the profile of the housing and the pins.

Dimensions and Callouts:

- Top View: 4.1 (3.9) width, 4.1 (3.9) height, PIN 1 INDEX AREA, 0.1 (M) C A B, 0.05 (M) C.
- Front View: 1 MAX, 0.05 (0.00), 2X 2.5, 2.1 ± 0.1, 0.08 (C), 0.08 (C), 0.05 (M) C, 0.05 (M) C, 0.05 (M) C.
- Side View: (0.2) TYP.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

VQFN - 1 mm max height

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

VQFN - 1 mm max height

Technical drawing of a mechanical part, likely a bracket or plate, showing dimensions and features. The part is symmetrical about a vertical centerline (SYM) and a horizontal centerline (SYM).

Key dimensions and features:

- Overall width: 3.8
- Overall height: 3.8
- Top edge features: 24X (0.6), 24X (0.24), 20X (0.5)
- Central features: 4X (0.94), 19, 18, 13, 7, 12, 6, 25
- Bottom edge features: 7, 12, 25
- Material: METAL TYP
- Radius: (R0.05) TYP
- Typical hole diameter: (0.57) TYP

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X



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