SN65LVPE502x 双通道 USB 3.0 转接驱动器和均衡器

1 特性

- 单信道 USB 3.0 转接驱动器和均衡器
- 可选均衡、去加重以及输出摆幅控制
- 集成型端接
- 支持热插拔
- 低有源功耗（U0 状态）：
  - 315mW（典型值），V_{CC} = 3.3V
- USB 3.0 低功耗支持：
  - 未检测到连接时功耗为 7mW（典型值）
  - 在 U2/U3 模式下进行链接时功耗为 70mW（典型值）
- 优异的抖动与损耗补偿能力：
  - FR4 上总的 4mil 带状线大于 40 英寸
- 小尺寸 3mm × 3mm 和 4mm × 4mm 24 引脚 VQFN 封装
- 高水平的 ESD 瞬态保护：
  - 人体放电模式 (HBM)：5000V
  - 组件充电模式 (CDM)：1500V
  - 机器放电模式 (MM)：200V

2 应用

- 笔记本电脑
- 台式机
- 扩展坞
- 背板
- 有源线缆

3 说明

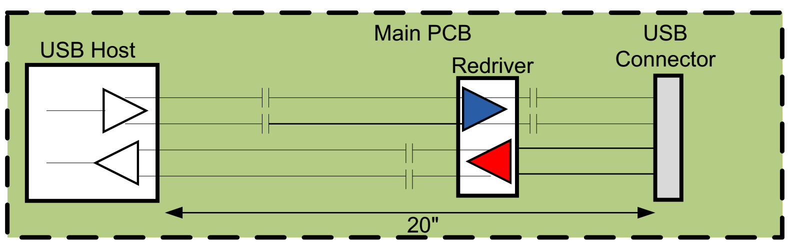
SN65LVPE502x 器件是支持 5Gbps 数据速率的双通道、单信道 USB 3.0 转接驱动器和信号调节器。这些器件符合 USB 3.0 规范 1.0 版的要求，支持 USB 3.0 电源管理模式的电气空闲状态和低频率周期信号 (LFPS)。

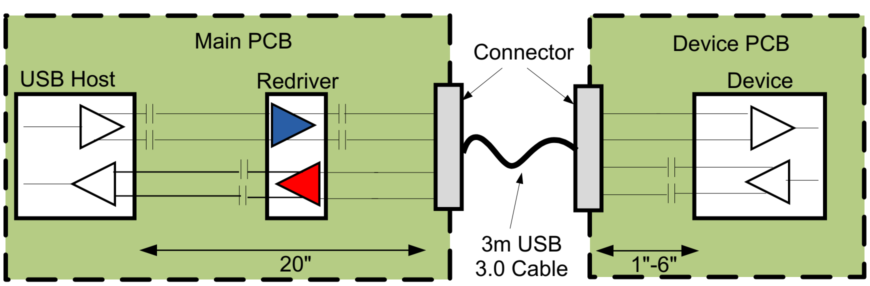
器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65LVPE502A	RLL (24)	3.00mm × 3.00mm
SN65LVPE502A、SN65LVPE502B	RGE (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用





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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2012) to Revision C — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- Added Storage temperature (–65 to 150°C) to the *Absolute Maximum Ratings* table 6

Changes from Revision A (March 2012) to Revision B — **Page**

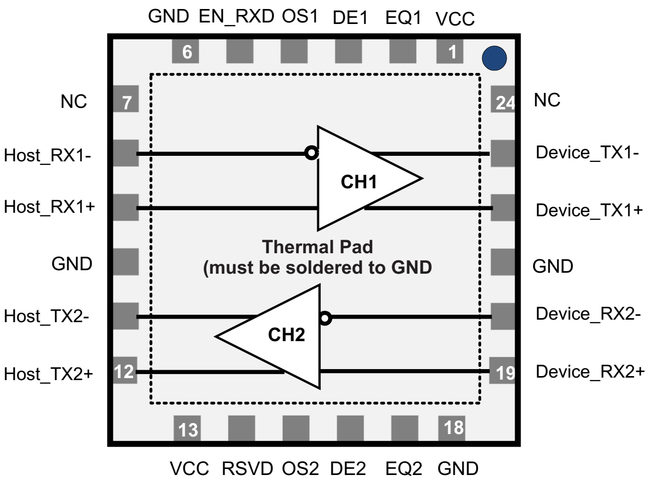
- 已添加 SN65LVPE502B 器件 1
- 已更改 将特性中的“小尺寸 – 24 引脚 (4mm x 4mm) QFN 封装”更改为“小尺寸 – 3x3mm 和 4x4mm 24 引脚 QFN 封装” 1
- Deleted bottom view pinout image 3
- Added RLL package pinout image 4
- Added RLL to *Pin Functions* table 5
- Added Host- and Device-Side Pins section 19

Changes from Original (March 2012) to Revision A — **Page**

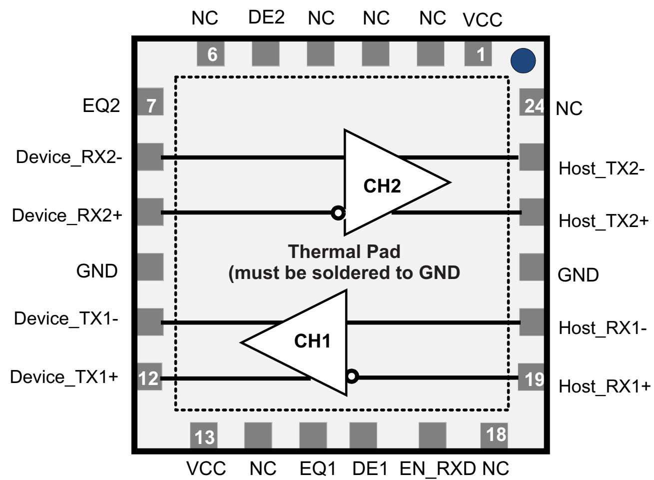
- 已删除 *订购信息* 表；请参阅产品说明书末尾的 POA 1

5 Pin Configuration and Functions

SN65LVPE502A RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



SN65LVPE502B RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions – RGE Packages

PIN			TYPE(1)	DESCRIPTION
NAME	SN65LVPE502A	SN65LVPE502B		
HIGH SPEED DIFFERENTIAL I/O PINS				
Host_RX1–	8	20	I	CML, inverting differential input for CH1. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 host side.
Host_RX1+	9	19	I	CML, noninverting differential input for CH1. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 host side.
Device_RX2–	20	8	I	CML, inverting differential input for CH2. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 Device side.
Device_RX2+	19	9	I	CML, noninverting differential input for CH2. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 Device side.
Device_TX1–	23	11	O	CML, inverting differential output for CH1. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Device side.
Device_TX1+	22	12	O	CML, noninverting differential output for CH1. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Device side.
Host_TX2–	11	23	O	CML, inverting differential output for CH2. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Host side.
Host_TX2+	12	22	O	CML, noninverting differential output for CH2. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Host side.
DEVICE CONTROL PINS				
EN_RXD	5	17	I	LVCMOS, sets device operation modes per Table 4; internally pulled to V_{CC}.
RSVD	14	—	I	LVCMOS; RSVD. Can be left as *No-Connect*.
NC	7, 24	2, 3, 4, 6, 14, 18, 24	—	Pads are not internally connected.

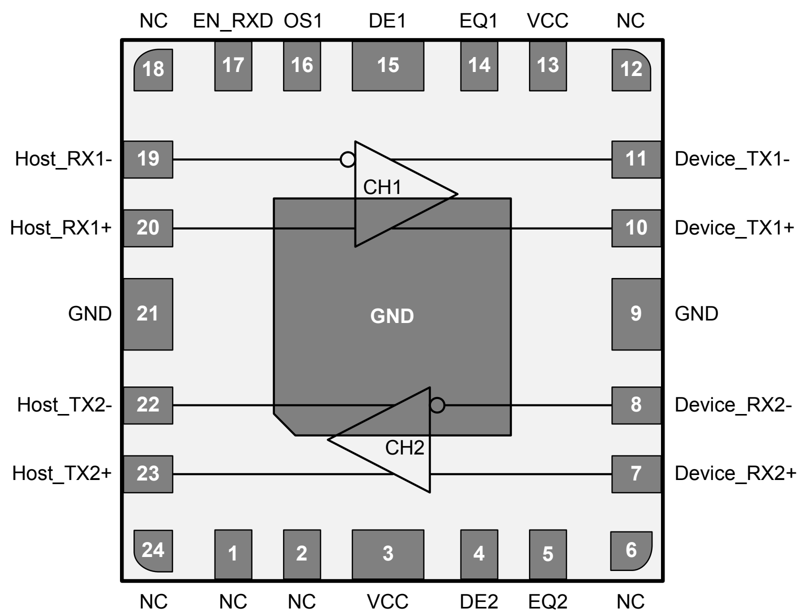
(1) I = Input, O = Output, P = Power

Pin Functions – RGE Packages (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	SN65LVPE502A	SN65LVPE502B		
EQ CONTROL PINS(2)				
DE1, DE2	3, 16	16, 5	I	LVCMOS, selects de-emphasis settings for CH1 and CH2 per Table 4; internally tied to V_{CC}/2.
EQ1, EQ2	2, 17	15, 7	I	LVCMOS, selects equalization settings for CH1 and CH2 per Table 4, internally tied to V_{CC}/2.
OS1, OS2	4, 15	—	I	LVCMOS, selects output amplitude for CH1 and CH2 per Table 4, internally tied to V_{CC}/2.
POWER PINS(3)				
GND	6, 10, 18, 21, Thermal Pad	10, 21, Thermal Pad	P	Supply ground
VCC	1,13	1, 13	P	Positive supply; must be 3.3 V ±10%

(2) Internally biased to V_{CC}/2 with >200 kΩ pullup or pulldown. When pins are left as NC, board leakage at this pin pad must be <1 µA otherwise drive to Vcc/2 to assert mid-level state.
(3) For SN65LVPE502B, pins 10 and 21 must be connected to GND, while 6 and 18 may be NC. For SN65LVPE502A, TI recommends at least two of the four pins (6, 10, 18, 21) be connected to ground.

SN65LVPE502A RLL Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions – RLL Package

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/O PINS			
Host_RX1–	19	I	CML, inverting differential input for CH1. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 host side.
Host_RX1+	20	I	CML, noninverting differential input for CH1. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 host side.
Device_RX2–	8	I	CML, inverting differential input for CH2. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 Device side.
Device_RX2+	7	I	CML, noninverting differential input for CH2. This pin is tied to an internal voltage bias by dual termination resistor circuit. Must connect to the USB 3.0 Device side.
Device_TX1–	11	O	CML, inverting differential output for CH1. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Device side.
Device_TX1+	10	O	CML, noninverting differential output for CH1. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Device side.
Host_TX2–	22	O	CML, inverting differential output for CH2. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Host side.
Host_TX2+	23	O	CML, noninverting differential output for CH2. This pin is tied to an internal voltage bias by termination resistors. Must connect to the USB 3.0 Host side.
DEVICE CONTROL PINS			
EN_RXD	17	I	LVCMOS, sets device operation modes per Table 4; internally pulled to V_{CC}.
NC	1, 2, 6, 12, 18, 24	—	Pads are not internally connected.
EQ CONTROL PINS [2]			
DE1, DE2	15, 4	I	LVCMOS, selects de-emphasis settings for CH1 and CH2 per Table 4; internally tied to $V_{CC}/2$.
EQ1, EQ2	14, 5	I	LVCMOS, selects equalization settings for CH1 and CH2 per Table 4; internally tied to $V_{CC}/2$.
OS1, OS2	16, NC [3]	I	LVCMOS, selects output amplitude for CH1 and CH2 per Table 4; internally tied to $V_{CC}/2$.
POWER PINS			
GND	9, Thermal Pad	P	Supply ground
VCC	3	P	Positive supply; must be 3.3 V ±10%

(1) I = Input, O = Output, P = Power
(2) Internally biased to $V_{CC}/2$ with >200 kΩ pullup or pulldown. When pins are left as NC, board leakage at this pin pad must be <1 µA otherwise drive to Vcc/2 to assert mid-level state.
(3) The SN65LVPE502A RLL package has OS2 internal no-connect to select the 1042-mV_{pp} level on TX2.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control I/O	–0.5	VCC + 0.5	V
Continuous power dissipation		See *Dissipation Ratings*		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model(3)	±200	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(2) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	AC-coupling capacitor		75		200	nF
T_A	Operating free-air temperature		–40		85	°C
DEVICE PARAMETERS						
I_{CCCCCC}	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000 mV_{pp}		100	120	mA
$ICC_{RX.Detect}$	Supply current	In RX.Detect mode		2	5	mA
ICC_{sleep}	Supply current	EN_RXD = GND		0.01	0.1	mA
ICC_{U2-U3}	Supply current	Link in USB low power state		21		mA
	Maximum data rate				5	Gbps
t_{ENB}	Device enable time	Sleep mode exit time EN_RXD L → H with RX termination present			100	µs
t_{DIS}	Device disable time	Sleep mode entry time EN_RXD H → L			2	µs
$T_{RX.DETECT}$	RX.Detect start event	Power-up time			100	µs
CONTROL LOGIC						
V_{IH}	High-level input voltage		2.8		V_{CC}	V
V_{IL}	Low-level input voltage		–0.3		0.5	V
V_{HYS}	Input hysteresis			150		mV
I_{IH}	High level input current	OSx, EQx, DEx = V_{CC}			30	µA
		EN_RXD = V_{CC}			1	
		RSVD = V_{CC}			30	
I_{IL}	Low level input current	OSx, EQx, DEx = GND	–30			µA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

6.4 Thermal Information

THERMAL METRIC (1)		SN65LVPE502A, SN65LVPE502B		UNIT
		RGE (VQFN)	RLL (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	1.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVER AC/DC						
Vin_{diff_pp}	RX1, RX2 input voltage swing	AC-coupled differential RX peak-to-peak signal	100		1200	mV_{pp}
VCM_RX	RX1, RX2 common mode voltage			3.3		V
Vin_{COM_P}	RX1, RX2 AC peak common mode voltage	Measured at RX pins with termination enabled			150	mV_{pp}
Z_{CM_RX}	DC common mode impedance		18	26	30	Ω
Z_{diff_RX}	DC differential input impedance		72	80	120	Ω
$Z_{RX\_High\_IMP+}$	DC Input high impedance	Device in sleep mode RX termination not powered measured with respect to GND over 500 mV maximum	50	85		kΩ
$V_{RX-LFPS-DET-PP}$	Low frequency periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above maximum input signal is passed to output	100		300	mV_{pp}
$RL_{RX-DIFF}$	Differential return loss	50 MHz to 1.25 GHz	10	11		dB
		1.25 GHz to 2.5 GHz	6	7		
RL_{RX-CM}	Common mode return loss	50 MHz to 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
V_{TXDIFF_TB-PP}	Differential peak-to-peak output voltage, transition bit (VID = 800, 1200 mV_{pp}, 5 Gbps)	R_L = 100 Ω ±1%, DEx, OSx = NC	800	1042	1200	mV
		R_L = 100 Ω ±1%, DEx = NC, OSx = GND		908		
		R_L = 100 Ω ±1%, DEx = NC, OSx = VCC		1127		
V_{TXDIFF_NTB-PP}	Differential peak-to-peak output voltage, non-transition bit (VID = 800, 1200 mV_{pp}, 5 Gbps)	R_L = 100 Ω ±1%, DEx = NC, OSx = 0, 1, NC		1042		mV
		R_L = 100 Ω ±1%, DEx = 0, OSx = 0, 1, NC		661		
		R_L = 100 Ω ±1%, DEx = 1, OSx = 0, 1, NC		507		
DE	De-emphasis level OS1, 2 = NC (for OS1, 2 = 1 and 0, see Table 4)	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0 (SN65LVPE502A, RLL package)		–3.5		
		DE1/DE2 = 0 (SN65LVPE502x, RGE packages)	–3	–3.5	–4	
		DE1/DE2 = 1		–6		
T_{DE}	De-emphasis width			0.85		UI
Z_{diff_TX}	DC differential impedance		72	90	120	Ω
Z_{CM_TX}	DC common mode impedance	Measured w.r.t to AC ground over 0 V to 500 mV	18	23	30	Ω
RL_{diff_TX}	Differential return loss	f = 50 MHz to 1.25 GHz	9	10		dB
		f = 1.25 GHz to 2.5 GHz	6	7		
RL_{CM_TX}	Common mode return loss	f = 50 MHz to 2.5 GHz	11	12		dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND			60	mA
$V_{TX\_CM\_DC}$	Transmitter DC common mode voltage	OSx = NC	2	2.6	3	V
$V_{TX\_CM\_AC\_Active}$	TX AC common mode voltage active			30	100	mV_{pp}
VTX_idle_diff-AC_{pp}	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mV_{pp}

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TX\_CM\_DeltaU1-U0}$	Absolute delta of DC CM voltage during active and idle states			35	200	mV
$V_{TX\_idle\_diff-DC}$	DC Electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise and fall time	20% to 80% of differential voltage measured 1 in. from the output pin	30	65		ps
t_{RF_MM}	Output rise and fall time mismatch	20% to 80% of differential voltage measured 1 in. from the output pin		1.5	20	ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	De-emphasis = –3.5 dB (CH 0 and CH 1), propagation delay between 50% level at input and output		305	370	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times	See Figure 2		4	6	ns
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
JITTER						
T_{TX-EYE} (1)(2)	Total jitter (Tj) at point A	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.23	0.5	UI_{pp} (3)
DJ_{TX} (2)	Deterministic jitter (Dj)	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.14	0.3	UI_{pp} (3)
RJ_{TX} (2)(4)	Random jitter (Rj)	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.08	0.2	UI_{pp} (3)
T_{TX-EYE} (1)(2)	Total jitter (Tj) at point B	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7 dB		0.15	0.5	UI_{pp} (3)
DJ_{TX} (2)	Deterministic jitter (Dj)	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7 dB		0.07	0.3	UI_{pp} (3)
RJ_{TX} (2)(4)	Random jitter (Rj)	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7 dB		0.08	0.2	UI_{pp} (3)

(1) Includes RJ at 10^{-12} BER.
(2) Deterministic jitter measured with K28.5 pattern and Random jitter measured with K28.5 pattern at the ends of reference channel in Figure 5, VID = 1000 mV_{pp}, 5 Gbps, and –3.5 dB DE from source.
(3) UI = 200 ps
(4) Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER.

6.6 Dissipation Ratings

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX (1)	UNIT
P_D	Device power dissipation	RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 mV_{pp}		330	450	mW
P_{Slp}	Device power dissipation in sleep mode	EN_RXD = GND		0.03	0.4	mW

(1) The maximum rating is simulated under 3.6 V VCC. Device power: the SN65LVPE502x is designed to operate from a single, 3.3-V supply.

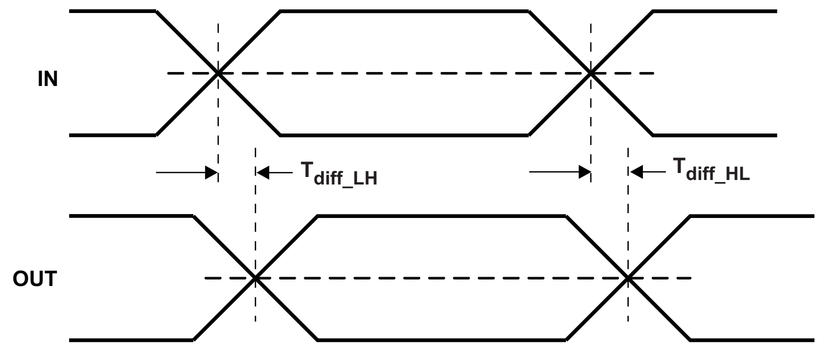


Figure 1. Propagation Delay

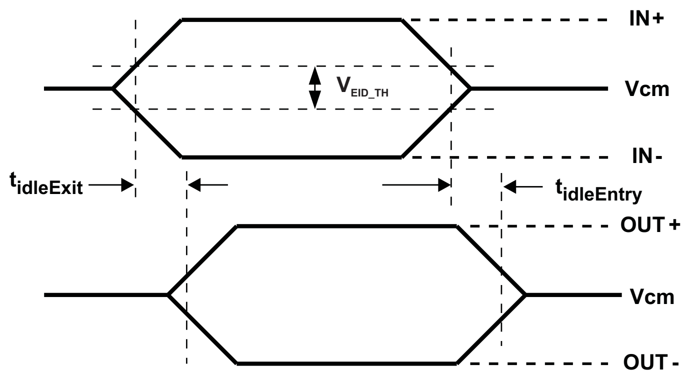


Figure 2. Electrical Idle Mode Exit and Entry Delay

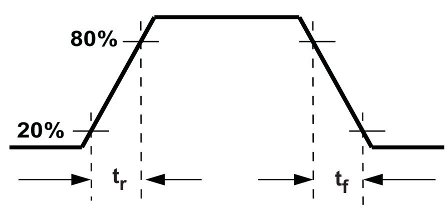


Figure 3. Output Rise and Fall Times

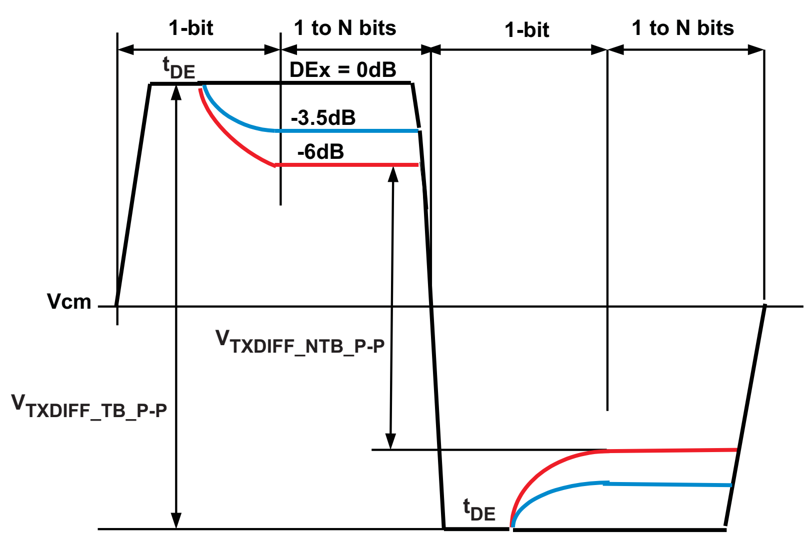


Figure 4. Output De-Emphasis Levels OSx = NC

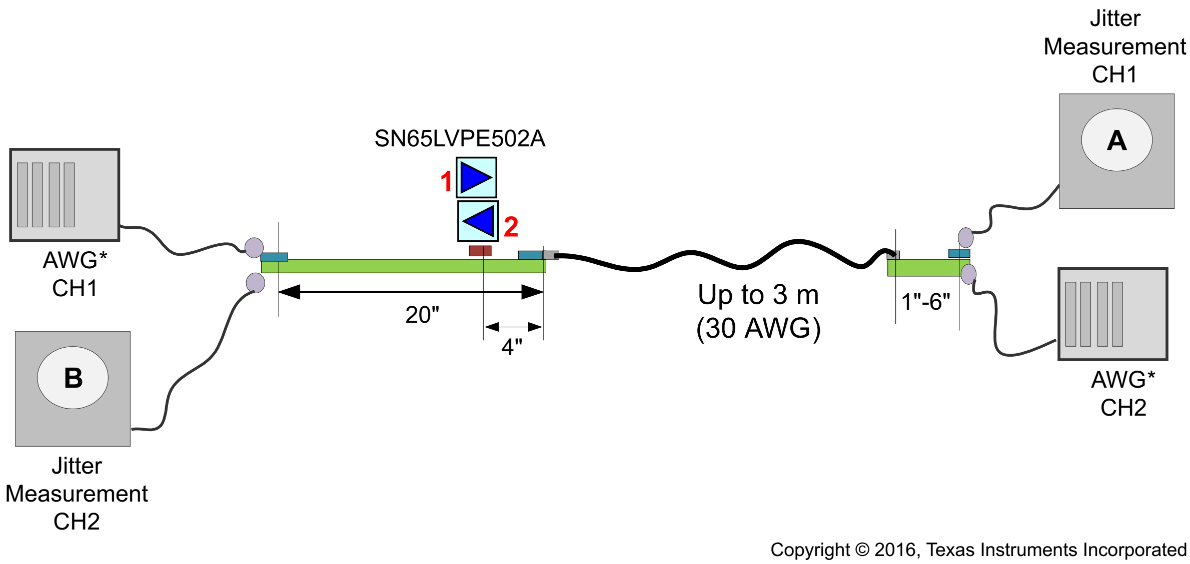
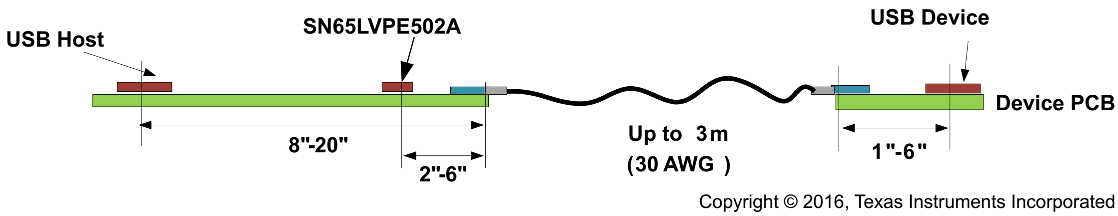


Figure 5. Jitter Measurement Setup



For more detailed placement example of redriver, see *Typical Characteristics*.

Figure 6. Redriver Placement Example

6.7 Typical Characteristics

Table 1. Case I Fixed Output and Variable Input Trace (3-m Cable)

GRAPH TITLE	FIGURE
DE = 0 dB, EQ = 0 dB, Input = 4 in., Output = 4 in., and 3-m Cable	Figure 7
DE = 0 dB, EQ = 0 dB, Input = 8 in., Output = 4 in., and 3-m Cable	Figure 8
DE = 0 dB, EQ = 0 dB, Input = 12 in., Output = 4 in., and 3-m Cable	Figure 9
DE = 0 dB, EQ = 0 dB, Input = 16 in., Output = 4 in., and 3-m Cable	Figure 10
DE = 0 dB, EQ = 0 dB, Input = 20 in., Output = 4 in., and 3-m Cable	Figure 11
DE = 0 dB, EQ = 7 dB, Input = 24 in., Output = 4 in., and 3-m Cable	Figure 12
DE = 0 dB, EQ = 7 dB, Input = 32 in., Output = 4 in., and 3-m Cable	Figure 13
DE = 0 dB, EQ = 7 dB, Input = 36 in., Output = 4 in., and 3-m Cable	Figure 14
DE = 0 dB, EQ = 15 dB, Input = 36 in., Output = 4 in., and 3-m Cable	Figure 15
DE = 0 dB, EQ = 15 dB, Input = 48 in., Output = 4 in., and 3-m Cable	Figure 16

Table 2. Case II Fixed Input and Variable Output Trace (3-m Cable)

GRAPH TITLE	FIGURE
DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 4 in., and 3-m Cable	Figure 17
DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 8 in., and 3-m Cable	Figure 18
DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 12 in., and 3-m Cable	Figure 19
DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 16 in., and 3-m Cable	Figure 20
DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 20 in., and 3-m Cable	Figure 21

Table 3. Case III Fixed Input and Variable Output Trace (No Cable)

GRAPH TITLE	FIGURE
DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 8 in.	Figure 22
DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 32 in.	Figure 23
DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 36 in.	Figure 24
DE = –3.5 dB, EQ = 7 dB, Input = 12 in., and Output = 36 in.	Figure 25
DE = –6 dB, EQ = 7 dB, Input = 12 in., and Output = 40 in.	Figure 26
DE = –6 dB, EQ = 7 dB, Input = 12 in., and Output = 44 in.	Figure 27

6.7.1 Case I – Fixed Output, Variable Input Trace, and 3-m Cable

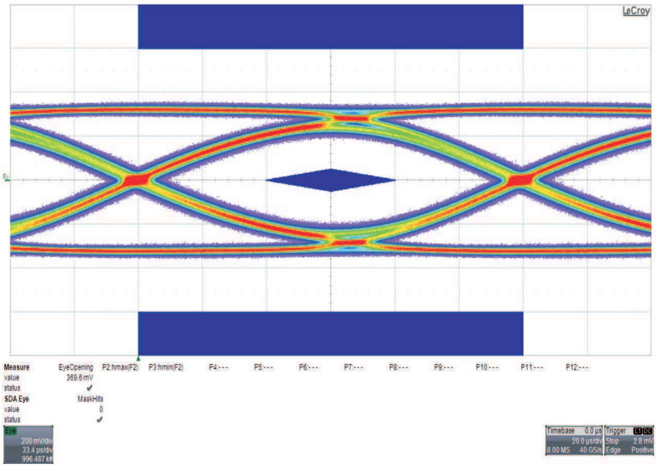


Figure 7. DE = 0 dB, EQ = 0 dB, Input = 4 in., Output = 4 in., and 3-m Cable

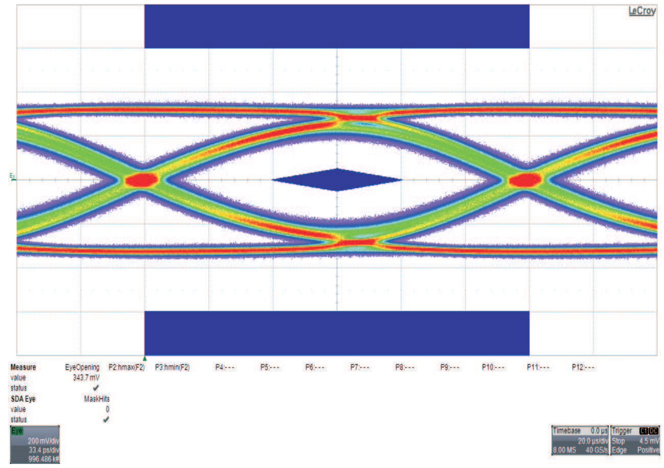


Figure 8. DE = 0 dB, EQ = 0 dB, Input = 8 in., Output = 4 in., and 3-m Cable

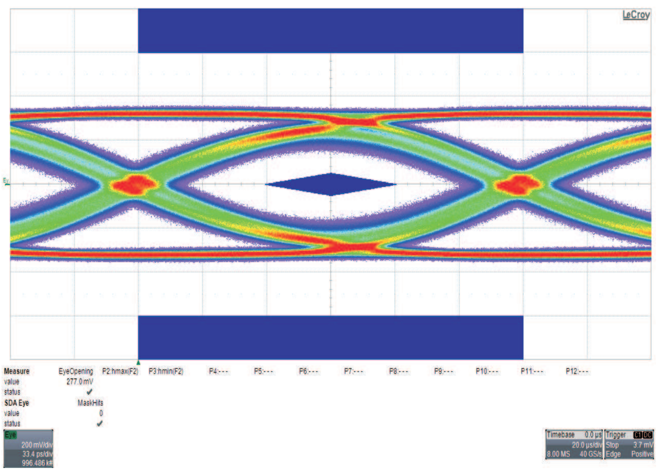


Figure 9. DE = 0 dB, EQ = 0 dB, Input = 12 in., Output = 4 in., and 3-m Cable

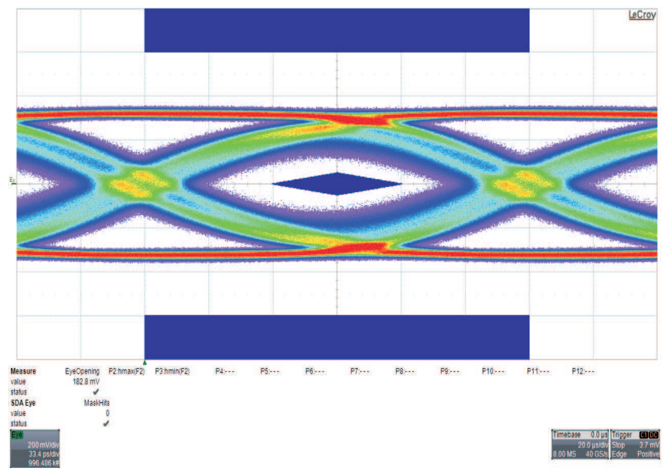


Figure 10. DE = 0 dB, EQ = 0 dB, Input = 16 in., Output = 4 in., and 3-m Cable

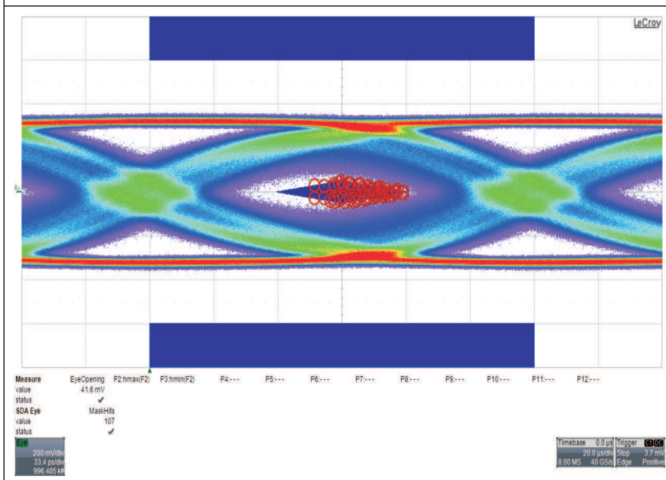


Figure 11. DE = 0 dB, EQ = 0 dB, Input = 20 in., Output = 4 in., and 3-m Cable

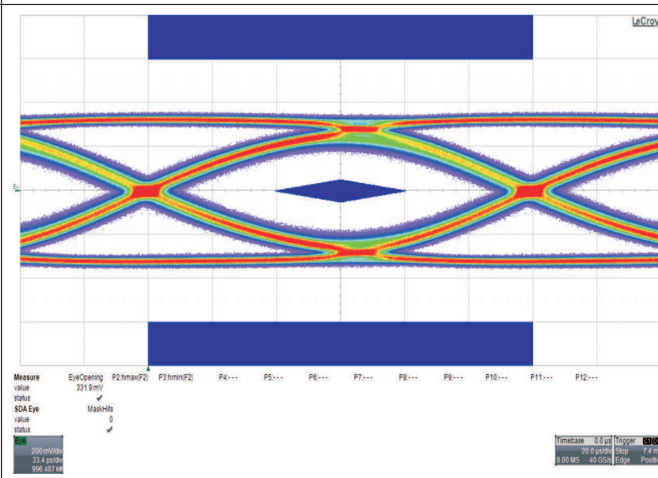


Figure 12. DE = 0 dB, EQ = 7 dB, Input = 24 in., Output = 4 in., and 3-m Cable

Case I – Fixed Output, Variable Input Trace, and 3-m Cable (continued)

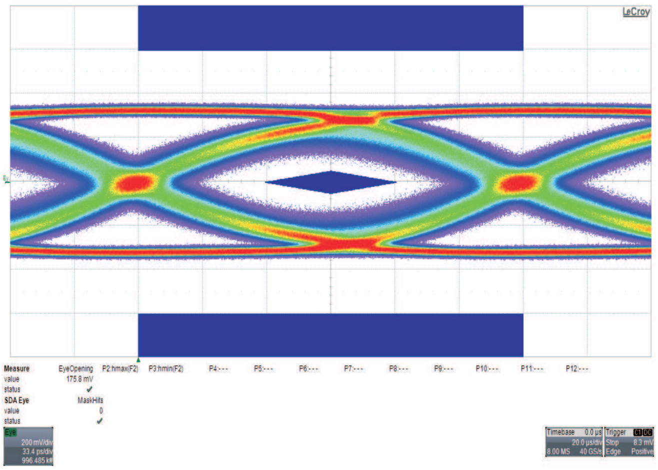


Figure 13. DE = 0 dB, EQ = 7 dB, Input = 32 in., Output = 4 in., and 3-m Cable

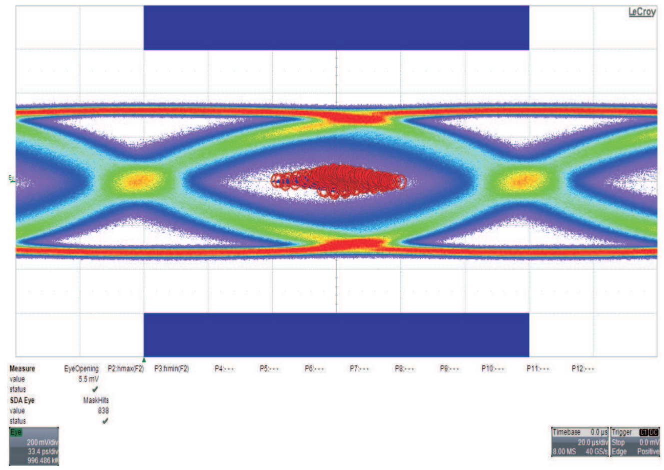


Figure 14. DE = 0 dB, EQ = 7 dB, Input = 36 in., Output = 4 in., and 3-m Cable

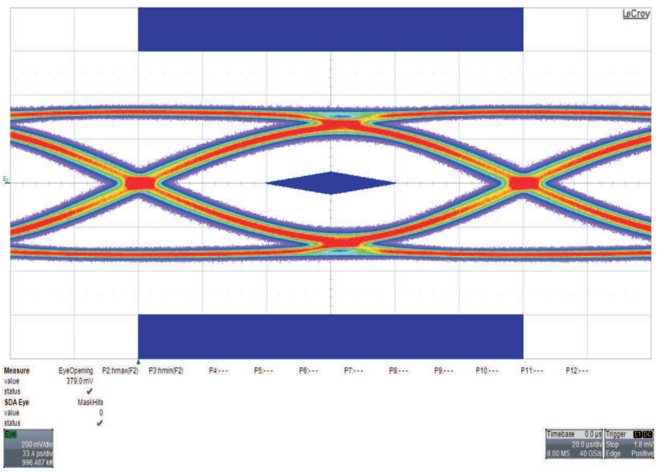


Figure 15. DE = 0 dB, EQ = 15 dB, Input = 36 in., Output = 4 in., and 3-m Cable

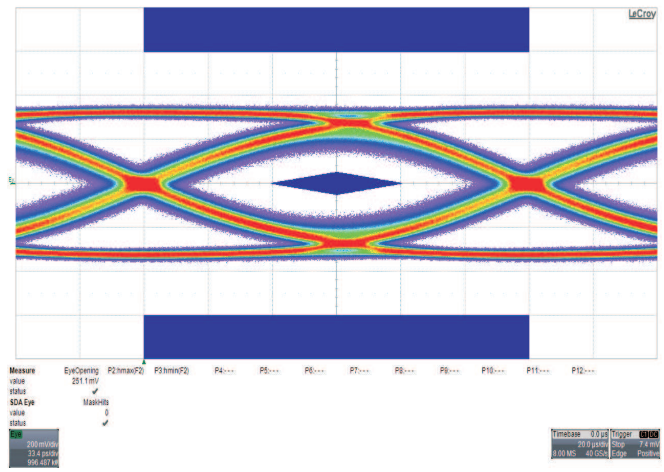


Figure 16. DE = 0 dB, EQ = 15 dB, Input = 48 in., Output = 4 in., and 3-m Cable

6.7.2 Case II – Fixed Input, Variable Output Trace, and 3-m Cable

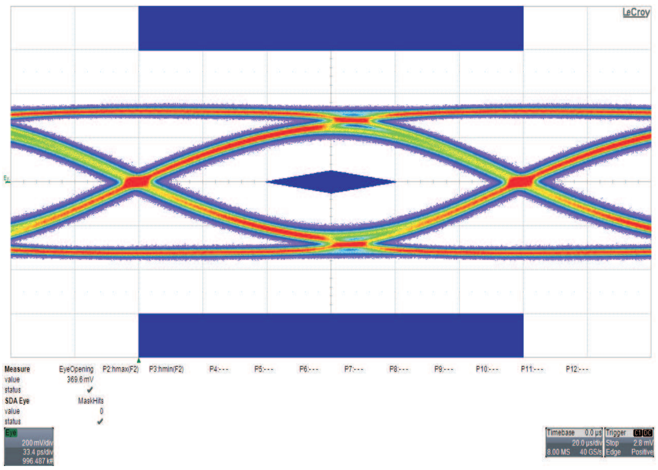


Figure 17. DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 4 in., and 3-m Cable

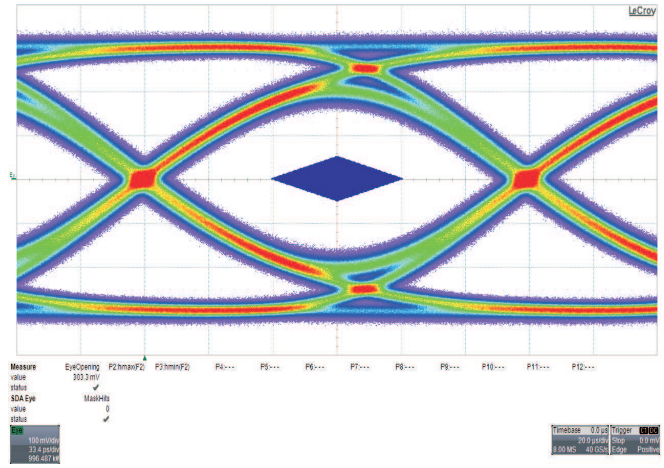


Figure 18. DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 8 in., and 3-m Cable

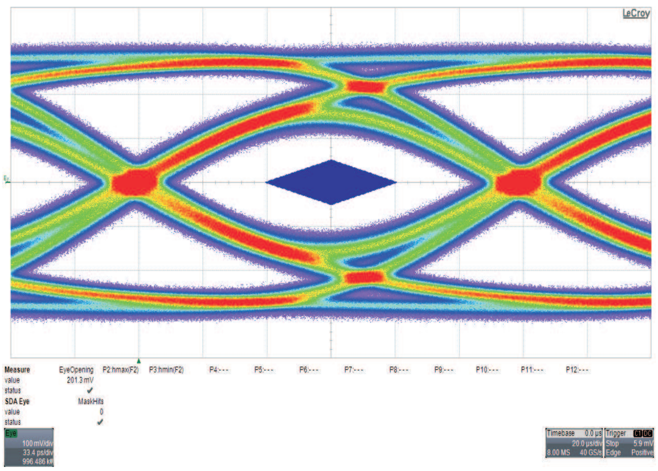


Figure 19. DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 12 in., and 3-m Cable

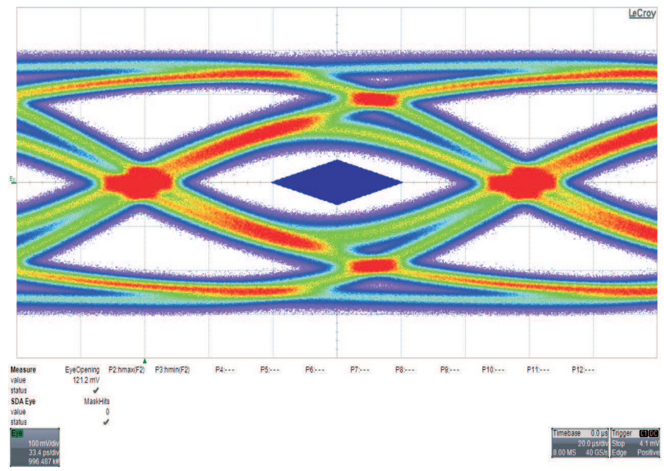


Figure 20. DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 16 in., and 3-m Cable

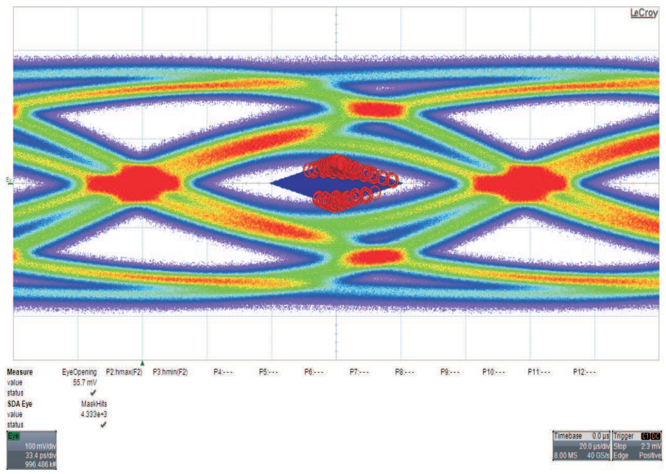


Figure 21. DE = 0 dB, EQ = 7 dB, Input = 12 in., Output = 20 in., and 3-m Cable

6.7.3 Case III – Fixed Input and Variable Output Trace (No Cable)

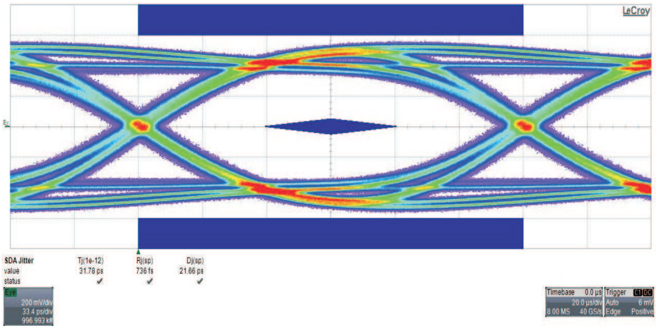


Figure 22. DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 8 in.

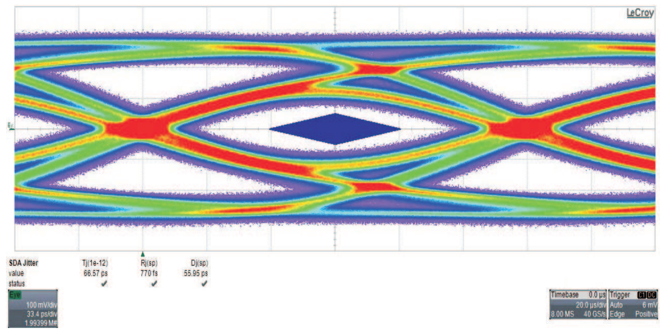


Figure 23. DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 32 in.

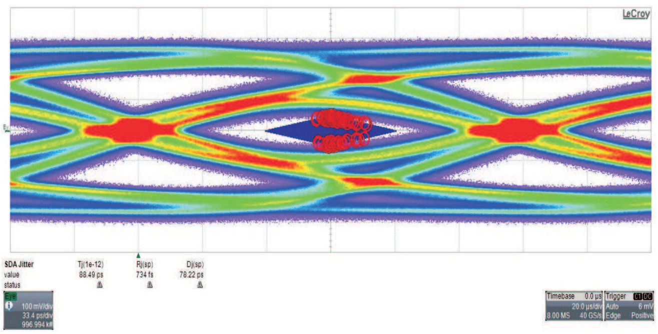


Figure 24. DE = 0 dB, EQ = 7 dB, Input = 12 in., and Output = 36 in.

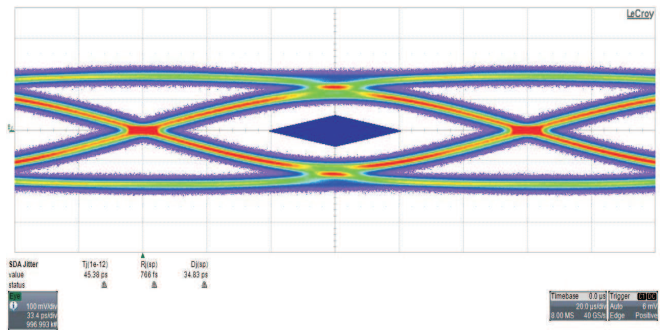


Figure 25. DE = –3.5 dB, EQ = 7 dB, Input = 12 in., and Output = 36 in.

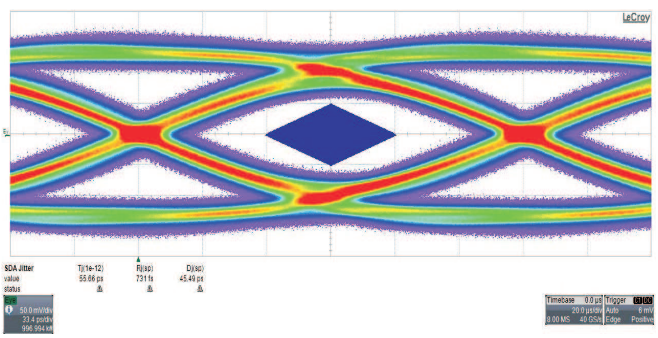


Figure 26. DE = –6 dB, EQ = 7 dB, Input = 12 in., and Output = 40 in.

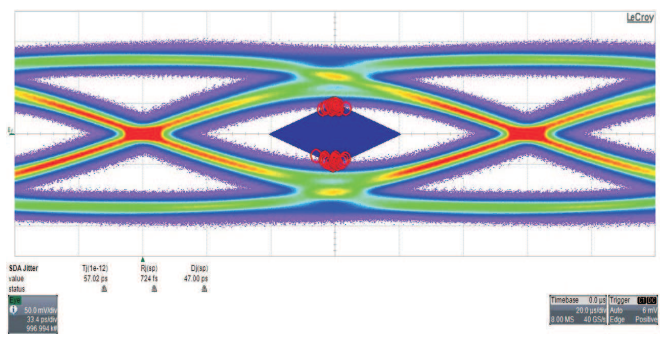


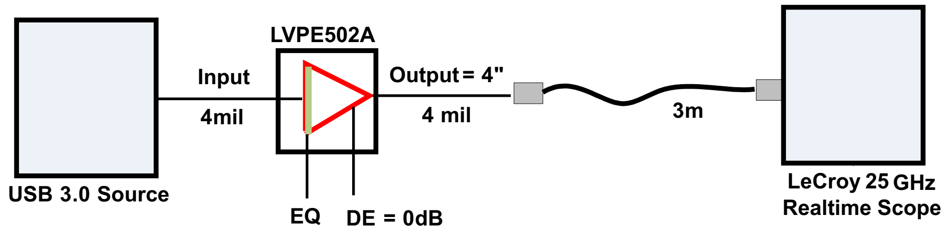
Figure 27. DE = –6 dB, EQ = 7 dB, Input = 12 in., and Output = 44 in.

7 Parameter Measurement Information

7.1 Typical Eye Diagram and Performance Curves

Device operating conditions: VCC = 3.3 V, temperature = 25°C, EQx, DEx, and OSx set to their default values (when not mentioned). Measurement equipment details:

- Generator (source) LeCroy PERT3
- Signal: 5 Gbps, 1000 mV_{pp}, 3.5 dB de-emphasis
- Tj and Dj measurements based on CP0 (USB 3.0 compliance pattern) which is D0.0 or logical idle with SKP sequences removed
- Rj measurements based on CP1 or D10.2 symbol containing alternating 0s and 1s at Nyquist frequency
- Oscilloscope (sink) LeCroy 25-GHz real-time oscilloscope
- LeCroy QualiPHY software used to measure jitter and collect compliance eye diagrams



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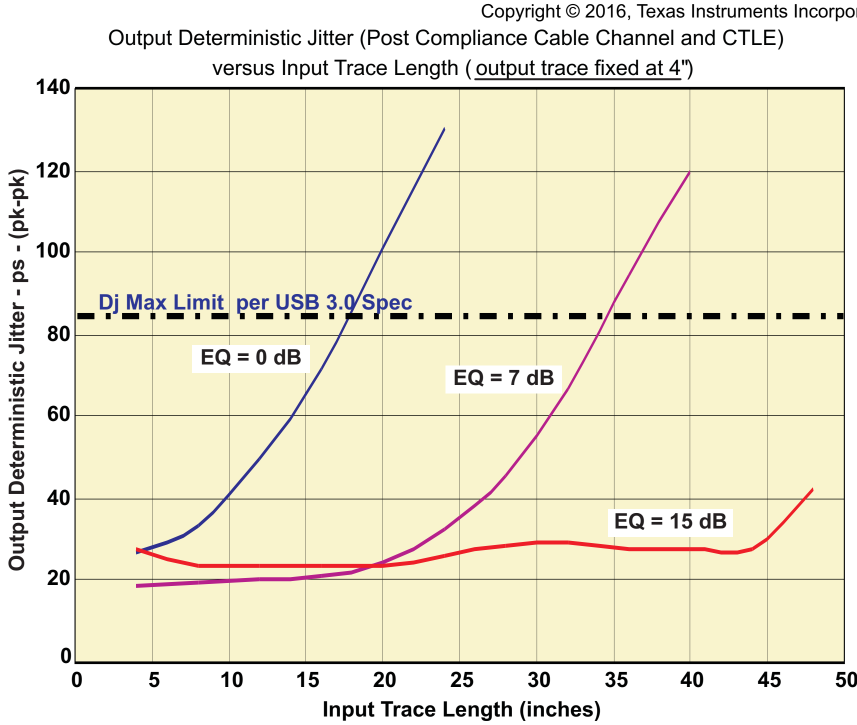


Figure 28. Plot 1 – Fixed Output Trace With Variable Input Trace and 3-m USB 3.0 Cable

Typical Eye Diagram and Performance Curves (continued)

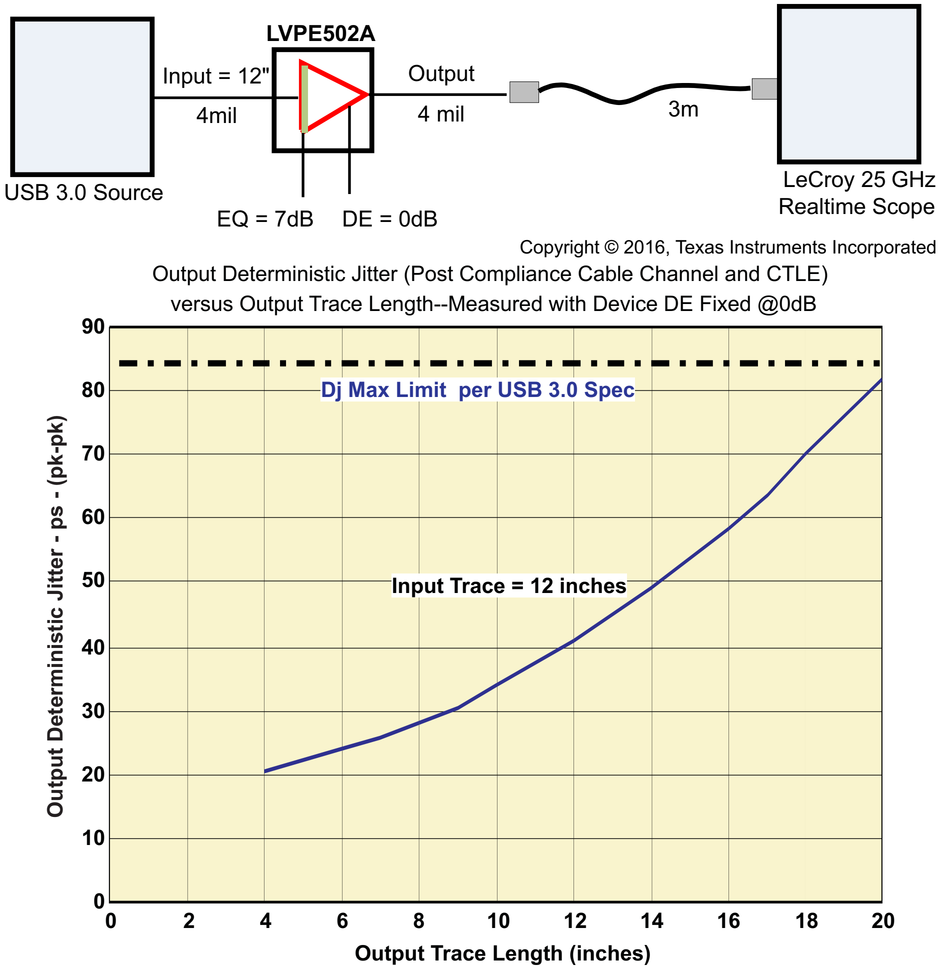


Figure 29. Plot 2 – Fixed Input Trace With Variable Output Trace and 3-m USB 3.0 Cable

Typical Eye Diagram and Performance Curves (continued)

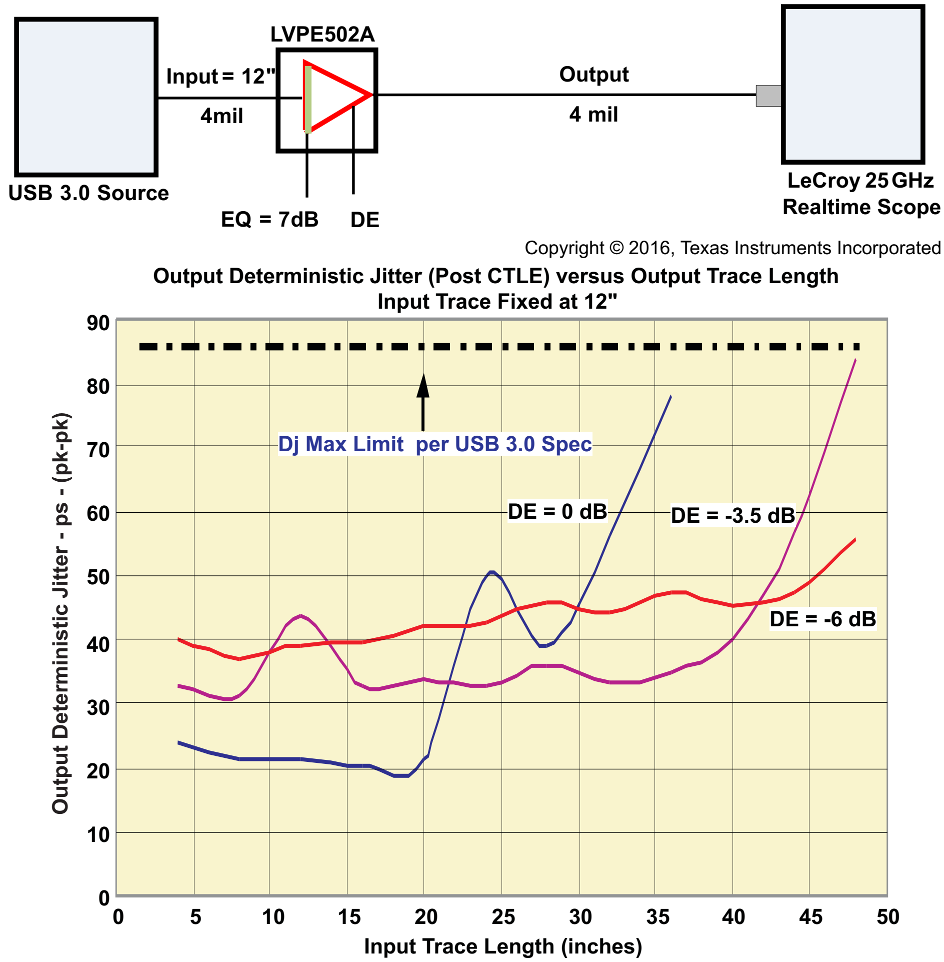


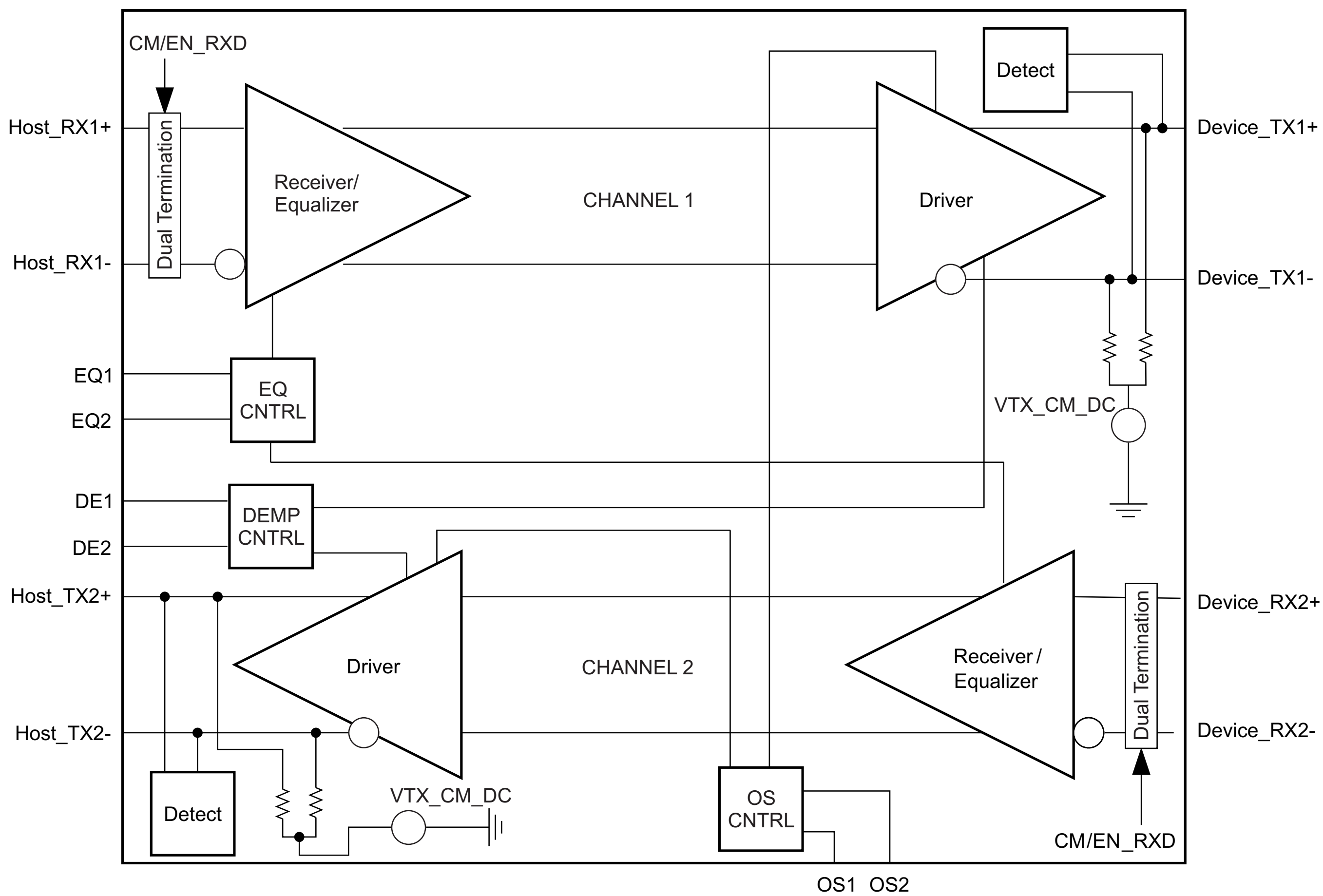
Figure 30. Plot 3 – Fixed Input Trace With Variable Output Trace (No Cable)

8 Detailed Description

8.1 Overview

When 5-Gbps SuperSpeed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference (ISI). The SN65LVPE502x devices recover incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.0 compliance. The SN65LVPE502x is located at the *Host* side. After power up, the SN65LVPE502x periodically performs receiver detection on the TX pair. If it detects a SuperSpeed USB receiver, the RX termination is enabled, and the SN65LVPE502x is ready to redrive. The receiver equalizer has three gain settings that are controlled by terminal EQ: 0 dB, 7 dB, and 15 dB. The equalization must be set based on amount of insertion loss in the channel before the SN65LVPE502x. Likewise, the output driver supports configuration of de-emphasis and output swing (terminals DE and OS).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Host- and Device-Side Pins

The SN65LVPE502x features a link state machine that makes the device transparent on the USB 3.0 bus while minimizing power. The state machine relies on the system host to be connected to the pins named *Host*. USB 3.0 devices must be connected to the pins named *Device*. Multiple SN65LVPE502x devices may be used in series.

Feature Description (continued)

8.3.2 Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE502x is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for any anticipated USB 3.0 signal distortion experienced. The level of de-emphasis depends on the length of interconnect and its characteristics. The SN65LVPE502x provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All RX and TX equalization settings supported by the device are programmed by six 3-state pins as shown in Table 4.

Table 4. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (AT 2.5 GHz)			
OSx(1)	**TRANSISTION BIT AMPLITUDE, TYPICAL (mV_{pp})**	**EQx(1)**	**EQUALIZATION (dB)**
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (AT 2.5 GHz)			
DEx(1)	**OSx(1) = NC**	**OSx(1) = 0**	**OSx(1) = 1**
NC (default)	0 dB	0 dB	0 dB
0	–3.5 dB	–2.2 dB	–4.4 dB
1	–6 dB	–5.2 dB	–6 dB

(1) Where x = Channel 1 or Channel 2

8.3.3 Receiver Detection

8.3.3.1 At Power Up or Reset

After power-up or anytime EN_RXD is toggled, RX.Detect cycle is performed by first setting RX termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If the receiver is detected on both channel, the TX and RX terminations are switched to Z_{DIFF_TX}, Z_{DIFF_RX} respectively.

If no receiver is detected on one or both channels, the transmitter is pulled to Hi-Z; the channel is put in low-power mode; and the device attempts to detect RX termination in 12 ms (typical) interval until termination is found or device is put in sleep mode.

8.3.3.2 During U2/U3 Link State

RX detection is also performed periodically when link is in U2/U3 states. However in these states during RX detection, input termination is not automatically disabled before performing RX.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power-up RX.Detect state.

8.3.4 Electrical Idle Support

Electrical idle support is required for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. SN65LVPE502x detects an electrical idle state when RX± voltage at the device pin falls below $VRX\_LFPS\_DIFF_{pp}$ minimum. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds $VRX\_LFPS\_DIFF_{pp}$ maximum normal operation is restored and output start passing input signal. Electrical idle exit and entry time is specified at <6 ns.

8.4 Device Functional Modes

8.4.1 Active Mode

This operating mode is enabled when EN_RXD is driven to VCC and the device has successfully detected the connection with *Host* and *Device*, the redriver applies the desired equalization to the inputs, and drives the output with the selected output swing and de-emphasis.

8.4.2 Low-Power Modes

Device supports three low-power modes as described in *Sleep Mode*, *RX Detect Mode*, and *U2/U3 Mode*.

8.4.2.1 Sleep Mode

Initiated anytime EN_RXD undergoes a high to low transition and stays low or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode maximum current consumption is 0.1 mA. Entry time is 2 µs, the device exits sleep mode to Rx.Detect mode after EN_RXD is driven to VCC, and exit time is 100 µs maximum. Table 5 lists the control pin settings for sleep mode.

Table 5. Control Pin Settings

EN_RXD	DEVICE FUNCTION
1 (default)	Normal operation
0	Sleep mode

8.4.2.2 RX Detect Mode

This mode is only achievable when no remote device is connected.

Anytime SN65LVPE502x detects a break in link (that is, when upstream device is disconnected) or after power up fails to find a remote device, SN65LVPE502x goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode, the input termination for both channels is driven to Hi-Z. In Rx Detect mode the maximum device current consumption is 5mA, which is about the 5% of its normal operating power. This feature is useful in saving system power in mobile applications, such as notebook PCs, where battery life is critical. Anytime an upstream device gets reconnected, the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

8.4.2.3 U2/U3 Mode

With the help of internal timers, the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes, link is in electrical idle state. SN65LVPE502x selectively turns off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device automatically reverts to active mode when signal activity (LFPS) is detected.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

One example of the SN65LVPE502x used in a *Host* application on transmit and receive channels is shown in *Typical Application*. The redriver is required on the PCB path to pass transmitter compliance due to loss between the *Host* and connector. The redriver uses its equalization to recover the insertion loss and re-drive the signal with boosted swing down the remaining channel, through the USB 3.0 cable, and into the device PCB. Additionally on the receiver path, the SN65LVPE502x compensated for the *Host* to pass receiver jitter tolerance. The redriver recovers the loss from the device PCB, connector, and USB 3.0 cable and redrives the signal going into the *Host* receiver. The equalization, output swing, and de-emphasis settings are dependent upon the type of USB 3.0 signal path and end application.

9.2 Typical Application

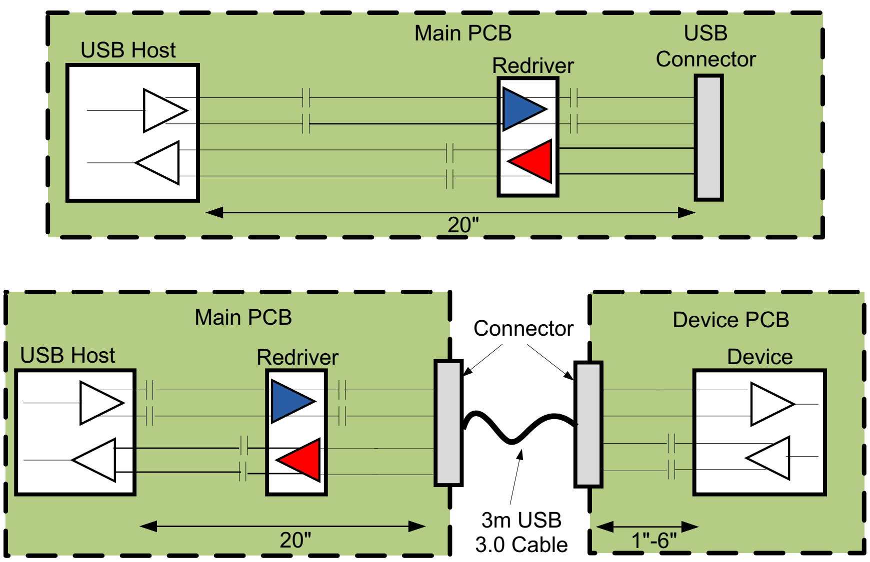


Figure 31. Typical Application Schematic

9.2.1 Design Requirements

Table 6 lists the parameters for this example.

Table 6. Application Parameters

PARAMETER	VALUE
Input voltage range	100 mV to 1200 mV
Output voltage range	1050 mV to 1200 mV
Equalization	0, 7, 15 bD (2.5 Gbps)
De-emphasis	0, –3, –5 dB (OS floating)
VCC	3.3-V nominal supply

9.2.2 Detailed Design Procedure

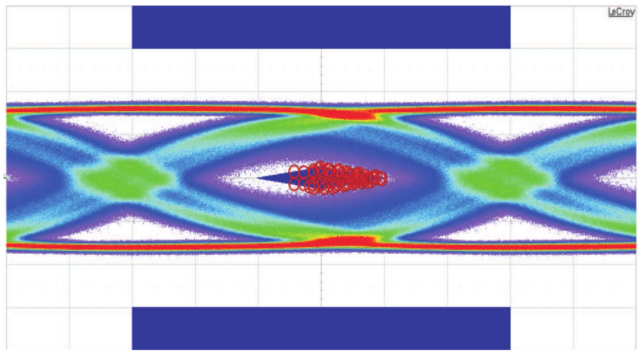
The SN65LVPE502x is placed in the *Host* side and connected to a USB3 Type-A connector. The EQ and DE terminals must be pulled up, pulled down, or left floating depending on the amount of equalization or de-emphasis that is desired. The OS terminal must be pulled down or left floating depending on the required output swing. This device has terminals to be exclusively connected to the *Host* and to the device accordingly. In this *Host* side (even though the RX and TX pairs must be AC-coupled), this is an embedded implementation and Figure 31 only shows the AC-coupling capacitors on the TX pair to follow the convention.

To begin the design process, determine the following:

- Equalization (EQ) setting
- De-emphasis (DE) setting
- Output swing amplitude (OS) setting

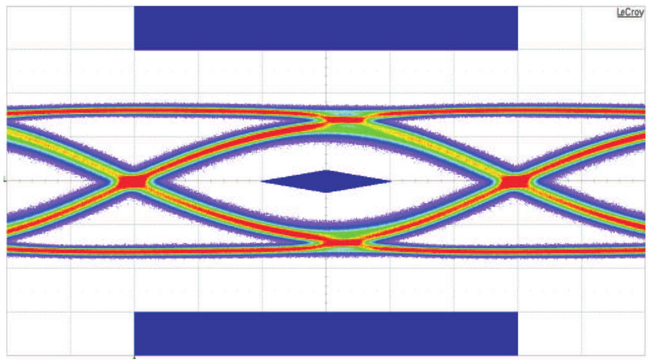
The equalization must be set based on the insertion loss in the pre-channel (channel before the SN65LVPE502x device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings. The EQ terminal can be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. The de-emphasis setting must be set based on the length and characteristics of the post channel (channel after the SN65LVPE502x device). Output de-emphasis can be tailored using the DE terminal. This terminal must be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. The output swing setting can also be configured based on the amplitude requirement to pass the compliance test. This setting is also based on the length of interconnect or cable the SN65LVPE502x is driving. This terminal must be pulled low through a resistor to ground or left floating.

9.2.3 Application Curves



Measured at device end with DE = 0 dB, EQ = 0 dB, pre-channel = 20 in., and post-channel = 4 in. plus 3-m cable

Figure 32. Eye-Mask Measured at the Device End With No Equalization



Measured at device end with DE = 0 dB, EQ = 7 dB, pre-channel = 20 in., and post-channel = 4 in. plus 3-m cable

Figure 33. Eye-Mask With 7-dB Equalization

10 Power Supply Recommendations

The SN65LVPE502x is designed to operate with a single, 3.3-V supply.

11 Layout

11.1 Layout Guidelines

1. The 100-nF capacitors on the TXP and SSTXN nets must be placed close to the USB connector (Type A, Type B, and so forth).
2. The ESD and EMI protection devices (if used) must also be placed as close as possible to the USB connector.
3. Place voltage regulators as far away as possible from the differential pairs.
4. In general, the large bulk capacitors associated with each power rail must be placed as close as possible to the voltage regulators.
5. TI recommends that small decoupling capacitors for the 1.8-V power rail be placed close to the SN65LVPE502x as shown below.
6. The SuperSpeed differential pair traces for RXP/N and TXP/N must be designed with a characteristic impedance of 90 Ω ±10%. The PCB stack-up and materials determine the width and spacing required for a characteristic impedance of 90 Ω.
7. The SuperSpeed differential pair traces must be routed parallel to each other as much as possible. TI recommends the traces be symmetrical.
8. To minimize crosstalk, TI recommends keeping high-speed signals away from each other. Each pair must be separated by at least 5 times the signal trace width. Separating with ground also helps minimize crosstalk.
9. Route all differential pairs on the same layer adjacent to a solid ground plane.
10. Do not route differential pairs over any plane split.
11. Adding test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
12. Match the etch lengths of the differential pair traces. There must be less than 5-mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs must not exceed 50-mils relative trace length difference.
13. The etch lengths of the differential pair groups do not need to match (that is, the length of the RXP/N pair to that of the TXP/N pair), but all trace lengths must be minimized.
14. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used must be placed as close as possible to the SN65LVPE502x device.
15. To ease routing, the polarity of the SS differential pairs can be swapped. This means that TXP can be routed to TXN or RXN can be routed to RXP.
16. Do not place power fuses across the differential pair traces.

11.2 Layout Example

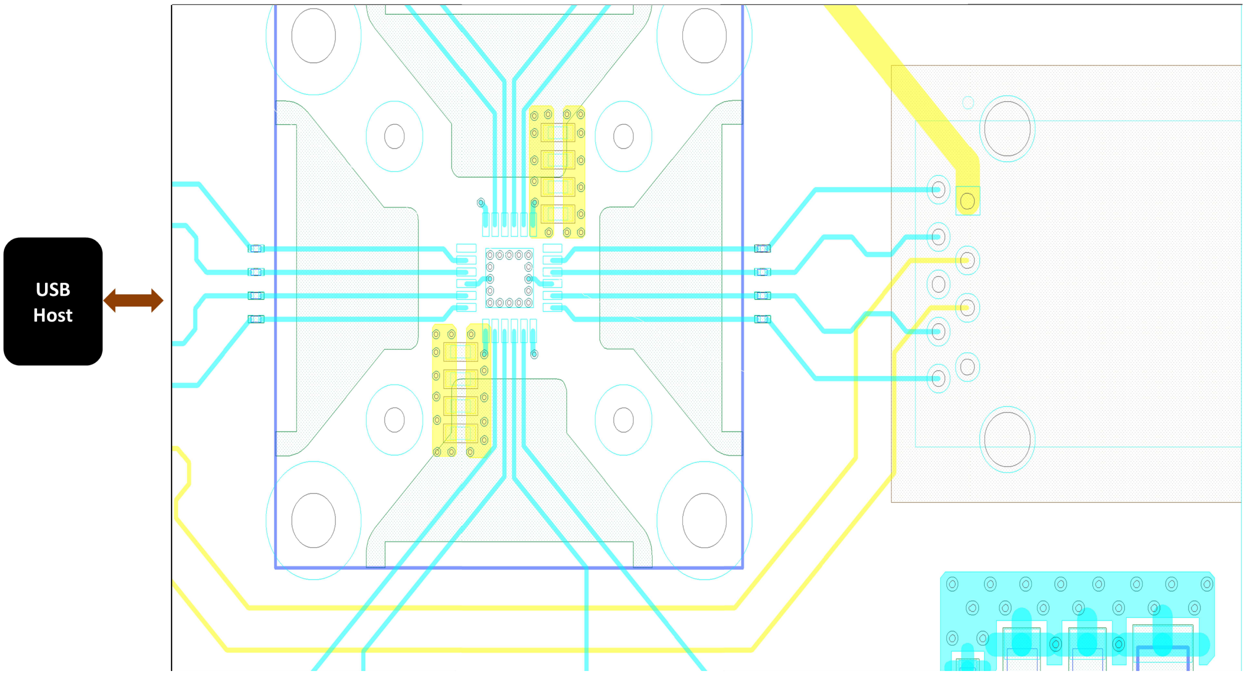


Figure 34. SN65LVPE502A USB 3.0 Signals Routing With Embedded Host and Std. Type A Connector

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

《SN65LVPE502A 至 TUSB522P 变更文档》(SLLA363)

12.2 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVPE502ARGER	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	502A
SN65LVPE502ARGER.B	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	502A
SN65LVPE502ARLLR	NRND	Production	VQFN (RLL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN502A
SN65LVPE502ARLLR.B	NRND	Production	VQFN (RLL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN502A
SN65LVPE502ARLLT	NRND	Production	VQFN (RLL) | 24	-	-	Call TI	Call TI	-40 to 85	
SN65LVPE502BRGER	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	502B
SN65LVPE502BRGER.B	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	502B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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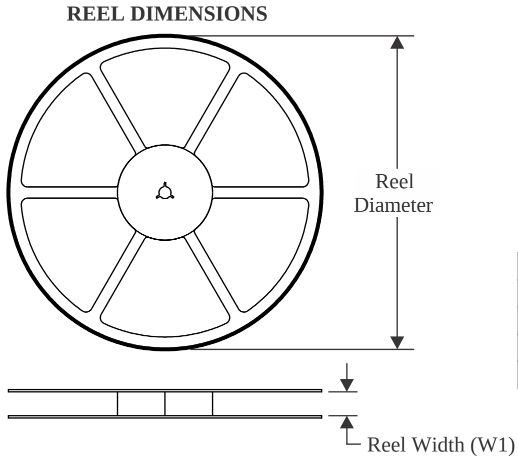
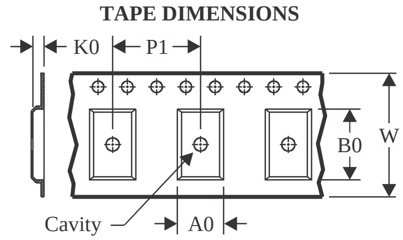
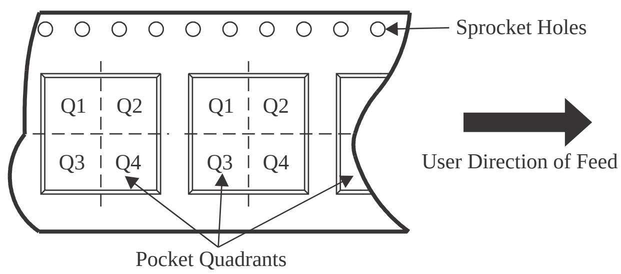
TAPE AND REEL INFORMATION





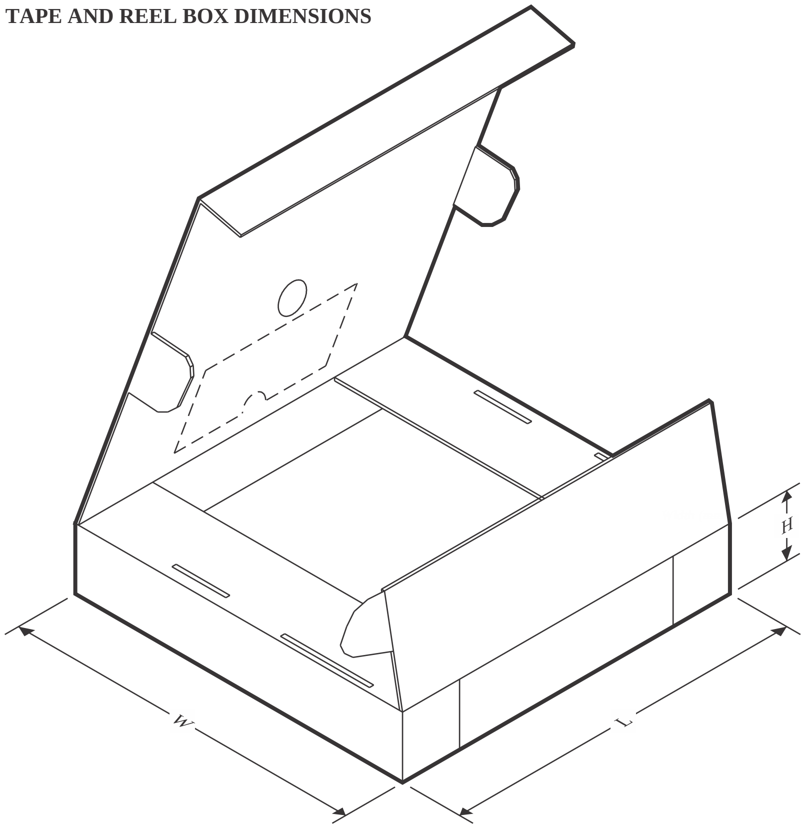
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

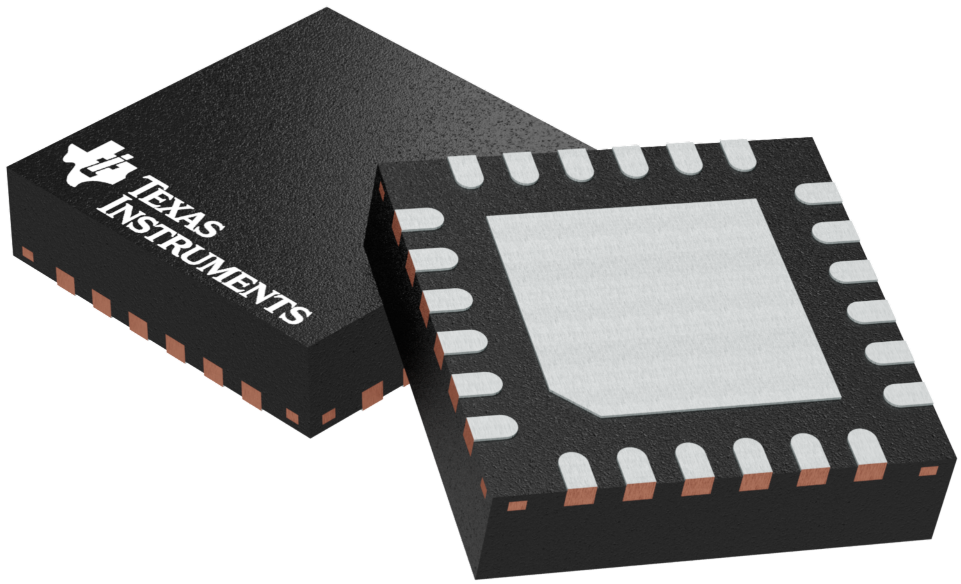
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE502ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE502ARLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65LVPE502BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

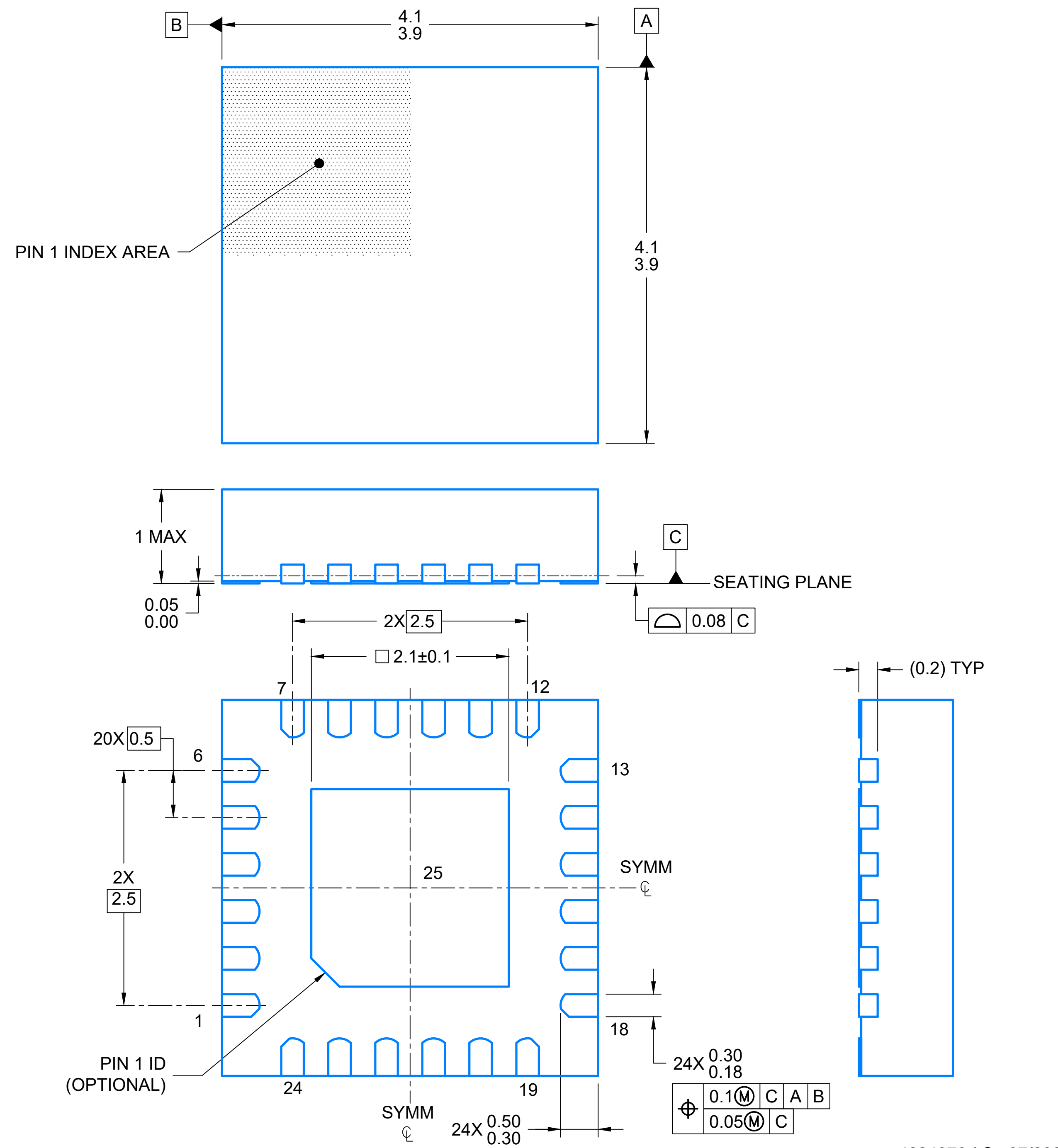


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE502ARGER	VQFN	RGE	24	3000	353.0	353.0	32.0
SN65LVPE502ARLLR	VQFN	RLL	24	3000	346.0	346.0	33.0
SN65LVPE502BRGER	VQFN	RGE	24	3000	353.0	353.0	32.0



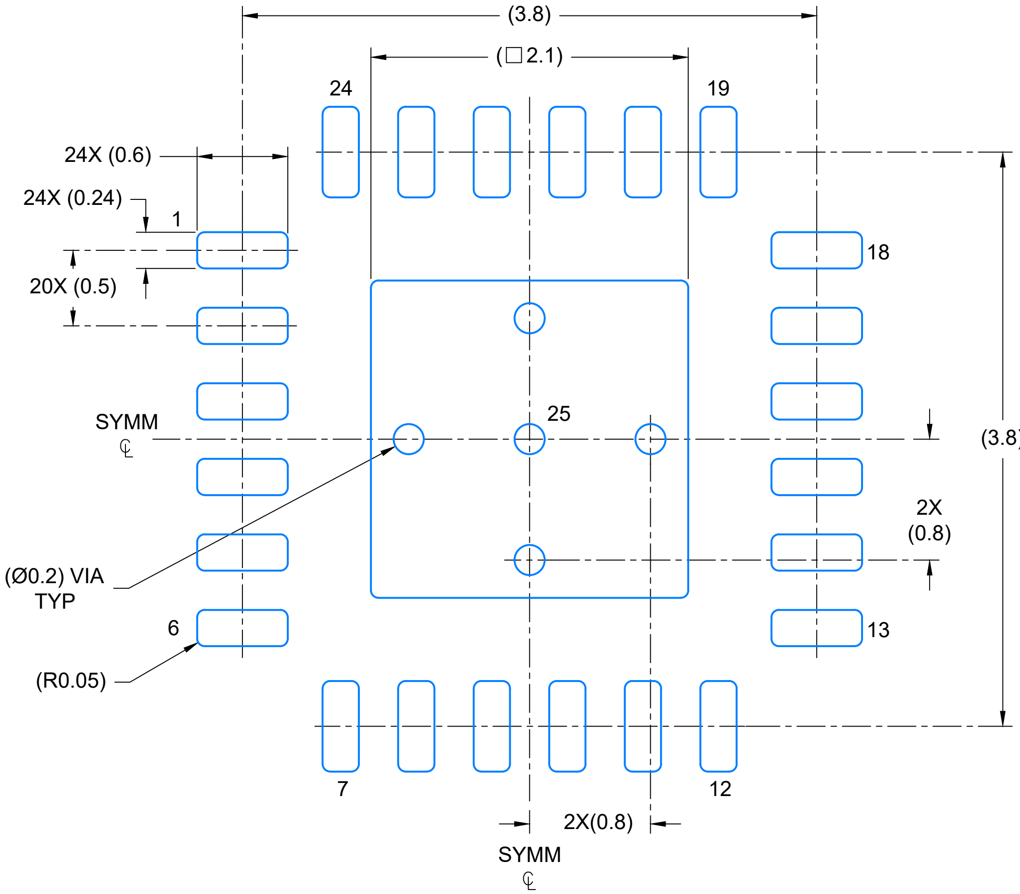
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



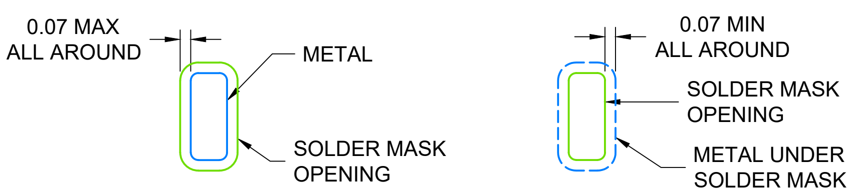
4224376 / C 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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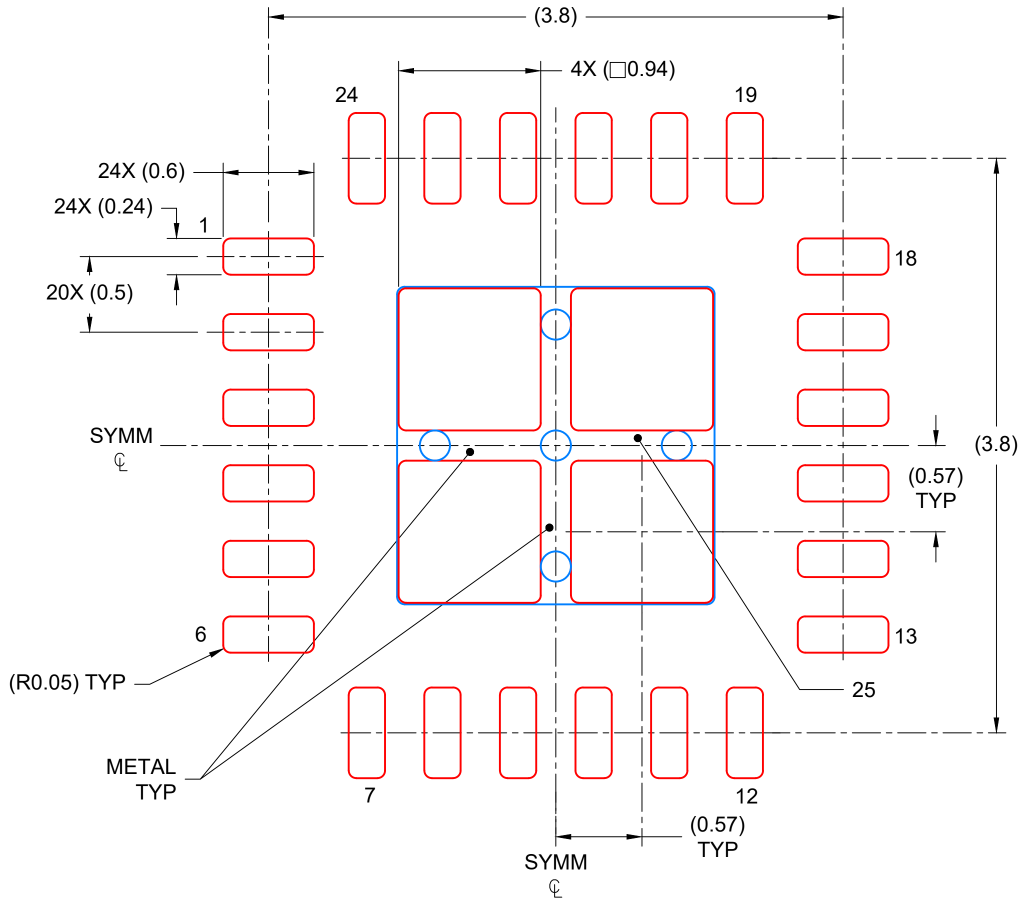
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

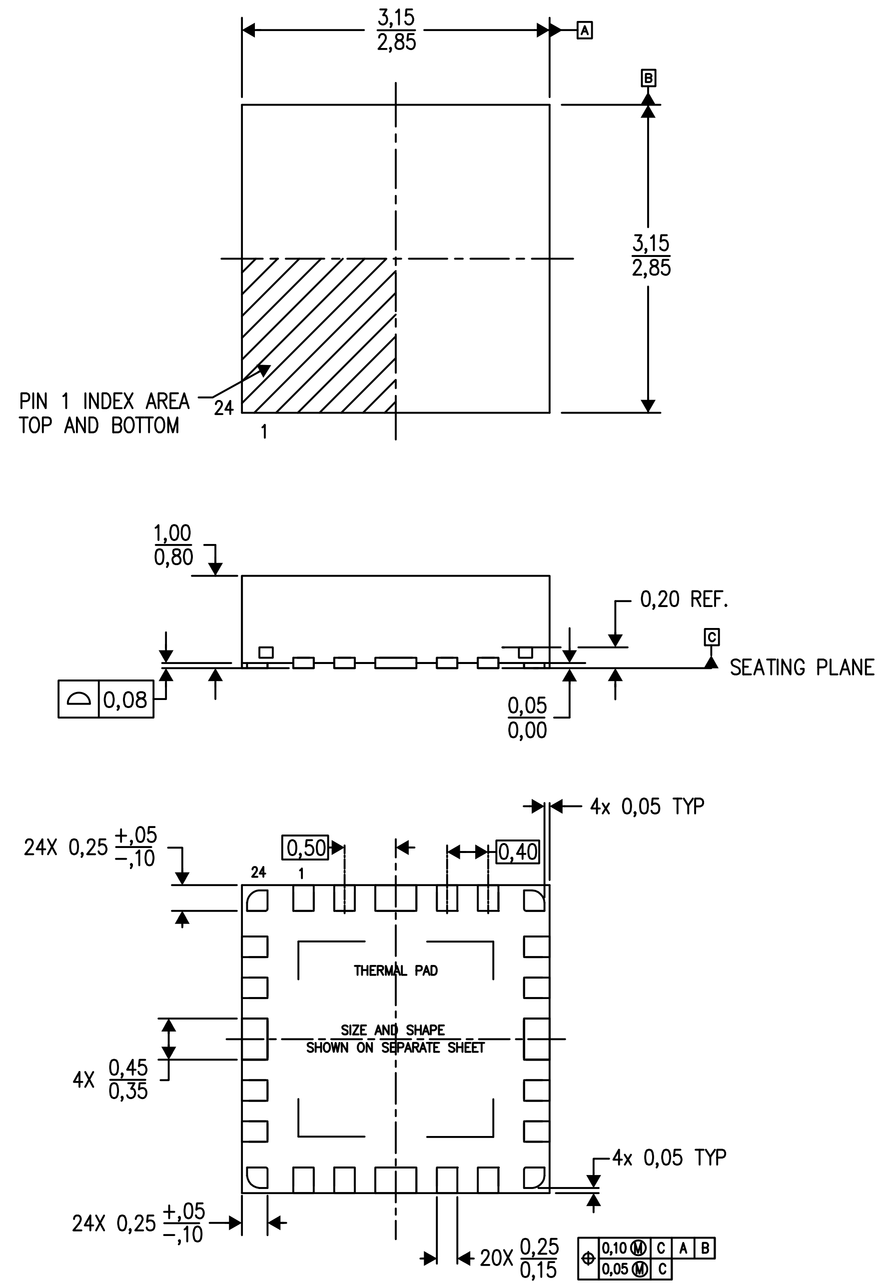
EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

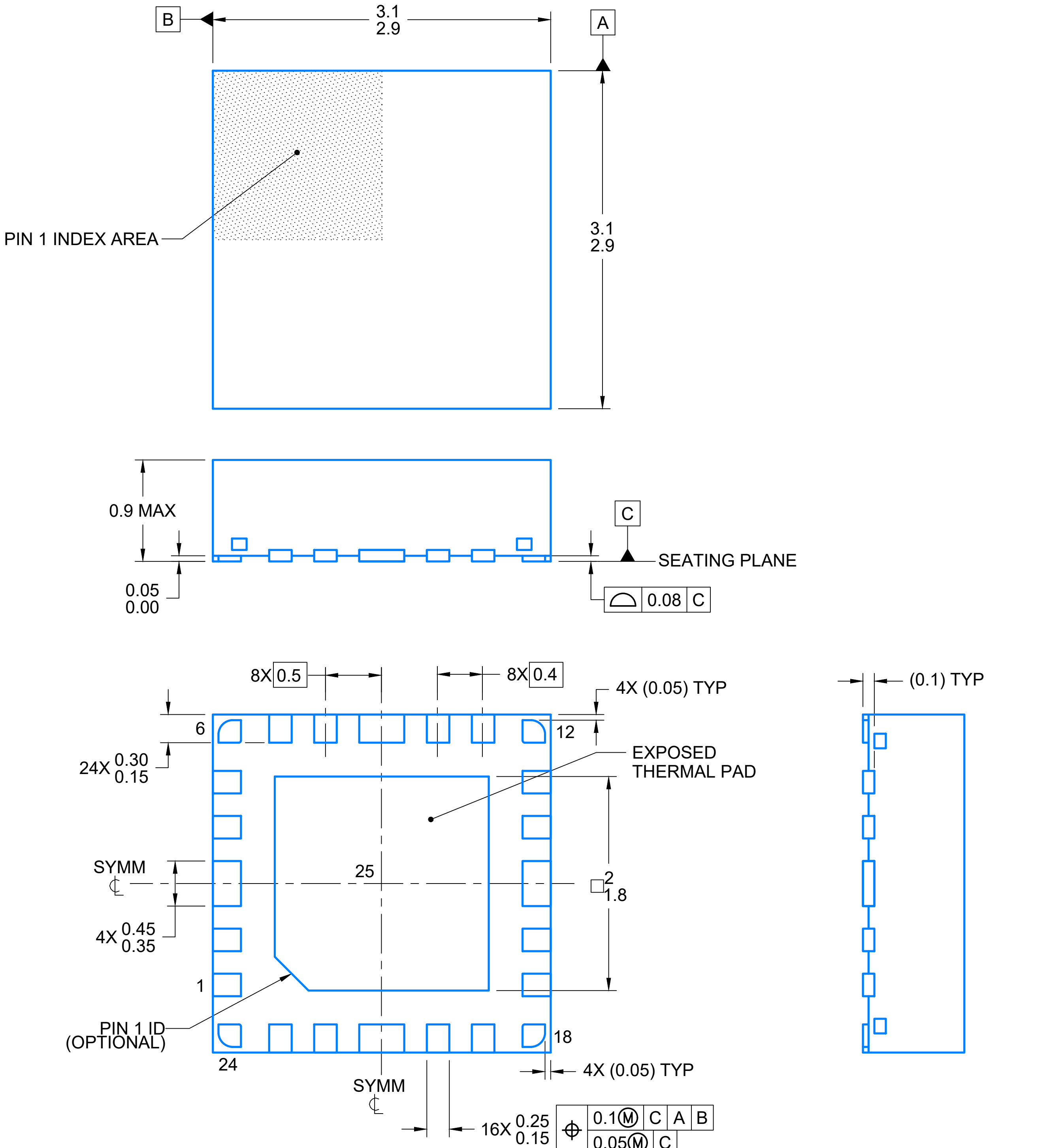
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

RLL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4214704/C 08/13

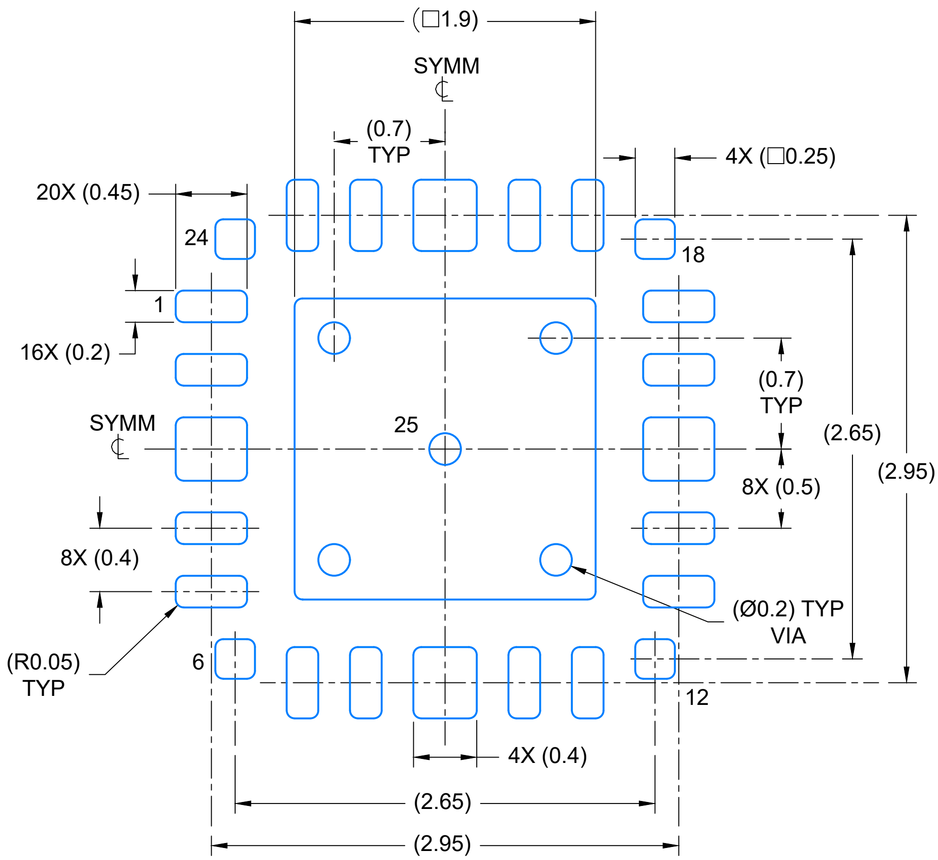
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



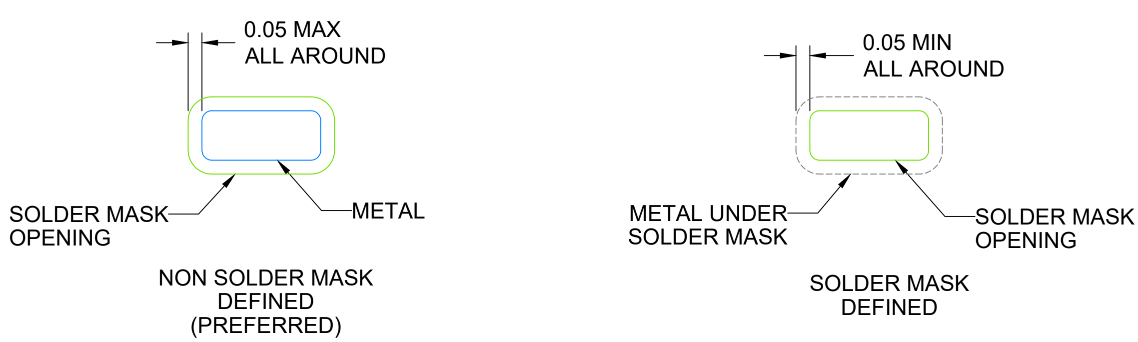
4217760 / C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

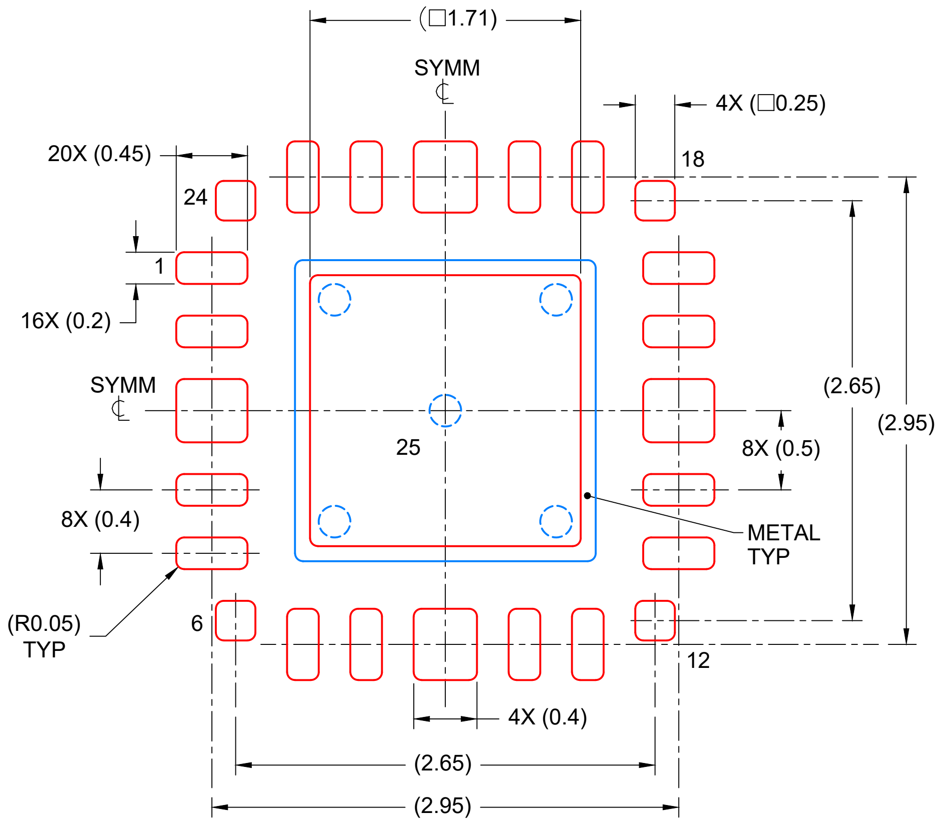


SOLDER MASK DETAILS

4217760 / C 10/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4217760 / C 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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