SN65LVDS822 Flatlink™ LVDS 接收器

1 特性

- 4:27 LVDS 到 CMOS 解串器
- 对于 160 × 120 至 1024 × 600 范围内的分辨率，像素时钟范围为 4MHz 至 54MHz
- 具有 14x 采样的特殊 2:27 模式允许只使用 2 条数据信道
- 具有 3 路可选 CMOS 转换率的极低电磁干扰 (EMI)
- 支持单个 3.3V 电源；V_{DDIO} 允许 1.8V 至 3.3V 电压范围，可提供灵活的面板支持
- 时钟输出为上升或下降边沿
- 针对灵活印刷电路板 (PCB) 布局布线的总线交换特性
- 集成型可切换输入端接
- 所有输入引脚是故障安全的；±3kV 人体模型 (HBM) 静电放电 (ESD) 保护
- 7mm x 7mm 48 引脚超薄四方扁平无引线 (VQFN)，0.5mm 间距
- 与 TIA/EIA-644-A 发送器兼容

2 应用范围

- 打印机
- 具有一个 LCD 的装置
- 数码照相机

3 说明

SN65LVDS822 是一种高级 Flatlink™ 低压差分信号 (LVDS) 接收器，采用现代化 CMOS 工艺。 该器件具有几个独特的功能，其中包括 3 个可选 CMOS 输出转换率，1.8V 至 3.3V 的 CMOS 输出电压支持，一个引脚分配交换选项，集成差分端接（可配置），一个自动低功耗模式和 4:27 和 2:27 解串化模式。 它与诸如 SN75LVDS83B、SN65LVDS93A 的 TI FlatLink™ 发送器以及符合 TIA/EIA 644-A 标准的标准工业用 LVDS 发送器兼容。

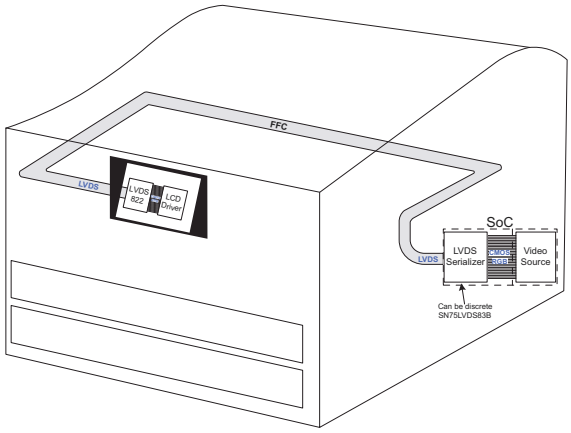
SN65LVDS822 特有一个自动低功耗待机模式，当 LVDS 时钟被禁用时激活。 此器件在将低压施加到引脚 SHTDN# 上时进入一个平均低功耗关断模式。

SN65LVDS822 采用 48 引脚 7mm x 7mm 塑料四方扁平无引线 (QFN) 封装，封装的焊球间距为 0.5mm，并且可在 –40°C 至 85°C 的工业环境温度范围内使用。

器件信息(1)

部件号	封装	封装尺寸（标称值）
SN65LVDS822	VQFN (48)	7.00mm x 7.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



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4 修订历史记录

Changes from Revision A (October 2013) to Revision B **Page**

- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

5 说明（继续）

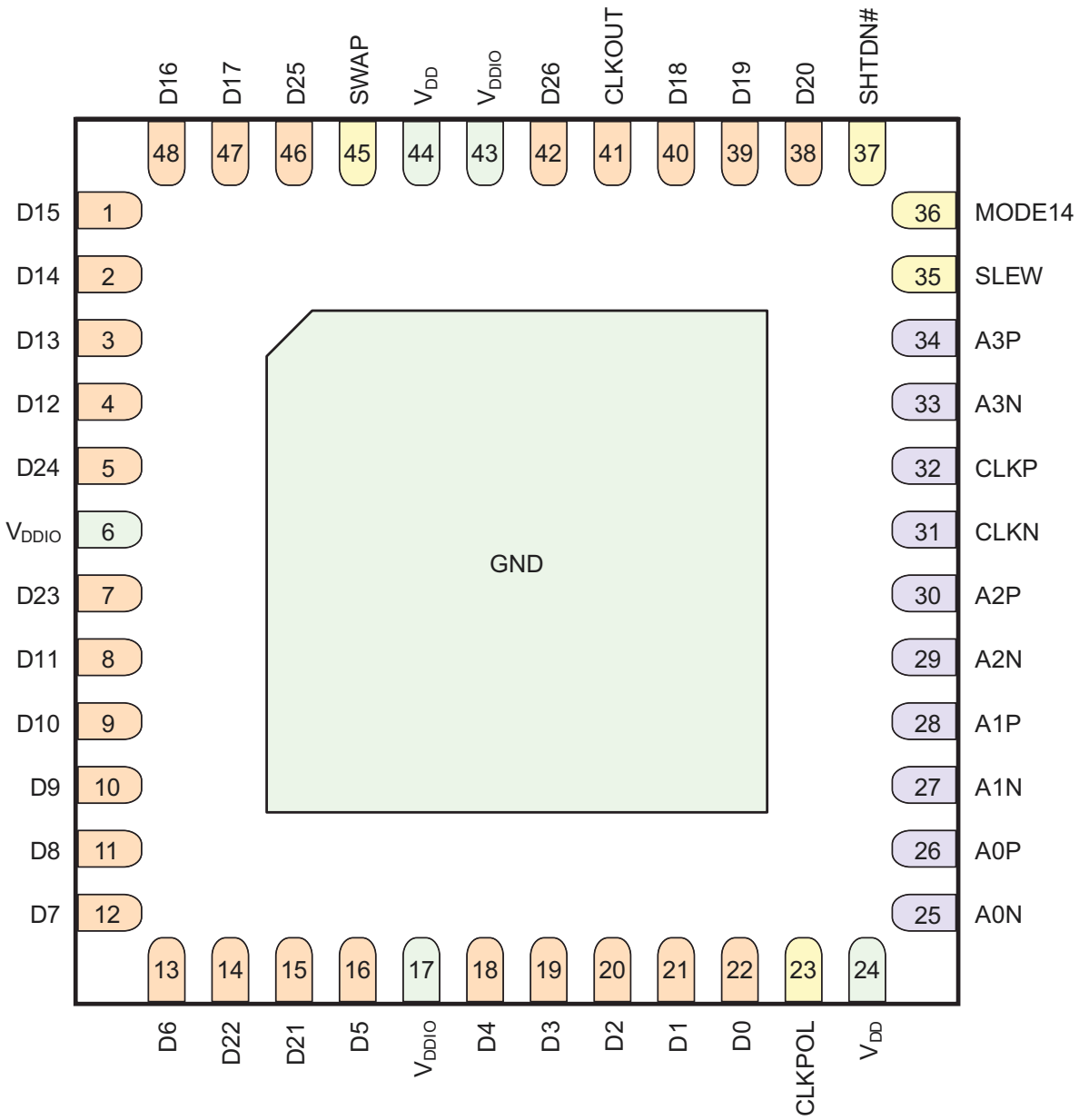
在标准 7x 模式下支持 4MHz 至 54MHz 的时钟频率范围，可与数据速率在 28Mbps 至 378Mbps 之间的 LVDS 数据一同使用。 对于 56Mbps 至 378Mbps 的 LVDS 的数据速率，此 14x 模式支持 4MHz 至 27MHz 的频率。 LVDS 时钟频率始终与 CMOS 输出时钟频率相匹配。 为了实现正常运行，在时钟线路上监视直流共模电压。 此器件的设计可支持 1/16 VGA (160 × 120) 至 1024 × 600 范围内的分辨率，每秒 60 帧，24 位彩色。

SN65LVDS822 特有一个自动低功耗待机模式，当 LVDS 时钟被禁用时激活。 此器件在将低压施加到引脚 SHTDN# 上时进入平均低功耗关断模式。 在这两个低功耗模式中，所有 CMOS 输出驱动为低电平。 所有输入引脚具有故障安全保护功能，此功能在电源电压为高值且稳定前，可防止器件损坏。

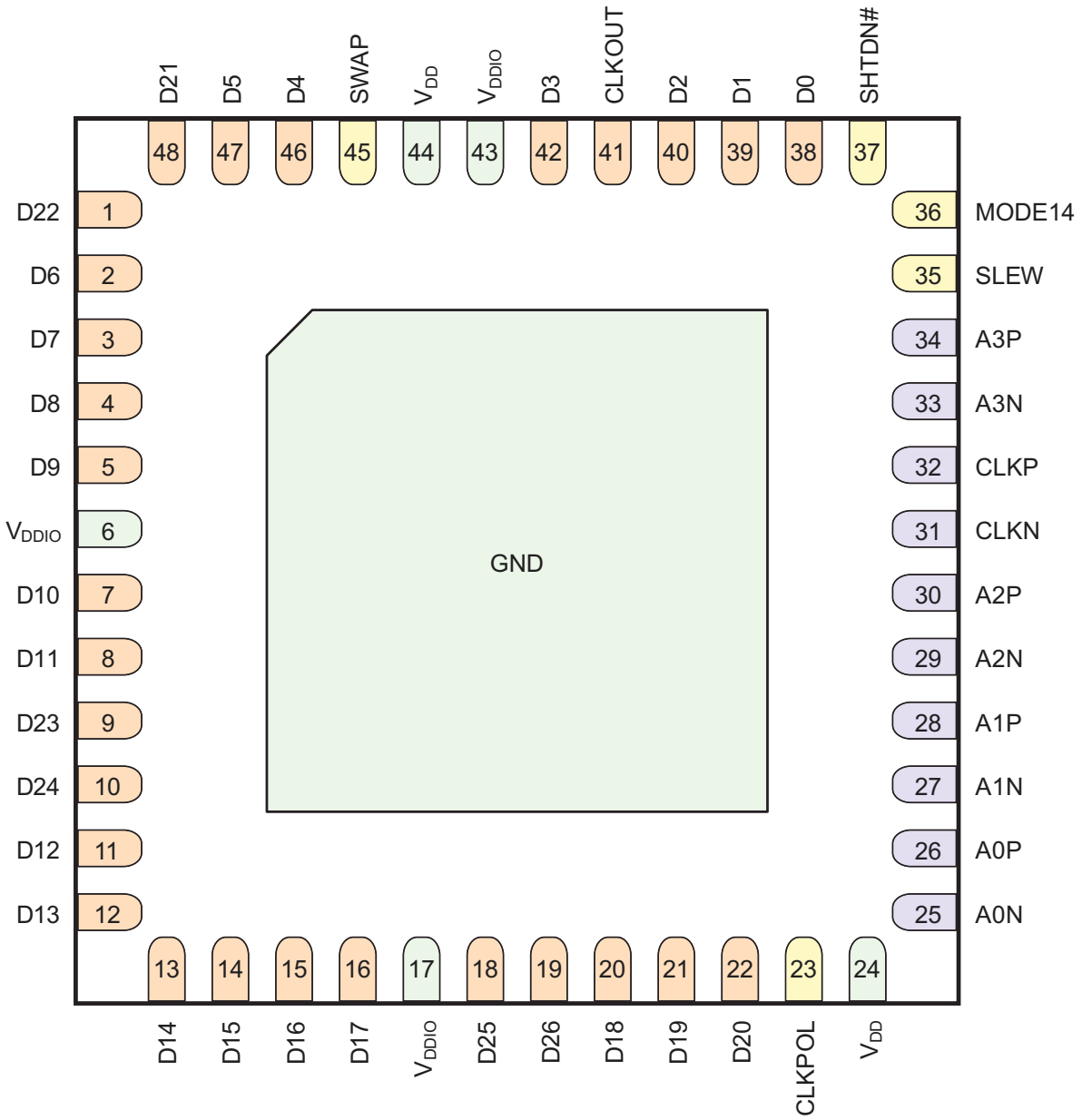
SN65LVDS822 采用 48 引脚 7mm x 7mm 塑料四方扁平无引线 (QFN) 封装，封装的焊球间距为 0.5mm，并且可在 –40°C 至 85°C 的工业环境温度范围内使用。

6 Pin Configuration and Functions

RGZ PACKAGE
(TOP VIEW)
SWAP Pin = Low or Floating



RGZ PACKAGE
(TOP VIEW)
SWAP Pin = High



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0P, A0N	26, 25	LVDS Input	LVDS Data Lane 0
A1P, A1N	28, 27		LVDS Data Lane 1
A2P, A2N	30, 29		LVDS Data Lane 2
A3P, A3N	34, 33		LVDS Data Lane 3
CLKP, CLKN	32, 31		LVDS Clock
	(SWAP = L / H)	CMOS Output	Data bus output
D0	22 / 38		
D1	21 / 39		
D2	20 / 40		
D3	19 / 42		
D4	18 / 46		
D5	16 / 47		
D6	13 / 2		
D7	12 / 3		
D8	11 / 4		
D9	10 / 5		
D10	9 / 7		
D11	8 / 8		
D12	4 / 11		
D13	3 / 12		
D14	2 / 13		
D15	1 / 14		
D16	48 / 15		
D17	47 / 16		
D18	40 / 20		
D19	39 / 21		
D20	38 / 22		
D21	15 / 48		
D22	14 / 1		
D23	7 / 9		
D24	5 / 10		
D25	46 / 18		
D26	42 / 19		
CLKOUT	41		Clock output for the data bus

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SWAP	45	CMOS Input	Selects the CMOS output pinout, and also controls differential input termination. Low – Default pinout, R_{ID} connected Floating – Default pinout, R_{ID} disconnected (requires external termination) High – Swapped pinout, R_{ID} connected
MODE14	36		Sets the number of LVDS serial bits per lane per clock period. Low – 7 bits (see 图 16) High – 14 bits; only lanes A0 and A2 are used (see 图 17)
CLKPOL	23		CLKOUT polarity Low – D[26:0] is valid during the CLKOUT falling edge Floating – Reserved; do not use High – D[26:0] is valid during the CLKOUT rising edge
SHTDN#	37		Shutdown Mode; Active-Low
SLEW	35		Sets the CMOS output slew rate Low – Slowest rise/fall time Floating – Medium rise/fall time High – Fastest rise/fall time
VDD	24, 44	Power Supply	Main power supply; 3.3 V
VDDIO	6, 17, 43		Power supply for CMOS outputs; 1.8 V to 3.3 V
GND	Thermal Pad		Reference Ground

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage range(2), V_{DD} , V_{DDIO}		–0.3	4	V
Voltage range at any input terminal	When V_{DDIO} > 0 V	–0.5	4	V
Voltage range at any output terminal	When V_{DDIO} ≤ 0 V	–0.5	V_{DDIO} + 0.7	
Maximum junction temperature, T_J			125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model(1) (all pins)	–3	3	V
		Charged device model(2) (all pins)	–1.5	1.5	

(1) In accordance with JEDEC Standard 22, Test Method A114-B
(2) In accordance with JEDEC Standard 22, Test Method C101

7.3 Recommended Operating Conditions

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Main power supply			3	3.3	3.6	V
V_{DDIO}	Power supply for CMOS outputs			1.65		3.6	V
V_{NOISE}	Power supply noise (peak-to-peak)	f_{NOISE} < 1 MHz				100	mV
		f_{NOISE} > 1 MHz				50	
T_A	Operating free-air temperature			–40		85	°C
T_C	Case temperature					98	°C
LVDS CLOCK (CLKP, CLKN)							
f_{CLK}	LVDS clock frequency	MODE14 = Low		4		54	MHz
		MODE14 = High		4		27	
		Standby Mode				0.5	
t_{DC}	LVDS clock duty cycle	MODE14 = Low			57%		
		MODE14 = High			50%		
LVDS INPUTS (A0P, A0N, A1P, A1N, A2P, A2N, A3P, A3N, CLKP, CLKN)							
$\|V_{ID}\|$	Input differential voltage[1]	$\|V_{AxP} – V_{AxN}\|$ and $\|V_{CLKP}-V_{CLKN}\|$		90		600	mV
ΔV_{ID}	Input differential voltage variation between lanes			–10%		10%	
V_{CM}	Input common mode voltage[1]			$\|V_{ID}\|/2$		2.4 - $\|V_{ID}\|/2$	V
ΔV_{CM}	Input common mode voltage variation between lanes			–100		100	mV
$t_{R/F(VID)}$	LVDS V_{ID} rise/fall time[2]	MODE14 = Low	f_{CLK} = 4 MHz to 14 MHz			3	ns
			f_{CLK} = 14 MHz to 22 MHz			2	
			f_{CLK} = 22 MHz to 30 MHz			1.5	
			f_{CLK} = 30 MHz to 54 MHz			1	
		MODE14 = High	f_{CLK} = 4 MHz to 7 MHz			3	
			f_{CLK} = 7 MHz to 11 MHz			2	
			f_{CLK} = 11 MHz to 15 MHz			1.5	
			f_{CLK} = 15 MHz to 27 MHz			1	
CMOS OUTPUTS (D[26:0], CLKOUT)							
C_L	Capacitive load on the outputs				10		pF

(1) See 图 1.
(2) See 图 6. Defined from 20% to 80% of the differential voltage transition. Faster edge rates are generally preferred, as they provide more timing margin.

7.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS822 RGZ 48 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	30.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	18.1	
θ_{JB}	Junction-to-board thermal resistance(4)	6.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	6.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVDS INPUTS (A0P, A0N, A1P, A1N, A2P, A2N, A3P, A3N, CLKP, CLKN)						
R_{ID}	Differential input termination resistance(1)	SWAP = Low or High	80		132	Ω
C_{ID}	Differential input capacitance	Measured across differential pairs		1		pF
R_{PU}	Pull-up resistor for standby detection	Measured from each input to VDD	90			kΩ
$\|I_I\|$	Input leakage current	V_{DD} = 3.6 V; R_{ID} disconnected; One P/N terminal is swept from 0 V to 2.4 V while the other is 1.2 V			70	µA
CMOS INPUTS (SWAP, MODE14, CLKPOL, SHTDN#, SLEW)						
C_{IN}	Input capacitance for CMOS inputs			2		pF
V_{IK}	Input clamp voltage	I_I = -18 mA	–1.2			V
V_{IH}	High-level input voltage		0.8 x V_{DD}			V
V_{IL}	Low-level input voltage				0.2 x V_{DD}	V
3-STATE CMOS INPUTS (SWAP, CLKPOL, SLEW)						
V_F	Floating voltage	V_{IN} = High impedance		V_{DD}/2		V
I_{IH}	High-level input current (through pull-down)	V_{IN} = 3.6 V			36	µA
I_{IL}	Low-level input current (through pull-up)	V_{IN} = GND, V_{DD} = 3.6 V	-36			µA
2-STATE CMOS INPUTS (MODE14, SHTDN#)						
I_{IH}	High-level input current (through pull-down)	V_{IN} = 3.6 V			20	µA
I_{IL}	Low-level input current	V_{IN} = GND	0			µA
CMOS OUTPUTS (D[26:0], CLKOUT)						
V_{OH}	High-level output voltage	SLEW = Low; I_{OH} = -250 µA	0.8 x V_{DDIO}		V_{DDIO}	V
		SLEW = Floating; I_{OH} = -500 µA	0.8 x V_{DDIO}		V_{DDIO}	
		SLEW = High; I_{OH} = -1.33 mA	0.8 x V_{DDIO}		V_{DDIO}	
V_{OL}	Low-level output voltage	SLEW = Low; I_{OL} = 250 µA	0		0.5	V
		SLEW = Floating; I_{OL} = 500 µA	0		0.5	
		SLEW = High; I_{OL} = 1.33 mA	0		0.5	

(1) When V_{DD} = 0 V, the connection of R_{ID} is unknown.

7.6 Power Supply Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)(2)			TYP	MAX(1)	UNIT
I_{DD}	Total average supply current of V_{DD} and V_{DDIO}	Grayscale pattern; outputs terminated with 10 pF; MODE14 = Low, V_{DD} = 3.3 V, V_{DDIO} = 1.8 V		SLEW = Low; f_{CLK} = 10 MHz	24.6		mA
		Grayscale pattern; outputs terminated with 10pF; MODE14 = Low, V_{DD} = V_{DDIO} = 3.3 V		SLEW = Low; f_{CLK} = 10 MHz	25.7		mA
				SLEW = Float; f_{CLK} = 20 MHz	30.9		
				SLEW = High; f_{CLK} = 54 MHz	51.5		
		1010 pattern; outputs terminated with 10 pF; MODE14 = Low, V_{DD} = V_{DDIO} = 3.6 V		SLEW = Float; f_{CLK} = 20 MHz	48.2	59	mA
				SLEW = High; f_{CLK} = 54 MHz	101.7	124	
		Standby Mode	LVDS inputs are open; CMOS inputs held static; Outputs terminated with 10 pF	f_{CLK} < 500 kHz; $V_{CM-CLKP/N}$ ≤ 0.80 x V_{DD}	4	7	mA
				$V_{CM-CLKP/N}$ > 0.95 x V_{DD}	75	130	µA
		Shutdown Mode		SHTDN# = Low	4	20	
P_D	Power Dissipation	Grayscale pattern; outputs terminated with 10 pF; MODE14 = Low, V_{DD} = 3.3 V, V_{DDIO} = 1.8 V		SLEW = Low; f_{CLK} = 10 MHz	83		mW
		1010 pattern; outputs terminated with 10 pF; MODE14 = Low, V_{DD} = V_{DDIO} = 3.6 V		SLEW = High; f_{CLK} = 54 MHz	366	446	

(1) Grayscale and 1010 test patterns are described by 图 5 to 图 6 and 表 1 to 表 2.
(2) Standby Mode can be entered in two ways: f_{CLK} = zero to 500 kHz, or a high V_{CM} on the LVDS clock. If the LVDS transmitter device disables its clock driver to a high-impedance state, the SN65LVDS822's integrated R_{PU} will pull V_{CM} high for the lower-power Standby state.

7.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
INPUT TO OUTPUT RESPONSE TIME							
t_{PD}	Propagation delay of data	Measured from CLK input to CLKOUT			2.4/f_{CLK}		s
t_{PWRUP}	Enable time, exiting Shutdown	From Shutdown Mode, time from SHTDN# pulled High to valid output data (see 图 9)				2	ms
t_{WAKE}	Enable time, exiting Standby	From Standby Mode, time from when CLK input starts switching to valid output data				2	ms
t_{PWRDN}	Disable time, entering Shutdown	From Active Mode, time from SHTDN# pulled Low until all outputs are static-Low				11	µs
$t_{STANDBY}$	Disable time, entering Standby	From Active Mode, time from CLK input stopping until all outputs are static-Low				3	µs
f_{BW}	PLL bandwidth(1)	Tested from CLK input to CLKOUT			6% x f_{CLK}		Hz
LVDS INPUTS (A0P, A0N, A1P, A1N, A2P, A2N, A3P, A3N, CLKP, CLKN)							
t_{RSKM}	Receiver input skew margin(2) (3) (4)	$t_{R/F(VID)}$ = 600 ps V_{ID} = 90 mV See 图 2	MODE14 = Low	1/(14 x f_{CLK}) – 620E-12			s
			MODE14 = High	1/(28 x f_{CLK}) – 620E-12			
t_{SU1}	LVDS data setup time required before internal clock edge					620	ps
t_{H1}	LVDS data hold time required after internal clock edge					620	ps
CMOS OUTPUTS (D[26:0], CLKOUT)							
t_{DCYC}	Duty cycle of CLKOUT	MODE14 = Low	CLKPOL = Low		43%		
			CLKPOL = High		57%		
		MODE14 = High			50%		
$t_{R/F}$	CMOS output rise and fall time (20% to 80%)	C_L = 10 pF	SLEW = Low	10	15	20	ns
			SLEW = Floating	5	7.5	10	
			SLEW = High	1.3	2.1	3	
t_{SU2}	Setup time available for the downstream receiver(5)	MODE14 = Low; C_L = 10 pF	SLEW = Low	0.38/f_{CLK} – 2.2E-9			s
			SLEW = Floating	0.38/f_{CLK} – 1.2E-9			
			SLEW = High	0.38/f_{CLK} – 0.7E-9			
		MODE14 = High; C_L = 10 pF	SLEW = Low	0.45/f_{CLK} – 2.5E-9			
			SLEW = Floating	0.45/f_{CLK} – 1.5E-9			
			SLEW = High	0.45/f_{CLK} – 1E-9			
t_{H2}	Hold time available for the downstream receiver(5)	MODE14 = Low; C_L = 10 pF	SLEW = Low	0.52/f_{CLK} – 18.2E-9			s
			SLEW = Floating	0.52/f_{CLK} – 9.2E-9			
			SLEW = High	0.52/f_{CLK} – 3.7E-9			
		MODE14 = High; C_L = 10 pF	SLEW = Low	0.45/f_{CLK} – 18.5E-9			
			SLEW = Floating	0.45/f_{CLK} – 9.5E-9			
			SLEW = High	0.45/f_{CLK} – 4E-9			

(1) The PLL bandwidth describes the typical highest modulation frequency that can be tracked. If the LVDS transmitter device generates a spread spectrum, the LVDS clock and data must stay synchronized throughout modulation. The SN65LVDS822 will track and pass through modulation, and the downstream CMOS receiver must be able to track it.
(2) Receiver Input Skew Margin (t_{RSKM}) is the timing margin available for transmitter output pulse position (t_{PPOS}), interconnect skew, and interconnect inter-symbol interference. t_{RSKM} represents the reminder of the serial bit time not taken up by the receiver strobe uncertainty. The t_{RSKM} assumes a bit error rate better than 10^{-12}.
(3) t_{RSKM} is indirectly proportional to: internal setup and hold time uncertainty, ISI, duty cycle distortion from the front end receiver, skew mismatch between LVDS clock and data, and PLL cycle-to-cycle jitter.
(4) LVDS input timing defined here is based on a simulated statistical analysis across process, voltage, and temperature ranges.
(5) See 图 3 and 图 4.

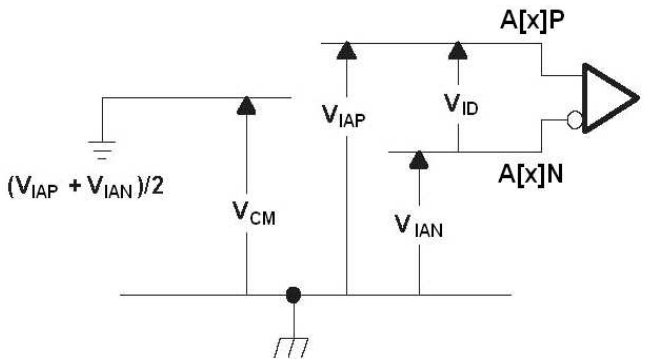


图 1. FlatLink™ Input Voltage Definitions

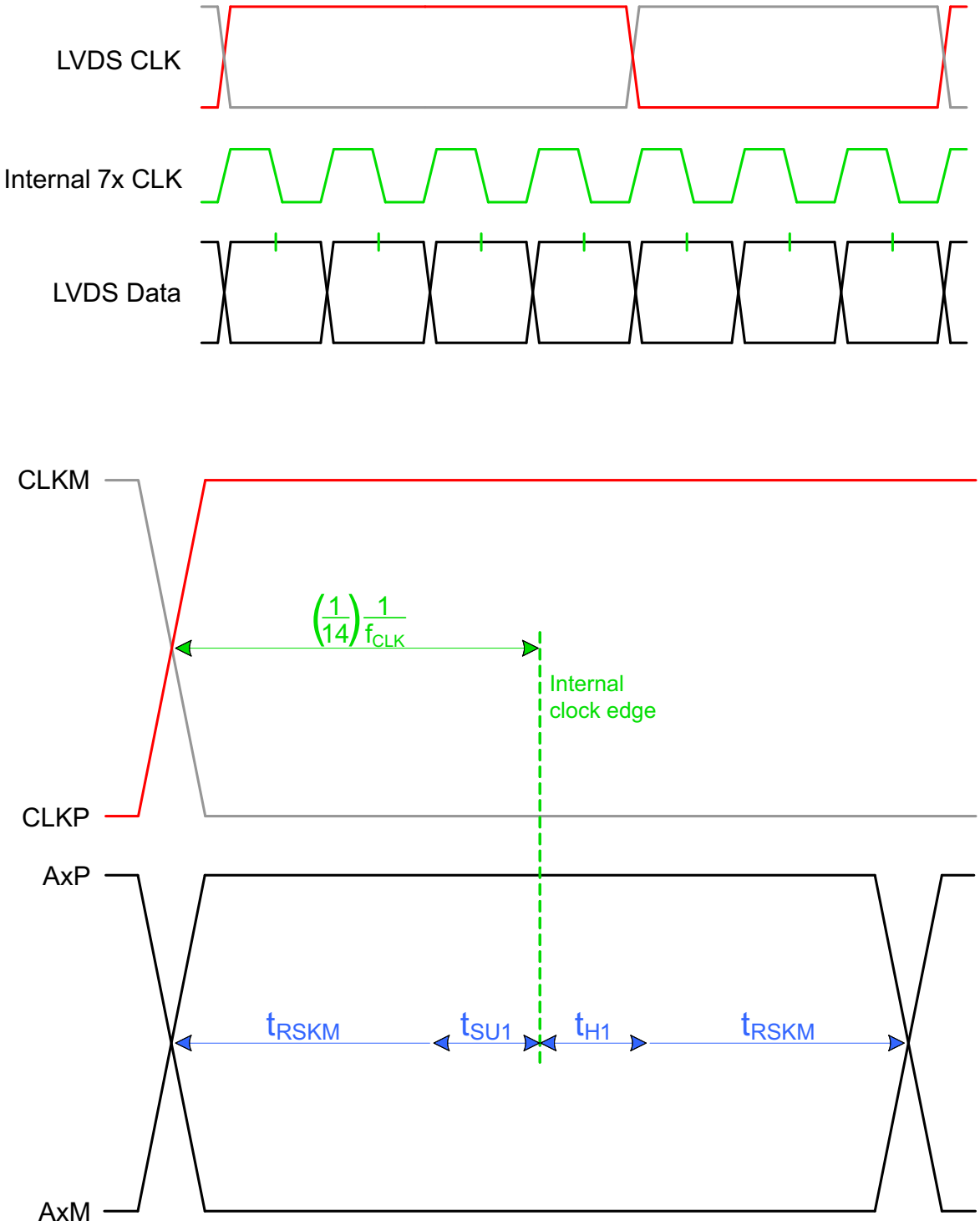


图 2. LVDS Input Timing (MODE14 = Low)

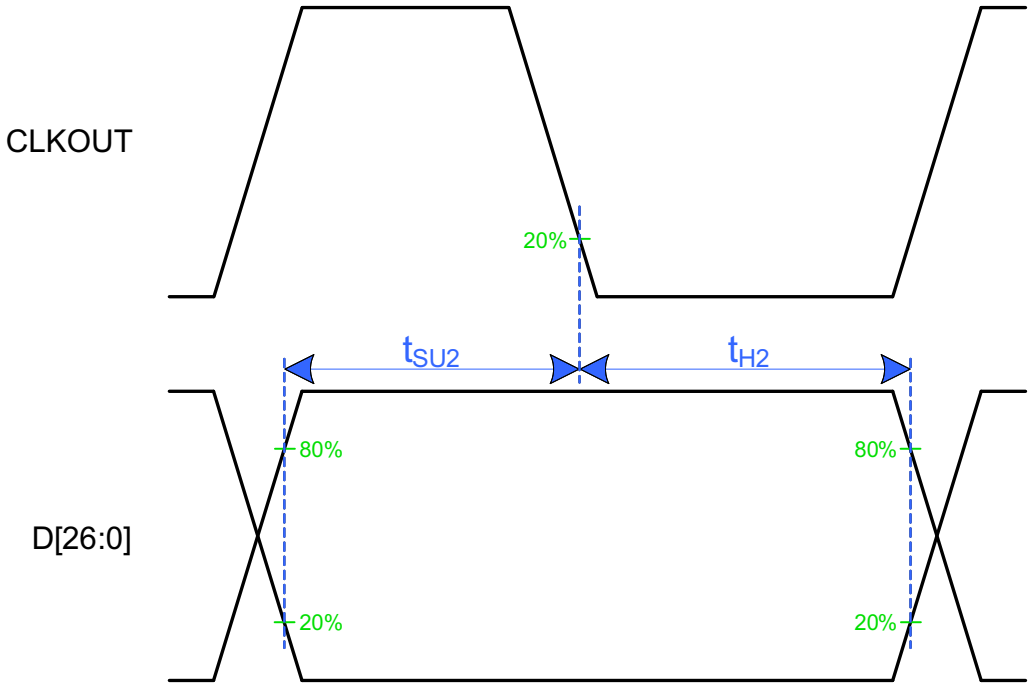


图 3. CMOS Output Timing (CLKPOL = Low)

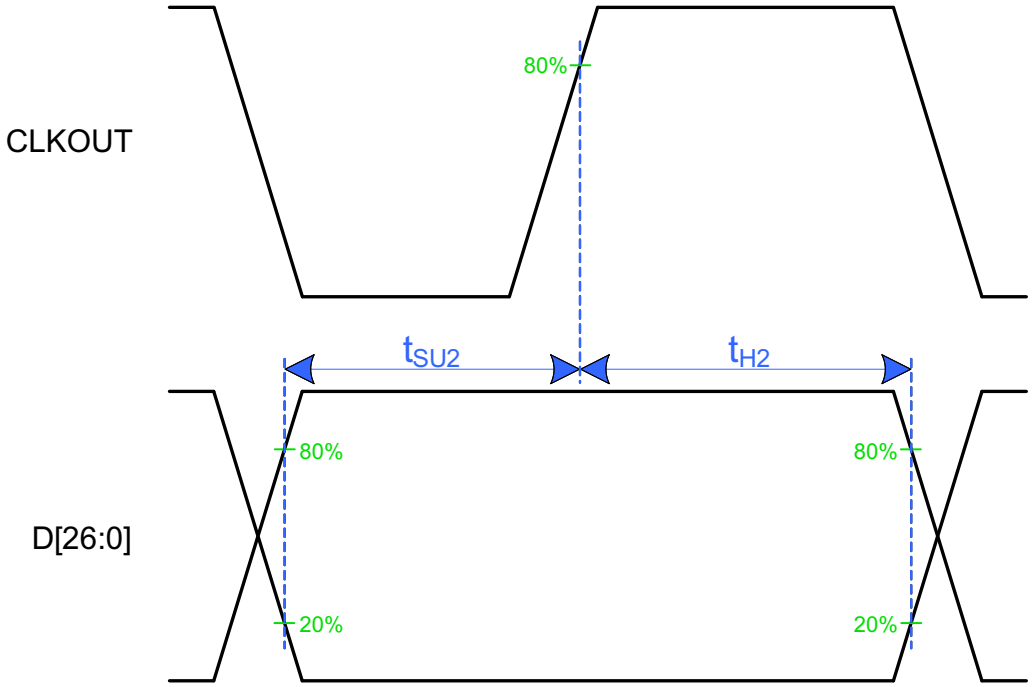


图 4. CMOS Output Timing (CLKPOL = High)

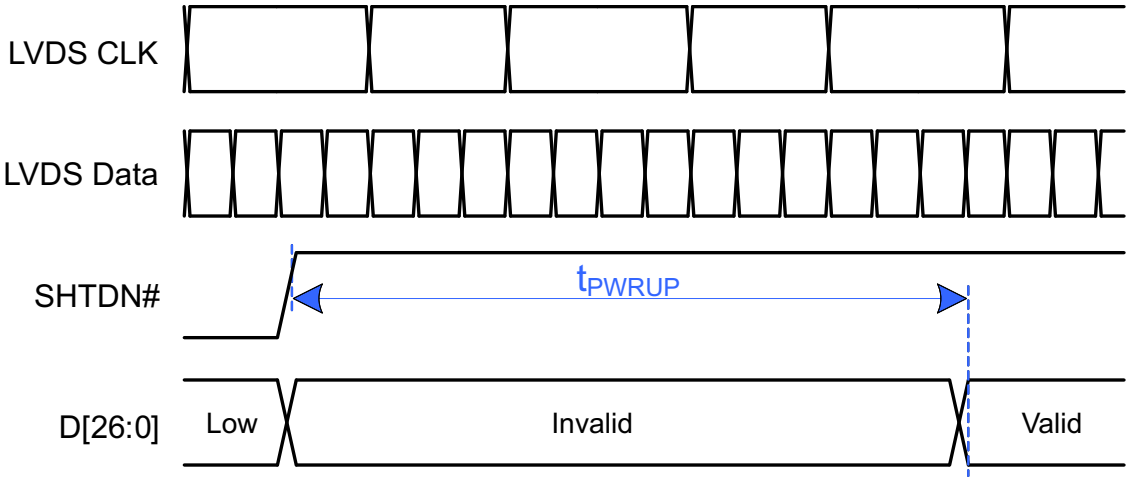


图 5. Time to Exit Shutdown Mode

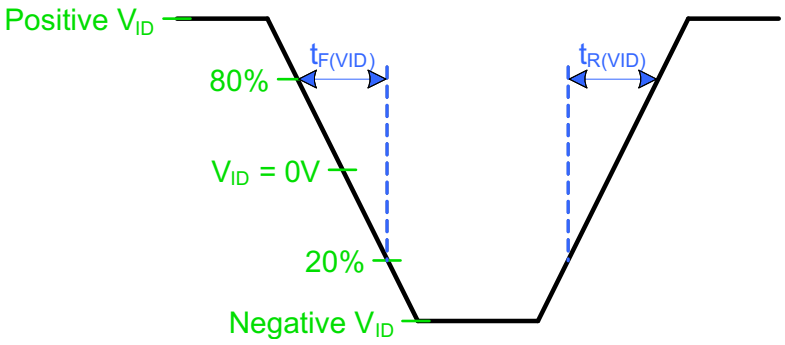


图 6. LVDS Rise/Fall Time (Differential Voltage)

7.8 Typical Characteristics

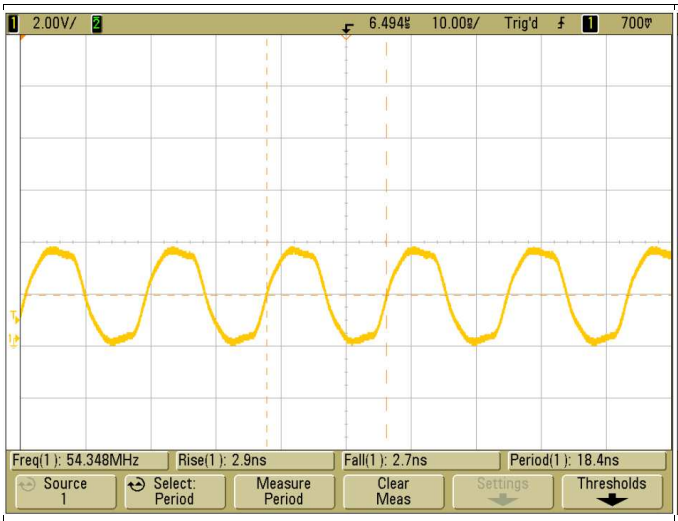
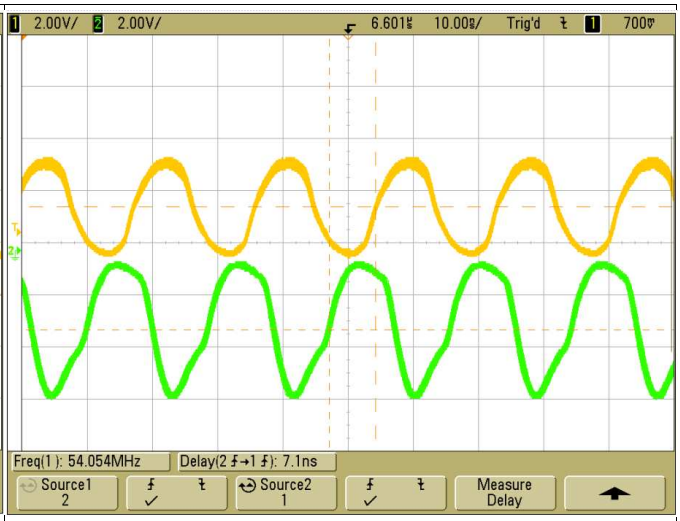


图 7. Output Rise & Fall times - SLEW = High



Input: channel 2 (green), Output: channel 1 (yellow)

图 8. Total Output Delay

8 Parameter Measurement Information

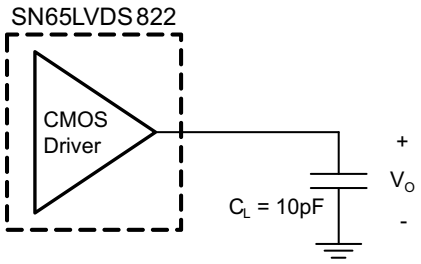


图 9. CMOS Output Test Circuit

8.1 Test Patterns

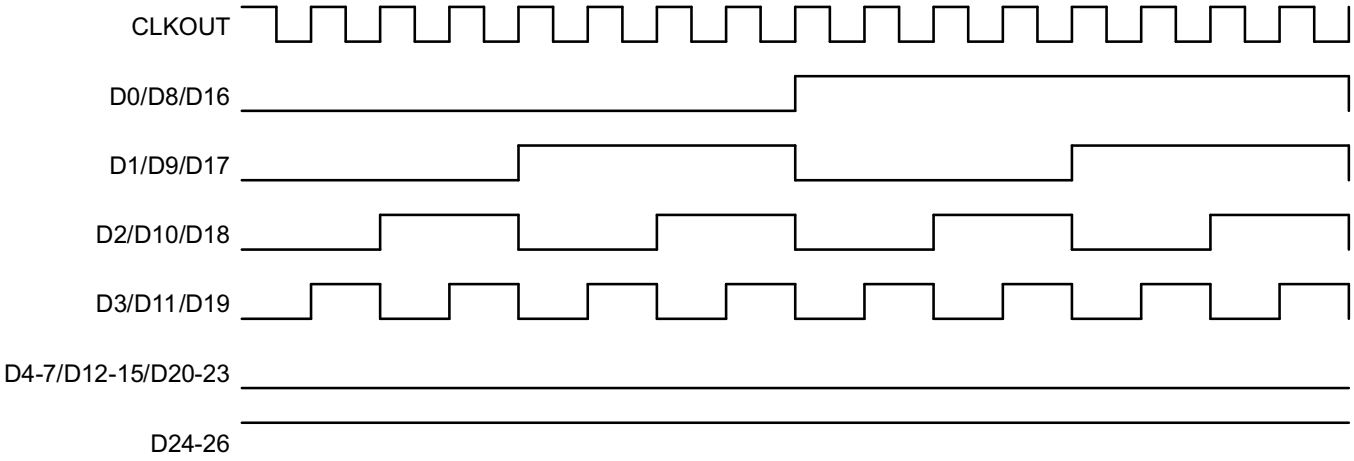


图 10. Grayscale Pattern (CLKPOL = Low); Used for Typical Power Data

表 1. Grayscale Pattern Data; Repeats Every 16 Words

Word	D[26:0]
1	0x7000000
2	0x7080808
3	0x7040404
4	0x70C0C0C
5	0x7020202
6	0x70A0A0A
7	0x7060606
8	0x70E0E0E
9	0x7010101
10	0x7090909
11	0x7050505
12	0x70D0D0D
13	0x7030303
14	0x70B0B0B
15	0x7070707
16	0x70F0F0F

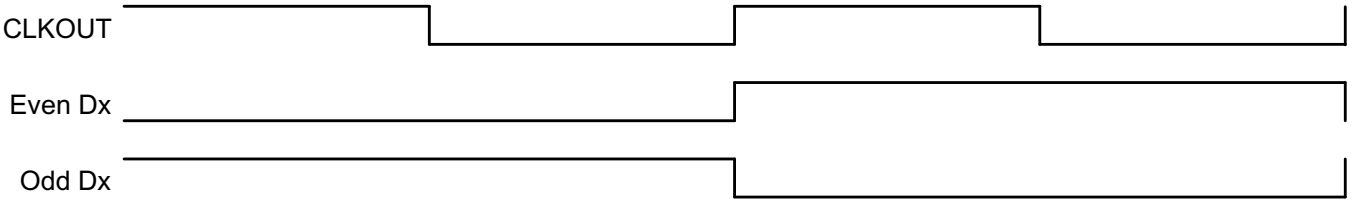


图 11. 1010 Pattern (CLKPOL = Low); Used for Maximum Power Data

表 2. 1010 Pattern Data; Repeats Every 2 Words

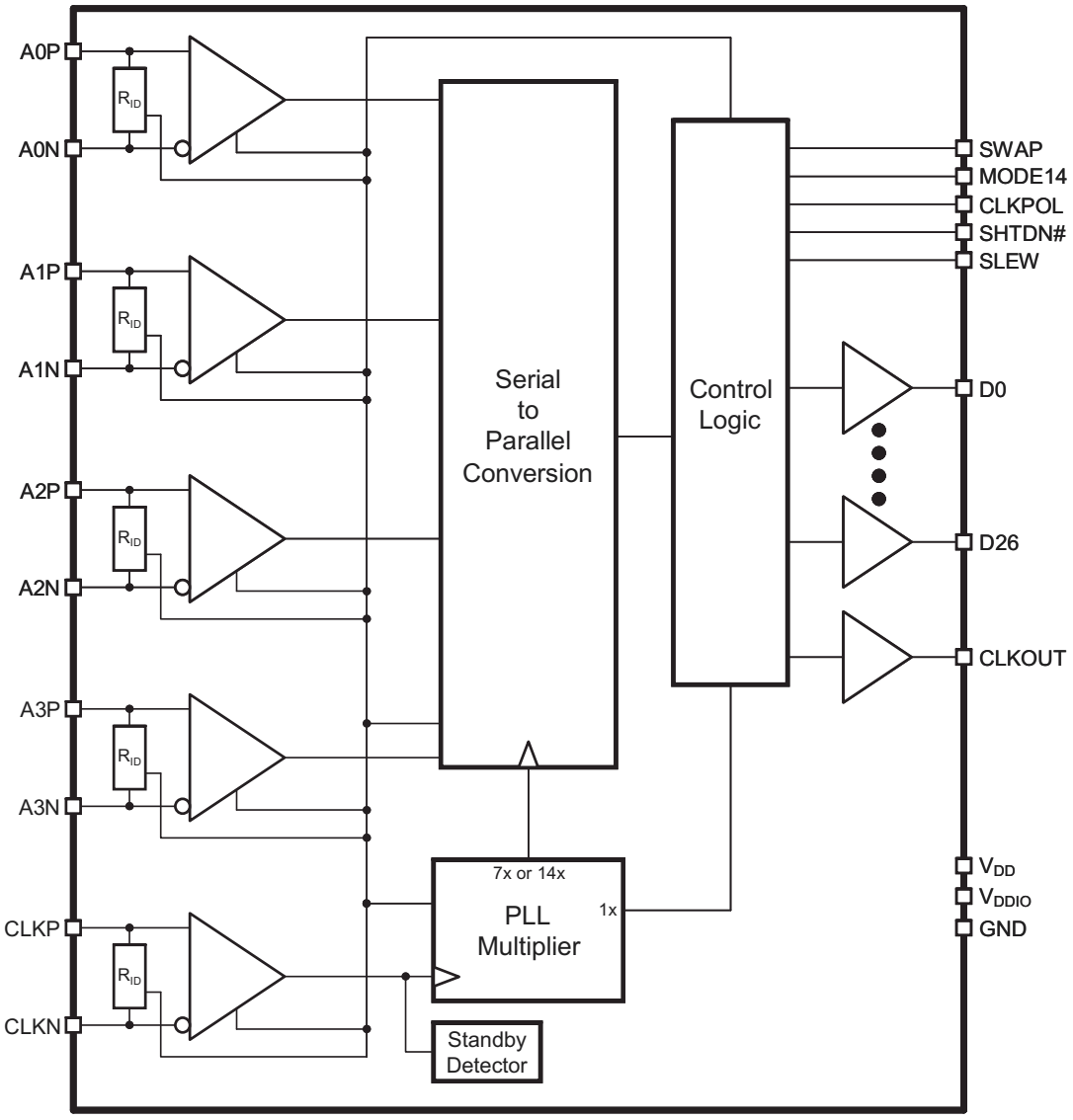
Word	D[26:0]
1	0x2AAAAAA
2	0x5555555

9 Detailed Description

9.1 Overview

The SN65LVDS822 implements five low-voltage differential signal (LVDS) line receivers: 4 data lanes and 1 clock lane. The clock is internally multiplied by 7 or 14 (depending on pin MODE14), and used for sampling LVDS data. The device operates in either 4-lane 7x mode, or 2-lane 14x mode. Each input lane contains a shift register that converts serial data to parallel. 27 total bits per clock period are deserialized and presented on the CMOS output bus, along with a clock that uses either rising- or falling-edge alignment.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Unused LVDS Data Lanes

When MODE14 = Low and fewer than 4 data lanes are used, or when MODE14 = High and only 1 data lane is used, it's recommended that the unused lanes are biased with a constant differential voltage. This prevents high-frequency noise from toggling the unused receiver, which injects noise into the device. This is not a hard requirement, but it's standard best-practice, and the amount of noise varies system-to-system.

Two implementations are shown below, depending on whether the internal termination R_{ID} is connected. A reasonable choice for R1 and R2 is 5kΩ, which produce a nominal V_{ID} of 34 mV and 0.3 mA of static current. Smaller resistors increase V_{ID} and noise floor margin, as well as static current.

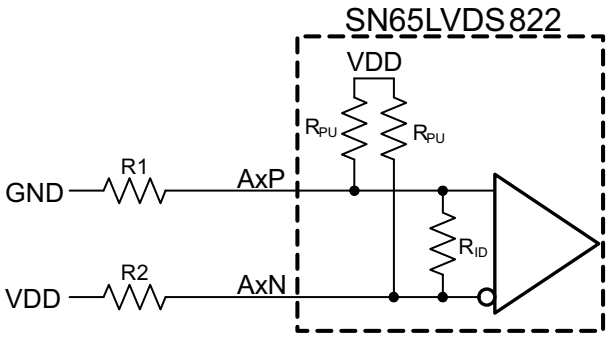


图 12. Bias When R_{ID} is Connected

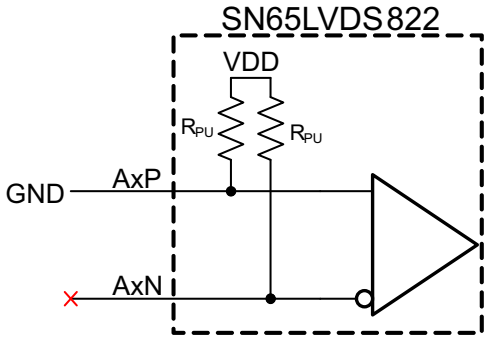


图 13. Bias When R_{ID} is Disconnected

9.3.2 Tying CMOS Inputs With Resistors

The I_{IH}/I_{IL} specifications indicate that 2-state CMOS input pins have an internal pull-down that's a minimum size of 180 kΩ, and 3-state CMOS input pins have an internal pull-up and pull-down that are a minimum size of 100 kΩ.

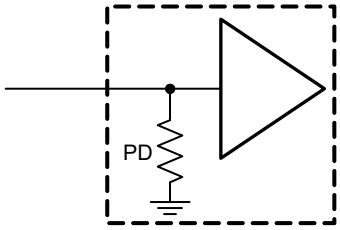


图 14. 2-State CMOS Input

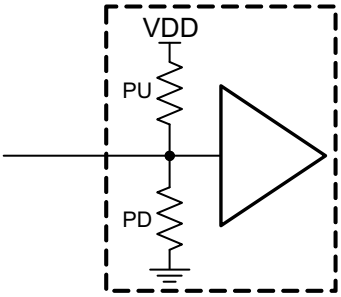


图 15. 3-State CMOS Input

CMOS inputs may be directly connected to V_{DD} or GND, or tied through a resistor. Using a resistor creates a voltage divider network, so it's important to use a small enough resistor to satisfy V_{IH}/V_{IL} at the pin, and to have voltage margin for system noise. When using a resistor, 5 kΩ or smaller is recommended. Of course, 3-state inputs may be left unconnected to select their floating pin state.

9.4 Device Functional Modes

9.4.1 Active Modes

9.4.1.1 4-Lanes 7-Bit Mode

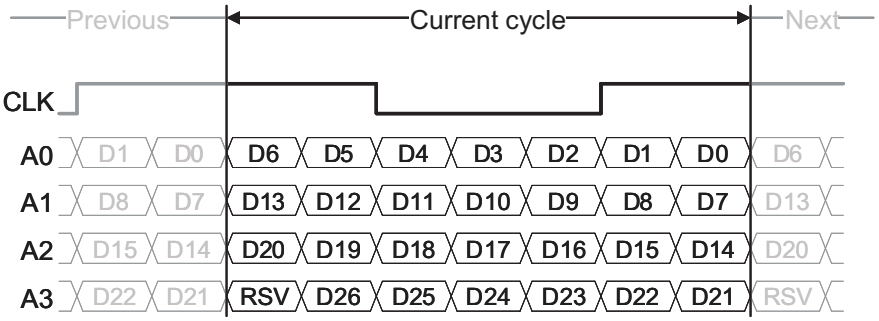


图 16. Data Bits Within the LVDS Stream (MODE14 = Low)

9.4.1.2 2-Lanes 14-Bit Mode

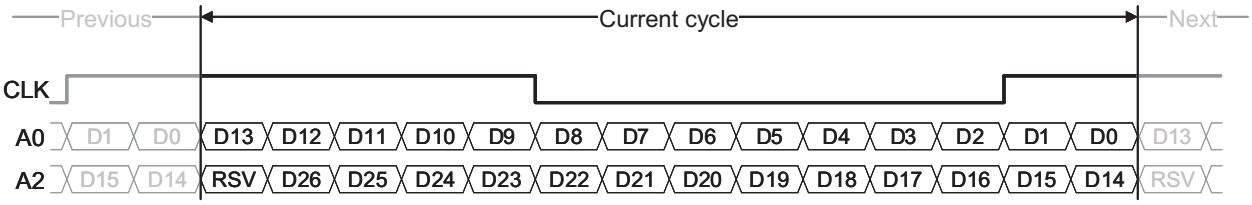


图 17. Data Bits Within the LVDS Stream (MODE14 = High)

9.4.2 Low-Power Modes

9.4.2.1 Standby Mode

In order to decrease the power consumption, the SN65LVDS822 automatically enters to standby when the LVDS clock is inactive.

9.4.2.2 Shutdown Mode

This is the lower-power mode, and the SN65LVDS822 enters to this mode only when the SHTDN# terminal is tied to low.

注

In both low-power modes, all CMOS outputs drive low. All input pins have failsafe protection that prevents damage from occurring before power supply voltages are high and stable.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Color Bit Mapping

The SN65LVDS822 is a simple deserializer that ignores bit representation in the LVDS stream. The CMOS output pin order was chosen so that if the color mapping within the LVDS stream matches the common VESA standard, the parallel output bus of red/green/blue fans out sequentially, which matches the order that many LCD panels require. Some LCD panels require a reversed order; for those, set pin "SWAP" high to reverse the output bus and simplify PCB routing. 图 19 shows the application setup when SWAP is in different statuses.

Any color bit mapping is supported, by correctly connecting the output to the panel. However, bit "RSV" is ignored and unavailable for use.

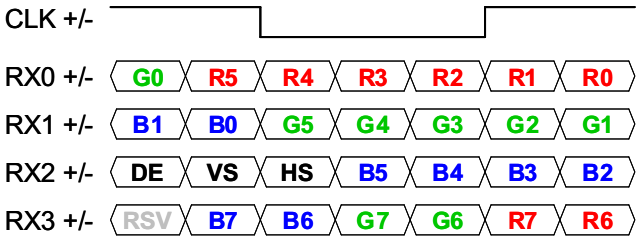
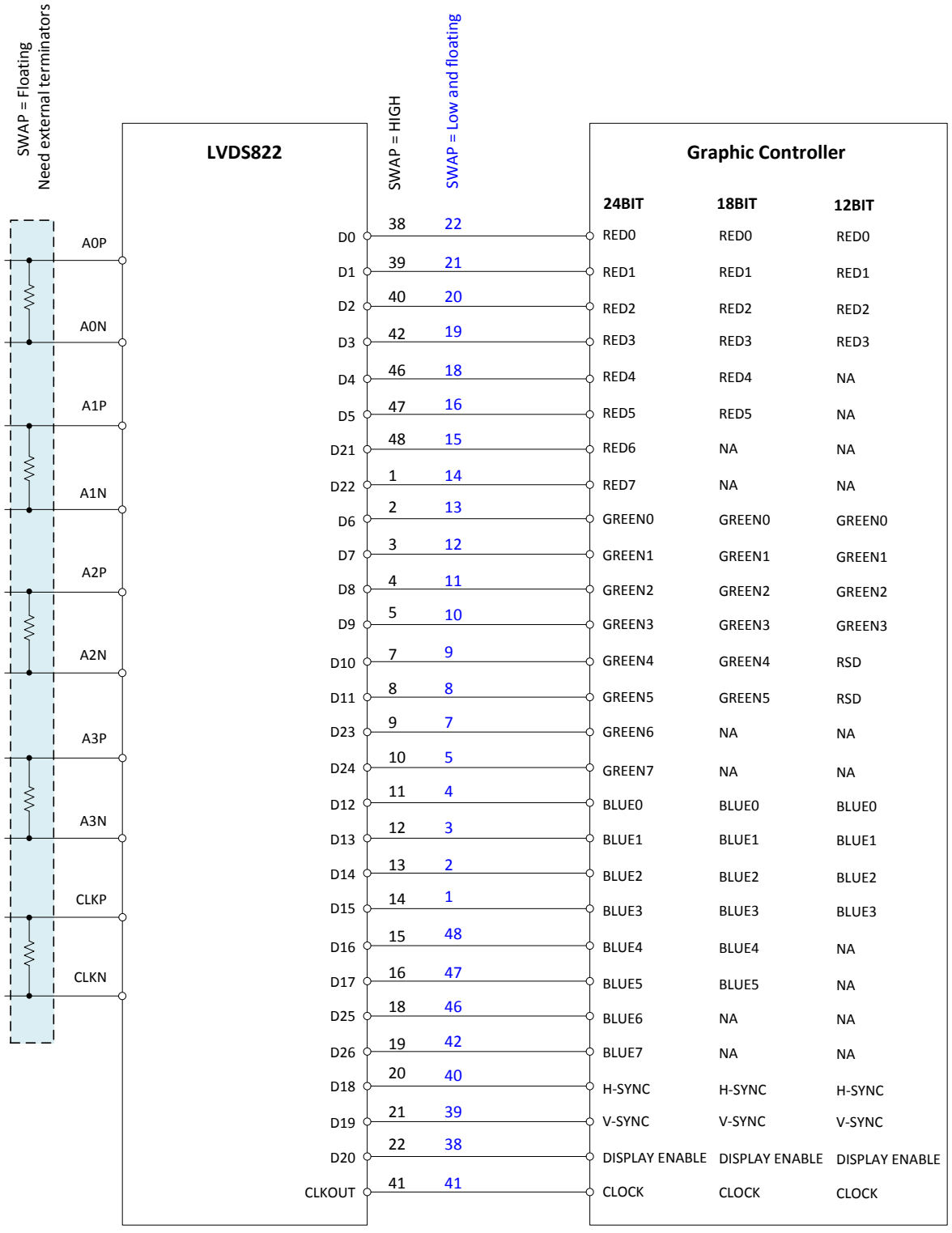


图 18. Common VESA Color Bit Mapping

Application Information (接下页)



NOTE: NA – not applicable, these unused inputs should be left open

图 19. Pin Assignments With SWAP

10.2 Typical Application

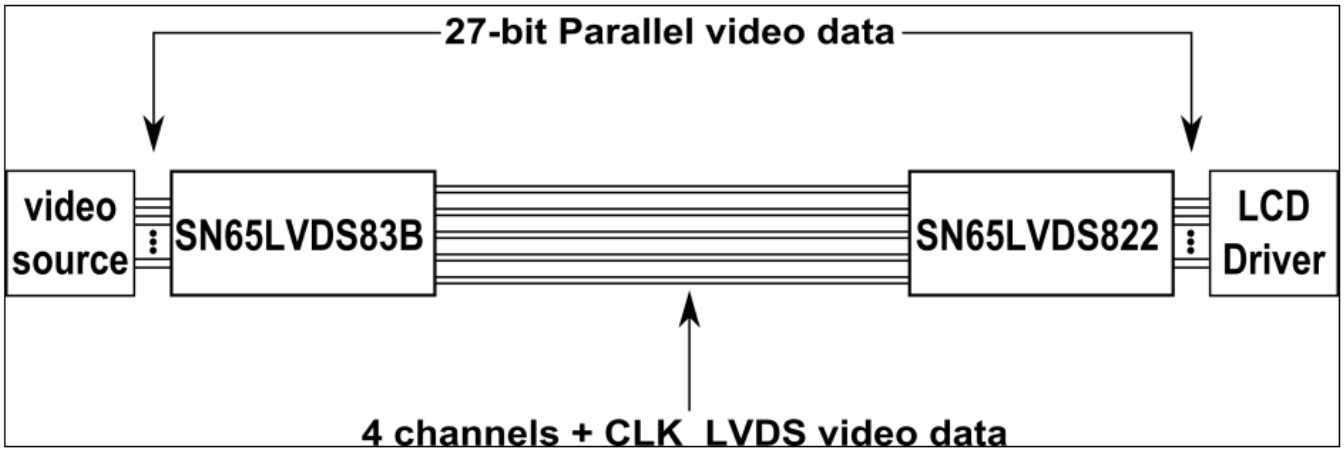


图 20. Typical Application

10.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
VDD Main Power Supply	3 - 3.6 V
VDDIO Power Supply for CMOS Outputs	1.65 - 3.6 V
Input LVDS Clock Frequency	4 - 54 MHz
RID Differential Input Termination Resistance	80 - 132 Ω
LVDS Input Channels	2 or 4
Output Load Capacitance	1 pF

10.2.2 Detailed Design Procedure

10.2.2.1 Power Supply

The implementation operates from the power provided by two banana jack connectors (P1 and P3) common ground. The VDD pin (P1) is connected to the main power supply to the SN65LVDS822 device and must be 3.3 V (±10%). The VDDIO pin (P3) is connected to the power supply of the SN65LVDS822 CMOS outputs and must be in the range of 1.8 to 3.3 V.

10.2.2.2 CMOS Output Bus Connector

Color Bit Mapping shows the CMOS output and bit mapping. Because some LCD panels require a reversed order, the SN65LVDS822 device is capable of reversing the output bus and simplifying PCB routing. When the pin is tied to high, the CMOS outputs are in normal order, otherwise the CMOS outputs are in reverse order.

10.2.2.3 Power-Up Sequence

The SN75LVDS822 does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC remains powered down and connected to GND. The input level of the SHTDN during this time does not matter as only the input stage is powered up while all other device blocks are still powered down. It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting SHTDN to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode. The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN75LVDS83B SHTDN input initially low):

1. Ramp up LCD power and SN65LVDS822 (maybe 0.5ms to 10ms) but keep backlight turned off.

2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Enable video source output; start sending black video data.
4. Toggle LVDS83B shutdown to SHTDN = VIH.
5. Toggle LVDS822 shutdown to SHTDN = VIH.
6. Send > 1 ms of black video data; this allows the LVDS83B to be phase locked, and the display to show black data first.
7. Start sending true image data.
8. Enable backlight.

Power Down sequence (SN75LVDS83B SHTDN input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for > 2 frame times.
3. Set SN75LVDS83B input SHTDN = GND; wait for 250 ns.
4. Set SN75LVDS822 input SHTDN = GND; wait for 250 ns.
5. Disable the video output of the video source.
6. Remove power from the LCD panel for lowest system power.

10.2.3 Application Curve

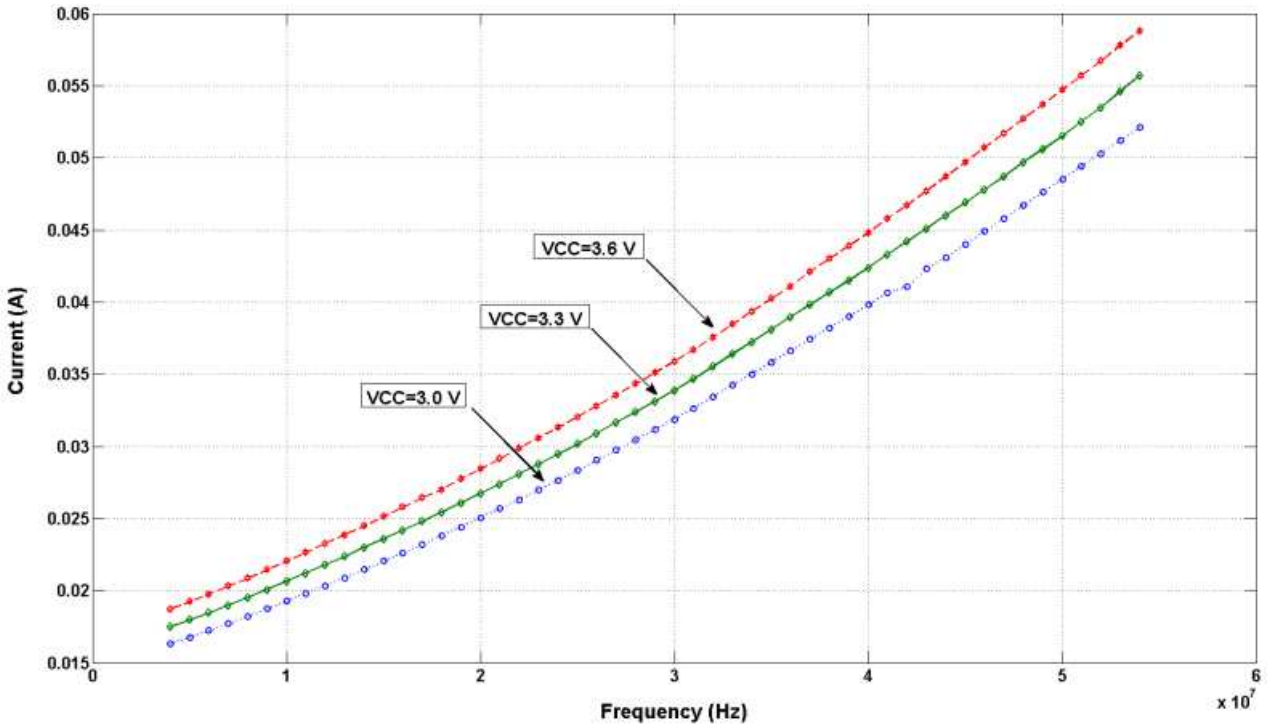


图 21. Total Current Consumption (VDD & VDDIO)

11 Power Supply Recommendations

11.1 Decoupling Capacitor Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVDS822 power pins. It is recommended to place one 0.01-µF ceramic capacitor at each power pin, and two 0.1-µF ceramic capacitors on each power node. The distance between the SN65LVDS822 and capacitors should be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the SN65LVDS822 on the bottom of the PCB is often a good choice. A 100-pF ceramic capacitor can be put at each power pin to optimize the EMI performance.

12 Layout

12.1 Layout Guidelines

Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45o bends is seen as a smaller discontinuity.

Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.

When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.

Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.

Use solid power and ground planes for 100 Ω impedance control and minimum power noise.

For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.

Keep the trace length as short as possible to minimize attenuation.

Place bulk capacitors (i.e. 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

12.2 Layout Example

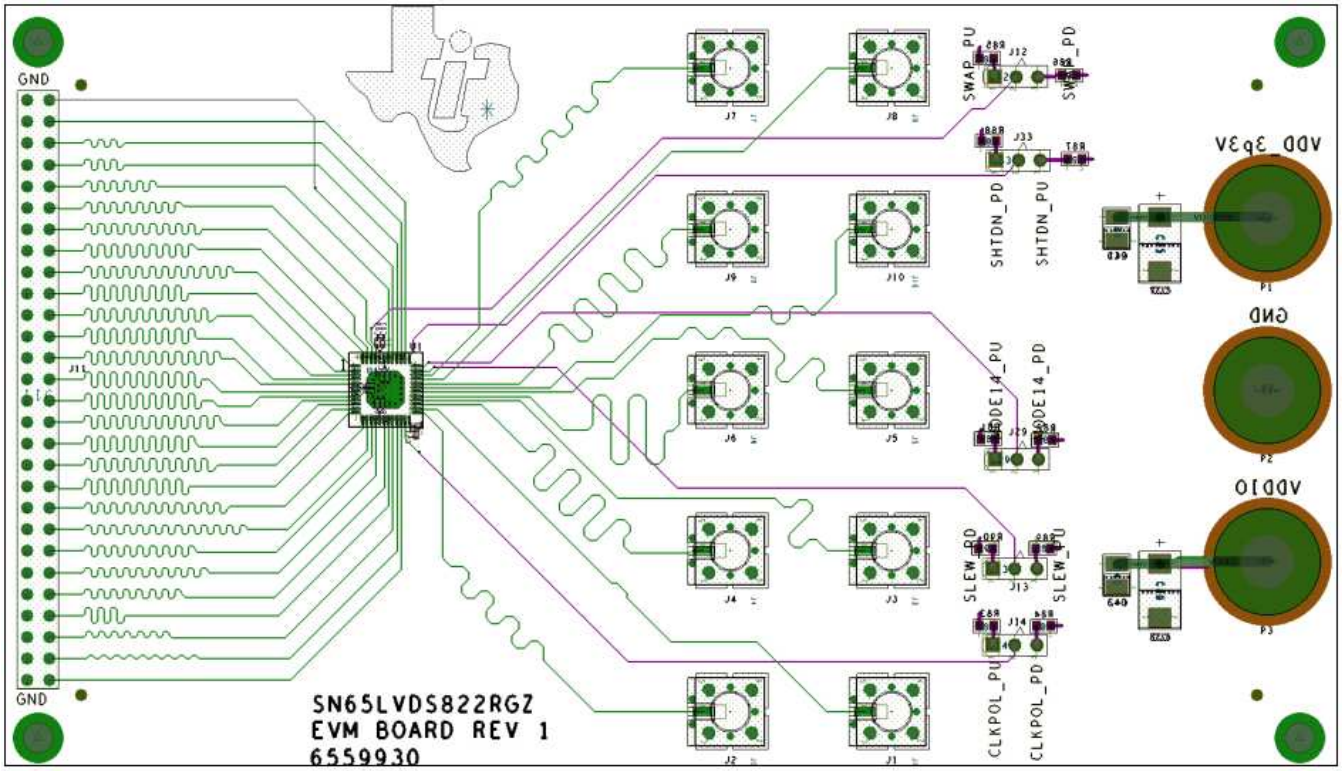


图 22. Layout Example

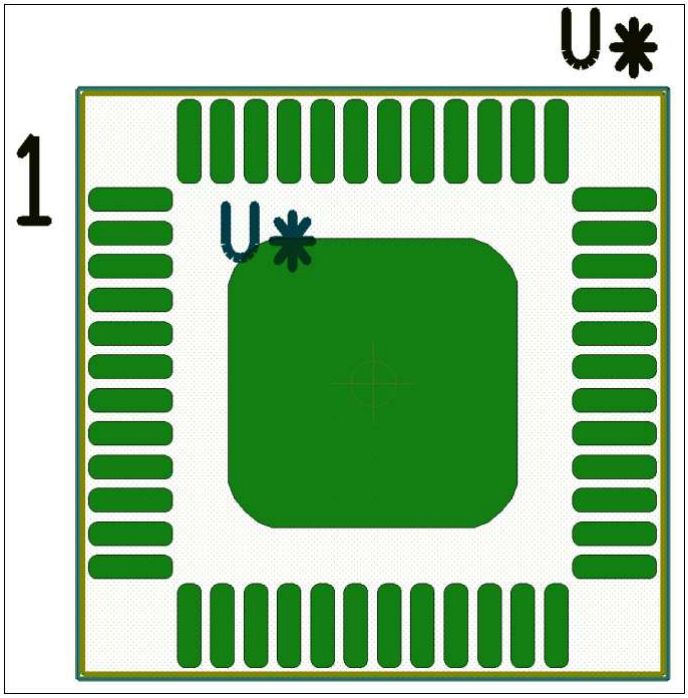


图 23. Footprint Example

13 器件和文档支持

13.1 商标

Flatlink is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS822RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS822
SN65LVDS822RGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS822
SN65LVDS822RGZRG4	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS822
SN65LVDS822RGZRG4.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS822

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

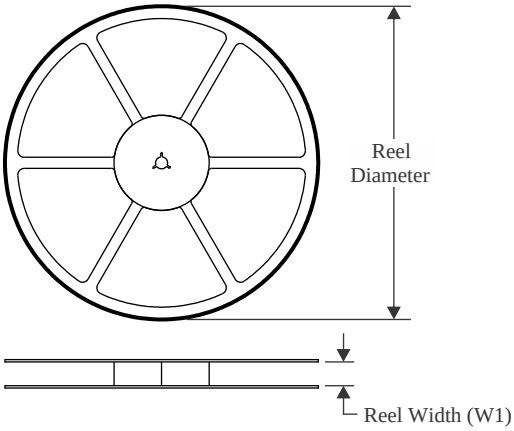
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

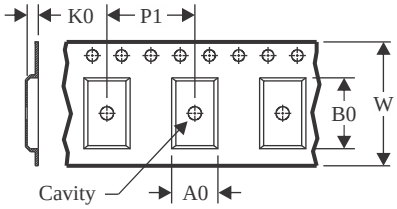
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

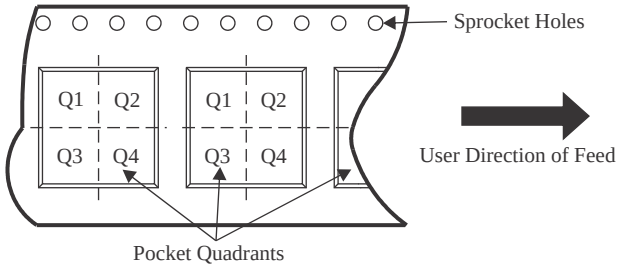


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

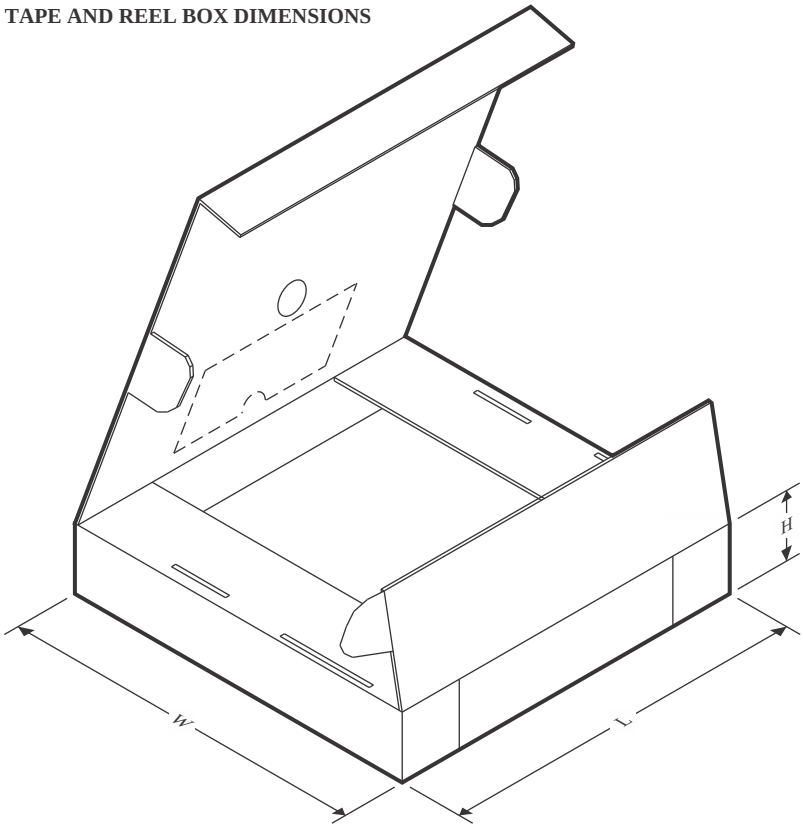
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS822RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN65LVDS822RGZRG4	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS822RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN65LVDS822RGZRG4	VQFN	RGZ	48	2500	367.0	367.0	38.0

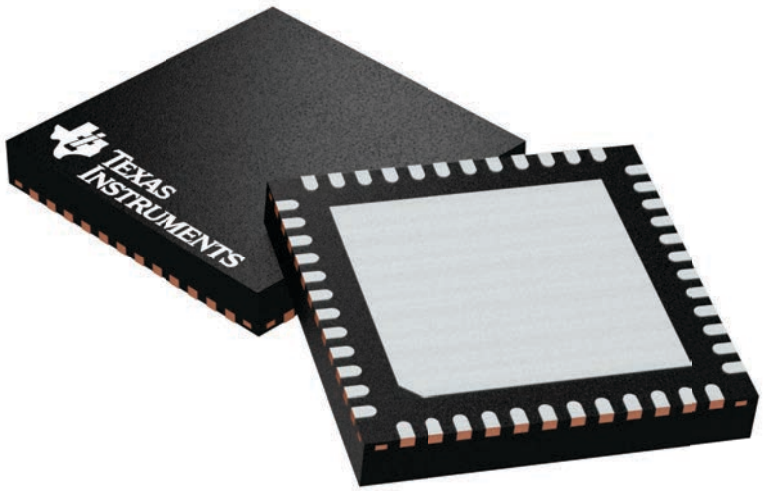
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

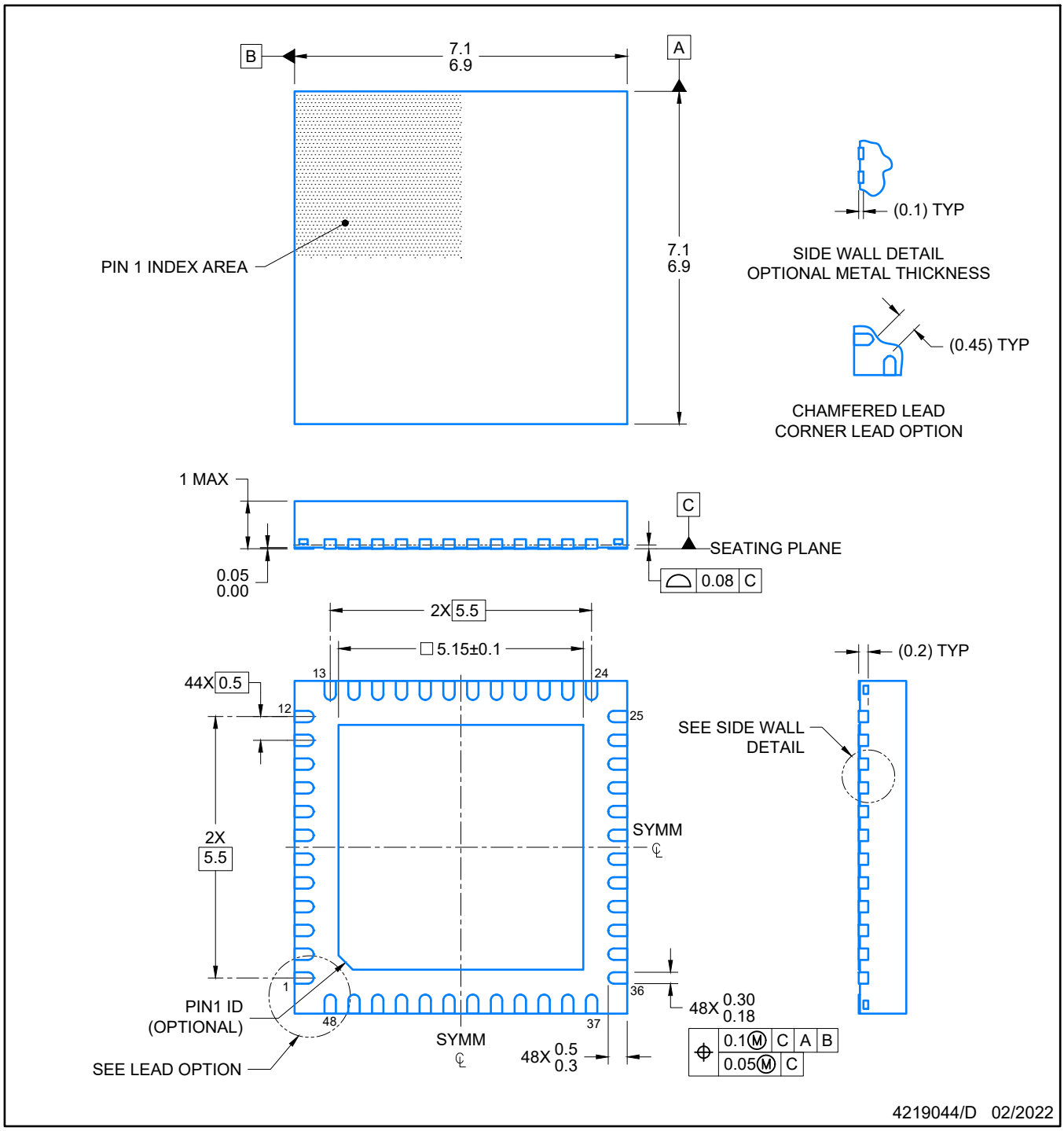
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

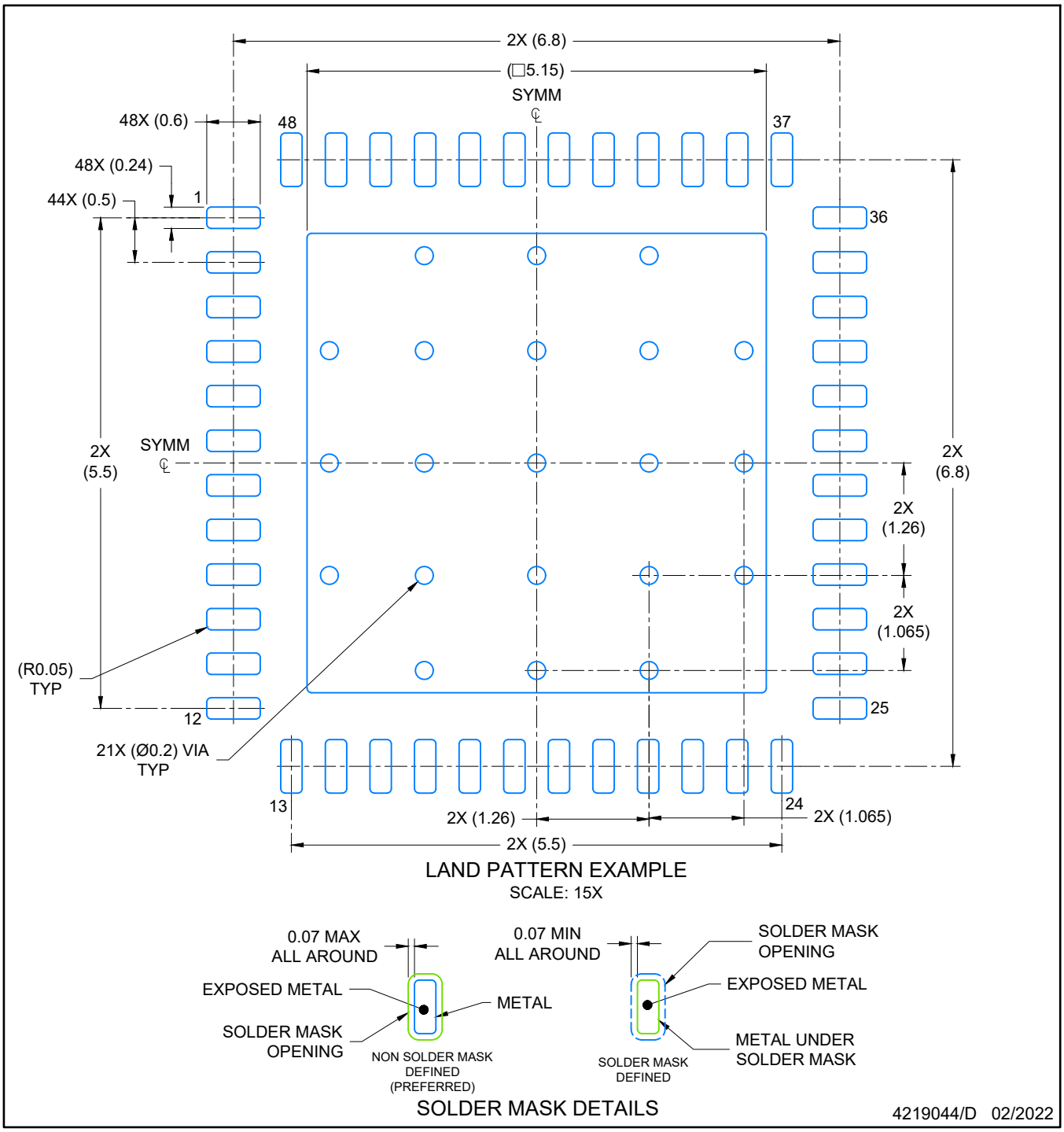
4224671/A

PLASTIC QUADFLAT PACK- NO LEAD



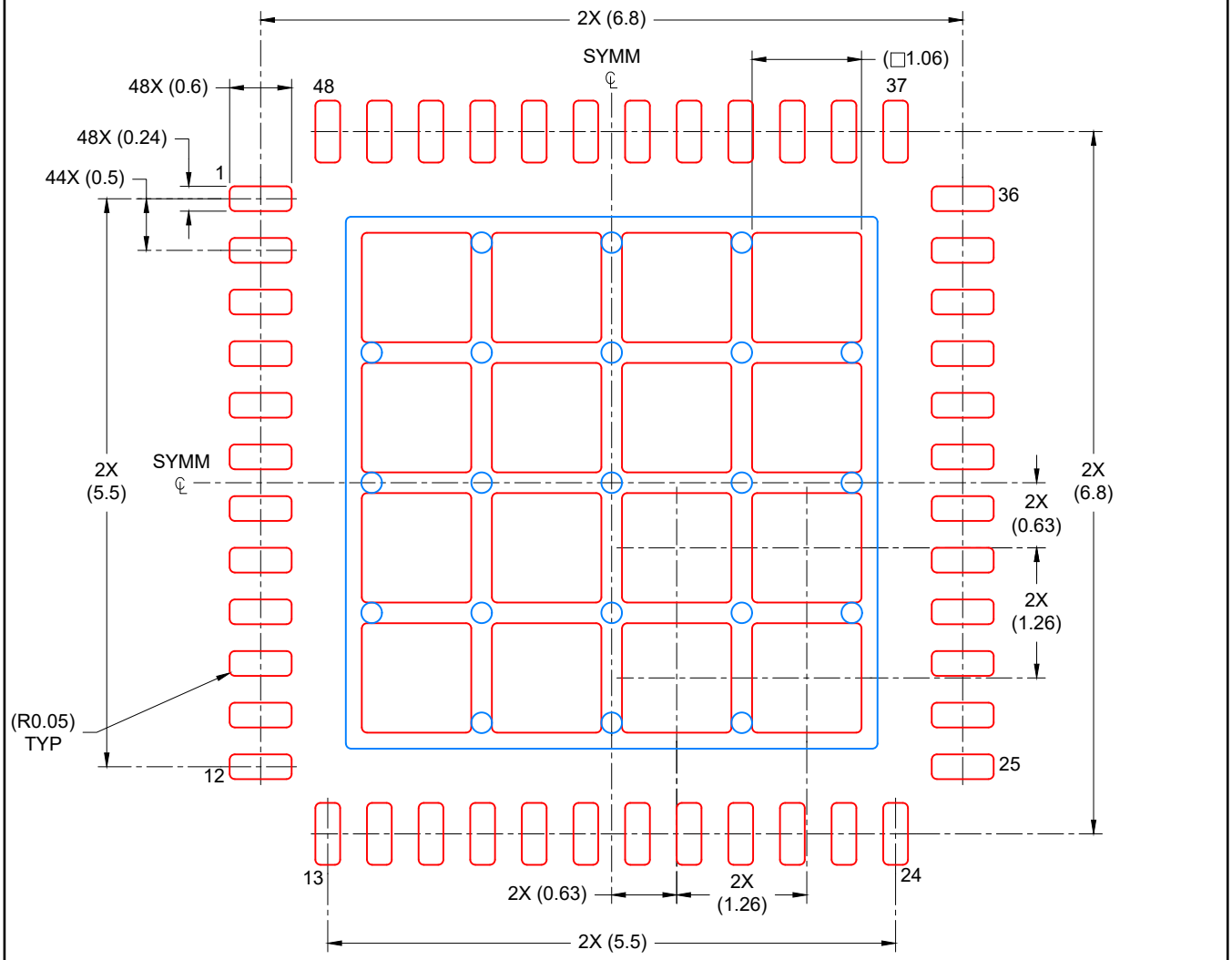
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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