

SN65LBC176-Q1 差分总线收发器

1 特性

- 符合汽车应用要求
- 双向收发器
- 符合或超出 ANSI 标准 RS-485 和 ISO 8482:1987(E) 的要求
- 高速低功耗 LinBiCMOS 电路
- 专为在串行和并行应用中实现高速运行而设计
- 低偏斜
- 适用于嘈杂环境中的长距离总线线路上的多点传输
- 超低禁用电源电流要求：200 μ A (最大值)
- 宽正负输入/输出总线电压范围
- 驱动器输出容量： ± 60 mA
- 热关断保护
- 驱动器正负电流限制
- 开路失效防护接收器设计
- 接收器输入灵敏度： ± 200 mV (最大值)
- 接收器输入迟滞：50mV (典型值)
- 由一个 5V 单电源供电运行
- 无干扰上电和断电保护

2 说明

SN65LBC176 差分总线收发器是单片集成电路，旨在实现多点总线传输线路上的双向数据通信。它专为平衡传输线路而设计，符合 ANSI 标准 RS-485 和 ISO 8482:1987(E)。

SN65LBC176 将一个三态差分线路驱动器和一个差分输入线路接收器组合在一起，这两个器件由一个 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于在禁用驱动器或 $V_{CC} = 0$ 时为总线提供最小负载。该端口具有较宽的正负共模电压范围，使得该器件适用于合用线应用。可以通过禁用驱动器和接收器来实现超低的器件待机电源电流。德州仪器 (TI) LinASIC 库中的驱动器和接收器均以单元形式提供。

此收发器适用于 ANSI 标准 RS-485 和 ISO 8482:1987 (E) 应用，前提是它们在此数据表的运行条件和特性部分中已指定。ANSI 标准 RS-485 和 ISO 8482:1987 (E) 中包含的某些限制不符合或无法在整个工作温度范围内进行测试。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN65LBC176-Q1	D (SOIC) (8)	4.90mm x 3.91mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

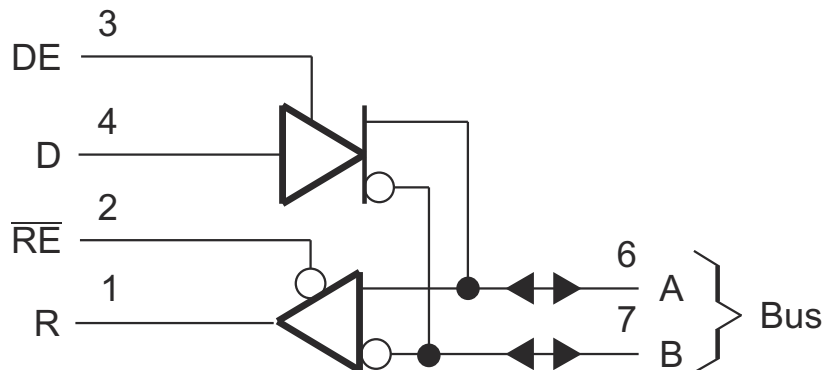


Table of Contents

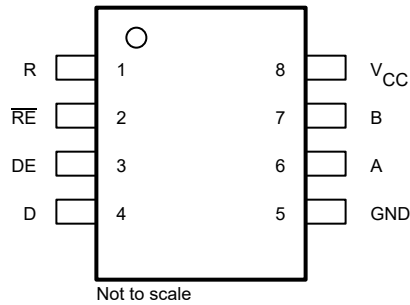
1 特性	1	Parameter Measurement Information	8
2 说明	1	6 Detailed Description	11
3 修订历史记录	2	6.1 Device Functional Modes.....	11
4 Pin Configuration and Functions	3	7 Device and Documentation Support	12
5 Specifications	4	7.1 Documentation Support.....	12
5.1 Absolute Maximum Ratings.....	4	7.2 接收文档更新通知.....	12
5.2 Recommended Operating Conditions.....	4	7.3 支持资源.....	12
5.3 Thermal Resistance Characteristics.....	5	7.4 Trademarks.....	12
5.4 Electrical Characteristics - Driver.....	5	7.5 静电放电警告.....	12
5.5 Switching Characteristics - Driver.....	6	7.6 术语表.....	12
5.6 Electrical Characteristics - Reciever.....	7	8 Mechanical, Packaging, and Orderable Information..	12
5.7 Switching Characteristics - Reciever.....	7		

3 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2003) to Revision B (January 2023)	Page
• 添加了封装信息表、引脚配置和实施、热性能信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 删除了订购信息表.....	1

4 Pin Configuration and Functions



**图 4-1. D Package, SOIC 8 Pins
(Top View)**

表 4-1. Pin Functions

NO	NAME	TYPE	DESCRIPTION
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Device ground
6	A	I/O	Bus I/O port, A (complementary to B)
7	B	I/O	Bus I/O port, B(complementary to A)
8	V _{CC}	P	5 V Supply Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{CC}	Supply voltage		7	V
	Voltage range at any bus terminal	-10	15	V
	Input voltage, V _I (D, DE, R, or $\overline{RE}$)	-0.3	V _{CC} + 0.5	V
T _A	Operating free-air temperature range	-40	125	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _I or V _{IC}	Voltage at any bus terminal (separately or common mode),				12	V
					-7	V
V _{IH}	High-level input voltage,	D, DE, and $\overline{RE}$	2			V
V _{IL}	Low-level input voltage,	D, DE, and $\overline{RE}$			0.8	V
V _{ID}	Differential input voltage ⁽¹⁾				±12	V
I _{OH}	High-level output current	Driver			60	mA
		Receiver			-400	μA
I _{OL}	Low-level output current	Driver			-60	mA
		Receiver			8	mA
T _A	Operating free-air temperature,		-40		125	°C

- (1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.3 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		SN65LBC176-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics - Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$ V_{OD1} $	Differential output voltage	$I_O = 0$		1.5		6	V
V_{OD3}	Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$	See Fig 2, ⁽²⁾	1.1			V
$ V_{OD2} $	Differential output voltage	$R_L = 54 \Omega$	See Fig 1, ⁽²⁾	1.1			V
$\Delta V_{OD} $	Change in magnitude of differential output voltage ⁽¹⁾	$R_L = 54 \Omega$ or 100Ω See Fig 1				±0.2	V
V_{OC}	Common-mode output voltage					-1	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage ⁽¹⁾					±0.2	V
I_O	Output current	Output disabled, ⁽³⁾	$V_O = 12 \text{ V}$			1	mA
			$V_O = -7 \text{ V}$			-0.8	mA
I_{IH}	High-level input current	$V_I = 2.4 \text{ V}$				-100	μA
I_{IL}	Low-level input current	$V_I = 0.4 \text{ V}$				-100	μA
I_{OS}	Short-circuit output current	$V_O = -7 \text{ V}$				-250	mA
		$V_O = 0 \text{ V}$				-150	mA
		$V_O = V_{CC}$				250	mA
		$V_O = 12 \text{ V}$				250	mA
I_{CC}	Supply current	$V_I = 0$ or V_{CC} , No Load	Receiver disabled and driver enabled			1.75	mA
			Receiver and driver disabled			0.25	mA

- (1) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input changes from a high level to a low level.
- (2) This device meets the ANSI Standard RS-485 VOD requirements above 0°C only.
- (3) This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

5.5 Switching Characteristics - Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$ $C_L = 50\ \text{pF}$ See Fig 3	8		31	ns
$t_{t(OD)}$	Differential output transition time			12		ns
$t_{sk(p)}$	Pulse skew ($ t_{d(ODH)} - t_{d(ODL)} $)				6	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$ See Figure 4			65	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$ See Figure 5			65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$ See Figure 4			105	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$ See Figure 5			105	ns

(1) All typical values are at $V_{CC} = 5\ \text{V}$, $T_A = 25^\circ\text{C}$.

5.5.1 Symbol Equivalents

Data Sheet Parameter	RS-485
V_O	V_{oa}, V_{ob}
$ V_{OD1} $	V_O
$ V_{OD2} $	$V_t (R_L = 54\ \Omega)$
$ V_{OD3} $	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - V_t $
V_{OC}	$ V_{OS} $
$\Delta V_{OC} $	$ V_{OS} - V_{OS} $
I_{OS}	None
I_O	I_{ia}, I_{ib}

5.6 Electrical Characteristics - Reciever

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$	$I_O = -0.4\text{ mA}$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$	$I_O = 8\text{ mA}$	-0.2 ⁽²⁾			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	(see Figure 4)			50		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18\text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$ $I_{OH} = -400\text{ }\mu\text{A}$	See Fig 6	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = 200\text{ mV}$ $I_{OL} = 8\text{ mA}$	See Fig 6			0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4\text{ V to } 2.4\text{ V}$				± 20	μA
I_I	Line input current	Other input = 0 $V^{(3)}$	$V_I = 12\text{ V}$			1	mA
			$V_I = -7$			-0.8	mA
I_{IH}	High-level enable-input current	$V_{IH} = 2.7\text{ V}$				-100	μA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4\text{ V}$				-100	μA
r_I	Input resistance			12			k Ω
I_{CC}	Supply current	$V_I = 0\text{ or } V_{CC}$, No Load	Receiver disabled and driver enabled			3.9	mA
			Receiver and driver disabled			0.25	mA

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

5.7 Switching Characteristics - Reciever

over operating free-air temperature range (unless otherwise noted), $C_L = 15\text{ pF}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level single-ended output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$ See Figure 7	11		37	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11		37	ns
$t_{sk(p)}$	Pulse skew ($ t_{d(ODH)} - t_{d(ODL)} $)				10	ns
t_{PZH}	Output enable time to high level	See Figure 8			35	ns
t_{PZL}	Output enable time to low level				35	ns
t_{PHZ}	Output disable time from high level	See Figure 8			35	ns
t_{PLZ}	Output disable time from low level				35	ns

Parameter Measurement Information

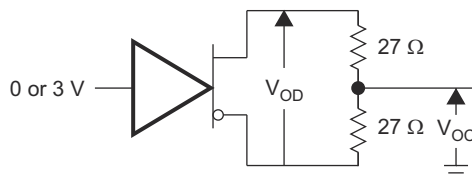


图 6-1. Driver V_{OD} and V_{OC}

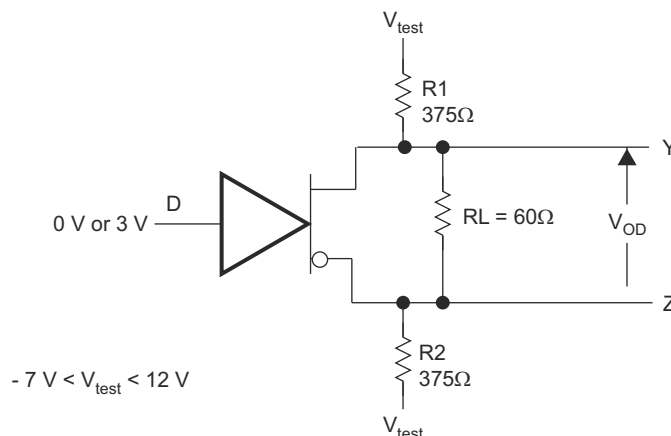
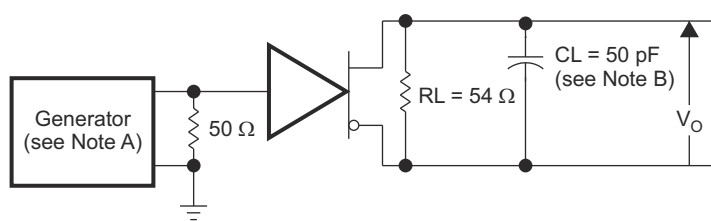
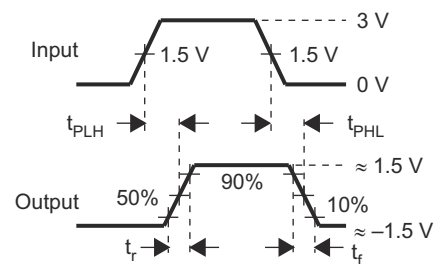


图 6-2. Driver V_{OD3}



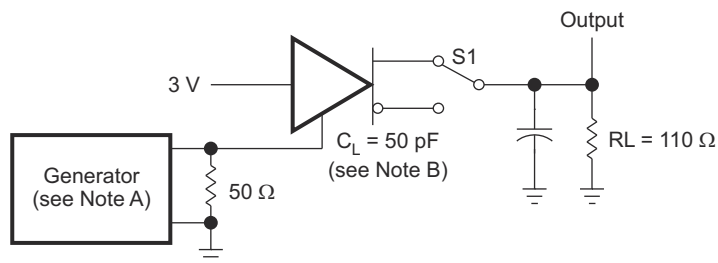
TEST CIRCUIT



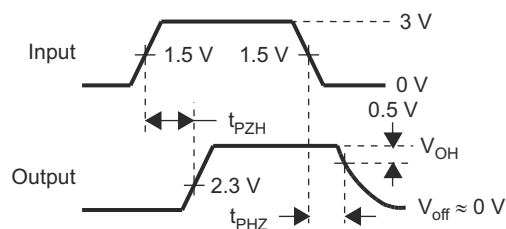
VOLTAGE WAVEFORMS

- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

图 6-3. Driver Test Circuit and Voltage Waveforms



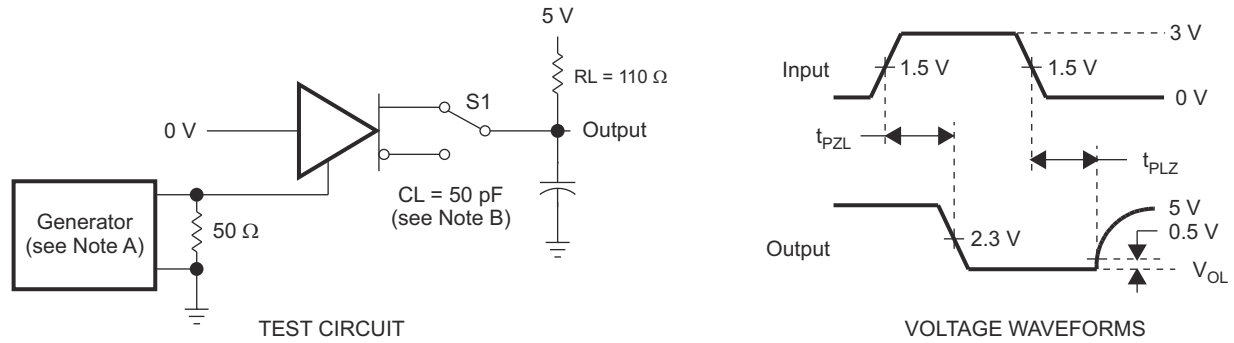
TEST CIRCUIT



VOLTAGE WAVEFORMS

- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

图 6-4. Driver Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

图 6-5. Driver Test Circuit and Voltage Waveforms

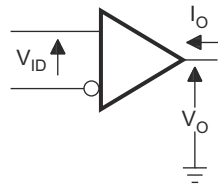
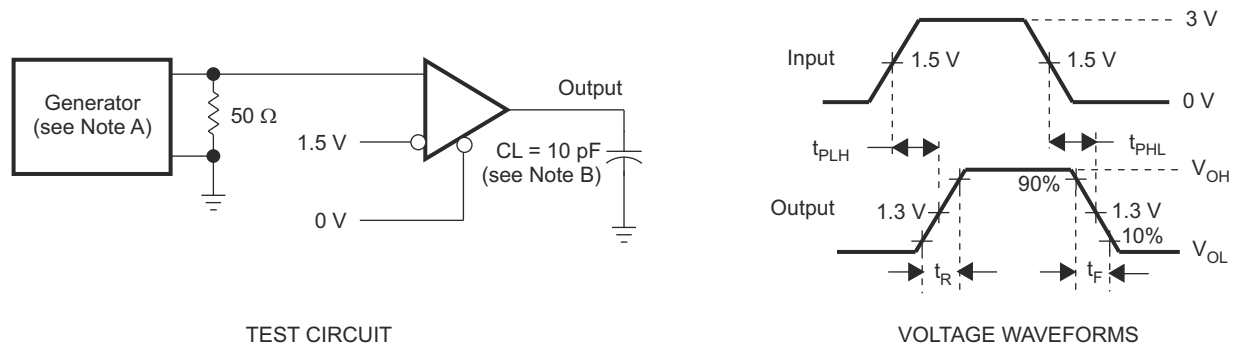
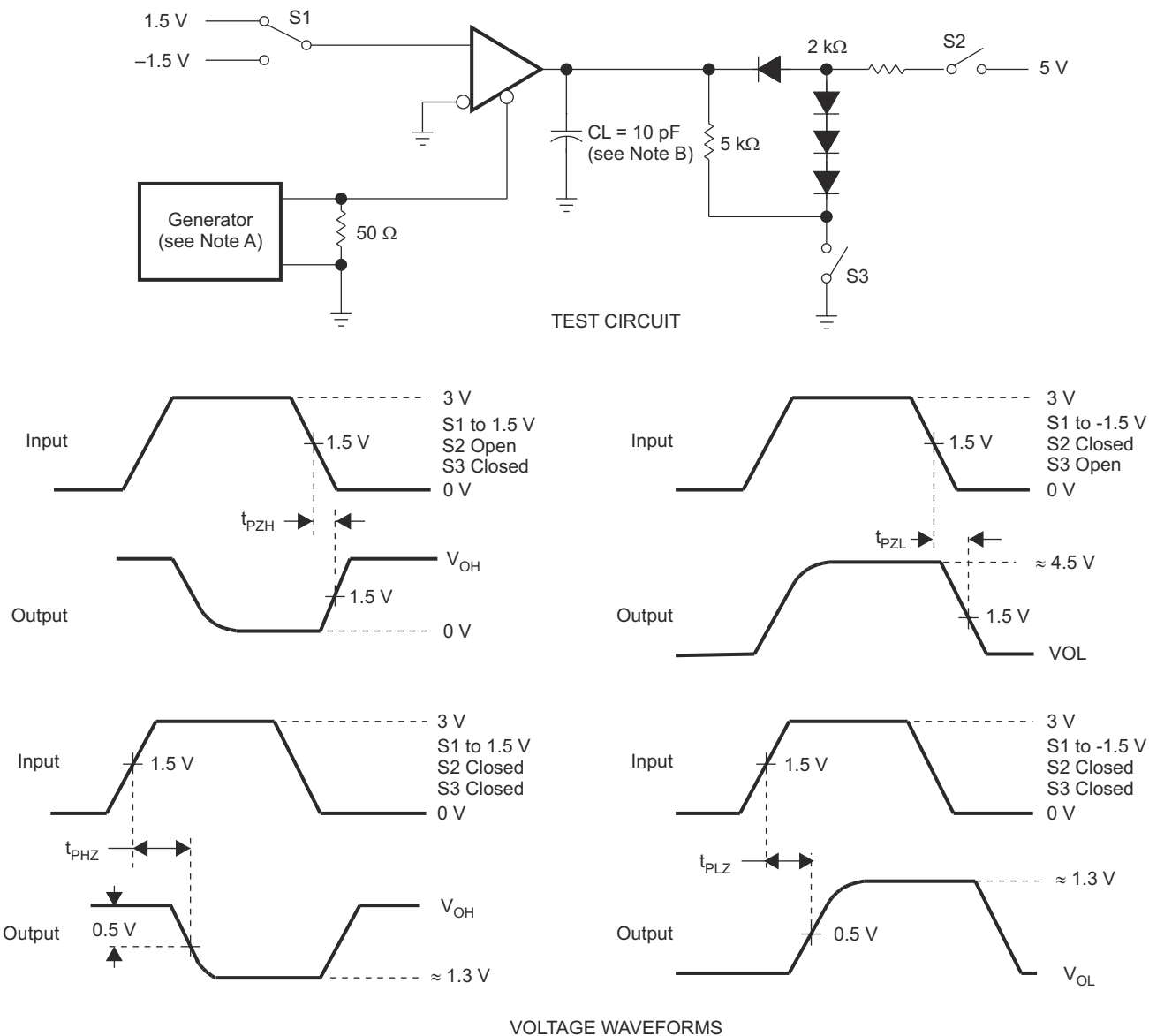


图 6-6. Receiver V_{OH} and V_{OL}



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

图 6-7. Receiver Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

图 6-8. Receiver Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Device Functional Modes

表 6-1. Function Table - Driver

Input ⁽¹⁾	Output	Outputs	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 6-2. Function Table - Receiver

Differential Inputs	ENABLE	Output
A-B	RE	R
$VID \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < VID < 0.2 \text{ V}$	L	?
$VID \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

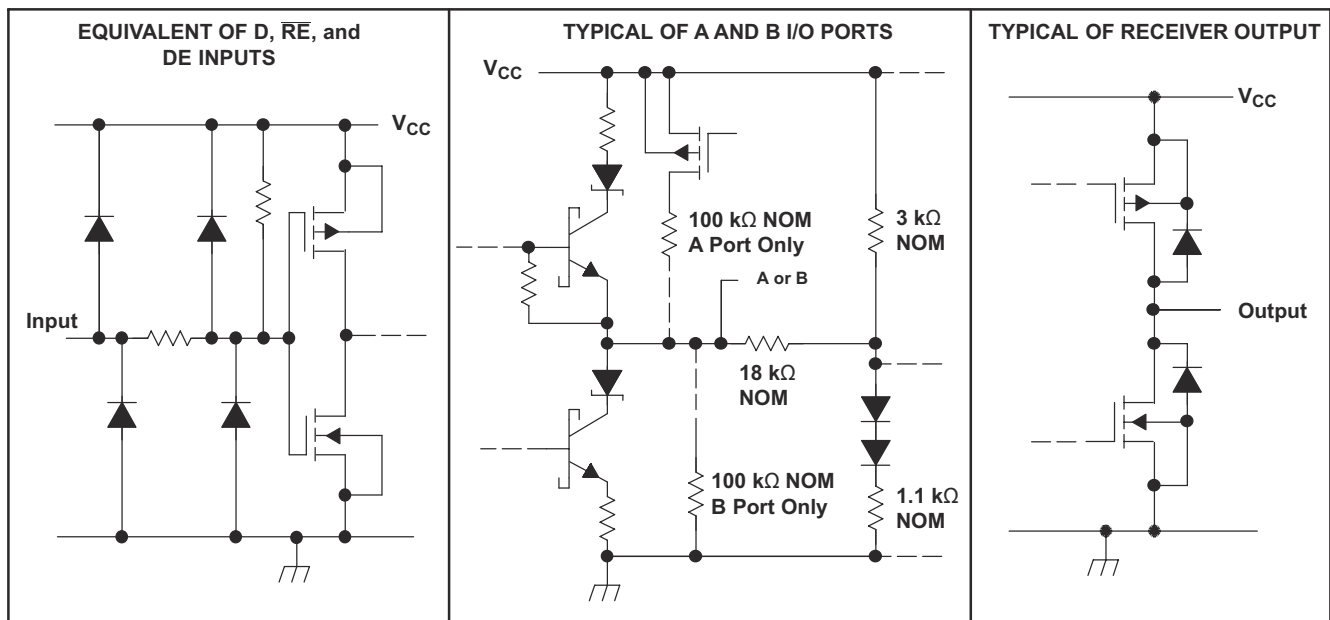


图 6-1. Schematics of Inputs and Outputs

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

7.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC176QDRG4Q1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1
SN65LBC176QDRG4Q1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1
SN65LBC176QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1
SN65LBC176QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LBC176-Q1 :

- Catalog : [SN65LBC176](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

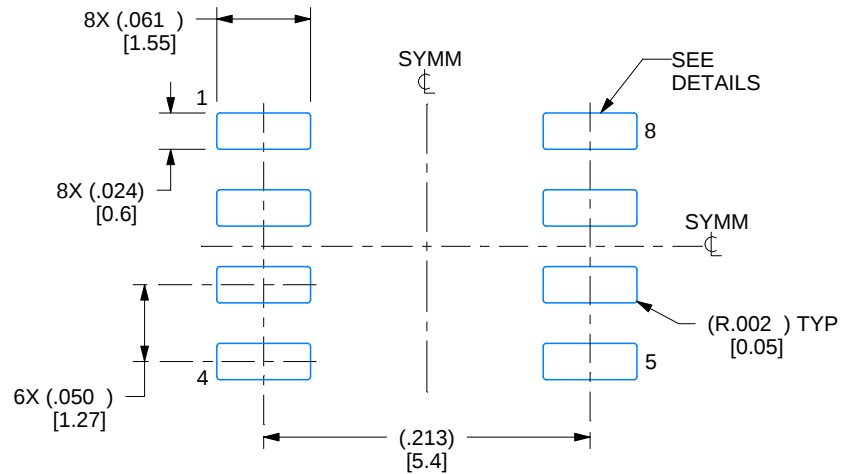


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

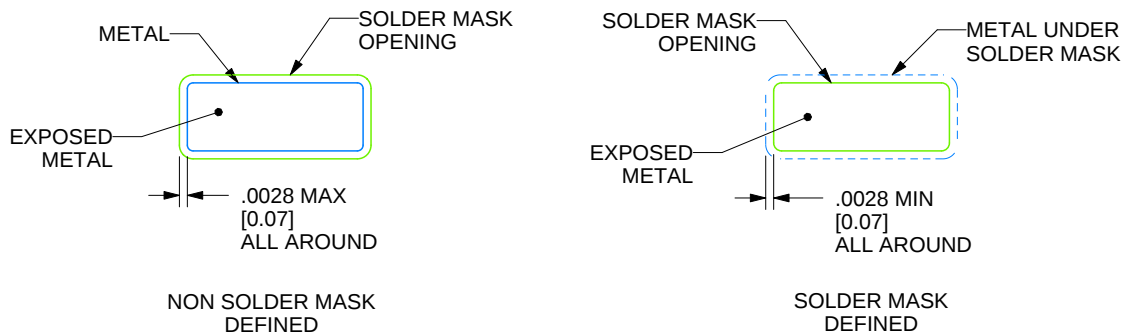
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

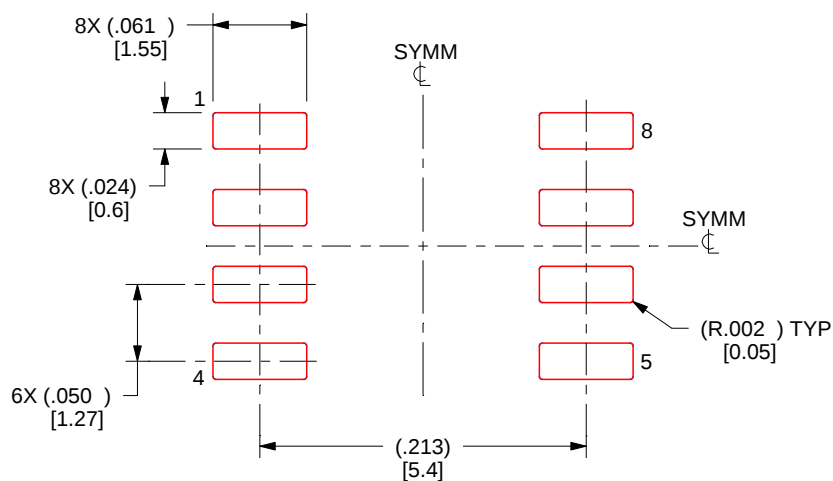
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月