TEXAS INSTRUMENTS

SN65LBC173A-EP 四路 RS-485 差分线路接收器

1 特性

- 专为 TIA/EIA-485、TIA/EIA-422 和 ISO 8482 应用 设计
- 信号传输速率 [1]高达 50Mbps
- 在总线短路、开路和空闲总线条件下提供故障保护
- 为总线输入提供的静电放电 (ESD) 保护电压超过 6kV
- 共模总线电压输入范围：-7V 至 12V
- 传播延迟时间 < 18ns
- 低待机功耗：< 32μA
- 针对 AM26LS32、DS96F173、LTC488 和 SN75173 进行引脚兼容升级

2 应用

- 支持国防、航天和医疗 应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 延长的产品生命周期
  - 延长产品的变更通知周期
  - 产品可追溯性

(1) 线路的信号传输速率是指每秒钟的电压转换次数，单位为 bps （每秒比特数）。

3 说明

SN65LBC173A 是一款具有三态输出的四路差分接收器，专为 TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422) 和 ISO 8482（欧盟的 RS-485）应用 而设计。

当数据速率高达甚至超过 5000bps 时，该器件针对均衡后的多点总线通信进行了优化。传输介质可采用双绞线电缆、印刷电路板走线或背板。最终数据传输速率和距离取决于介质衰减特性和环境噪声耦合。

接收器的正负共模输入电压范围较大， 其 ESD 保护电压高达 6kV，适用于严苛环境中的 高速多点数据传输 应用。这些器件通过 LinBiCMOS®进行设计，兼具低功耗特性和极强稳定性。

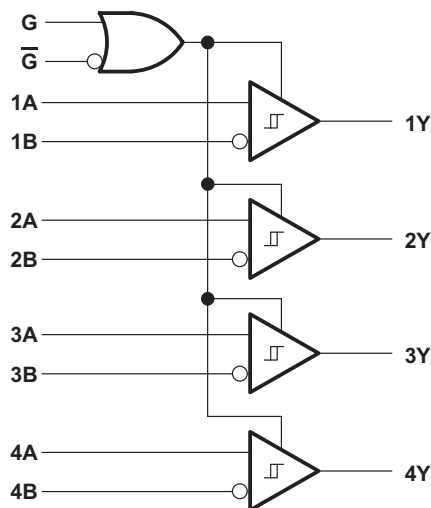G 和 $\overline{\text{G}}$ 输入为正/负逻辑提供使能控制逻辑，从而使能全部四个驱动器。禁用或关闭器件后，接收器输入针对总线呈现高阻抗状态，从而降低系统负载。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
SN65LBC173A-EP	SOIC (16)	9.90mm x 3.90mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

逻辑图

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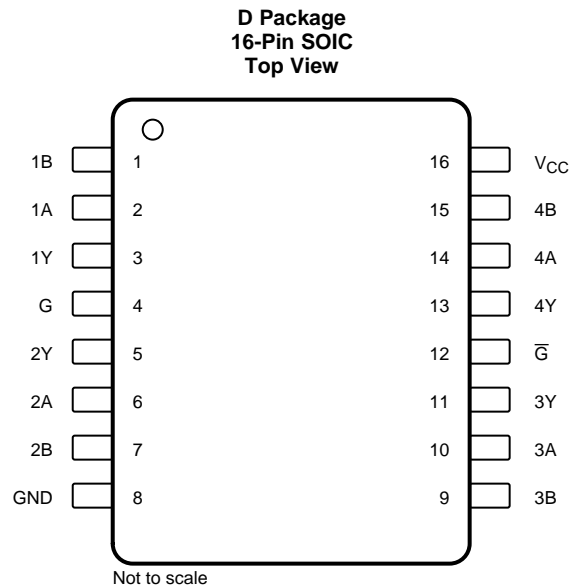English Data Sheet: SLLSEH1

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4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	最初发布版本。

5 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View

1B	1	16	V_{CC}
1A	2	15	4B
1Y	3	14	4A
G	4	13	4Y
2Y	5	12	$\overline{G}$
2A	6	11	3Y
2B	7	10	3A
GND	8	9	3B

Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS-485 differential input (noninverting).
1B	1	I	RS-485 differential input (inverting).
1Y	3	O	Logic level output.
2A	6	I	RS-485 differential input (noninverting).
2B	7	I	RS-485 differential input (inverting).
2Y	5	O	Logic level output.
3A	10	I	RS-485 differential input (noninverting).
3B	9	I	RS-485 differential input (inverting).
3Y	11	O	Logic level output.
4A	14	I	RS-485 differential input (noninverting).
4B	15	I	RS-485 differential input (inverting).
4Y	13	O	Logic level output.
$\overline{G}$	12	I	Active-low select.
G	4	I	Active-high select.
GND	8	—	Ground.
V_{CC}	16	—	Power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}[2]	−0.3	6	V
Voltage at any bus input (DC)	−10	15	V
Voltage at any bus input (transient pulse through 100 Ω, see 图 10)	−30	30	V
Input voltage at G and $\overline{G}$, V_I	−0.5	V_{CC} + 0.5	V
Receiver output current, I_O	−10	10	mA
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] — A and B to GND	±6000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] — All pins	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2] — All pins	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at any bus terminal	A, B	−7		12	V
V_{IH}	High-level input voltage	G, $\overline{G}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
	Output current	Y	−8		8	mA
T_J	Junction temperature		−55		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN65LBC173A-EP D (SOIC) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	78	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	39.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions

	PARAMETER	TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	$-7\ V \le V_{CM} \le 12\ V\ (V_{CM} = (V_A + V_B)\ /\ 2)$				−80	−10	mV
V_{IT-}	Negative-going differential input voltage threshold				−200	−120		mV
V_{HYS}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					40		mV
VIK	Input clamp voltage	$I_I = -18\ mA$			−1.5	−0.8		V
V_{OH}	High-level output voltage	$V_{ID} = 200\ mV$, $I_{OH} = -8\ mA$	See 图 6		2.7	4.8		V
V_{OL}	Low-level output voltage	$V_{ID} = -200\ mV$, $I_{OL} = 8\ mA$				0.2	0.4	V
I_{OZ}	High-impedance-state output current	$V_O = 0\ V$ to V_{CC}			−1		1	µA
I_I	Line input current	Other input at 0 V, $V_{CC} = 0\ V$ or 5 V	$V_I = 12\ V$				0.9	mA
			$V_I = -7\ V$		−0.7			
I_{IH}	High-level input current	Enable inputs G, $\overline{G}$					110	µA
I_{IL}	Low-level input current				−100			µA
R_I	Input resistance	A, B inputs			12			kΩ
I_{CC}	Supply current	$V_{ID} = 5\ V$	G at 0 V, $\overline{G}$ at V_{CC}				32	µA
		No load	G at V_{CC}, $\overline{G}$ at 0 V			11	16	mA

(1) All typical values are at $V_{CC} = 5\ V$ and 25°C.

6.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Differential output voltage rise time	$V_{ID} = -3\ V$ to 3 V, See 图 7		2	7	ns
t_f	Differential output voltage fall time			2	7	ns
t_{PLH}	Propagation delay time, low-to-high level output		8	12	18	ns
t_{PHL}	Propagation delay time, high-to-low level output		8	12	18	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 图 8		27	39	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance			7	24	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See 图 9		29	39	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance			12	18	ns
$t_{sk(p)}$	Pulse skew ($|t_{PLH} - t_{PHL}|$)			0.2	2	ns
$t_{sk(o)}$	Output skew[1]				3	ns
$t_{sk(pp)}$	Part-to-part skew[2]				3	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.
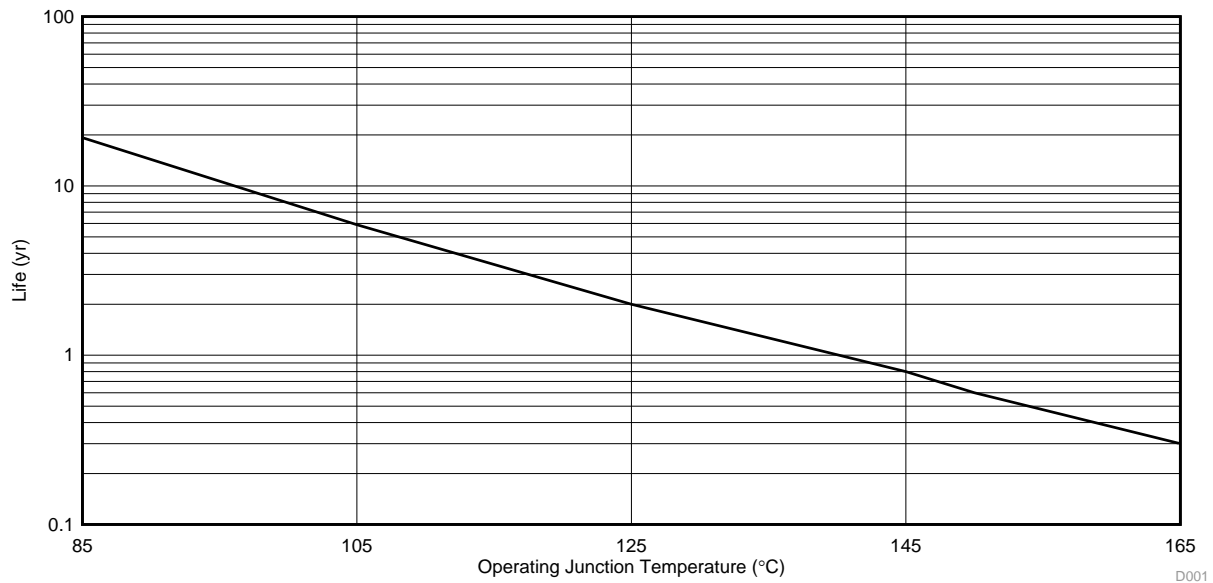
(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

图 1. **SN65LBC173A-EP Wirebond Life Derating Chart**
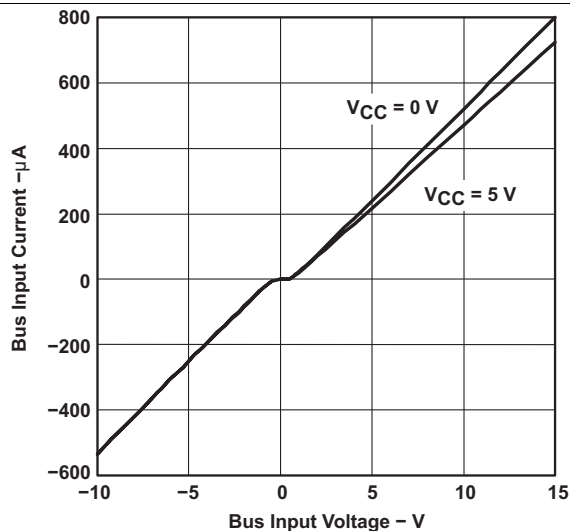
6.7 Typical Characteristics
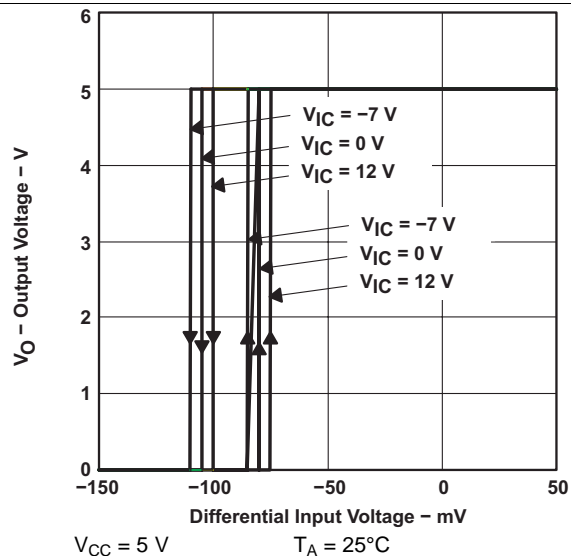

图 2. Bus Input Current vs Bus Input Voltage

$V_{CC} = 5\ V$ $T_A = 25°C$
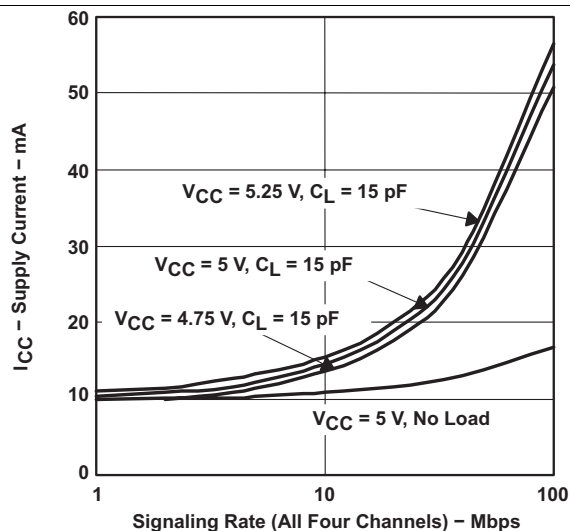
图 3. Output Voltage vs Differential Input Voltage

图 4. Supply Current vs Signaling Rate (All Four Channels)
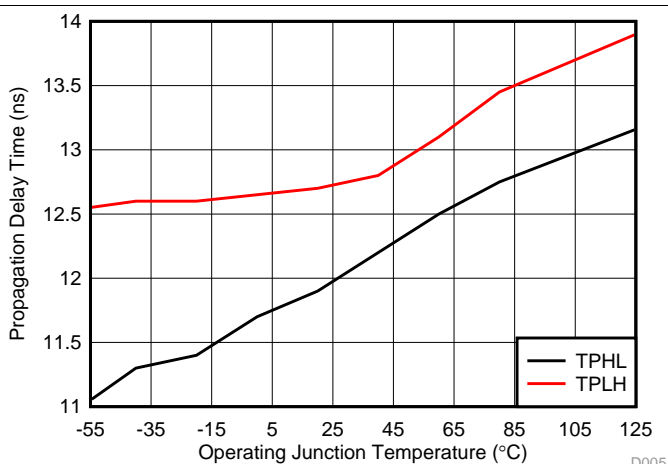

图 5. Propagation Delay Time vs Free-Air Temperature

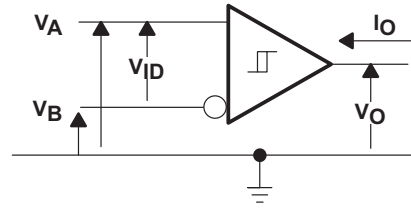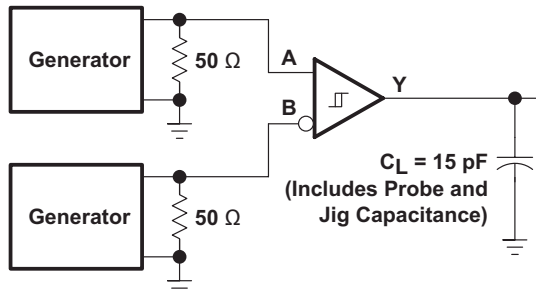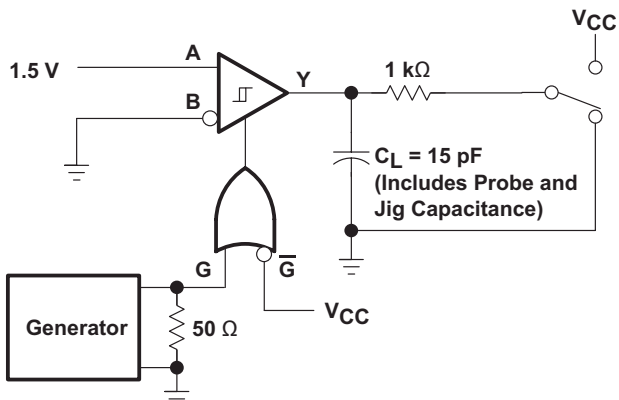# 7 Parameter Measurement Information

图 6. **Voltage and Current Definitions**

Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

图 7. **Switching Test Circuit and Waveforms**

Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

图 8. **Test Circuit Waveforms, t_{PZH} and t_{PHZ}**

Parameter Measurement Information (接下页)

Generators: PRR = 1 MHz, 50% Duty Cycle,
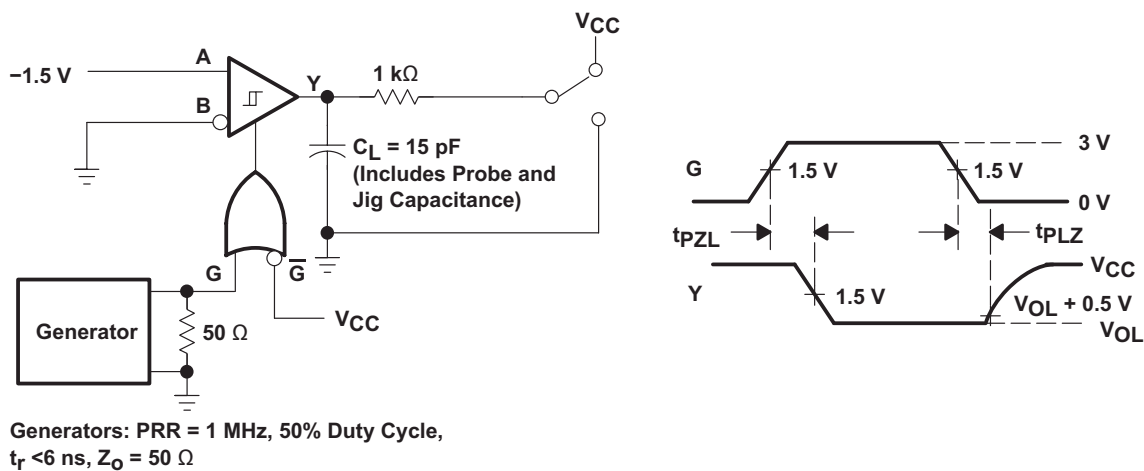t_r **<6 ns, Z_O = 50 Ω**

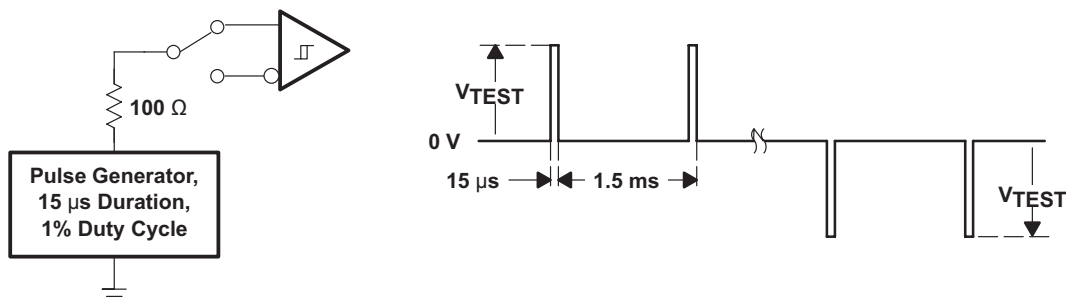图 9. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

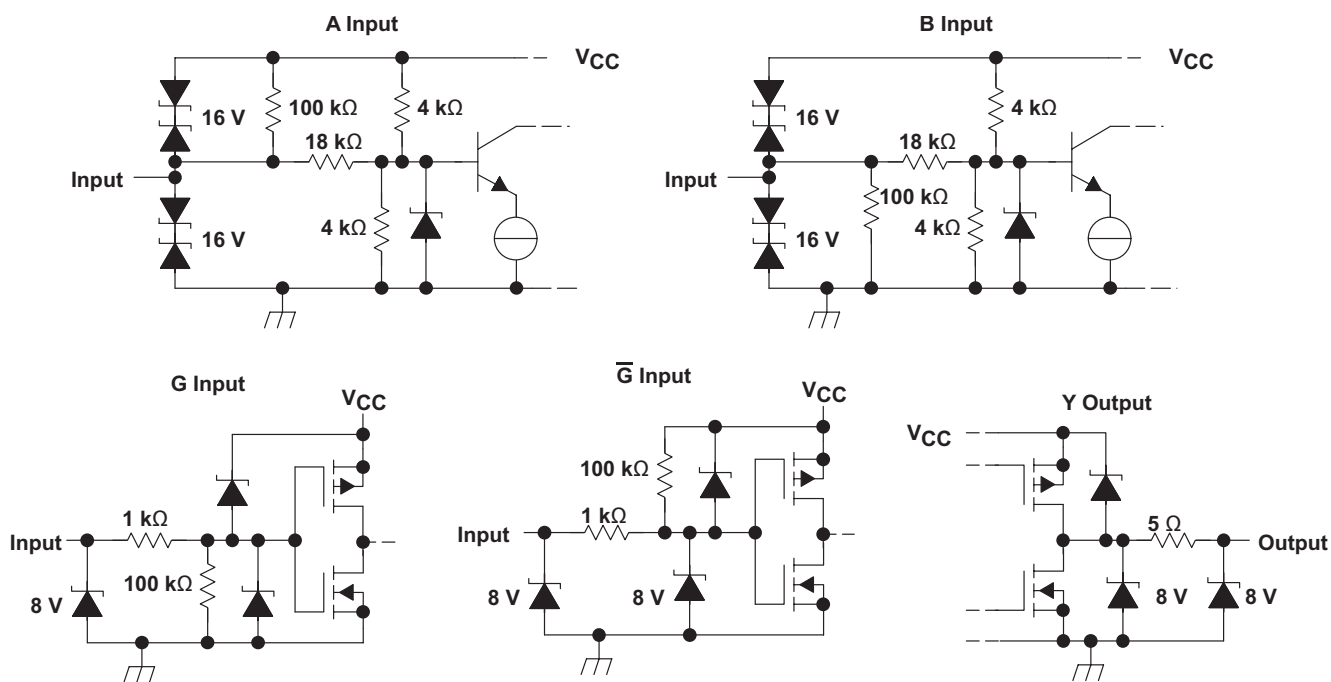图 10. Test Circuit and Waveform, Transient Over-Voltage Test

图 11. Equivalent Input and Output Schematic Diagrams

8 Detailed Description

8.1 Overview

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

The G and $\overline{G}$ inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

8.2 Functional Block Diagram

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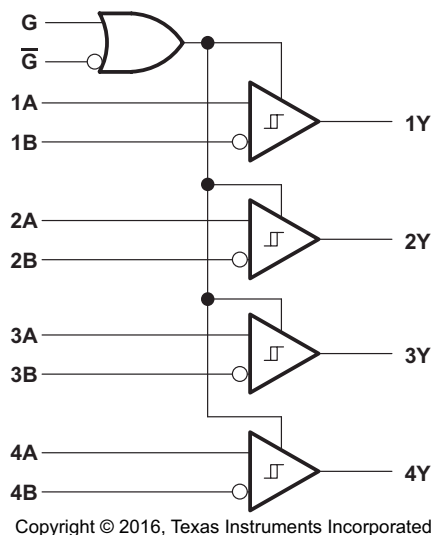
8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.4 Device Functional Modes

The receivers implemented in these RS-485 device can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

表 1. Function Table[1]

INPUT	ENABLES		OUTPUT
A - B (V_{ID})	G	$\overline{G}$	Y
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	
-0.2 V $< V_{ID} < -0.01$ V	H	X	?
	X	L	
-0.01 V $\leq V_{ID}$	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate
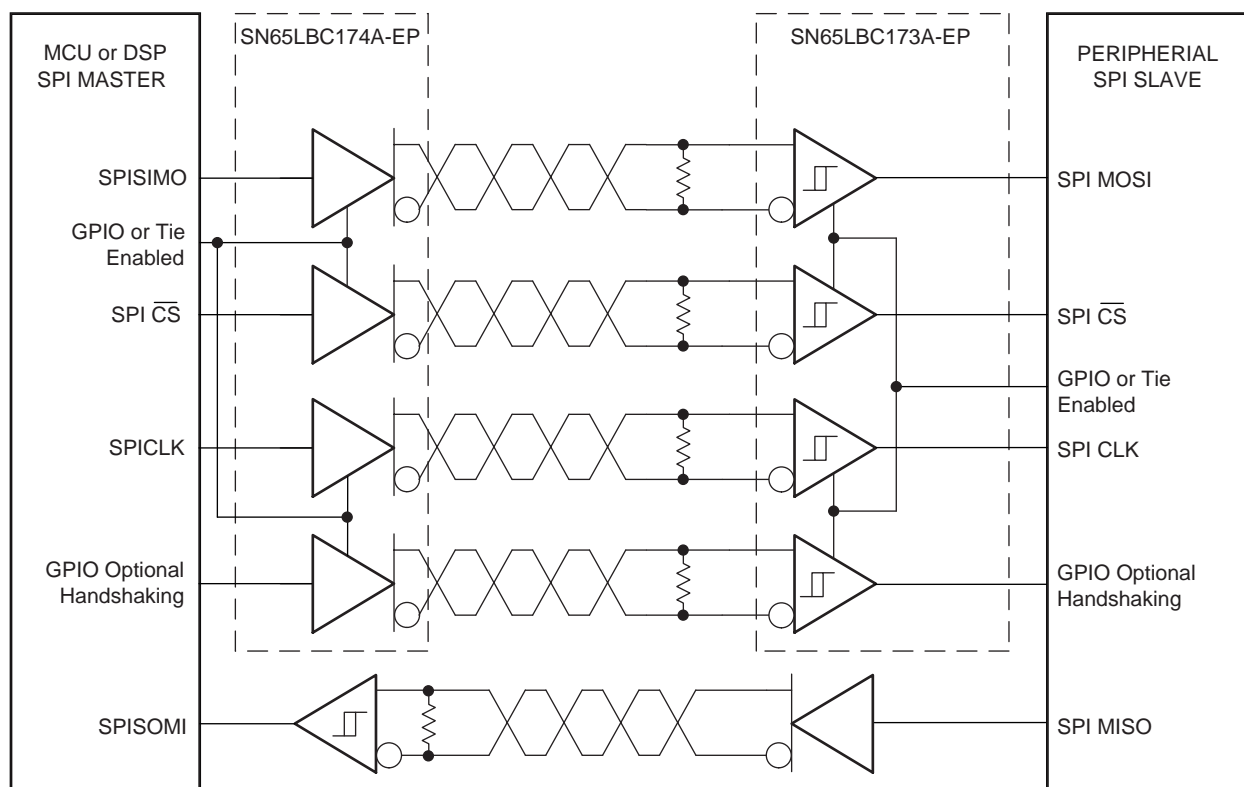
9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Extending SPI operation over RS-485 link.

9.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.

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图 12. **DSP-to-DSP Link via Serial Peripheral Interface**

9.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

9.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled.

Typical Application (接下页)

The link shown can operate at up to 50 Mbps, well within the capability of most SPI links.
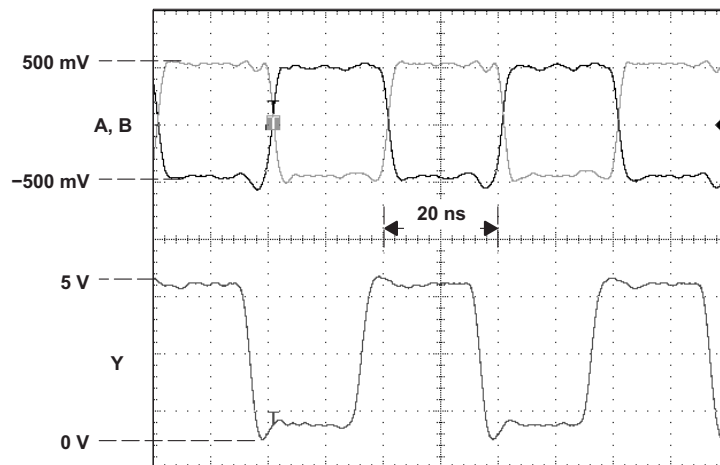
9.2.3   Application Curves

图 13. Receiver Inputs and Outputs, 50-Mbps Signaling Rate

10 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to buss as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
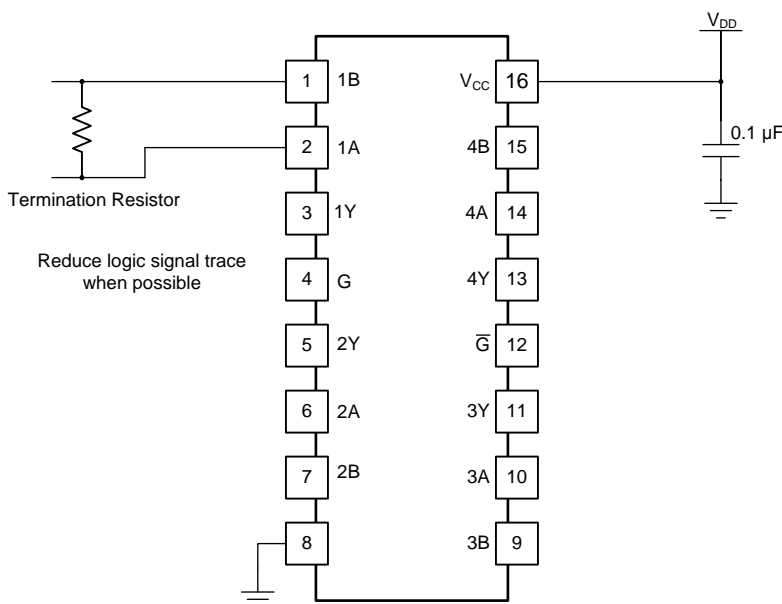
11.2 Layout Example

图 14. **Layout with PCB Recommendations**

12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.2 社区资源

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TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC173AMDREP	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP
SN65LBC173AMDREP.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP
V62/13623-02XE	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
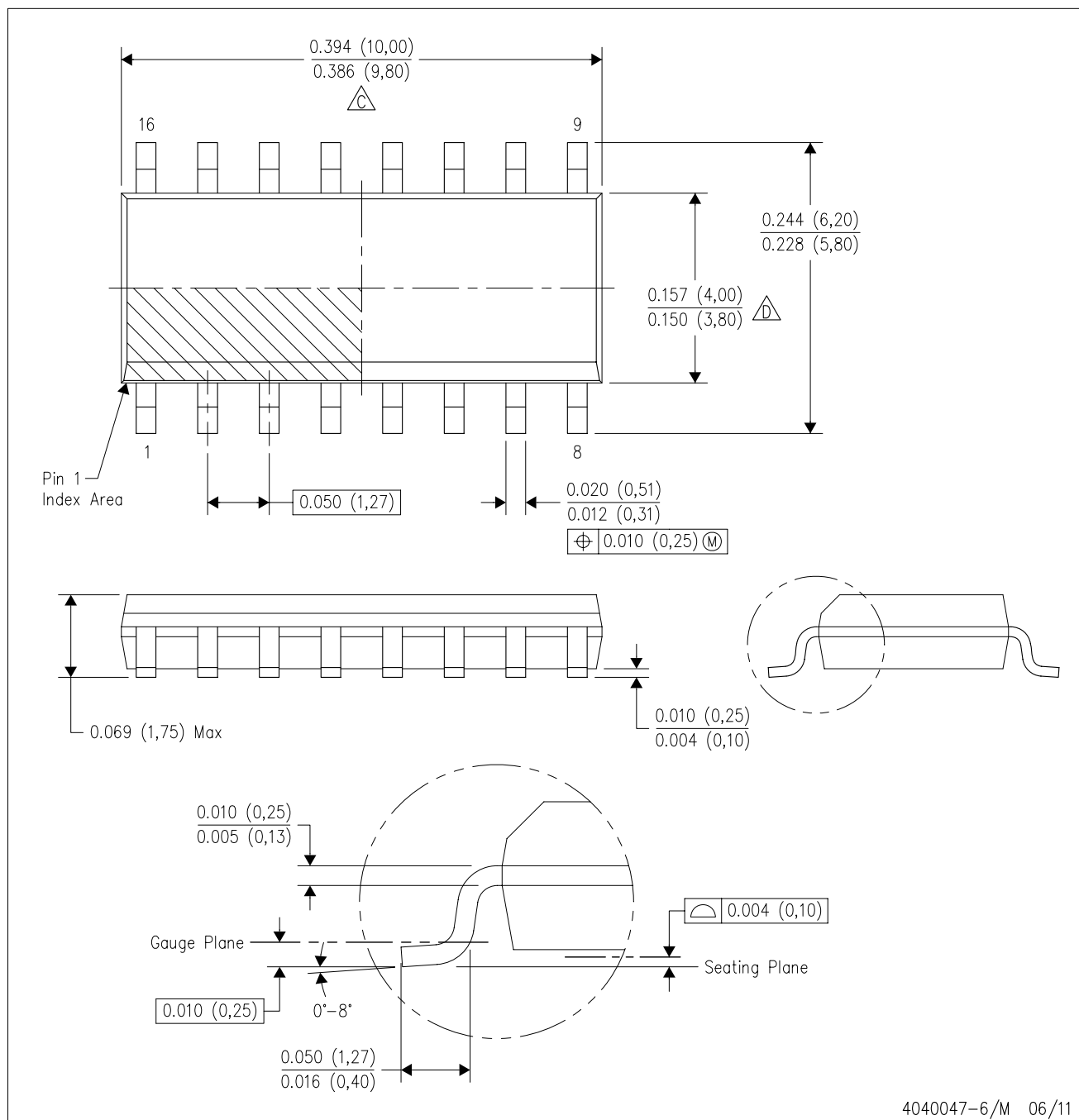
OTHER QUALIFIED VERSIONS OF SN65LBC173A-EP :

● Catalog : SN65LBC173A

PACKAGE OPTION ADDENDUM

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⟋C⟍

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟋D⟍

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

△ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
     ⟋C⟍ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
     ⟋D⟍ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

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