

## 低功耗、3.3V 电源全双工 RS-485 驱动器/接收器

查询样品: **SN65HVD37**

### 特性

- 低电流待机模式:  $<1\ \mu\text{A}$  典型值
- 工作静态电流  $<1\ \text{mA}$
- 为避免噪声干扰的高接收器迟滞 (典型值  $60\text{mV}$ )
- $1/8$  单位负载 (在总线上多达 **256** 个结点)
- 超过 **15 kV HBM** 的总线引脚 **ESD** 保护
- 用于高达 **20 Mbps** 信号传输速度的驱动器输出转换时间优化
- 用于带电插入应用的无波形干扰的加电和断电保护
- **5V**-容错逻辑输入
- 总线空闲、打开和短路故障安全
- 驱动器电流限制和热关断
- 全面符合所有**TIA-485-A** 规范

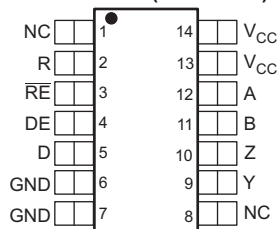
### 应用

- 电信设备
- 工业自动化
- 过程自动化
- 楼宇自动化
- 销售点 (**POS**) 终端
- 是 **ADM3076**, **ADM3491**, **LTC2852**, **MAX3491** 和 **SP3491** 的改良替代产品

### 说明

SN65HVD37 将一个强健的差分驱动器和一个具有高抗噪性的接收器结合在一起以满足要求严格的工业应用的需要。这个驱动器的差分输出和接收器的差分输入是分离的引脚,这样的话就形成了一个用于全双工(四线制)通讯的总线端口。这个驱动器和接收器可以独立启用并特有一个宽泛的共模电压范围,这使得此设备适合在长线缆上运行的多点应用。SN65HVD37 额定工作温度范围为  $-40^{\circ}\text{C}$  至  $85^{\circ}\text{C}$ 。

#### D PACKAGE (TOP VIEW)



NC - No internal connection

#### LOGIC DIAGRAM (POSITIVE LOGIC)

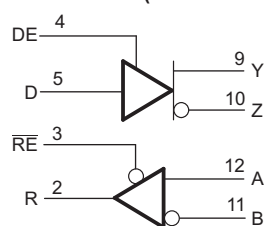


图 1. 为避免噪声干扰的**60 mV** 接收器迟滞



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated  
English Data Sheet: **SLLSE92**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		VALUE/UNITS
V <sub>CC</sub>	Supply voltage	–0.5 V to 7 V
	Voltage range at A, B, Y, Z pins	–13 V to 13 V
	Input voltage range at any logic pin	–0.3 V to 5.7 V
	Voltage range, transient pulse, A, B, Y, Z, through 100Ω	–25 V to 25 V
	Receiver output current	–24 mA to 24 mA
T <sub>J</sub>	Junction temperature	170°C
	Continuous total power dissipation	(see Thermal Table)
	IEC 60749-26 ESD (Human Body Model), bus terminals and GND	±16 kV
JEDEC Standard 22	Test Method A114 (Human Body Model), all pins	±5 kV
	Test Method C101 (Charged Device Model), all pins	±1.5 kV
JEDEC Standard 22	Test Method A115 (Machine Model), all pins	±150 V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		SN65HVD37	UNITS
		D	
		14 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	79.3	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	44.8	
θ <sub>JB</sub>	Junction-to-board thermal resistance	33.5	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	33.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	3	3.3	3.6	V
V <sub>I</sub>	Input voltage at any bus terminal (separately or common mode) <sup>(2)</sup>	–7		12	V
V <sub>IH</sub>	High-level input voltage (Driver, driver enable, and receiver enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (Driver, driver enable, and receiver enable inputs)	0		0.8	V
V <sub>ID</sub>	Differential input voltage	–12		12	V
I <sub>O</sub>	Output current	Driver		60	mA
		Receiver		8	
R <sub>L</sub>	Differential load resistance	54	60		Ω
C <sub>L</sub>	Differential load capacitance		50		pF
	Signaling rate	HVD37		20	Mbps
T <sub>A</sub>	Operating free-air temperature (See application section for thermal information)	–40		85	°C
T <sub>J</sub>	Junction Temperature	–40		150	°C

- (1) Both pins 13 and 14 should be connected to the supply voltage; both pins 6 and 7 should be connected to ground.  
 (2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Driver differential output voltage magnitude	See Figure 1, R <sub>L</sub> = 60 Ω, V <sub>CC</sub> ≥ 3.15 V, 375 Ω on each output to −7 V to 12 V		1.5	1.9		V
		R <sub>L</sub> = 54 Ω (RS-485)	See Figure 3	1.5	2		V
		R <sub>L</sub> = 100 Ω (RS-422), T <sub>J</sub> ≥ 25°C, V <sub>CC</sub> ≥ 3.3 V		2	2.2		V
Δ V <sub>OD</sub>	Change in magnitude of driver differential output voltage	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF		−0.1	0	0.1	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	Center of two 27-Ω load resistors, C <sub>L</sub> = 50 pF	See Figure 3	1.5	V <sub>CC</sub> /2	2.5	V
ΔV <sub>OC</sub>	Change in differential driver output common-mode voltage			−0.1	0	0.1	V
V <sub>OC(PP)</sub>	Peak-to-peak driver common-mode output voltage				400		mV
C <sub>ID</sub>	Differential input capacitance	A, B			3		pF
C <sub>OD</sub>	Differential output capacitance	Y, Z			14		pF
V <sub>IT+</sub>	Positive-going receiver differential input voltage threshold			See <sup>(1)</sup>	−60	−20	mV
V <sub>IT−</sub>	Negative-going receiver differential input voltage threshold			−200	−120	See <sup>(1)</sup>	mV
V <sub>HYS</sub>	Receiver differential input voltage threshold hysteresis (V <sub>IT+</sub> − V <sub>IT−</sub> )			30	60		mV
V <sub>OH</sub>	Receiver high-level output voltage	I <sub>OH</sub> = −8 mA		2.4	V <sub>CC</sub> −0.3		V
V <sub>OL</sub>	Receiver low-level output voltage	I <sub>OL</sub> = 8 mA			0.2	0.4	V
I <sub>I</sub>	Driver input, driver enable, and receiver enable input current			−2		2	μA
I <sub>OZ</sub>	Receiver output high-impedance current	V <sub>O</sub> = 0 V or V <sub>CC</sub> , $\overline{\text{RE}}$ at V <sub>CC</sub>		−1		1	μA
I <sub>OS</sub>	Driver short-circuit output current			−250		250	mA
I <sub>I</sub>	Bus input current (disabled driver)	V <sub>CC</sub> = 3 to 3.6 V or V <sub>CC</sub> =0 V, DE at 0 V	V <sub>I</sub> = 12 V		75	125	μA
			V <sub>I</sub> = −7 V	−100	−40		
I <sub>CC</sub>	Supply current, steady-state, no load (quiescent)	Driver and Receiver enabled	DE = V <sub>CC</sub> , RE = GND		720	850	μA
		Driver enabled, receiver disabled	DE = V <sub>CC</sub> , RE = V <sub>CC</sub>			400	μA
		Driver disabled, receiver enabled	DE = GND, RE = GND			800	μA
		Driver and receiver disabled (standby)	DE = GND, D = open, RE = V <sub>CC</sub>		0.2	1	μA
Supply current (dynamic)		See “TYPICAL CHARACTERISTICS” section					

(1) Under any specific conditions,  $V_{IT+}$  is assured to be at least  $V_{HYS}$  higher than  $V_{IT-}$ .

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t <sub>r</sub> , t <sub>f</sub>	Driver differential output rise/fall time	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF, See <a href="#">Figure 4</a>		3	6	14	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay			10		20	
t <sub>SK(P)</sub>	Driver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>			1			
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time	See <a href="#">Figure 5</a> and <a href="#">Figure 6</a>		20	50	ns	
t <sub>PZH</sub> , t <sub>PZL</sub>	Driver enable time	Receiver enabled	See <a href="#">Figure 5</a> and <a href="#">Figure 6</a>	8	25	ns	
		Receiver disabled		2.6	8	μs	
RECEIVER							
t <sub>r</sub> , t <sub>f</sub>	Receiver output rise/fall time	C <sub>L</sub> = 15 pF, See <a href="#">Figure 7</a>		2	5	9	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Receiver propagation delay time			40	50	75	ns
t <sub>SK(P)</sub>	Receiver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>			2	5	ns	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Receiver disable time			15	25	ns	
t <sub>PZL(1)</sub> , t <sub>PZH(1)</sub> , t <sub>PZL(2)</sub> , t <sub>PZH(2)</sub>	Receiver enable time	Driver enabled, See <a href="#">Figure 8</a>		35	50	ns	
		Driver disabled, See <a href="#">Figure 8</a>		3	8	μs	

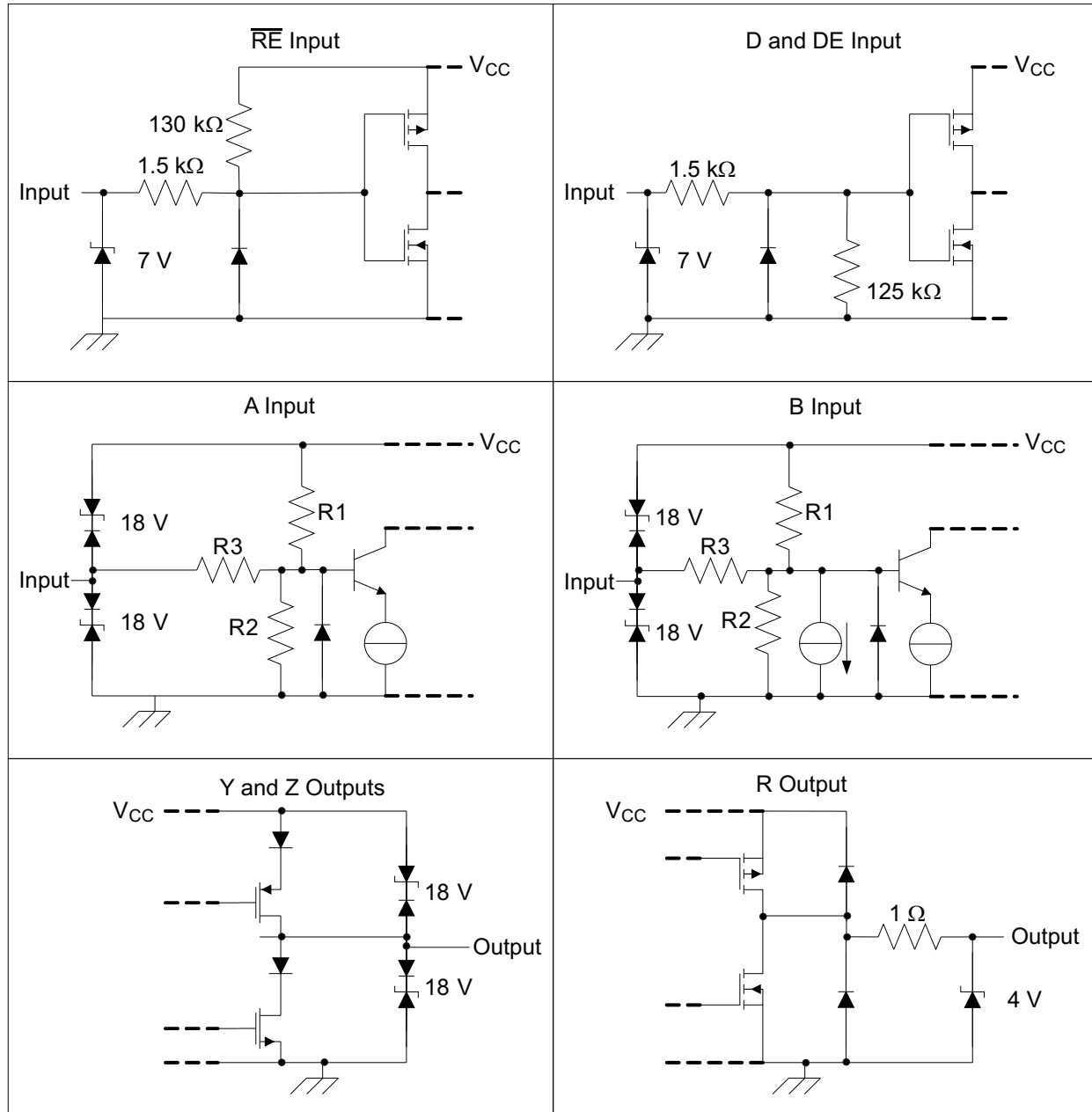
**DRIVER FUNCTION TABLE**

INPUT	ENABLE	OUTPUTS		
D	DE	Y	Z	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

**RECEIVER FUNCTION TABLE**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

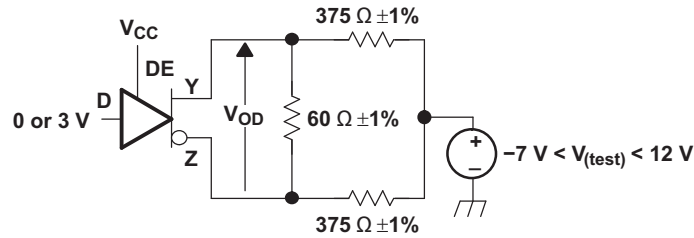
## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



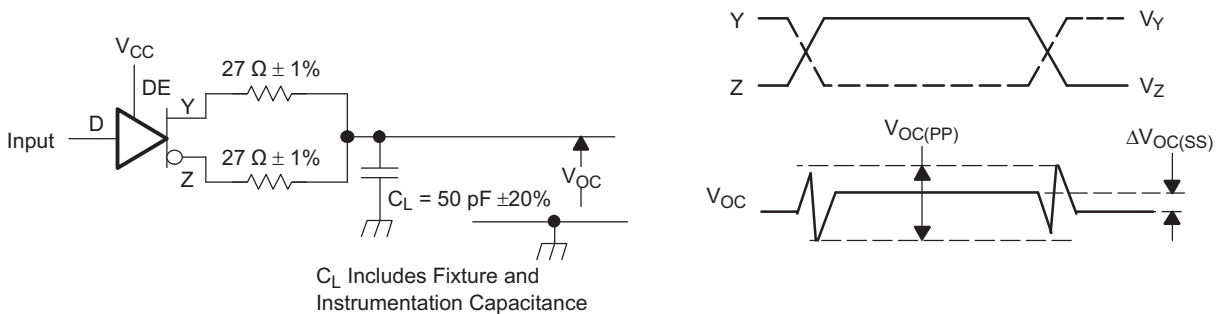
	<b>R1/R2</b>	<b>R3</b>
SN65HVD37	18 kΩ	190 kΩ

## PARAMETER MEASUREMENT INFORMATION

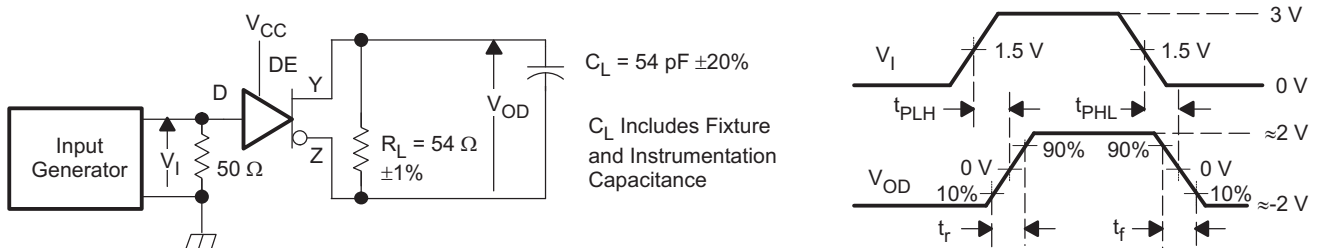
Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50  $\Omega$



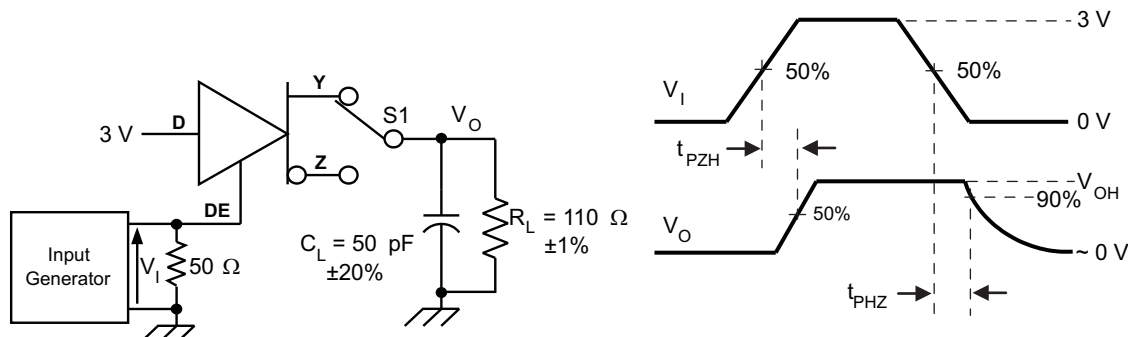
**Figure 2. Measurement of Driver Differential Output Voltage With Common-mode Load**



**Figure 3. Measurement of Driver Differential and Common-mode Output with RS-485 Load**



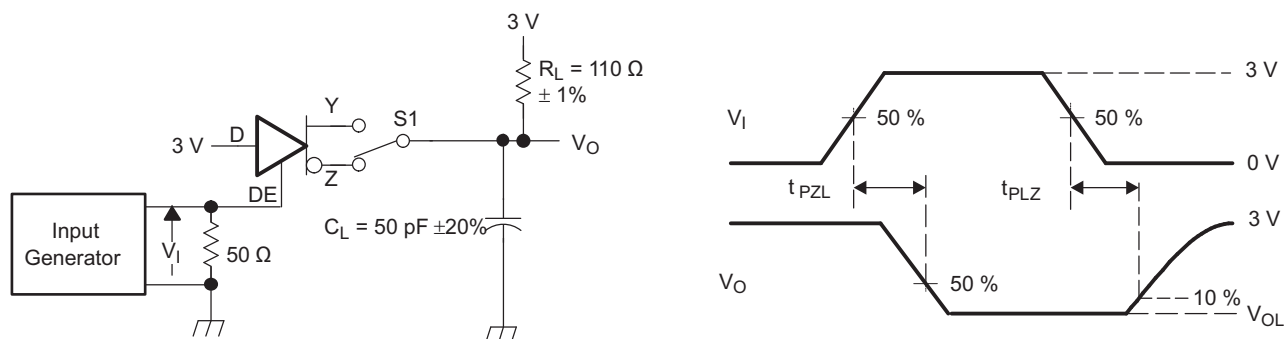
**Figure 4. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays**



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.  
CL includes Fixture and Instrumentation Capacitance

**Figure 5. Measurement of Driver Enable and Disable Times with Active High Output and Pull-down Load**

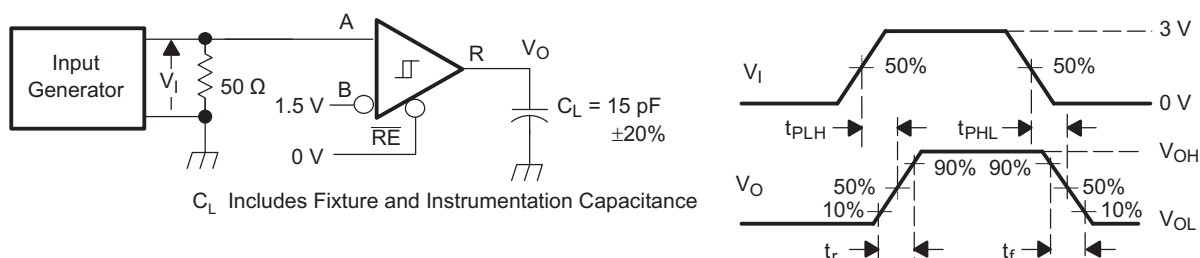
## PARAMETER MEASUREMENT INFORMATION (continued)



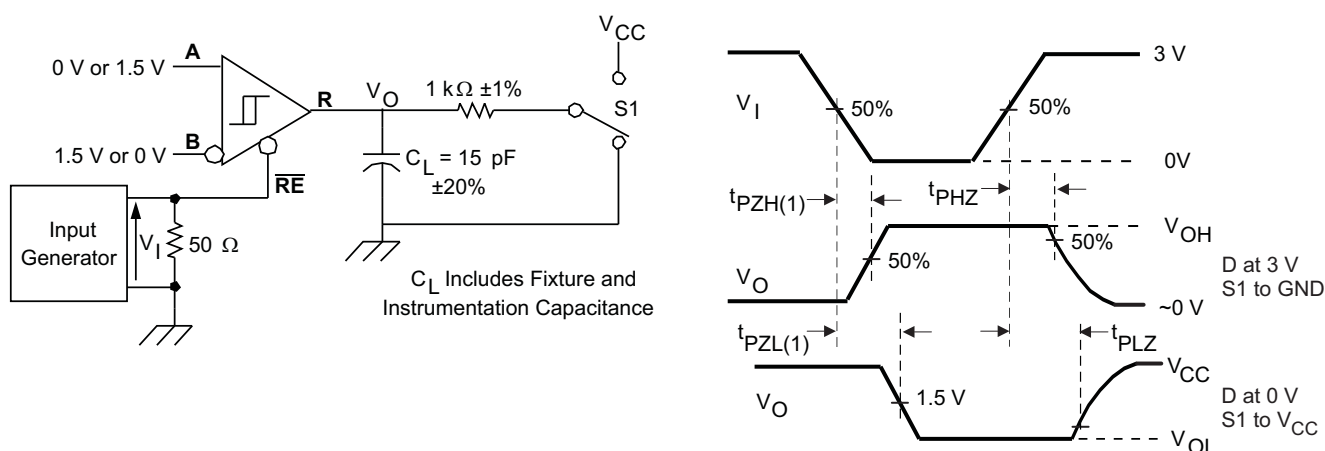
NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

$C_L$  Includes Fixture and Instrumentation Capacitance

**Figure 6. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-up Load**



**Figure 7. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**



**Figure 8. Measurement of Receiver Enable/Disable Times**

## TYPICAL CHARACTERISTICS

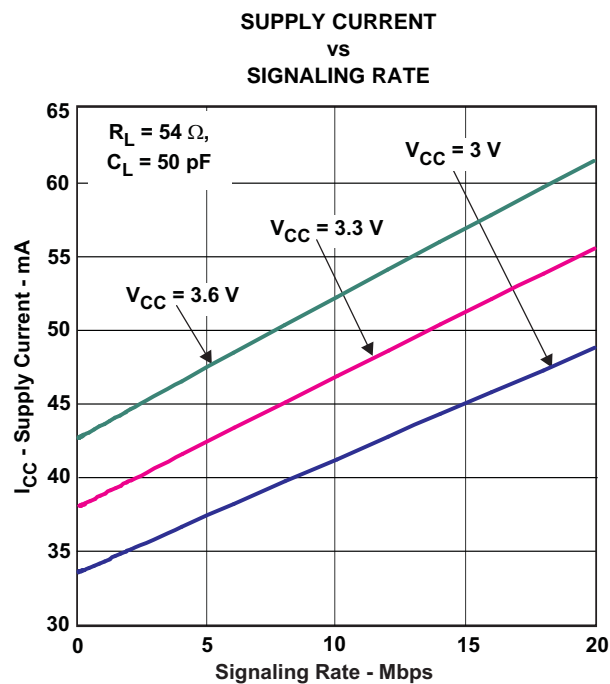


Figure 9.

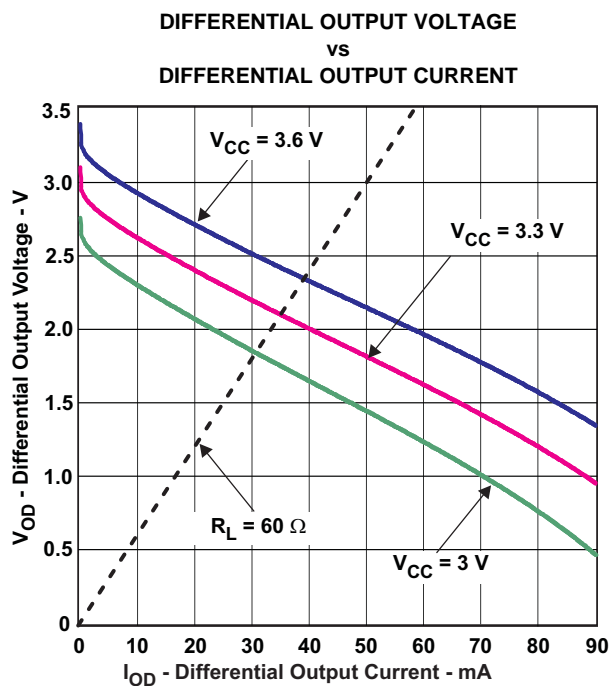


Figure 10.

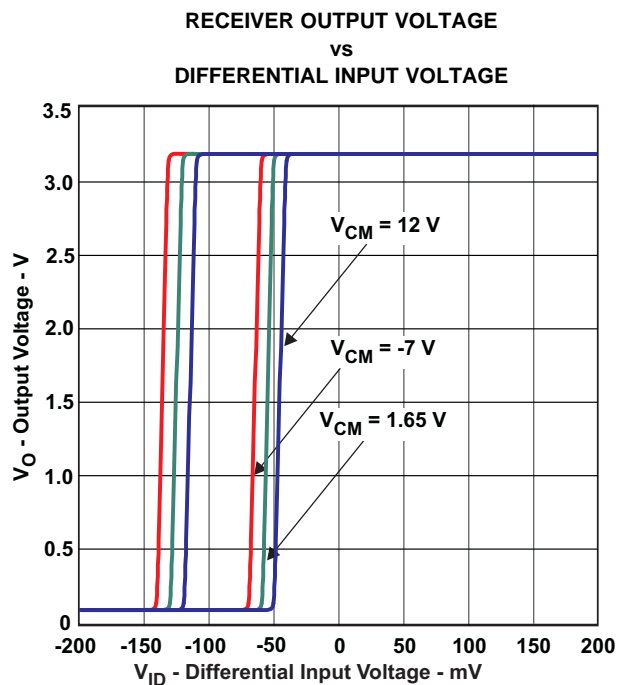


Figure 11.

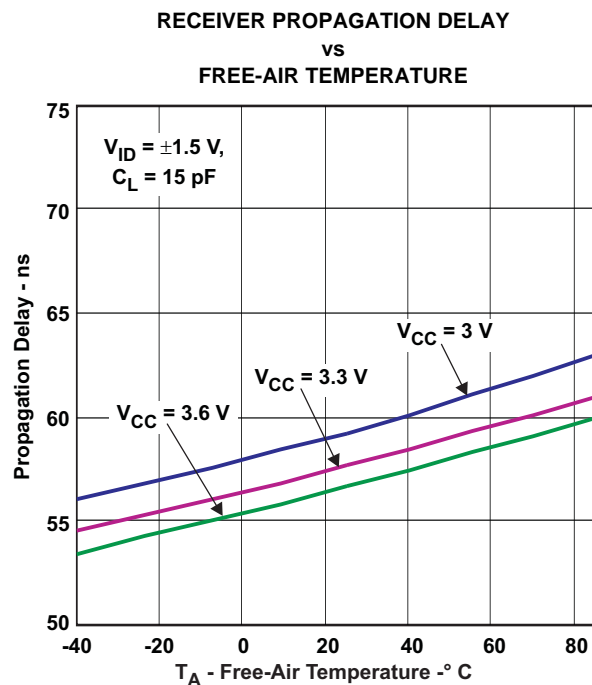


Figure 12.



## TYPICAL CHARACTERISTICS (continued)

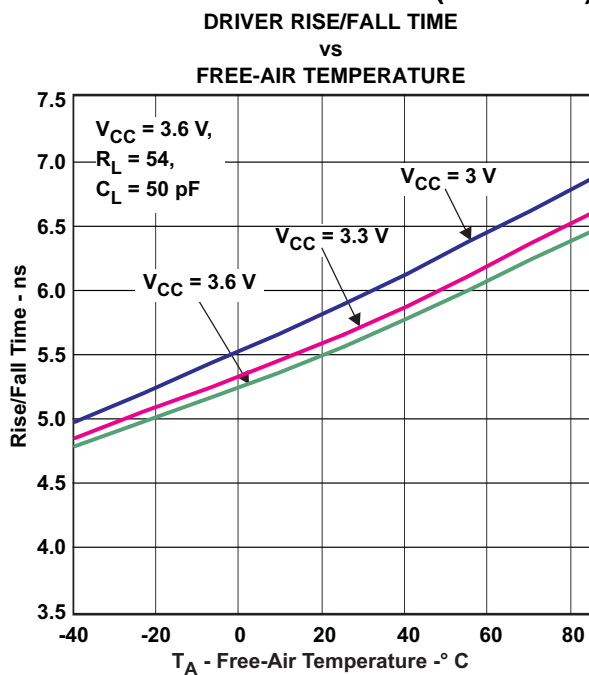


Figure 13.

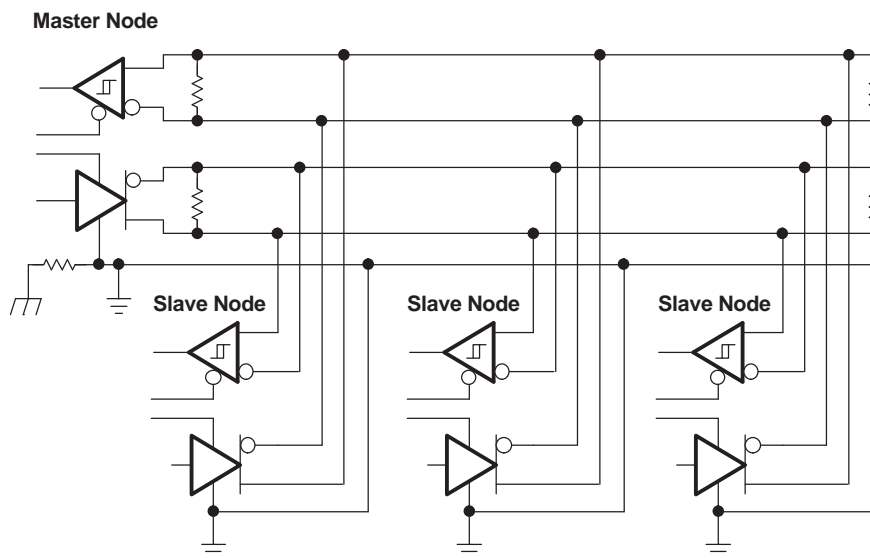


Figure 14. Example Full-Duplex Master/Slave Application Circuit

## APPLICATION INFORMATION

### RECEIVER FAILSAFE

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the HVD37, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input  $V_{ID}$  is more positive than 200 mV, and must output a Low when the  $V_{ID}$  is more negative than -200 mV. The receiver parameters which determine the failsafe performance are  $V_{IT+}$  and  $V_{IT-}$  and  $V_{HYS}$ . In the Electrical Characteristics table,  $V_{IT-}$  has a typical value of -120 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of  $V_{IT+}$  is -60mV, and  $V_{IT+}$  is never more positive than -20 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the  $V_{IT+}$  threshold, and the receiver output will be High. Only when the differential input is more negative than  $V_{IT-}$  will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value  $V_{HYS}$  (the separation between  $V_{IT+}$  and  $V_{IT-}$  ) as well as the value of  $V_{IT+}$ .

For the HVD37, the typical noise immunity is about 120 mV, which is the negative noise level needed to exceed the  $V_{IT-}$  threshold ( $V_{IT-}$  TYP = -120 mV). In the worst case, the failsafe noise immunity is never less than 50 mV, which is set by the maximum positive threshold ( $V_{IT+}$  MAX = -20mV) plus the minimum hysteresis voltage ( $V_{HYS}$  MIN = 30 mV).

### HOT-PLUGGING

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLE, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

### LOW POWER STANDBY MODE

As is customary with RS-485 devices, the receiver output is directly enabled/disabled by  $\overline{RE}$ , and the driver outputs are directly enabled/disabled by DE.

When both the driver and receiver are disabled, (DE=LO and  $\overline{RE}$ =HI) the receiver differential comparator stage enters a standby mode for reduced power.

When either the Driver or Receiver is enabled, the receiver differential comparator stage is enabled for fast response to signal changes.

## REVISION HISTORY

Changes from Original (October 2011) to Revision A	Page
• Changed the device From: Product Preview To: Production .....	<a href="#">1</a>

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65HVD37D</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37D.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
<a href="#">SN65HVD37DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD37DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD37DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD37DR	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD37DRG4	SOIC	D	14	2500	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD37D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD37D.A	D	SOIC	14	50	506.6	8	3940	4.32



**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月