

# 具有 $\pm 15\text{kV}$ IEC ESD 保护功能的 3V 至 5.5V 单通道 RS-232 1Mbits 线路驱动器和接收器

## 1 特性

- 为 RS-232 引脚提供 ESD 保护
  - $\pm 15\text{kV}$  人体放电模型 (HBM)
  - $\pm 8\text{kV}$  IEC 61000-4-2 接触放电
  - $\pm 15\text{kV}$  IEC 61000-4-2 气隙放电
- 由 3V 至 5.5V  $V_{CC}$  电源供电
- 速率高达 1Mbit/s
- 低待机电流 ...1  $\mu\text{A}$  (典型值)
- 外部电容器 ...4  $\times 0.1 \mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 使用人体放电模型 (HBM) 时, RS-232 总线引脚 ESD 保护大于  $\pm 15\text{kV}$
- 自动断电功能可自动禁用驱动器以节省能耗

## 2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

## 3 说明

SN65C3221E 和 SN75C3221E 包含一个线路驱动器、一个线路接收器和一个具有引脚对引脚 (串行端口连接引脚, 包括 GND)  $\pm 15\text{kV}$  IEC ESD 保护功能的双

电荷泵电路。这些器件可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。

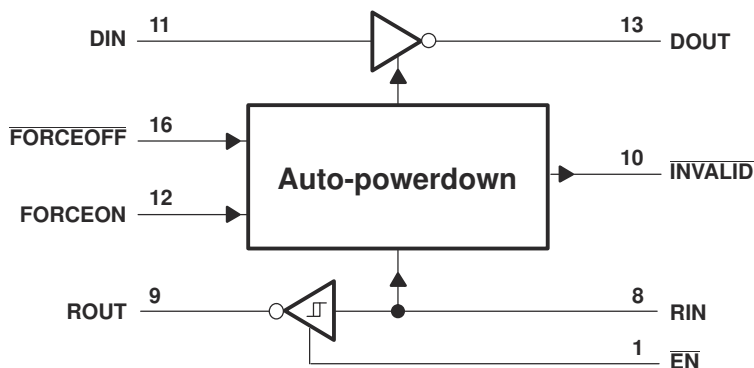
这些器件以高达 1Mbit/s 的数据信号传输速率运行, 驱动器输出压摆率为  $24\text{V}/\mu\text{s}$  至  $150\text{V}/\mu\text{s}$ 。

串行端口处于非活动状态时, 可提供灵活的电源管理控制选项。当 FORCEON 为低电平且 FORCEOFF 为高电平时, 自动断电功能启用。在这种运行模式下, 如果器件在接收器输入端未感应到有效的 RS-232 信号, 则会禁用驱动器输出。如果 FORCEOFF 设定为低电平且 EN 为高电平, 则驱动器和接收器均关闭, 且电源电流降低至  $1 \mu\text{A}$ 。断开串行端口的连接或关闭外围驱动器会导致发生自动断电情况。当 FORCEON 和 FORCEOFF 均为高电平时可禁用自动断电。启用自动断电的情况下, 向接收器输入施加有效信号时, 器件会自动激活。INVALID 输出会通知用户接收器输入端是否存在 RS-232 信号。如果接收器输入电压大于 2.7V 或小于 -2.7V, 或者介于 -0.3V 至 0.3V 之间的时间少于  $30 \mu\text{s}$ , 则 INVALID 为高电平 (有效数据)。如果接收器输入电压在 -0.3V 至 0.3V 之间的时间超过  $30 \mu\text{s}$ , 则 INVALID 为低电平 (无效数据)。有关接收器输入电平的信息, 请参阅图 8-5。

### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
SNx5C3221E	SSOP (DB) 16	6.20mm x 5.30mm
	TSSOP (DW) 16	10.3mm x 7.50mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)



## Table of Contents

<b>1 特性</b> .....	1	7.11 Auto-powerdown Section: Electrical Characteristics.....	9
<b>2 应用</b> .....	1	7.12 Switching Characteristics: Auto-powerdown.....	9
<b>3 说明</b> .....	1	<b>8 Parameter Measurement Information</b> .....	10
<b>4 Revision History</b> .....	2	<b>9 Detailed Description</b> .....	13
<b>5 Device Comparison Table</b> .....	3	9.1 Device Functional Modes.....	13
<b>6 Pin Configuration and Functions</b> .....	4	<b>10 Application and Implementation</b> .....	14
<b>7 Specifications</b> .....	5	10.1 Application Information.....	14
7.1 Absolute Maximum Ratings.....	5	<b>11 Device and Documentation Support</b> .....	15
7.2 ESD Ratings.....	5	11.1 接收文档更新通知.....	15
7.3 ESD Ratings - IEC Specifications.....	5	11.2 支持资源.....	15
7.4 Recommended Operating Conditions.....	6	11.3 Trademarks.....	15
7.5 Thermal Information.....	6	11.4 Electrostatic Discharge Caution.....	15
7.6 Electrical Characteristics.....	7	11.5 术语表.....	15
7.7 Driver Section: Electrical Characteristics.....	7	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	15
7.8 Switching Characteristics: Driver.....	7		
7.9 Receiver Section: Electrical Characteristics.....	8		
7.10 Switching Characteristics: Receiver.....	8		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2009) to Revision C (July 2021)	Page
• 更改了应用列表.....	1
• 删除了“订购信息”表.....	1
• 添加了器件信息表.....	1
• Added the <i>Pin Configuration and Functions</i> .....	4
• Removed the thermal information from <i>Absolute Maximum Rating</i> stable and moved the thermal information to its own table.....	5
• Added a table note for PW package of SN65C3221E regarding the minimum capacitance in <i>ESD Ratings - IEC Specifications</i> table.....	5
• Changed thermal information for PW package of SN65C3221E. Added additional thermal information for other packages.....	6
• Added the <i>Detailed Descriptiton</i> section.....	13

## 5 Device Comparison Table

**表 5-1. 1-Mbit/s RS-232 Parts**

PART NO.	TEMPERATURE RANGE	DRIVER NO.	RECEIVER NO.	ESD	SUPPLY V <sub>CC</sub> (V)	FEATURE	PIN/PACKAGE
SN65C3221E	- 40°C to 85°C	1	1	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN65C3232E		2	2	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
MAX3227I		1	1	±8-kV Air-Gap, ±8-k V Contact, ±15-kV HBM	3.3 or 5	Auto powerdown plus, ready signal	16-pin SSOP
SN65C3221		1	1	±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN65C3223		2	2	±15-kV HBM	3.3 or 5	Auto powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
SN65C3222		2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
SN65C3232		2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
SN65C3238		5	3	±15-kV HBM	3.3 or 5	Auto powerdown plus	28-pin SOIC, SSOP, TSSOP
SN65C3243		3	5	±15-kV HBM	3.3 or 5	Auto powerdown	28-pin SOIC, SSOP, TSSOP
SN75C3221E	0°C to 70°C	1	1	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN75C3232E		2	2	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
MAX3227C		1	1	±8-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown plus, ready signal	16-pin SSOP
SN75C3221		1	1	±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN75C3223		2	2	±15-kV HBM	3.5 or 5	Auto powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
SN75C3222		2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
SN75C3232		2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
SN75C3238		5	3	±15-kV HBM	3.3 or 5	Auto powerdown plus	28-pin SOIC, SSOP, TSSOP
SN75C3243		3	5	±15-kV HBM	3.3 or 5	Auto powerdown	28-pin SOIC, SSOP, TSSOP

## 6 Pin Configuration and Functions

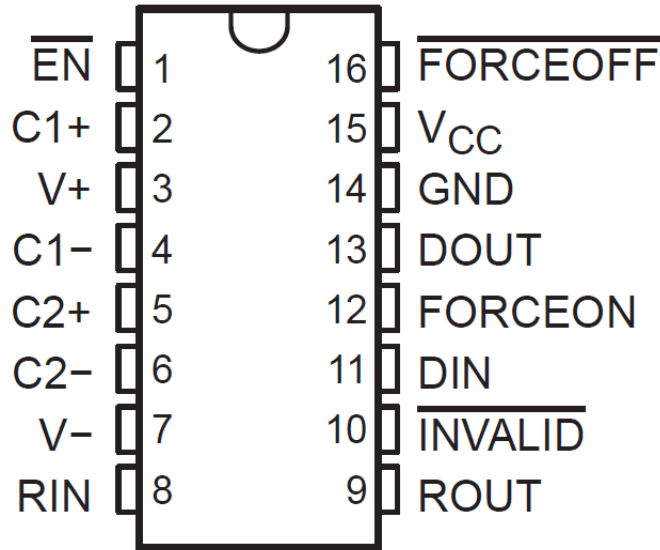


图 6-1. DB or PW Package  
Top View

表 6-1. Pin Configurations

PIN		I/O	DESCRIPTION
NAME	NO		
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
V+	3	O	5.5-V supply generated by the charge pump
C1-	4	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2+	5	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2-	6	—	Negative terminals of the voltage-doubler charge-pump capacitors
V-	7	O	- 5.5-V supply generated by the charge pump
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
INVALID	10	O	Invalid output pin. Output low when all RIN inputs are unpowered.
DIN	11	I	Driver input
FORCEON	12	I	Automatic power-down control input
DOUT	13	O	RS-232 driver output
GND	14	—	Ground
V <sub>CC</sub>	15	—	3-V to 5.5-V supply voltage
FORCEOFF	16	I	Automatic power-down control input

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	- 0.3	6	V	
V+	Positive output supply voltage range <sup>(2)</sup>	- 0.3	7	V	
V-	Negative output supply voltage range <sup>(2)</sup>	0.3	- 7	V	
V+ - V-	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage range	Driver ( FORCEOFF, FORCEON, EN)	- 0.3	6	V
		Receiver	- 25	25	
V <sub>O</sub>	Output voltage range	Driver	- 13.2	13.2	V
		Receiver ( INVALID)	- 0.3	V <sub>CC</sub> + 0.3	
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	- 65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 7.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	DOUT, RIN	±15000	V
			All other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 ESD Ratings - IEC Specifications

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge <sup>(1)</sup>	RIN and DOUT pins only	±8000	V
		IEC 61000-4-2 Air Discharge <sup>(1)</sup>	RIN and DOUT pins only	±15000	

- (1) For the PW package of SN65C3221E only, a minimum of 1-μF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

## 7.4 Recommended Operating Conditions

See 图 10-1. see (1)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
$V_{IH}$	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
$V_{IL}$	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN			0.8	V
$V_I$	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
$V_I$	Receiver input voltage		- 25		25	V
$T_A$	Operating free-air temperature	SN65C3221E	- 40		85	°C
		SN75C3221E	0		70	

(1) Test conditions are C1 - C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2 - C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

## 7.5 Thermal Information

THERMAL METRIC <sup>1</sup>		SN65C3221E		SN75C3221E		UNIT
		PW (TSSOP)	DB (SSOP)	PW (TSSOP)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.9	82	108	82	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	45.7	41.1	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	44.4	51.4	44.4	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	4.2	11.0	3.9	11.0	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	56.6	43.8	50.9	43.8	°C/W

## 7.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 10-1](#))

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$I_I$	Input leakage current	FORCEOFF, FORCEON, EN		±0.01	±1	μA
$I_{CC}$	Supply current ( $T_A = 25^\circ\text{C}$ )	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at $V_{CC}$	0.3	1	mA
		Powered off	No load, FORCEOFF at GND	1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at $V_{CC}$ , FORCEON at GND, All RIN are open or grounded	1	10	

(1) Test conditions are C1 - C4 = 0.1 μF at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047 μF, C2 - C4 = 0.33 μF at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## 7.7 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 10-1](#))

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = GND	5	5.4		V
$V_{OL}$	Low-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = $V_{CC}$	-5	-5.4		V
$I_{IH}$	High-level input current	$V_I = V_{CC}$		±0.01	±1	μA
$I_{IL}$	Low-level input current	$V_I$ at GND		±0.01	±1	μA
$I_{OS}$	Short-circuit output current <sup>(3)</sup>	$V_{CC} = 3.6\text{ V}$ , $V_O = 0\text{ V}$		±35	±60	mA
		$V_{CC} = 5.5\text{ V}$ , $V_O = 0\text{ V}$		±35	±90	
$r_o$	Output resistance	$V_{CC}$ , $V+$ , and $V- = 0\text{ V}$ , $V_O = \pm 2\text{ V}$	300	10M		Ω
$I_{off}$	Output leakage current	FORCEOFF = GND	$V_O = \pm 12\text{ V}$ , $V_{CC} = 3\text{ V to } 3.6\text{ V}$		±25	μA
			$V_O = \pm 10\text{ V}$ , $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		±25	

(1) Test conditions are C1 - C4 = 0.1 μF at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047 μF, C2 - C4 = 0.33 μF at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

## 7.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 10-1](#))

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate (see <a href="#">Figure 8-1</a> )	$R_L = 3\text{ k}\Omega$	$C_L = 1000\text{ pF}$		250		kbit/s
		$C_L = 250\text{ pF}$ , $V_{CC} = 3\text{ V to } 4.5\text{ V}$		1000		
		$C_L = 1000\text{ pF}$ , $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		1000		
$t_{sk(p)}$	Pulse skew <sup>(3)</sup>	$C_L = 150\text{ pF to } 2500\text{ pF}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See <a href="#">Figure 8-2</a>		100		ns
SR(tr)	Slew rate, transition region (see <a href="#">Figure 8-1</a> )	$V_{CC} = 3.3\text{ V}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 150\text{ pF to } 1000\text{ pF}$		18	150	V/μs

(1) Test conditions are C1 - C4 = 0.1 μF at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047 μF, C2 - C4 = 0.33 μF at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

(3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

## 7.9 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 10-1](#))

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6 V	V <sub>CC</sub> - 0.1 V		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>off</sub>	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r <sub>i</sub>	Input resistance	V <sub>i</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1 - C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 7.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 10-1](#))

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">图 8-3</a>	150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">图 8-3</a>	150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">图 8-4</a>	200	ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">图 8-4</a>	200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See <a href="#">图 8-3</a>	50	ns

(1) Test conditions are C1 - C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

## 7.11 Auto-powerdown Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 8-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = $V_{CC}$		2.7	V
$V_{T-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	- 2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	- 0.3	0.3	V
$V_{OH}$	INVALID high-level output voltage	$I_{OH} = -1 \text{ mA}$ , FORCEON = GND, FORCEOFF = $V_{CC}$	$V_{CC} - 0.6$		V
$V_{OL}$	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$ , FORCEON = GND, FORCEOFF = $V_{CC}$		0.4	V

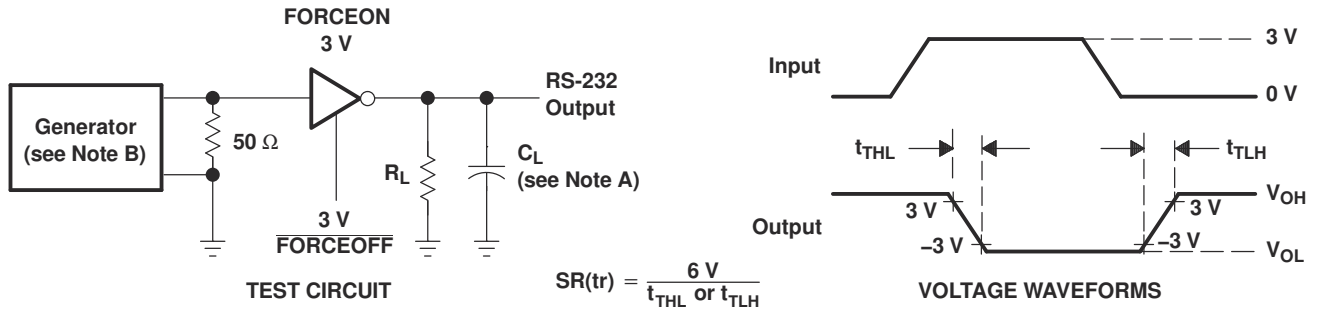
## 7.12 Switching Characteristics: Auto-powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 8-5](#))

PARAMETER		TYP <sup>(1)</sup>	UNIT
$t_{valid}$	Propagation delay time, low- to high-level output	1	$\mu\text{s}$
$t_{invalid}$	Propagation delay time, high- to low-level output	30	$\mu\text{s}$
$t_{en}$	Supply enable time	100	$\mu\text{s}$

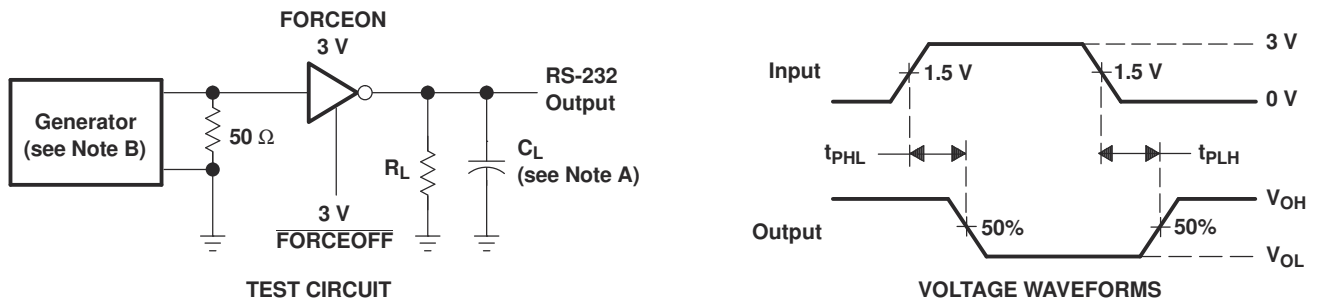
(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## 8 Parameter Measurement Information



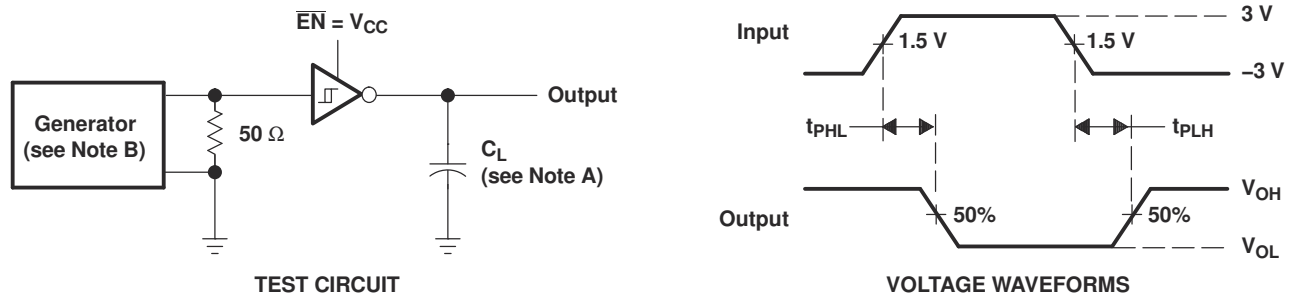
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

图 8-1. Driver Slew Rate



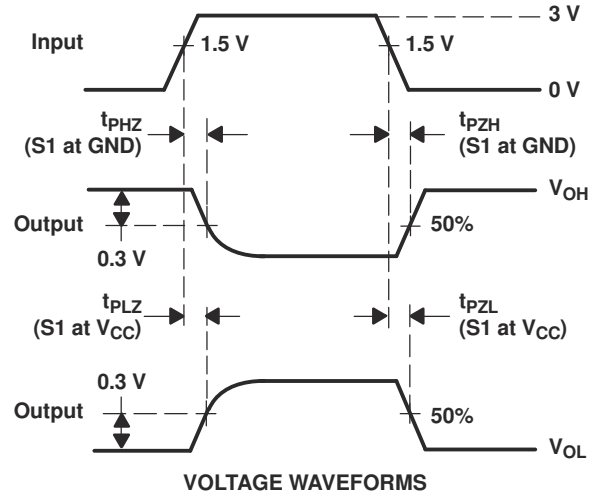
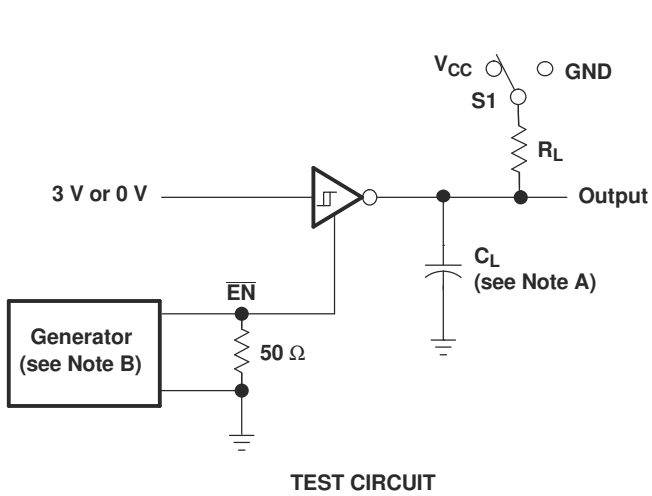
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

图 8-2. Driver Pulse Skew



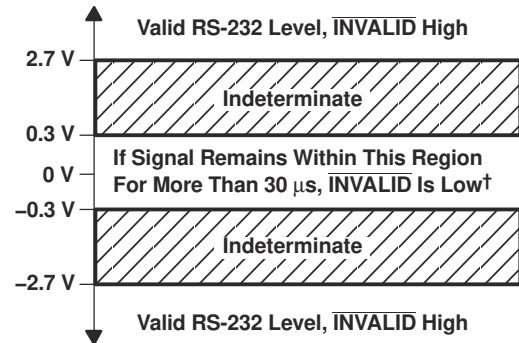
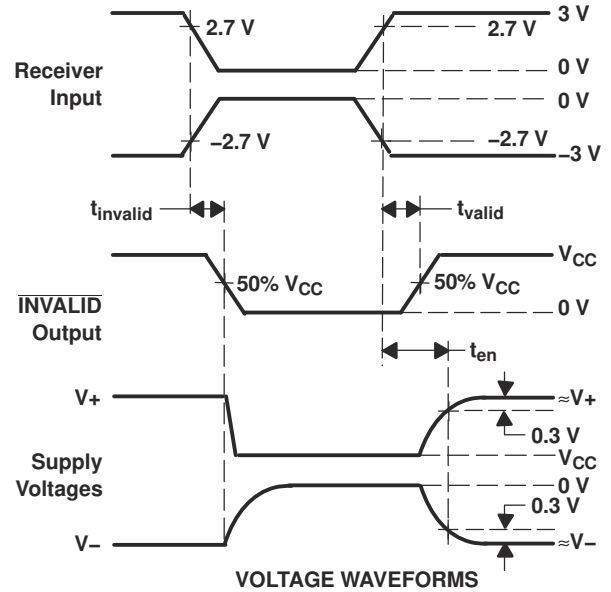
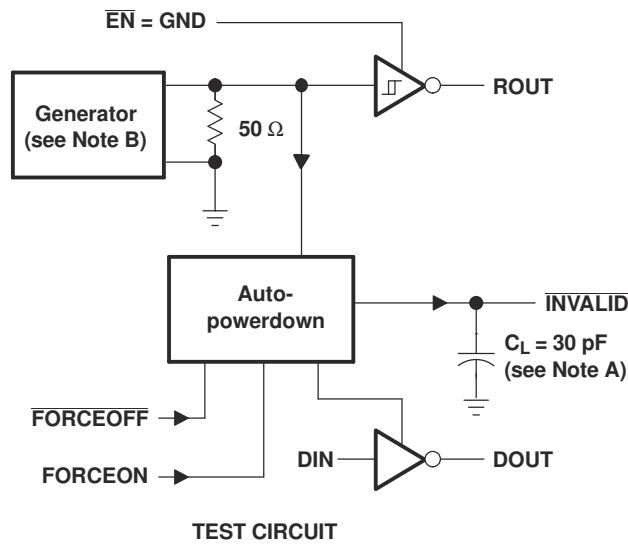
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

图 8-3. Receiver Propagation Delay Times



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .
  - C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**图 8-4. Receiver Enable and Disable Times**



† Auto-powerdown disables drivers and reduces supply current to 1  $\mu$ A.

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

图 8-5. INVALID Propagation Delay Times and Driver Enabling Time

## 9 Detailed Description

### 9.1 Device Functional Modes

表 9-1. Each Driver

INPUTS <sup>(1)</sup>				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 9-2. Each Receiver

INPUTS <sup>(1)</sup>			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

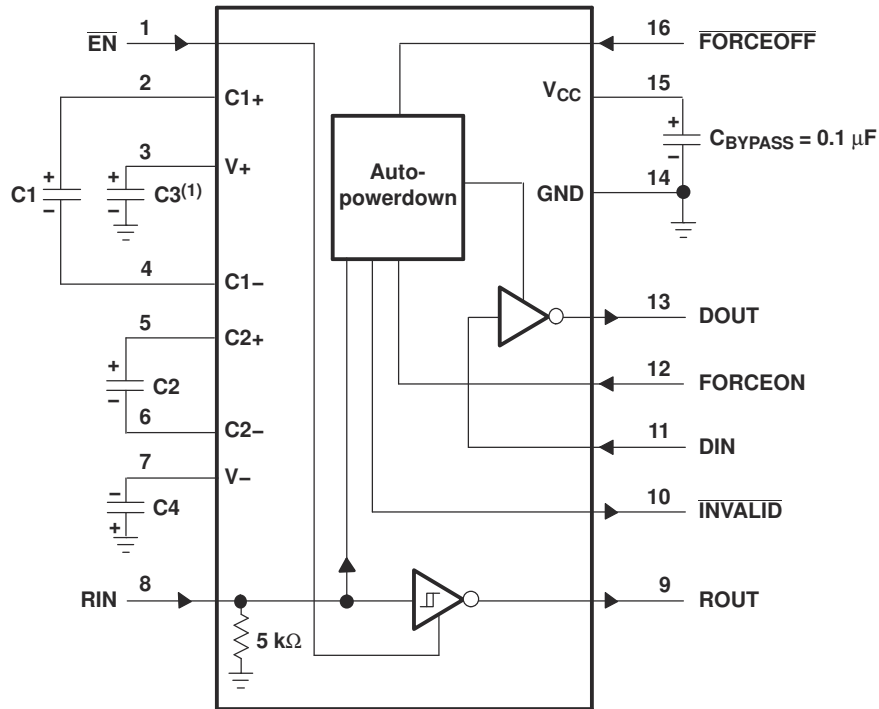
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

## 10 Application and Implementation

### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 10.1 Application Information



(1) C3 can be connected to  $V_{CC}$  or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

$V_{CC}$  vs CAPACITOR VALUES

$V_{CC}$	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 $\mu$ F	0.1 $\mu$ F
5 V $\pm$ 0.5 V	0.047 $\mu$ F	0.33 $\mu$ F
3 V to 5.5 V	0.1 $\mu$ F	0.47 $\mu$ F

图 10-1. Typical Operating Circuit and Capacitor Values

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65C3221EDB</a>	Obsolete	Production	SSOP (DB)   16	-	-	Call TI	Call TI	-40 to 85	MU221E
<a href="#">SN65C3221EDBR</a>	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EDBR.A	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EDBRG4	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EDBRG4.A	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
<a href="#">SN65C3221EPWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EPWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EPWRG4	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
SN65C3221EPWRG4.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E
<a href="#">SN75C3221EDB</a>	Obsolete	Production	SSOP (DB)   16	-	-	Call TI	Call TI	0 to 70	MY221E
<a href="#">SN75C3221EDBR</a>	Obsolete	Production	SSOP (DB)   16	-	-	Call TI	Call TI	0 to 70	MY221E

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3221EDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN65C3221EDBRG4	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN65C3221EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221EPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3221EDBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN65C3221EDBRG4	SSOP	DB	16	2000	353.0	353.0	32.0
SN65C3221EPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C3221EPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN65C3221EPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

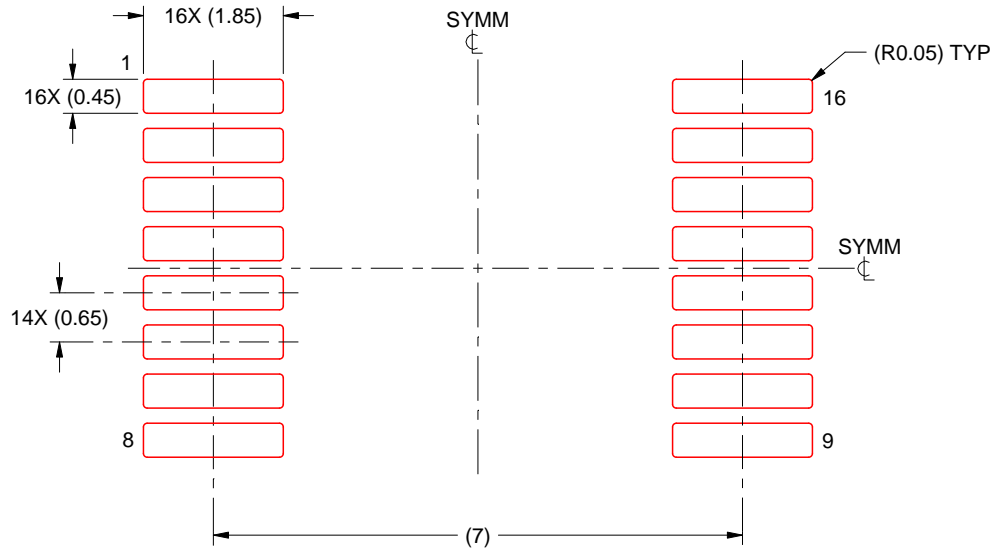
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

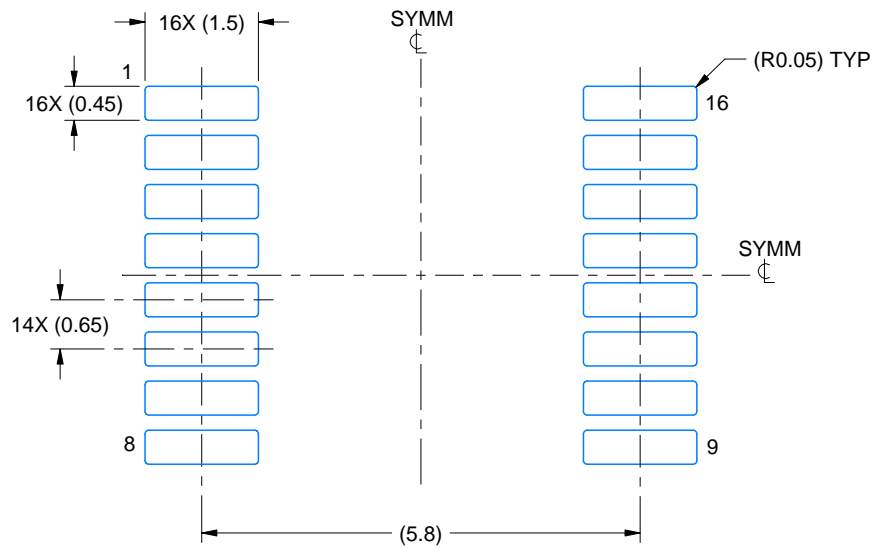
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月