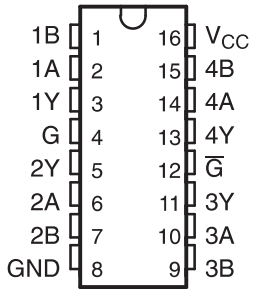
高速差分线路接收器

查询样品: SN55LVDS32-SP

特性

- 符合 **QML-V，SMD 5962-97621**
- 由一个单 **3.3V** 电源供电运行
- 设计用于信号传输速率高达 **100Mbps** 的应用
- 最大差分输入阈值为 **±100mV**
- 典型传播延迟时间为 **2.1ns**
- 在最大数据速率下每个接收器的功率耗散典型值为 **60mW**
- 总线-端子静电放电 **(ESD)** 保护超过 **8kV**
- 低压 **TTL(LVTTL)** 逻辑输入电平
- 开电路故障安全
- 针对有冗余需求的太空和高可靠性应用的冷备用

J OR W PACKAGE
(TOP VIEW)



说明

SN55LVDS32 是一款差分线路驱动器，此驱动器执行低压差分信号传输 (LVDS) 的电气特性。 这个信号传输技术降低了 5V 差分标准电平（例如 EIA/TIA-422B）的输出电压电平，从而减少了功耗、增加了开关速度、并可实现在 3.3V 电源轨供电下的运行。 四个差分接收器中的任何一个在输入共模电压范围内提供具有 ±100mV 差分输入电压的有效逻辑输出状态。 此输入共模电压范围允许两个 LVDS 节点间 1V 的接地电势差。

这些器件和信号传输技术用于接近 100Ω 的受控阻抗介质上的点到点和多支路（一个驱动器和多个接收器）的数据传输应用。此传输介质可以是印刷电路板走线、底板、或者电缆。 数据传输的最终速率和距离取决于介质的衰减特性和环境的噪声耦合。

SN55LVDS32 额定运行温度介于 -55°C 至 125°C 之间。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP - J	5962-9762201VEA	5962-9762201VEA
	CFP - W	5962-9762201VFA	5962-9762201VFA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SN55LVDS32 logic diagram (positive logic)

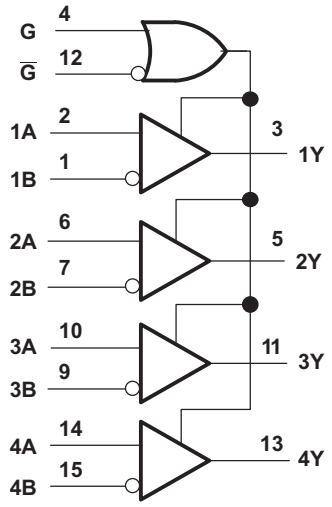
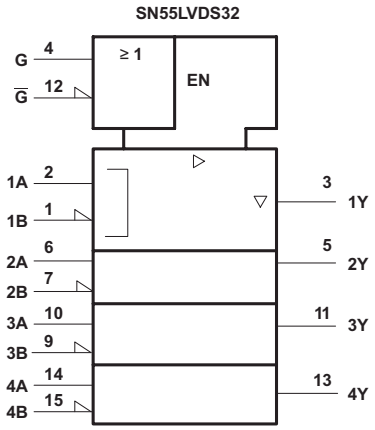


Table 1. FUNCTION TABLE(1)

SN55LVDS32			
DIFFERENTIAL INPUT A, B	ENABLES		OUTPUT
	G	$\overline{G}$	Y
$V_{ID} \geq 100$ mV	H	X	H
	X	L	H
-100 mV $< V_{ID} \leq 100$ mV	H	X	?
	X	L	?
$V_{ID} \leq -100$ mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

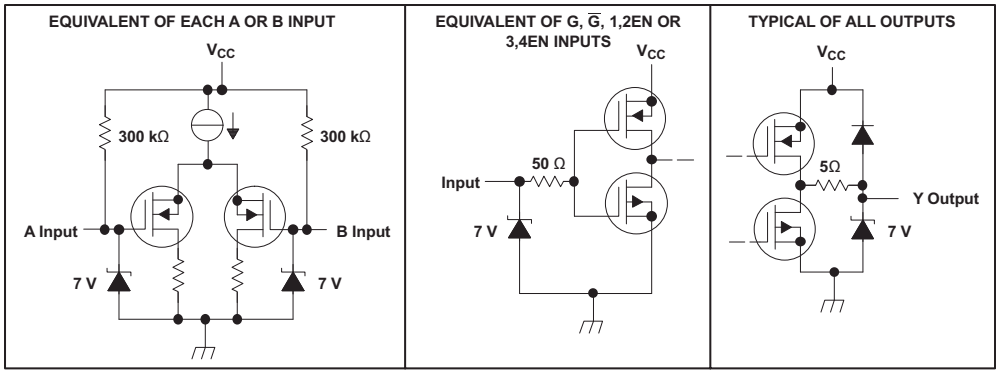
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{CC}	Supply voltage range(2)		–0.5 V to 4 V
V_I	Input voltage range	Enables and output	–0.5 V to V_{CC} + 0.5 V
		A or B	–0.5 V to 4 V
	Continuous total power dissipation		See Dissipation Rating Table
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
W	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	G, $\overline{G}$, 1,2EN, or 3,4EN	2			V
V_{IL}	Low-level input voltage	G, $\overline{G}$, 1,2EN, or 3,4EN			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 1)		$\|V_{ID}\|/2$		$2.4 - \|V_{ID}\|/2$	V
					$V_{CC} - 0.8$	
T_A	Operating free-air temperature		–55		125	°C

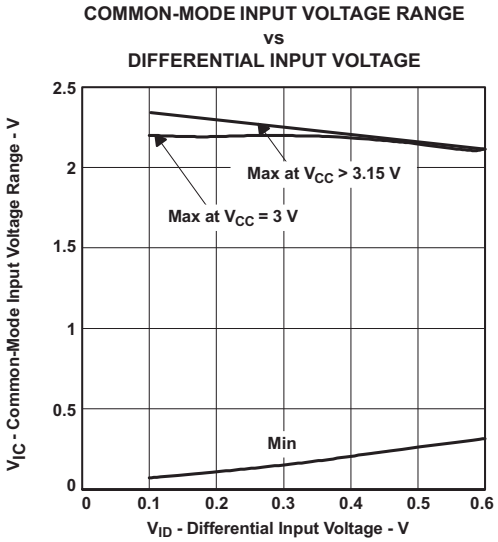


Figure 1. V_{IC} Versus V_{ID} and V_{CC}

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2, Table 2, and (2)			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold(3)	See Figure 2, Table 2, and (2)	-100			mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{CC}	Supply current	Enabled, No load		10	18	mA
		Disabled		0.25	0.5	
I_I	Input current (A or B inputs)	V_I = 0	-2	-10	-20	µA
		V_I = 2.4 V	-1.2	-3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0, V_I = 2.4 V		6	20	µA
I_{IH}	High-level input current (EN, G, or $\overline{G}$ inputs)	V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (EN, G, or $\overline{G}$ inputs)	V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±12	µA

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) $|V_{ITH}|$ = 200 mV for operation at –55°C.
(3) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	1.3	2.3	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.2	6.1	ns
$t_{sk(o)}$	Channel-to-channel output skew(1)			0.1		ns
t_r	Differential output signal rise time (20% to 80%)			0.6		ns
t_f	Differential output signal fall time (80% to 20%)			0.7		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		6.5	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

(1) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

PARAMETER MEASUREMENT INFORMATION

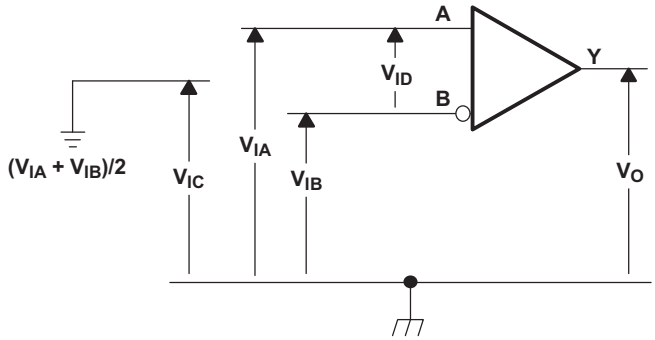
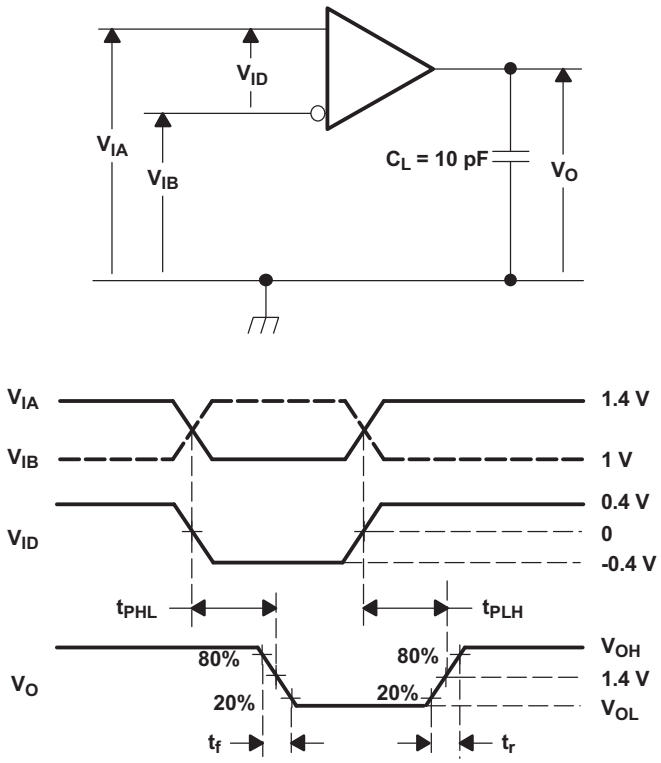


Figure 2. Voltage Definitions

Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES(1)		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

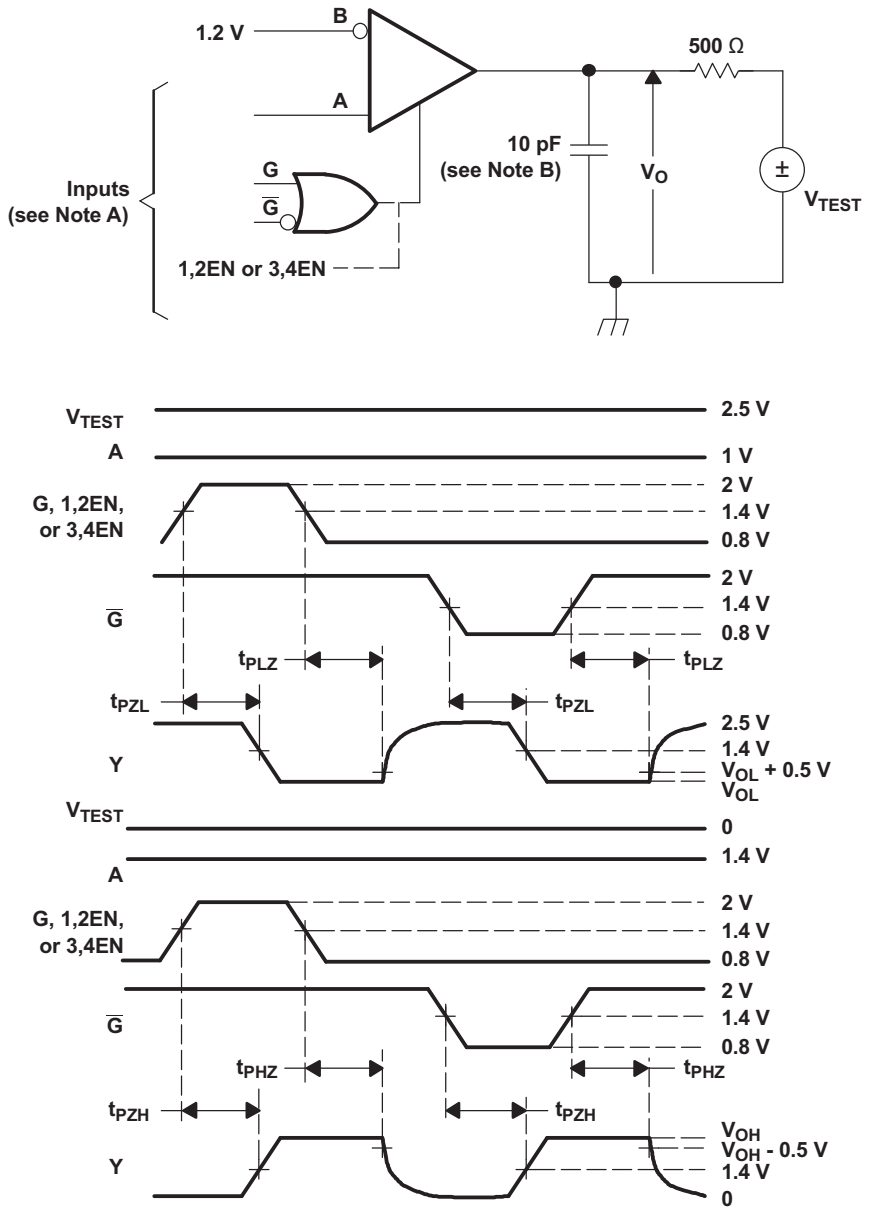
(1) These voltages are applied for a minimum of 1.5 µs.



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate(PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate(PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable- and Disable-Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT vs FREQUENCY

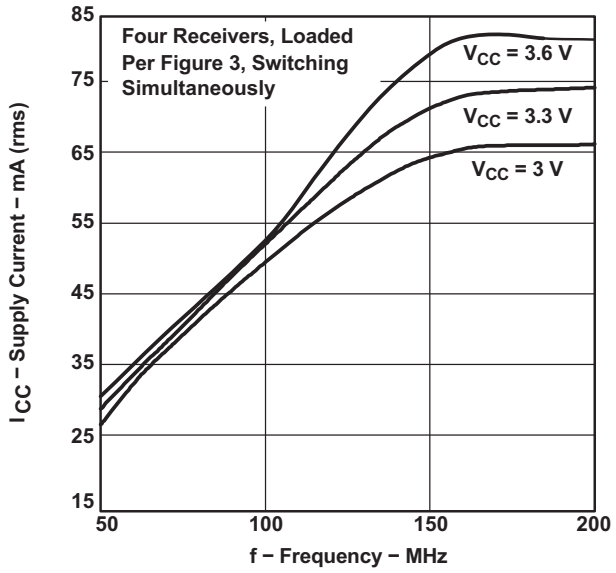


Figure 5.

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

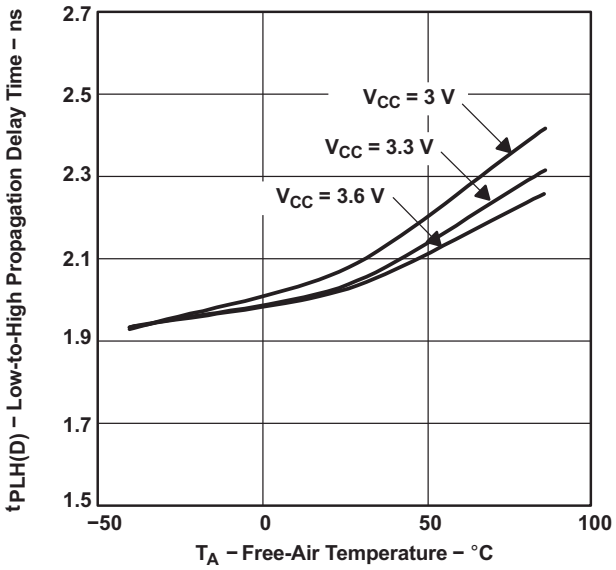


Figure 6.

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

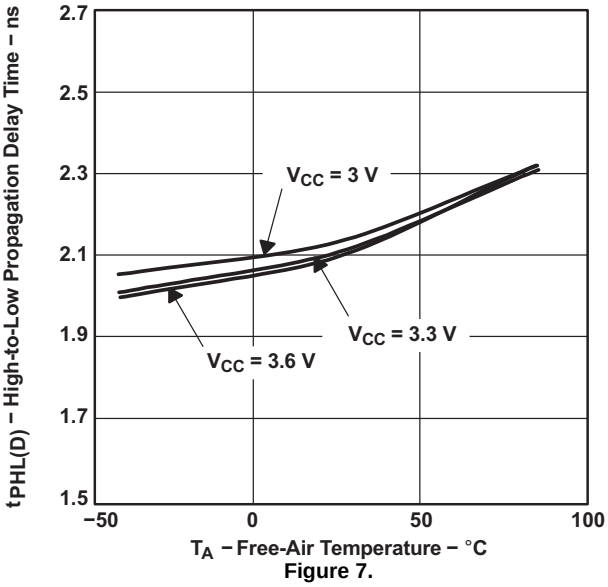


Figure 7.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

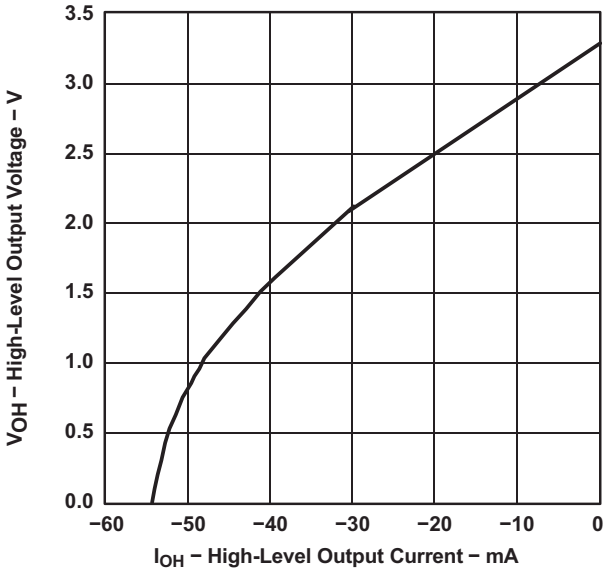


Figure 8.

HIGH-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

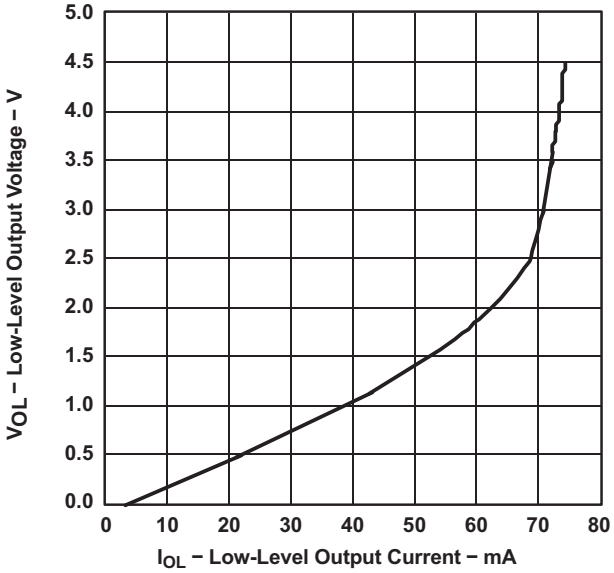


Figure 9.

APPLICATION INFORMATION

EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

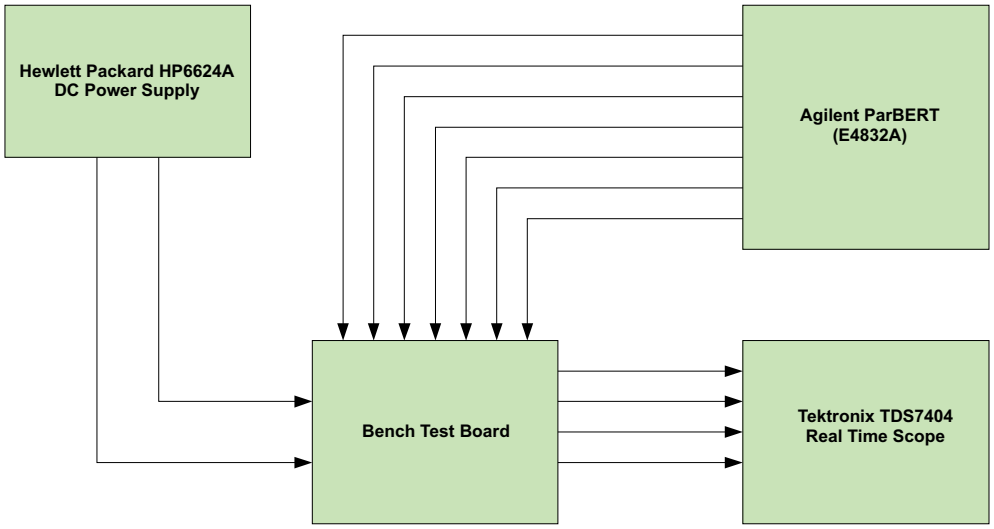
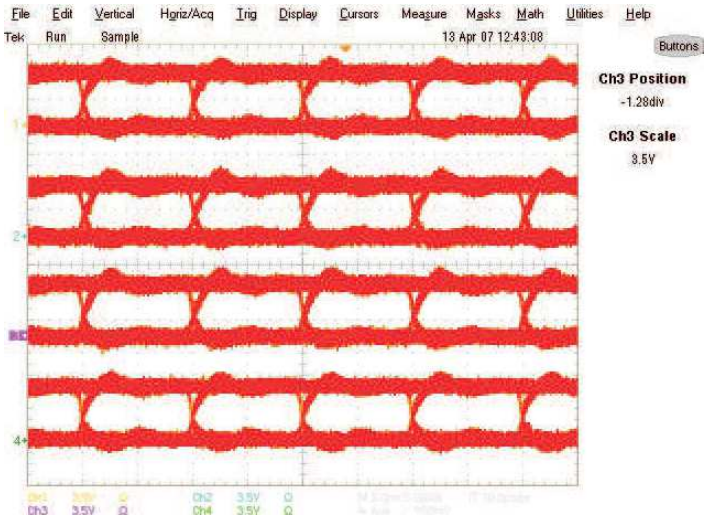


Figure 10. Equipment Setup



All Rx running at 100 Mbps; Channel 1: 1Y, Channel 2: 2Y; Channel 3: 3Y; Channel 4: 4Y

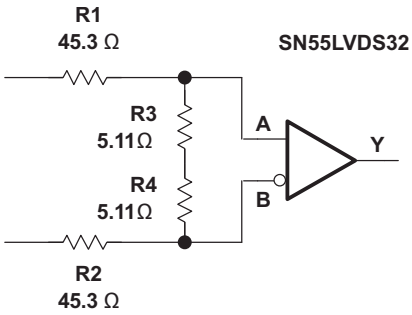
Figure 11. Typical Eye Patterns SN55LVDS32: (T = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})

USING AN LVDS RECEIVER WITH RS-422 DATA

Receipt of data from a TIA/EIA-422 line driver can be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than ±1 V), the answer can be as simple as shown in Figure 12. A resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of 100 Ω to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal, or 6 V, is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a greater than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.

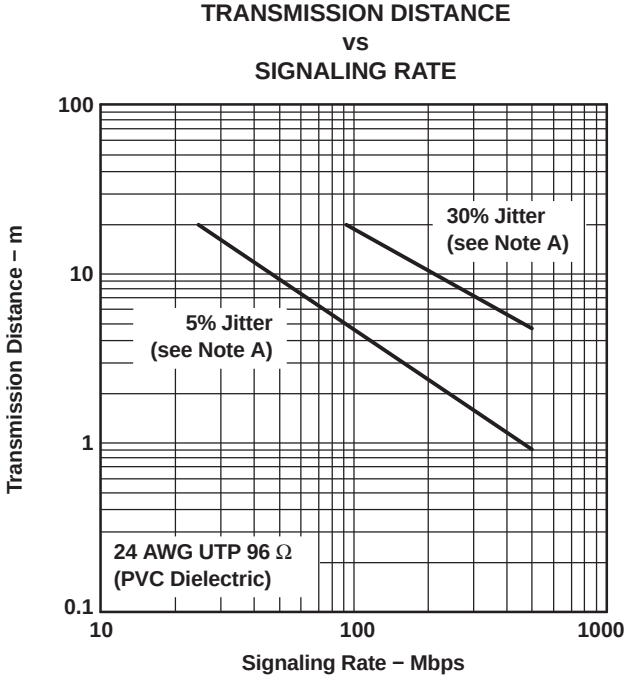


NOTE: The components used were standard values. (1) R1, R2 = NRC12F45R3TR, NIC components, 45.3 Ω, 1/8 W, 1%, 1206 package (2) R3, R4 = NRC12F5R11TR, NIC components, 5.11 Ω, 1/8 W, 1%, 1206 package (3) The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than 100 Ω in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

Figure 12. RS-422 Data Input to an LVDS Receiver Under Low Ground-Noise Conditions

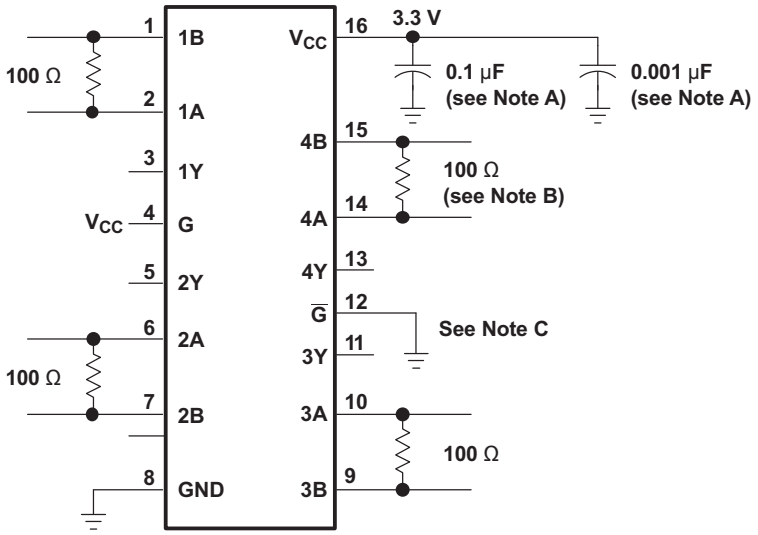
If ground noise between the RS-422 driver and LVDS receiver is a concern, the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from ±1 V to greater than ±4.5 V.

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual-supply requirements.



A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 13. Typical Transmission Distance Versus Signaling Rate

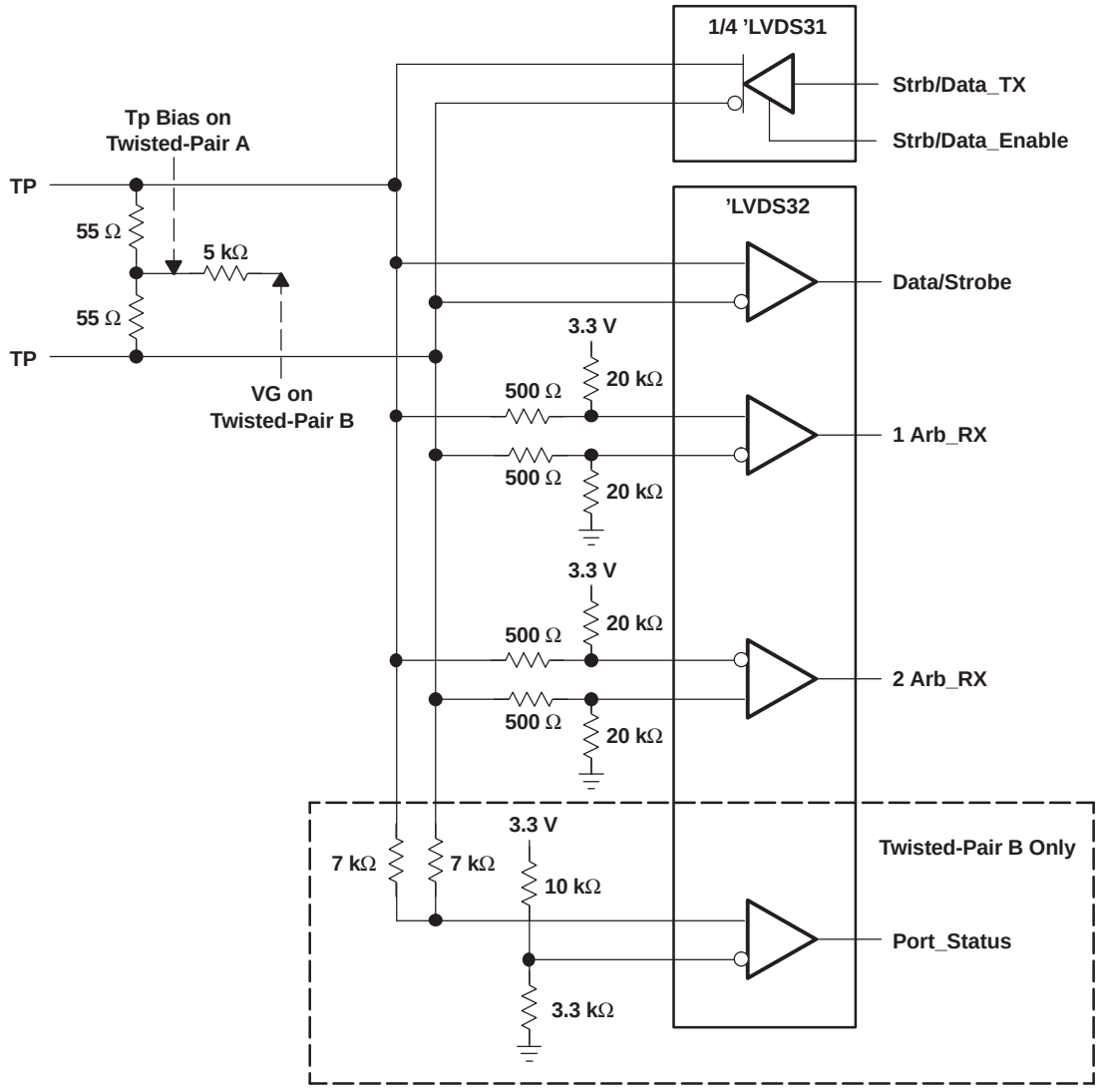


A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between VCC and the ground plane. The capacitors should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 14. Typical Application Circuit Schematic



NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
B. Decoupling capacitance is not shown, but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 15. 100-Mbps IEEE 1394 Transceiver

FAIL-SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and100 mV if it is within its recommended input common-mode voltage range. However, TI LVDS receivers handle the open-input circuit situation differently.

Open-input circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors (see Figure 16). The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level, regardless of the differential input voltage.

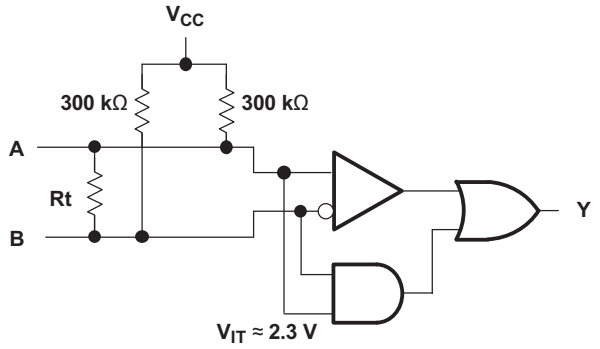
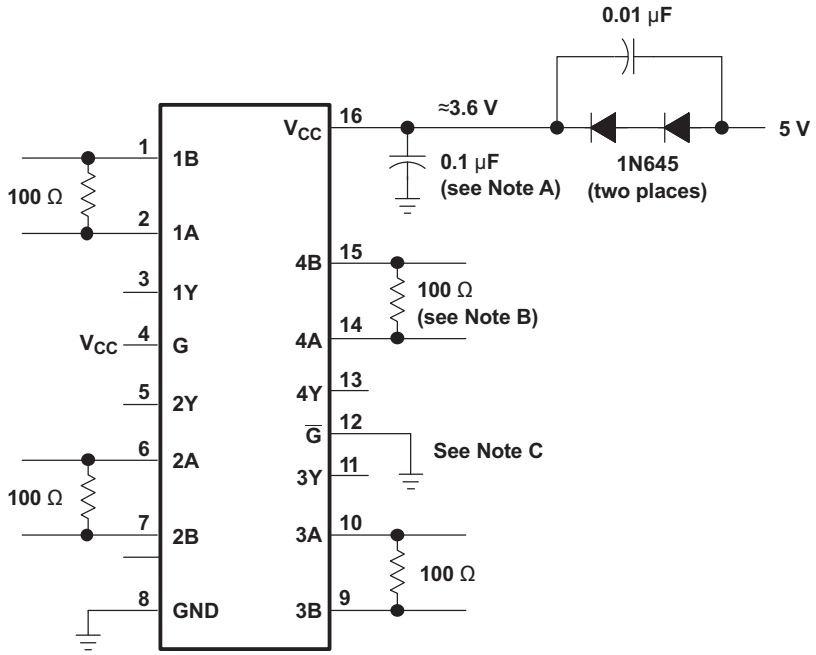


Figure 16. Open-Circuit Fail-Safe of LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 16. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.



A. Place a 0.1-µF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 17. Operation With 5-V Supply

COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9762201VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201VF A SNV55LVDS32W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

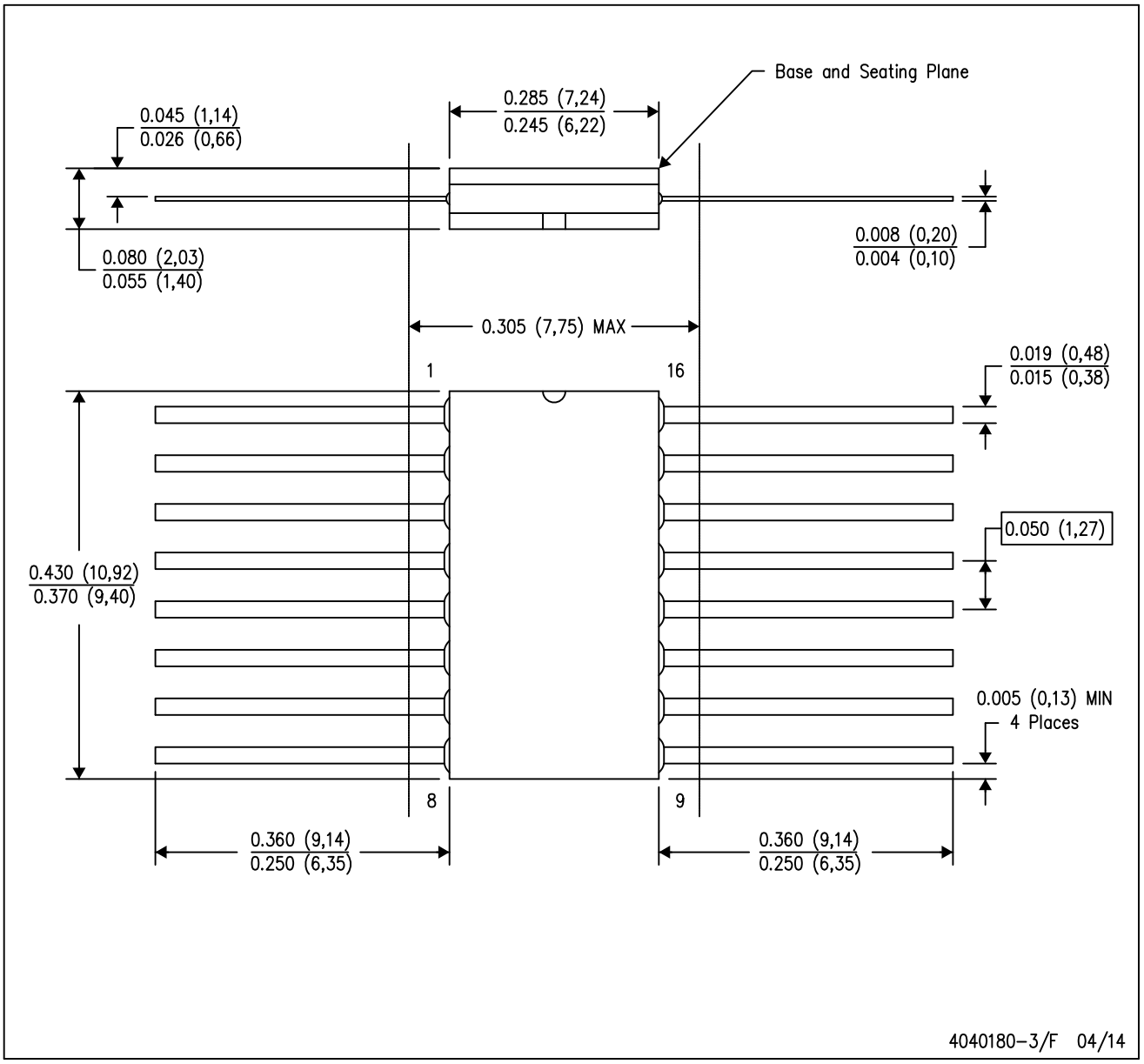
OTHER QUALIFIED VERSIONS OF SN55LVDS32-SP :

- Catalog : SN55LVDS32

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月