

SNx4HC253 具有三态输出的双路 4 线至 1 线数据选择器/多路复用器

1 特性

- 三态版本的 HC153
- 2V 至 6V 的宽工作电压范围
- 高电流反相输出可驱动多达 15 个 LSTTL 负载
- 低功耗, I_{CC} 最大值为 80 μ A
- t_{pd} 典型值 = 9ns
- 电压为 5V 时, 输出驱动为 ± 6 mA
- 低输入电流, 最大值 1 μ A
- 允许从 n 条线路复用至一条线路
- 执行并行转串行转换

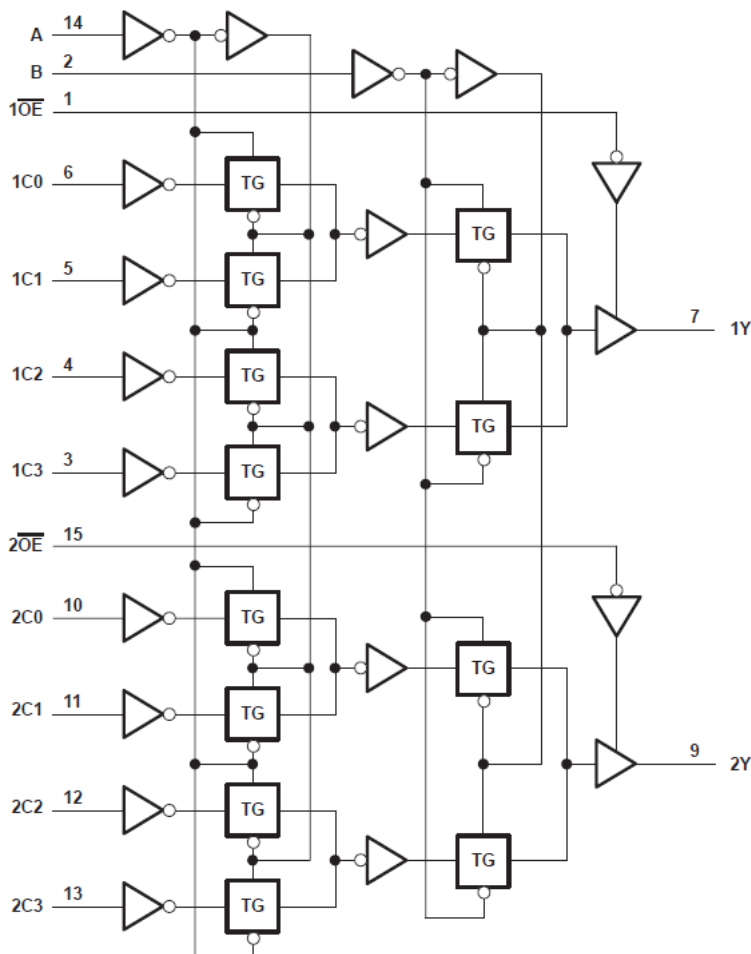
2 说明

SNx4HC253 器件包含两个具有完整二进制解码的独立数据选择器/多路复用器, 可从四个数据源中选择其中一个, 并提供选通控制 ($\overline{OE}$) 三态输出。

器件信息

零件编号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN74HC253D	SOIC (16)	9.90mm × 3.90mm
SN74HC253DB	SSOP (16)	6.20mm × 5.30mm
SN74HC253N	PDIP (16)	19.31mm × 6.35mm
SN74HC253NS	SO (16)	6.20mm × 5.30mm
SN54HC253J	CDIP (16)	24.38mm × 6.92mm
SNJ54HC253FK	LCCC (20)	8.89mm × 8.45mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



所示引脚编号用于 D、DB、J、N、NS 和 W 封装。

功能框图



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3 Revision History

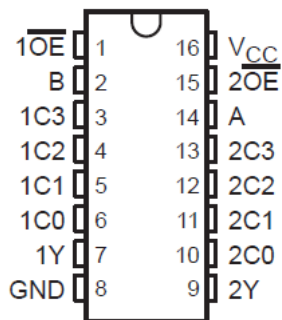
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2003) to Revision F (February 2022)

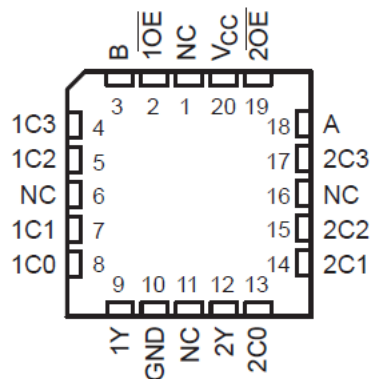
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- 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准..... **1**

4 Pin Configuration and Functions



J, D, DB, N, or NS Package
16-Pin CDIP, SOIC, SSOP, PDIP, SO
Top View



NC – No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		- 0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HC253			SN74HC253			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			0.5	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 6$ V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t / \Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	UNIT
THERMAL METRIC ⁽¹⁾		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	67	64	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			SN54HC253		SN74HC253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 μA	2	1.9	1.998		1.9		1.9		V
		4.5	4.4	4.499		4.4		4.4		
		6	5.9	5.999		5.9		5.9		
	I _{OH} = -6 mA	4.5	3.98	4.3		3.7		3.84		
	I _{OH} = -7.8 mA	6	5.48	5.8		5.2		5.34		
V _{OL}	I _{OL} = 20 μA	2		0.002	0.1		0.1		0.1	V
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	I _{OL} = 6 mA	4.5		0.17	0.26		0.4		0.33	
	I _{OL} = 7.8 mA	6		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0	6		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0 I _O = 0	6			8		160		80	μA
C _i		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} (V)	T _A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Any Y	2		62	150		225		190	ns
			4.5		19	30		45		38	
			6		16	26		38		32	
	Data (Any C)	Y	2		54	126		210		175	
			4.5		16	28		42		35	
			6		13	23		36		30	
t _{en}	OE	Y	2		28	100		150		125	ns
			4.5		11	20		30		25	
			6		9	17		26		21	
t _{dis}	OE	Y	2		21	135		203		170	ns
			4.5		14	30		45		38	
			6		12	35		38		31	
t _t		Y	2		28	60		90		75	ns
			4.5		8	12		18		15	
			6		6	10		15		13	

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	$T_A = 25^\circ\text{C}$			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2		76	235		355		295	ns
			4.5		23	47		71		59	
			6		20	41		60		51	
	Data (Any C)	Y	2		68	220		335		275	
			4.5		20	44		67		55	
			6		17	38		57		51	
t_{en}	$\overline{OE}$	Y	2		44	185		280		230	ns
			4.5		16	37		56		46	
			6		14	32		48		40	
t_t		Y	2		45	210		315		265	ns
			4.5		17	42		63		53	
			6		13	36		53		45	

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	No load	45	pF

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

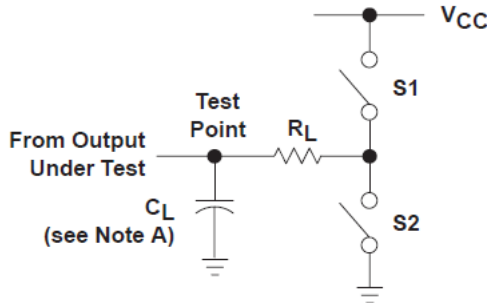


图 6-1. Load Circuit

PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open

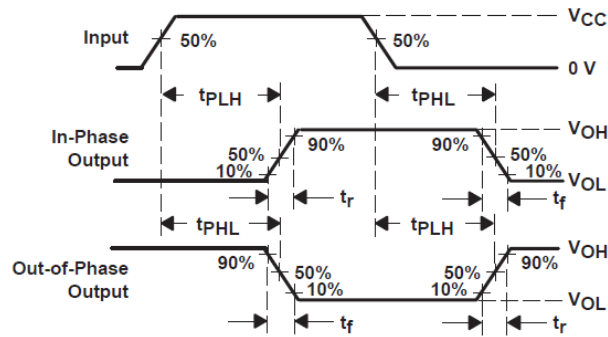


图 6-2. Voltage Waveforms
Propagation Delay and Output Transition Times

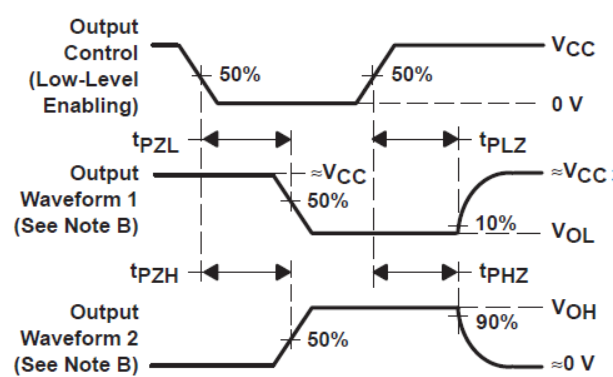


图 6-3. Voltage Waveforms
Enable and Disable Times for 3-State Outputs

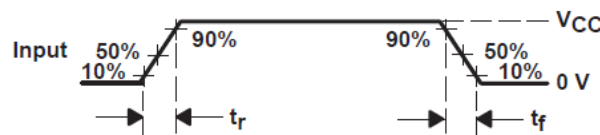


图 6-4. Voltage Waveform
Input Rise and Fall Times

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

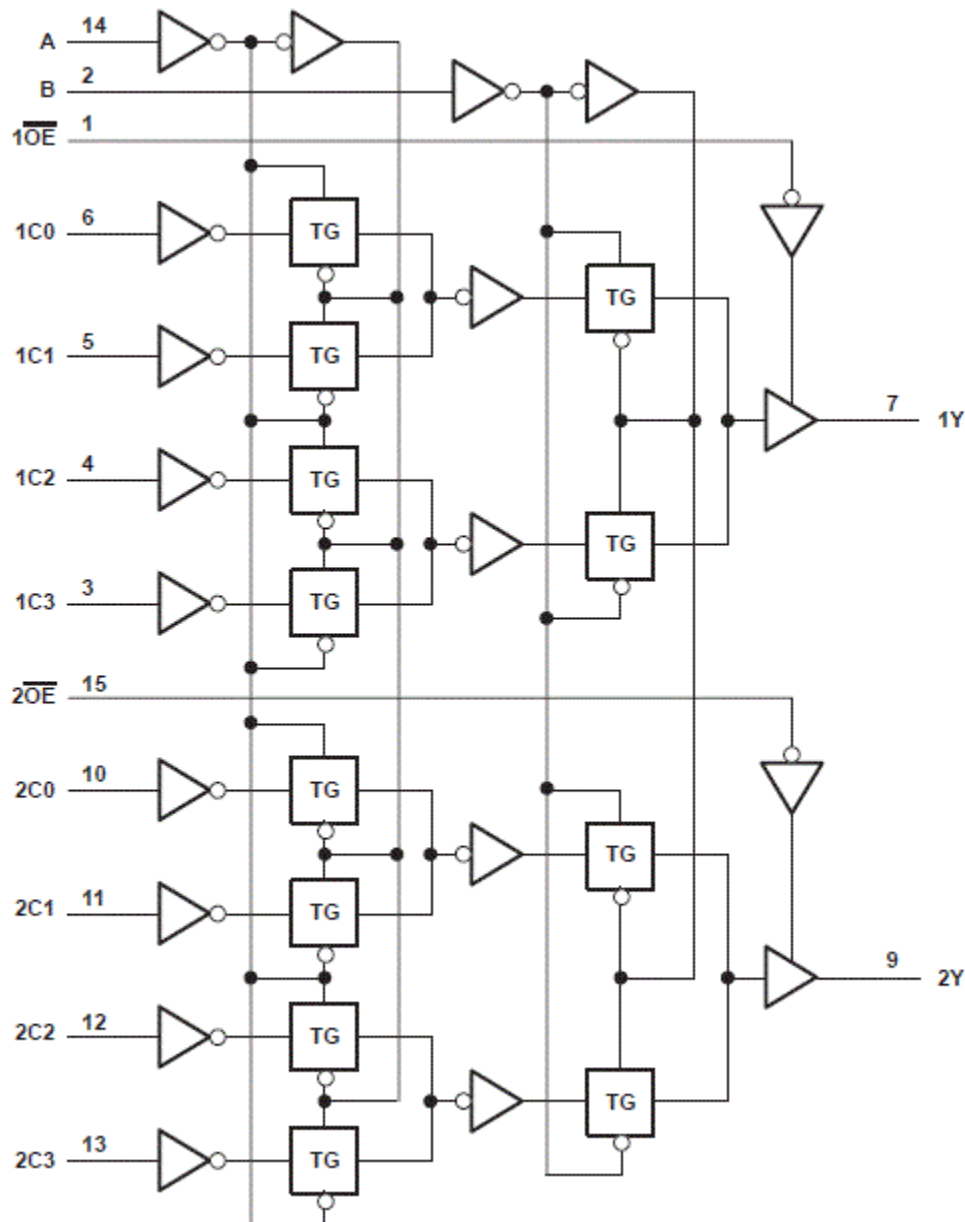
7 Detailed Description

7.1 Overview

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable ($\overline{OE}$) input. The outputs are disabled when their respective $\overline{OE}$ is high.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table

INPUTS							OUTPUT Y
SELECT ⁽¹⁾		DATA				OE	
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

(1) Select inputs A and B are common to both sections.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88682012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 88682012A SNJ54HC 253FK	Samples
5962-8868201EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8868201EA SNJ54HC253J	Samples
SN54HC253J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC253J	Samples
SN74HC253DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SN74HC253DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SN74HC253N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC253N	Samples
SN74HC253NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC253N	Samples
SN74HC253NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SNJ54HC253FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 88682012A SNJ54HC 253FK	Samples
SNJ54HC253J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8868201EA SNJ54HC253J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC253, SN74HC253 :

- Catalog : [SN74HC253](#)
- Automotive : [SN74HC253-Q1](#), [SN74HC253-Q1](#)
- Enhanced Product : [SN74HC253-EP](#), [SN74HC253-EP](#)
- Military : [SN54HC253](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC253DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC253NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC253NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC253DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC253DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC253NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC253NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

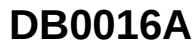
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88682012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC253N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC253N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC253NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC253NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC253FK	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



SSOP - 2 mm max height

Technical drawing of a connector housing, showing three views: Top View, Side View, and Detail A (Typical).

Top View:

- Overall Width: 8.2 TYP (8.2 typical)
- Overall Height: 6.5 (5.9) (NOTE 3)
- Pin 1 Index Area: Circular area indicating the location of Pin 1.
- Pin 16: Located at the top right corner.
- Pin 8: Located at the bottom left corner.
- Pin 9: Located at the bottom right corner.
- Pin 14: Located at the top right corner.
- Pin 2: Located at the bottom right corner.
- Pin 16X 0.65: Dimension indicating the length of the pins.
- Pin 2X 4.55: Dimension indicating the length of the pins.
- Pin 16X 0.38 0.22: Dimension indicating the length of the pins.
- Pin 5.6 (5.0) (NOTE 4): Dimension indicating the pitch between pins.
- Feature Control Frame: $\oplus 0.1 \text{ (M)} \text{ C A B}$

Side View:

- Seating Plane: Indicated by a vertical line.
- Feature Control Frame: $\text{C} \text{ 0.1 C}$

Detail A (Typical):

- Overall Width: 0.25
- Overall Height: 0.09
- Gage Plane: Indicated by a horizontal line.
- Pin 0.25: Dimension indicating the length of the pins.
- Pin 0.95 0.55: Dimension indicating the length of the pins.
- Pin 0.05 MIN: Dimension indicating the minimum length of the pins.
- Pin 2 MAX: Dimension indicating the maximum length of the pins.
- Pin 0° - 8°: Dimension indicating the angle of the pins.

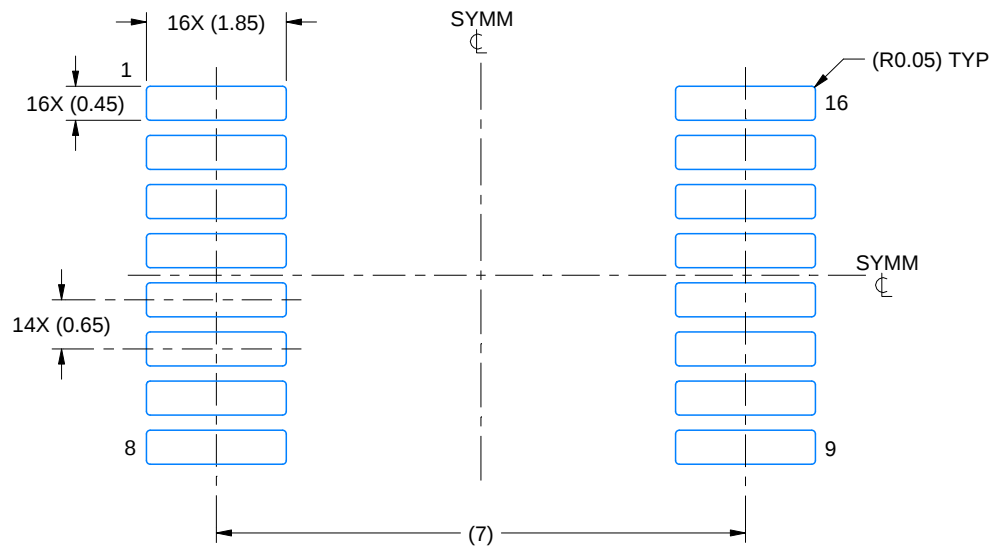
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

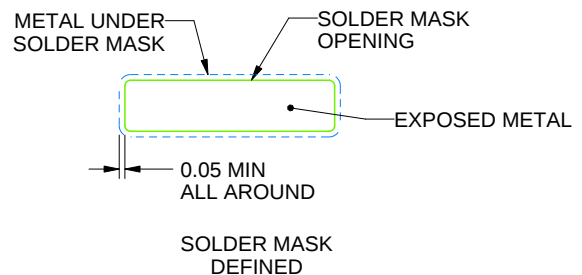
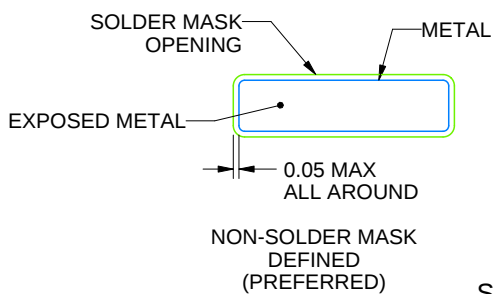
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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