

SNx4AHC540 具有三态输出的八路缓冲器/驱动器

1 特性

- 工作范围为 2V 至 5.5V V_{CC}
- 门锁性能超过 250mA，符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 服务器
- PC 和笔记本电脑
- 网络交换机
- 可穿戴保健和健身设备
- 电信基础设施
- 电子销售终端

3 说明

SNx4AHC540 八通道缓冲器/驱动器非常适合用于驱动总线或缓冲存储器地址寄存器。该类器件在封装的相对两侧具有输入端和输出端，有助于印刷电路板布局布线。

器件信息

| 器件型号 | 封装 (引脚) ⁽¹⁾ | 本体尺寸 (标称值) |
|---------------|------------------------|------------------|
| SN74AHC540N | PDIP (20) | 25.40mm × 6.35mm |
| SN74AHC540DB | SSOP (20) | 7.50mm × 5.30mm |
| SN74AHC540PW | TSSOP (20) | 6.50mm × 4.40mm |
| SN74AHC540DGV | TVSOP (20) | 5.00mm × 4.40mm |
| SN74AHC540DW | SOIC (20) | 12.80mm × 7.50mm |
| SNJ54AHC540FK | LCCC (20) | 9.0mm × 9.0mm |
| SNJ54AHC540W | CFP (20) | 13.72mm × 8.13mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

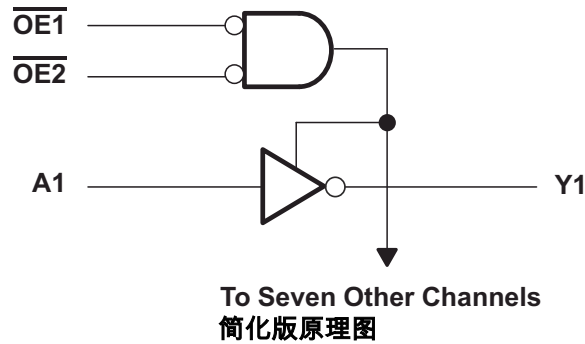
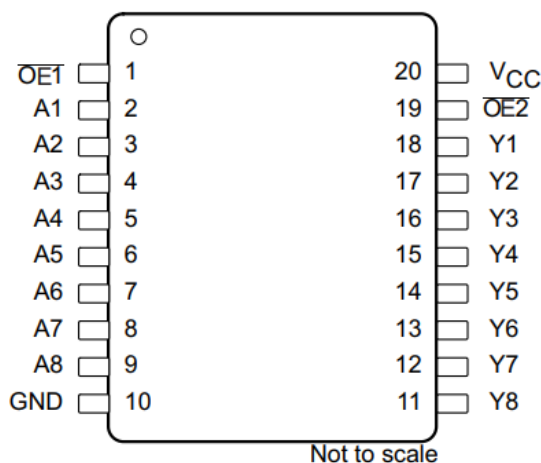


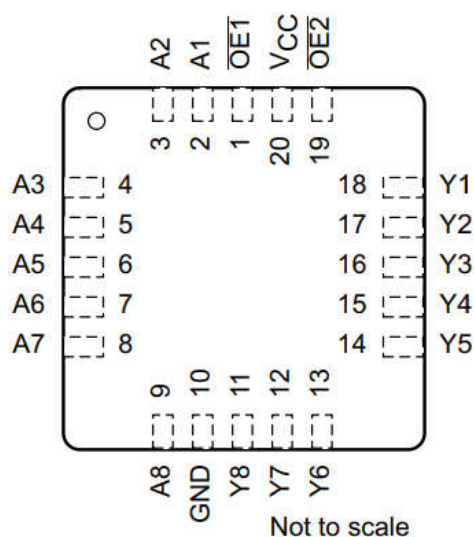
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4 Pin Configuration and Functions



**图 4-1. SN54AHC540: J or W Package;
SN74AHC540: DB, DGV, DW, N, NS, or PW Package
SN54AHC540: 20-Pin CDIP or CFP; SN74AHC540:
20-Pin SSOP, TVSOP, SOIC, PDIP, PDIP, or TSSOP
Top View**



**图 4-2. SN54AHC540: FK Package 20-Pin LCCC Top
View**

表 4-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|-----------------|
| NO. | NAME | | |
| 1 | OE1 | I | Output Enable 1 |
| 2 | A1 | I | A1 Input |
| 3 | A2 | I | A2 Input |
| 4 | A3 | I | A3 Input |
| 5 | A4 | I | A4 Input |
| 6 | A5 | I | A5 Input |
| 7 | A6 | I | A6 Input |
| 8 | A7 | I | A7 Input |
| 9 | A8 | I | A8 Input |
| 10 | GND | — | Ground |
| 11 | Y8 | O | Y8 Output |
| 12 | Y7 | O | Y7 Output |
| 13 | Y6 | O | Y6 Output |
| 14 | Y5 | O | Y5 Output |
| 15 | Y4 | O | Y4 Output |
| 16 | Y3 | O | Y3 Output |
| 17 | Y2 | O | Y2 Output |
| 18 | Y1 | O | Y1 Output |
| 19 | OE2 | I | Output Enable 2 |
| 20 | V _{CC} | — | Power Pin |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|---|--|------|-----------------------|------|
| V _{CC} | Supply voltage range | | −0.5 | 7 | V |
| V _I | Input voltage range ⁽²⁾ | | −0.5 | 7 | V |
| V _O | Output voltage range ⁽²⁾ | | −0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | −20 | | mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | ±20 | | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | ±25 | | mA |
| | Continuous current through V _{CC} or GND | | ±75 | | mA |
| T _J | Junction temperature | | 150 | | °C |
| T _{stg} | Storage temperature | | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | SN54AHC540 | | SN74AHC540 | | UNIT |
|---------------------|------------------------------------|--|------------|----------|------------|----------|------|
| | | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | | 1.5 | | V |
| | | $V_{CC} = 3\text{ V}$ | 2.1 | | 2.1 | | |
| | | $V_{CC} = 5.5\text{ V}$ | 3.85 | | 3.85 | | |
| V_{IL} | Low-level Input voltage | $V_{CC} = 2\text{ V}$ | | 0.5 | | 0.5 | V |
| | | $V_{CC} = 3\text{ V}$ | | 0.9 | | 0.9 | |
| | | $V_{CC} = 5.5\text{ V}$ | | 1.65 | | 1.65 | |
| V_I | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| V_O | Output voltage | | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | | −50 | | −50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | −4 | | −4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | −8 | | −8 | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | | 50 | | 50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 4 | | 4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 100 | | 100 | ns/V |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | 20 | | 20 | |
| T_A | Operating free-air temperature | | −55 | 125 | −40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHC540 | | | | | | UNIT |
|-------------------------------|--|--------------|----------------|--------------|-------------|--------------|---------------|------|
| | | DB (SSOP) | DGV (TVSOP) | DW (SOIC) | N (PDIP) | NS (PDIP) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 99.9 | 119.2 | 81.1 | 54.9 | 80.4 | 116.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 61.7 | 34.5 | 48.9 | 41.7 | 46.9 | 58.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.2 | 60.7 | 53.8 | 35.8 | 47.9 | 78.7 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 22.6 | 1.2 | 19.5 | 27.9 | 19.9 | 12.6 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 54.8 | 60.0 | 53.1 | 35.7 | 47.5 | 77.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54AHC540 | | SN74AHC540 | | –40°C to 125°C SN74AHC540 | | UNIT |
|----------------|---|--------------|--------------------------|-----|------------|------------|---------------|------------|-----------|------------------------------|-----------|---------------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | $I_{OH} = -50\ \mu\text{A}$ | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | |
| | $I_{OH} = -4\ \text{mA}$ | 3 V | 2.58 | | | 2.48 | | 2.48 | | 2.48 | | |
| | $I_{OH} = -8\ \text{mA}$ | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| V_{OL} | $I_{OL} = 50\ \mu\text{A}$ | 2 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OH} = 4\ \text{mA}$ | 3 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| | $I_{OH} = 8\ \text{mA}$ | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| I_I | $V_I = 5.5\ \text{V}$ or GND | 0 V to 5.5 V | | | ± 0.1 | | $\pm 1^{(1)}$ | | ± 1 | | ± 1 | μA |
| $I_{OZ}^{(2)}$ | $V_O = V_{CC}$ or GND $V_I (\text{OE}) = V_{IL}$ or V_{IH} | 5.5 V | | | ± 0.25 | | ± 2.5 | | ± 2.5 | | ± 2.5 | μA |
| I_{CC} | $V_I = V_{CC}$ or GND $I_O = 0$ | 5.5 V | | | 4 | | 40 | | 40 | | 40 | μA |
| C_i | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | | | pF |
| C_O | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0\ \text{V}$.

(2) For input and output pins, I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | SN54AHC540 | | SN74AHC540 | | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540 | | UNIT |
|-------------|------------------------|----------------|----------------------|--------------------------|---------------------|------------------|---------------------|------------|------|---|------|------|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 4.8 ⁽¹⁾ | 7 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 1 | 9.5 | ns |
| t_{PHL} | | | | 4.8 ⁽¹⁾ | 7 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 1 | 9.5 | |
| t_{PZH} | $\overline{\text{OE}}$ | Y | $C_L = 15\text{ pF}$ | 6.8 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | 1 | 13.5 | ns |
| t_{PZL} | | | | 6.8 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | 1 | 13.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Y | $C_L = 15\text{ pF}$ | 6.8 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | 1 | 13.5 | ns |
| t_{PLZ} | | | | 6.8 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | 1 | 13.5 | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 7.3 | 10.5 | 1 | 12 | 1 | 12 | 1 | 13.5 | ns |
| t_{PHL} | | | | 7.3 | 10.5 | 1 | 12 | 1 | 12 | 1 | 13.5 | |
| t_{PZH} | $\overline{\text{OE}}$ | Y | $C_L = 50\text{ pF}$ | 8 | 14 | 1 | 16 | 1 | 16 | 1 | 17 | ns |
| t_{PZL} | | | | 8 | 14 | 1 | 16 | 1 | 16 | 1 | 17 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Y | $C_L = 50\text{ pF}$ | 8 | 15.4 | 1 | 17.5 | 1 | 17.5 | 1 | 18.5 | ns |
| t_{PLZ} | | | | 8 | 15.4 | 1 | 17.5 | 1 | 17.5 | 1 | 18.5 | |
| $t_{sk(o)}$ | | | $C_L = 50\text{ pF}$ | | 1.5 ⁽²⁾ | | | | 1.5 | | | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | SN54AHC540 | | SN74AHC540 | | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC540 | | UNIT |
|-------------|------------------------|----------------|----------------------|--------------------------|--------------------|------------------|--------------------|------------|------|---|------|------|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 3.7 ⁽¹⁾ | 5 ⁽¹⁾ | 1 ⁽¹⁾ | 6 ⁽¹⁾ | 1 | 6 | 1 | 7 | ns |
| t_{PHL} | | | | 3.7 ⁽¹⁾ | 5 ⁽¹⁾ | 1 ⁽¹⁾ | 6 ⁽¹⁾ | 1 | 6 | 1 | 7 | |
| t_{PZH} | $\overline{\text{OE}}$ | Y | $C_L = 15\text{ pF}$ | 4.7 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 1 | 9.5 | ns |
| t_{PZL} | | | | 4.7 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | 1 | 9.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Y | $C_L = 15\text{ pF}$ | 4.5 ⁽¹⁾ | 6.8 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | 1 | 8 | 1 | 8.5 | ns |
| t_{PLZ} | | | | 4.5 ⁽¹⁾ | 6.8 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | 1 | 8 | 1 | 8.5 | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 5.2 | 7 | 1 | 8 | 1 | 8 | 1 | 9 | ns |
| t_{PHL} | | | | 5.2 | 7 | 1 | 8 | 1 | 8 | 1 | 9 | |
| t_{PZH} | $\overline{\text{OE}}$ | Y | $C_L = 50\text{ pF}$ | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | 1 | 11.5 | ns |
| t_{PZL} | | | | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | 1 | 11.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Y | $C_L = 50\text{ pF}$ | 6 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10.5 | ns |
| t_{PLZ} | | | | 6 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10.5 | |
| $t_{sk(o)}$ | | | $C_L = 50\text{ pF}$ | | 1 ⁽²⁾ | | | | 1 | | | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

| PARAMETER | | SN74AHC540 | | UNIT |
|-------------|--|------------|------|------|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 12 | pF |

5.10 Typical Characteristics

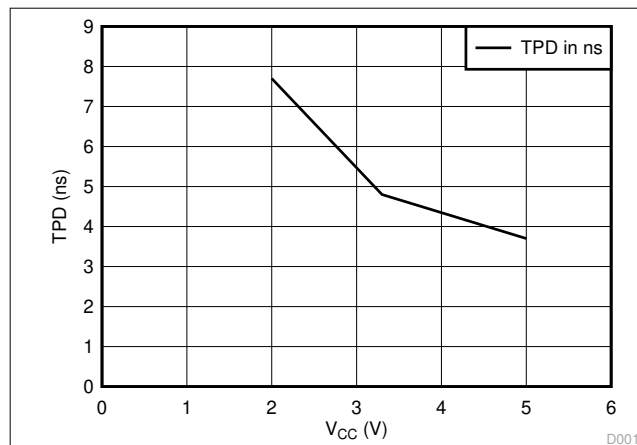


图 5-1. TPD vs V_{CC}

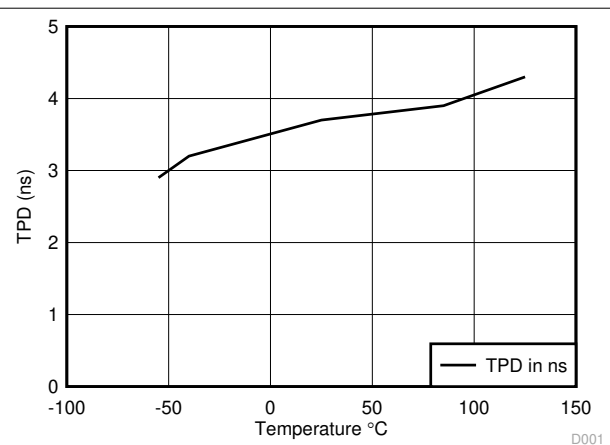
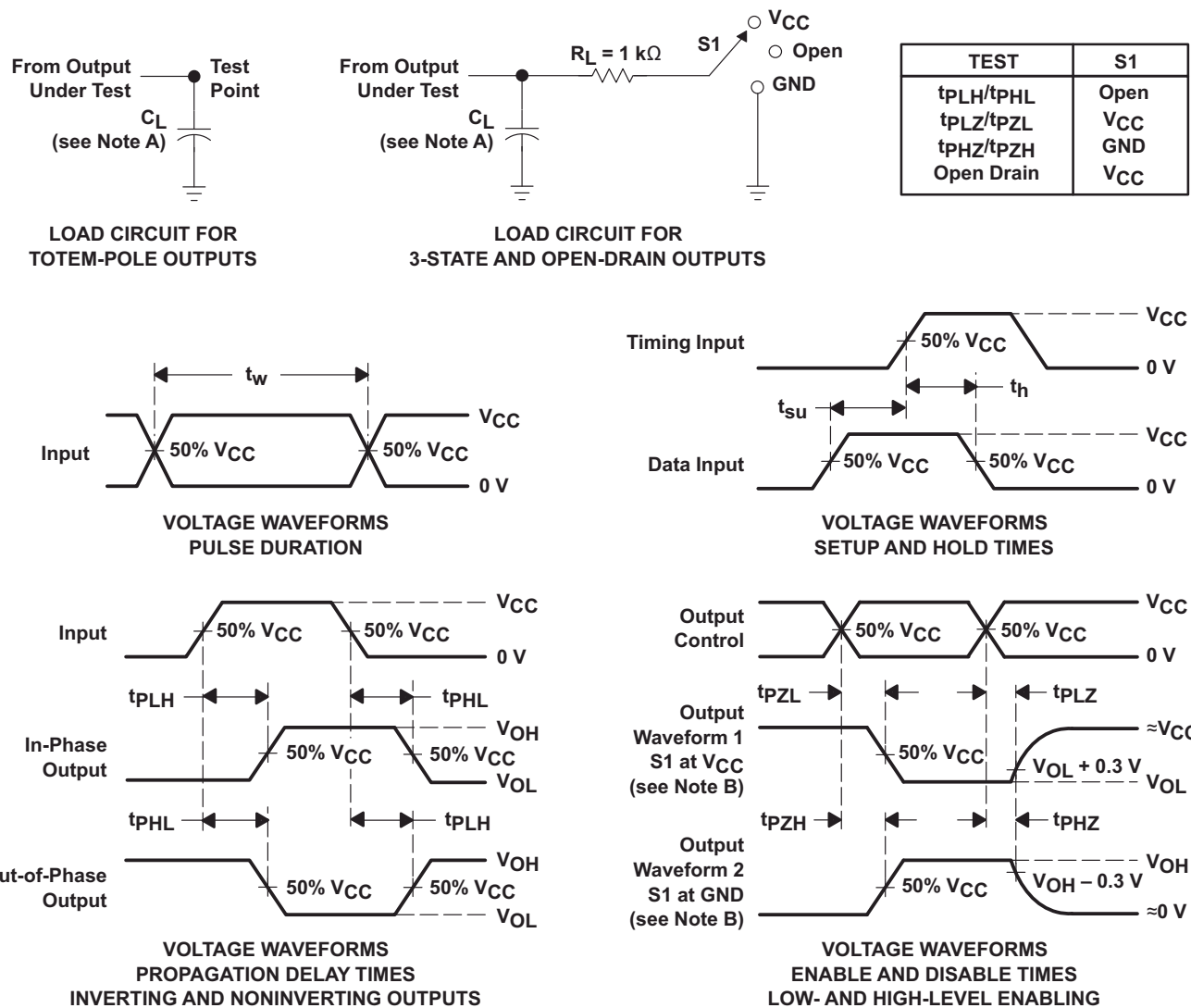


图 5-2. TPD vs Temperature

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

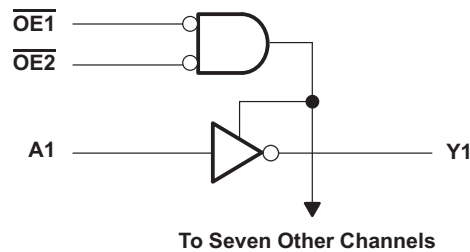
7.1 Overview

The SNx4AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

\overline{OE} should be tied to V_{CC} through a pullup resistor to ensure the high-impedance state during power up or power down. The minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

SNx4AHC540 device has a wide operating voltage range and operates from 2 V to 5.5 V. The inputs accept voltages up to 5.5 V, which allows for down translation. Slow input edges and low drive will minimize output overshoots and undershoots.

7.4 Device Functional Modes

表 7-1 shows the device functions for each buffer and driver.

表 7-1. Function Table (Each Buffer/Driver)

| INPUTS | | | OUTPUT Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Hi-Z |
| X | H | X | Hi-Z |

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AHC540 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V, which allows down translation to the V_{CC} level. 图 8-2 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

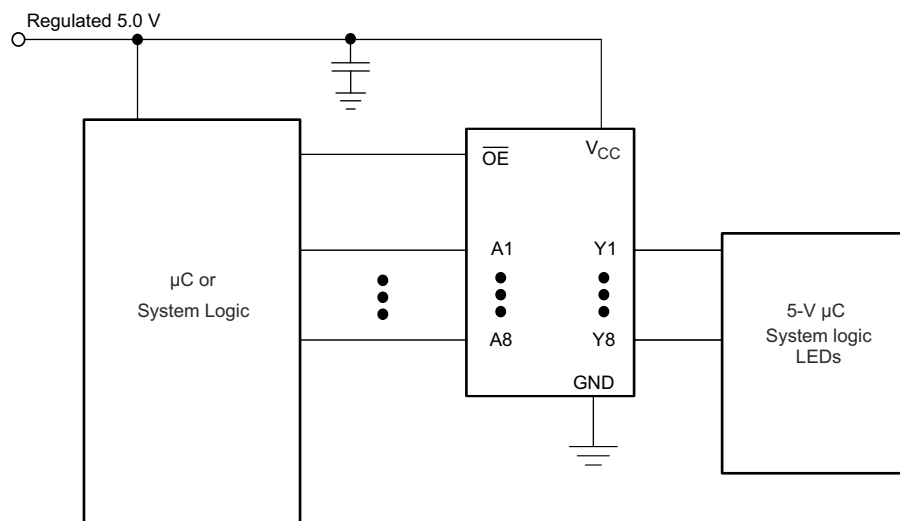


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended Output Conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curve

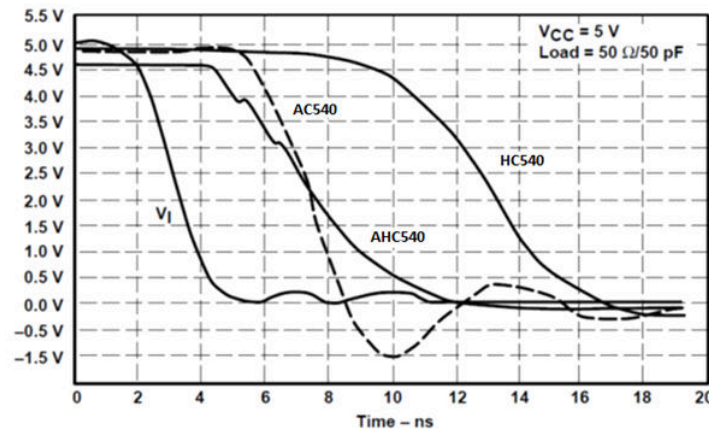


图 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the [图 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4 Layout

8.4.1 Layout Example

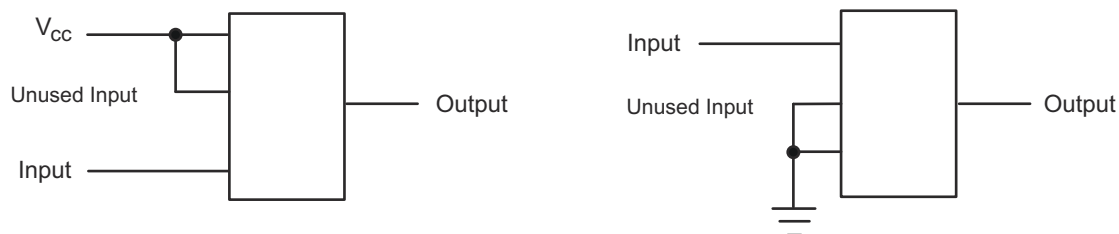


图 8-3. Layout Diagram

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision N (July 2024) to Revision O (January 2025) | Page |
|--|------|
| • Updated HBM and CDM values in <i>ESD Ratings</i> table..... | 4 |

| Changes from Revision M (May 2016) to Revision N (July 2024) | Page |
|--|------|
| • 通篇更新了表格、图和交叉参考的编号格式..... | 1 |
| • Updated RθJA values: PW = 105.4 to 116.8, DW = 83.0 to 81.1; Updated PW and DW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| 5962-9685001Q2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9685001Q2A SNJ54AHC 540FK |
| 5962-9685001QSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685001QS A SNJ54AHC540W |
| SN74AHC540DBR | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540DBR.A | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540DGSR | Active | Production | VSSOP (DGS) 20 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC540 |
| SN74AHC540DGVR | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540DGVR.A | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540DW | Obsolete | Production | SOIC (DW) 20 | - | - | Call TI | Call TI | -40 to 125 | AHC540 |
| SN74AHC540DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC540 |
| SN74AHC540DWR.A | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC540 |
| SN74AHC540N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC540N |
| SN74AHC540N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC540N |
| SN74AHC540PW | Obsolete | Production | TSSOP (PW) 20 | - | - | Call TI | Call TI | -40 to 125 | HA540 |
| SN74AHC540PWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540PWR.A | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA540 |
| SN74AHC540RKSR | Active | Production | VQFN (RKS) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC540 |
| SNJ54AHC540FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9685001Q2A SNJ54AHC 540FK |
| SNJ54AHC540FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9685001Q2A SNJ54AHC 540FK |
| SNJ54AHC540W | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685001QS A SNJ54AHC540W |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------------|
| SNJ54AHC540W.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685001QS A SNJ54AHC540W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC540, SN74AHC540 :

● Catalog : [SN74AHC540](#)

● Automotive : [SN74AHC540-Q1](#), [SN74AHC540-Q1](#)

- Military : [SN54AHC540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

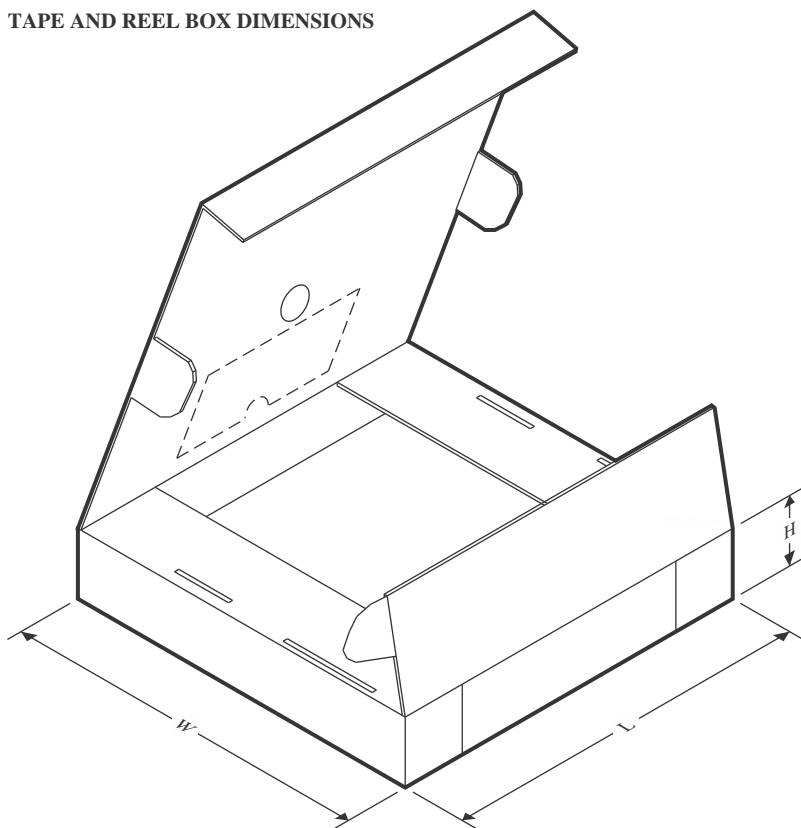
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC540DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC540DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74AHC540DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC540DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC540DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC540PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC540RKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC540DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC540DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74AHC540DGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC540DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC540DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC540PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC540RKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

TUBE

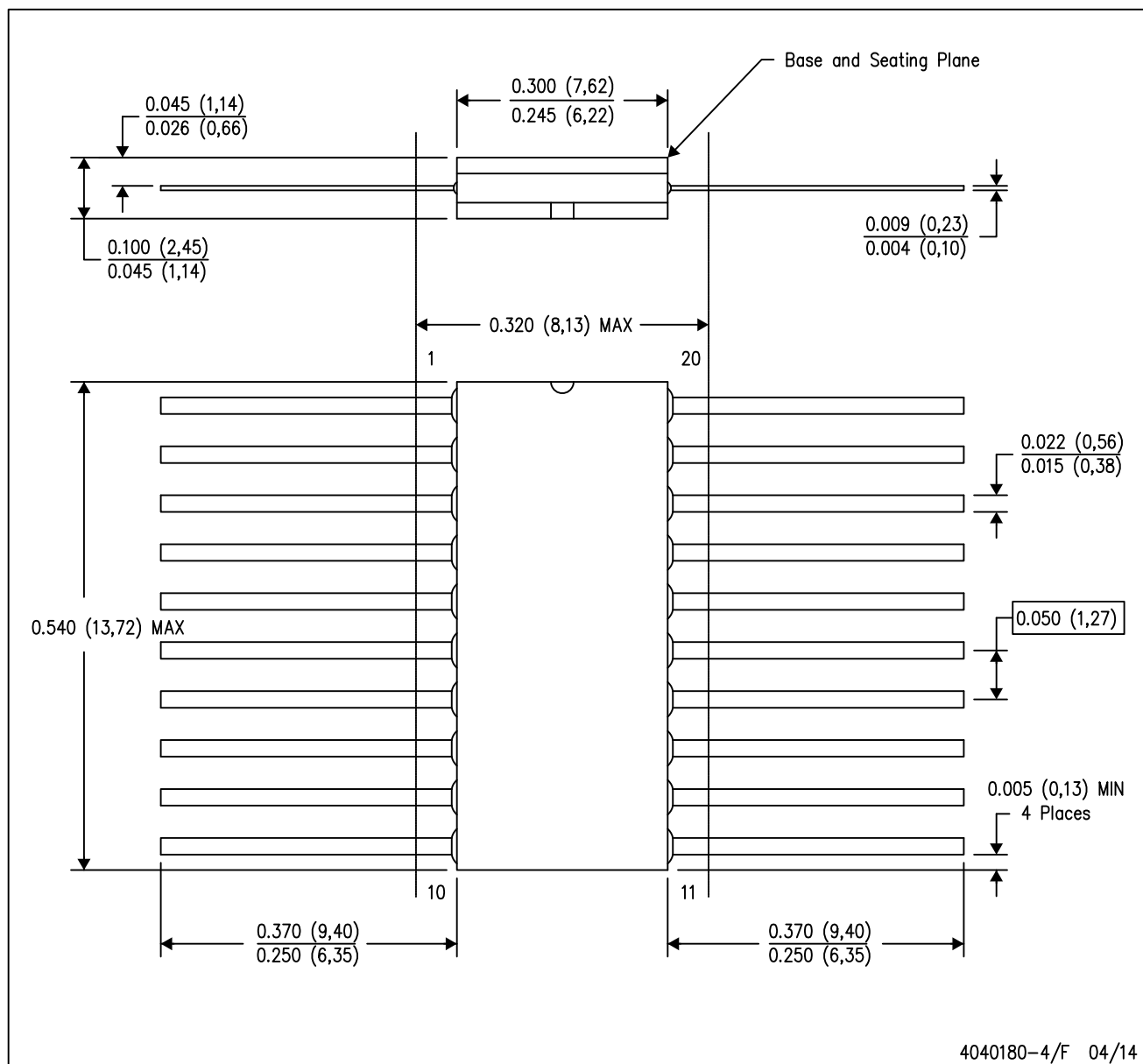


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9685001Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9685001QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC540N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC540N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC540FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC540FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC540W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AHC540W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK





TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



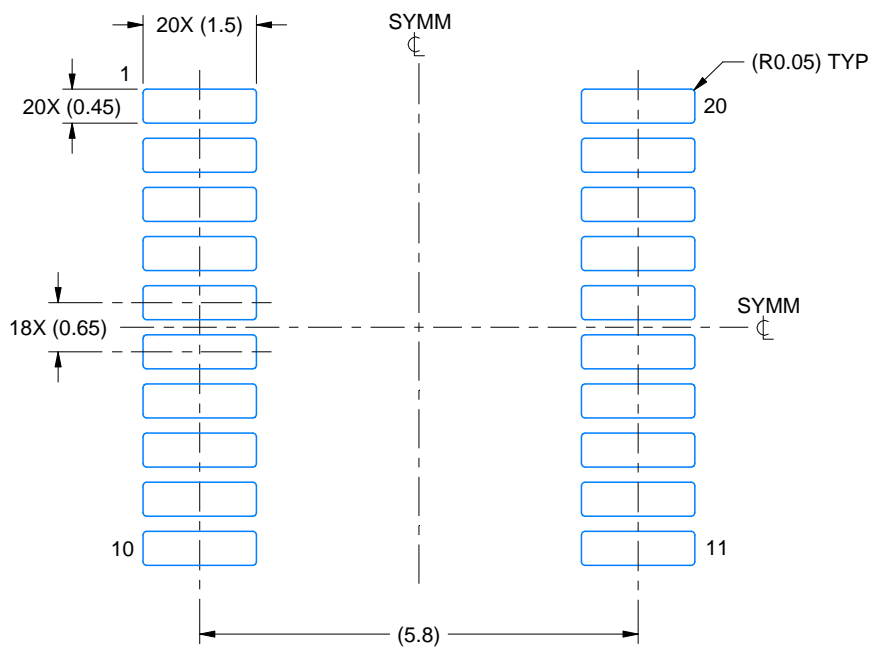
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

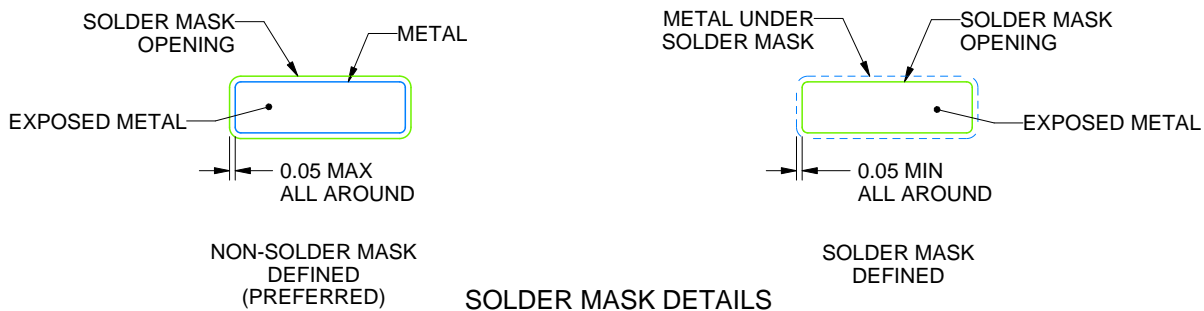
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

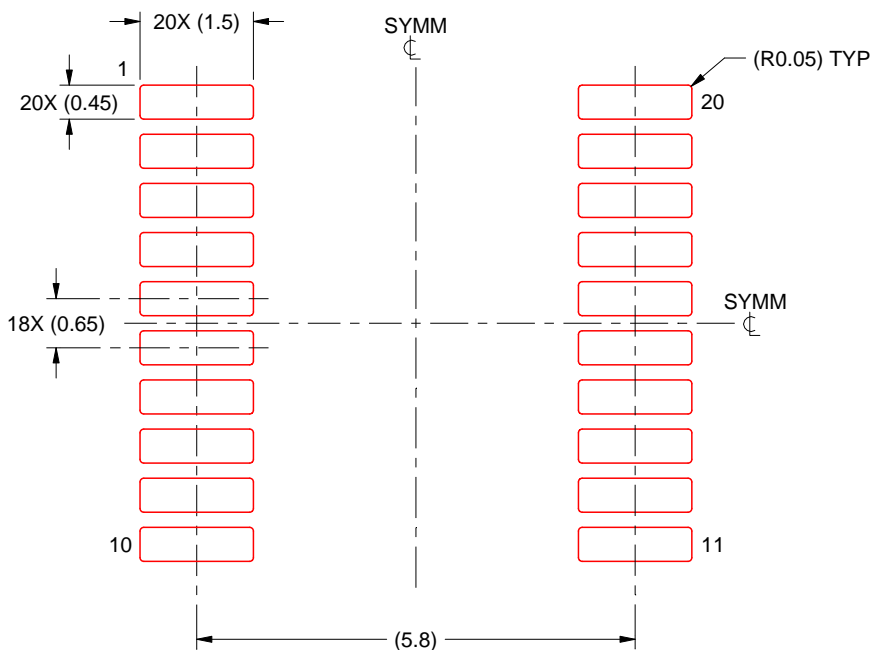
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

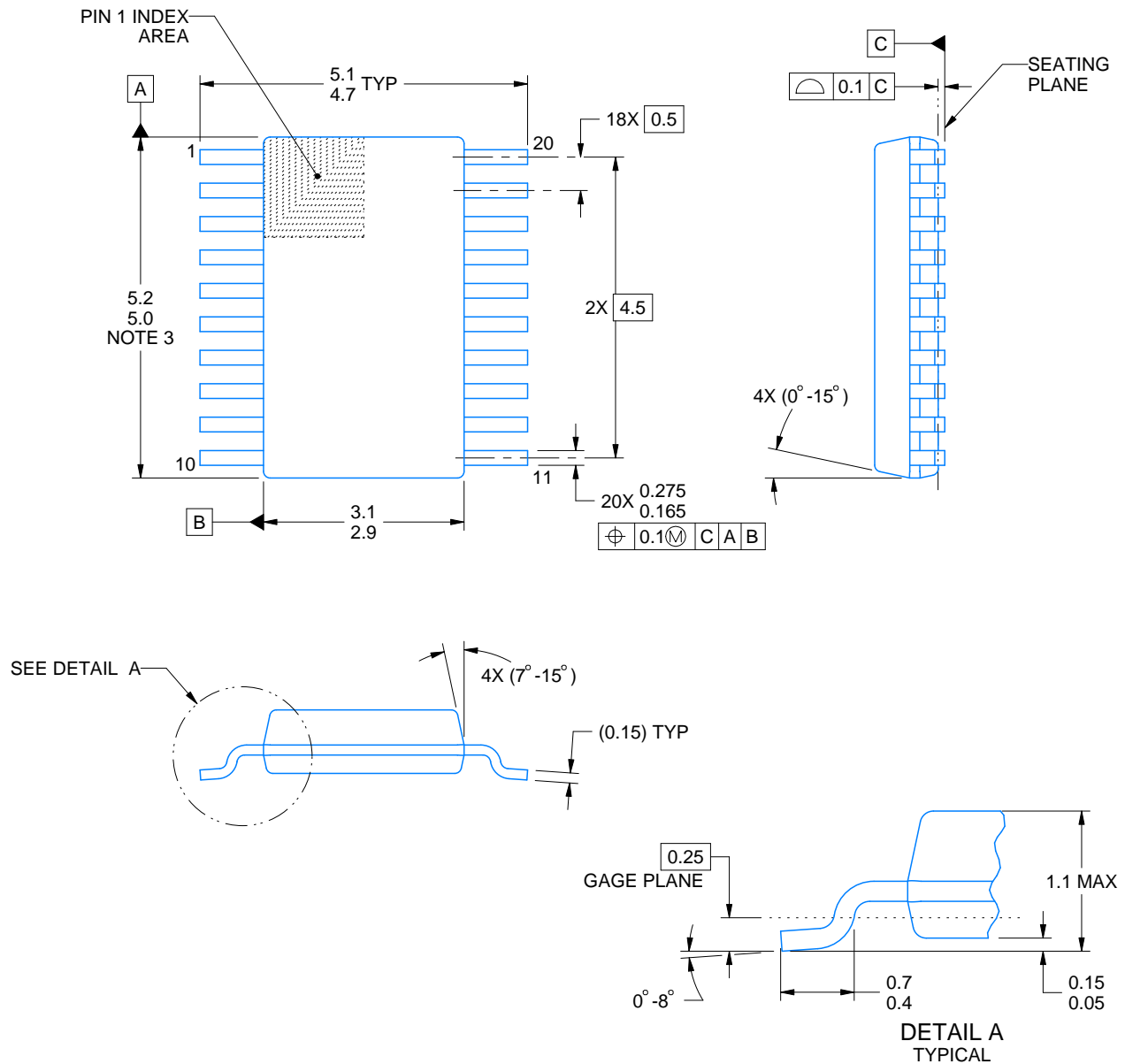


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

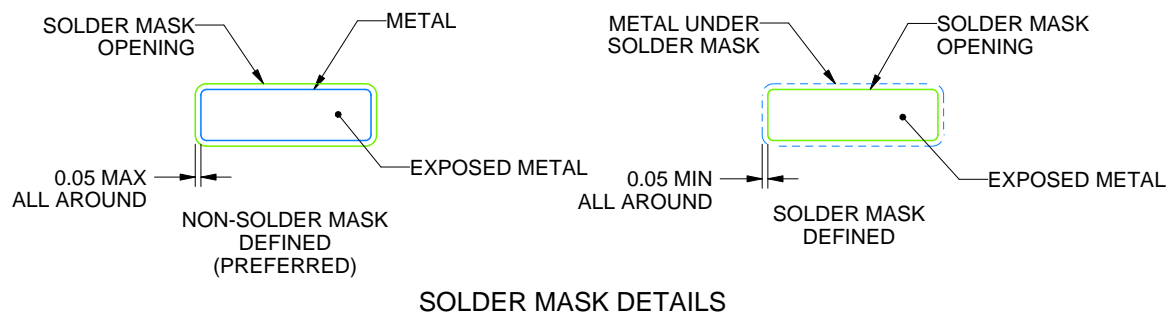
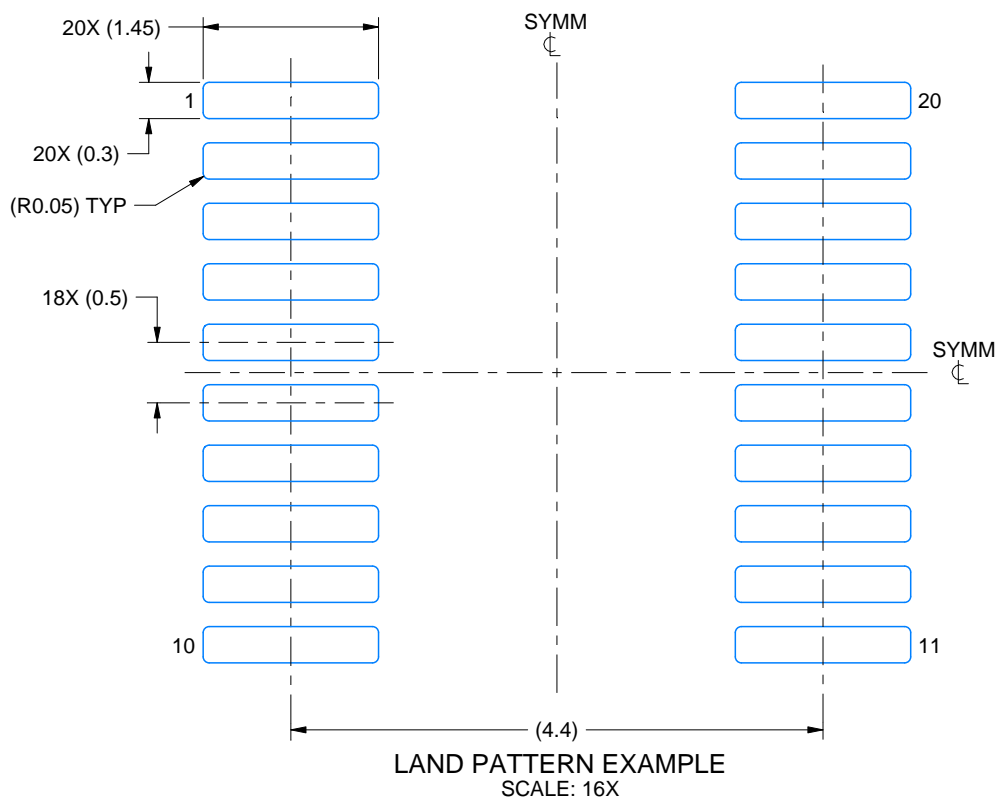
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

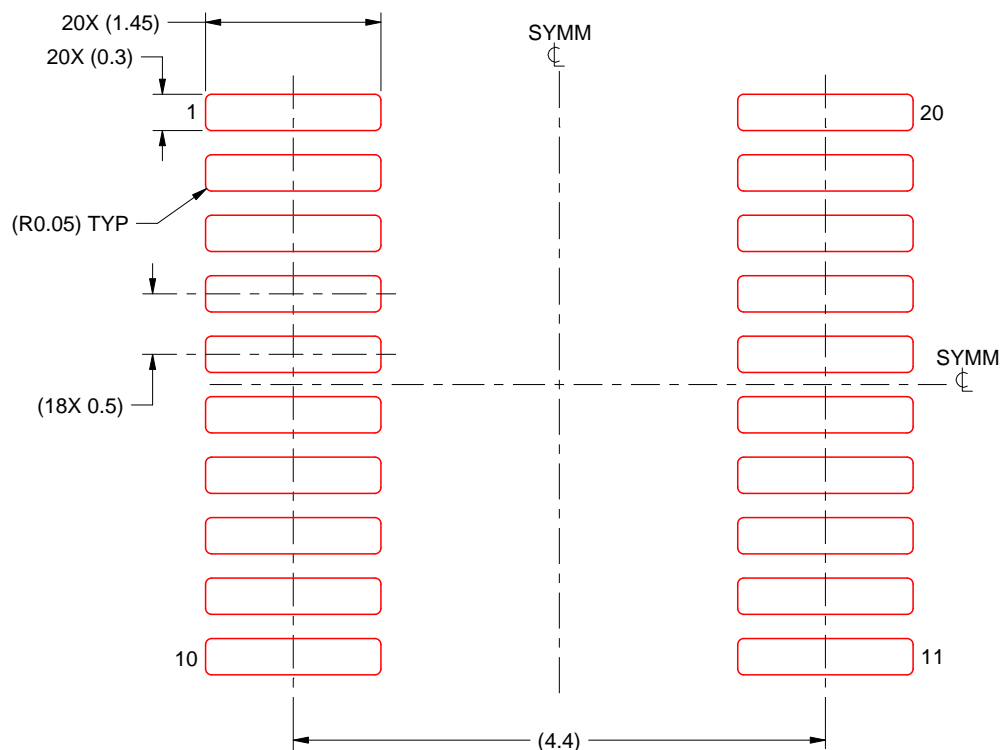
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

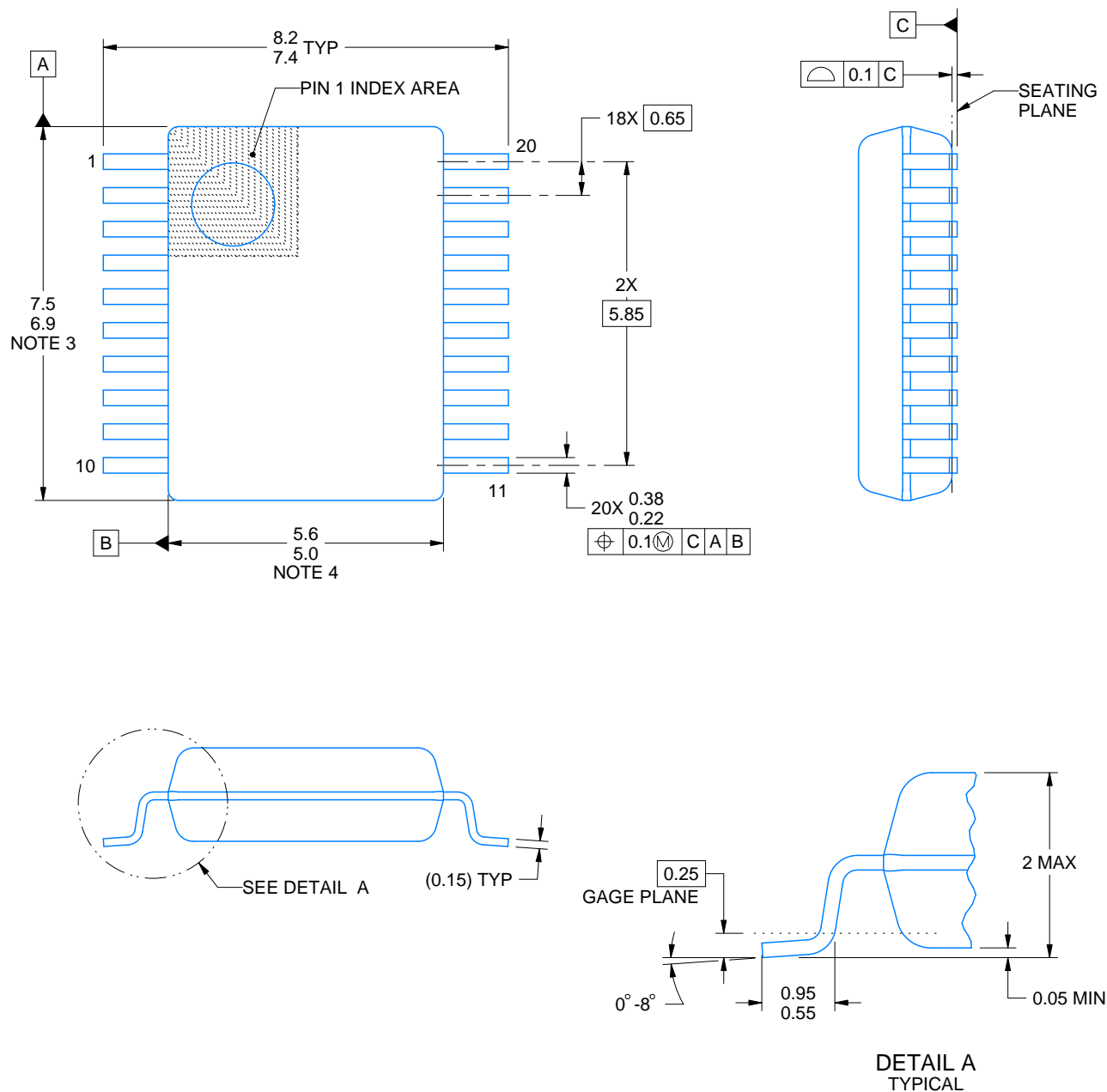
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

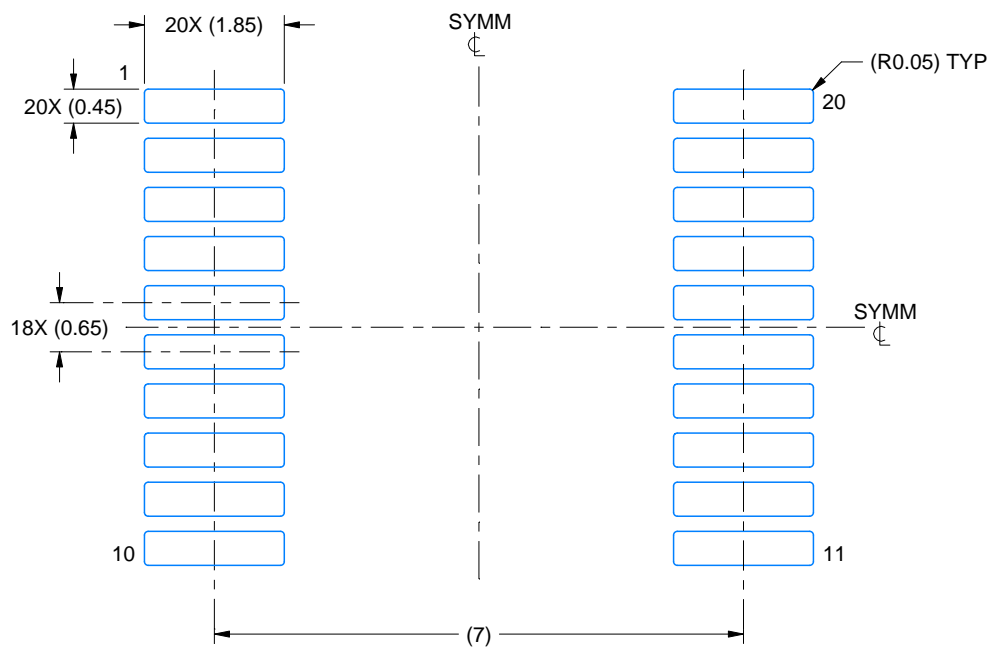
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

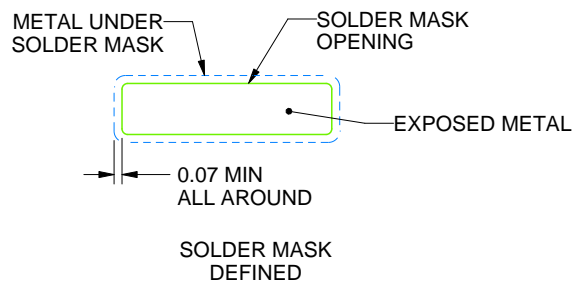
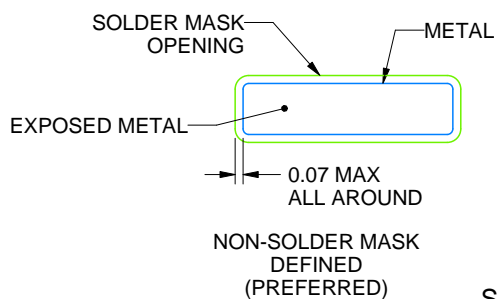
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

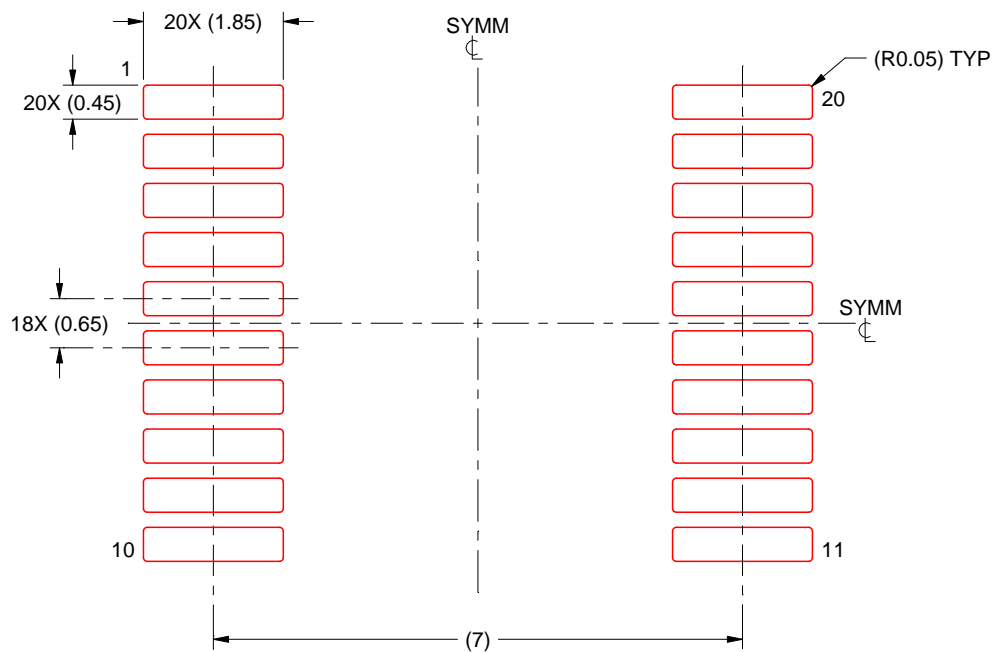
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

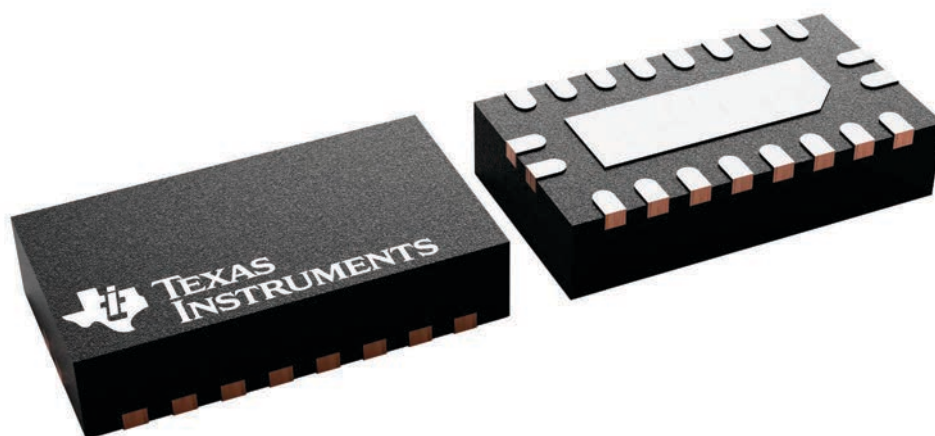
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

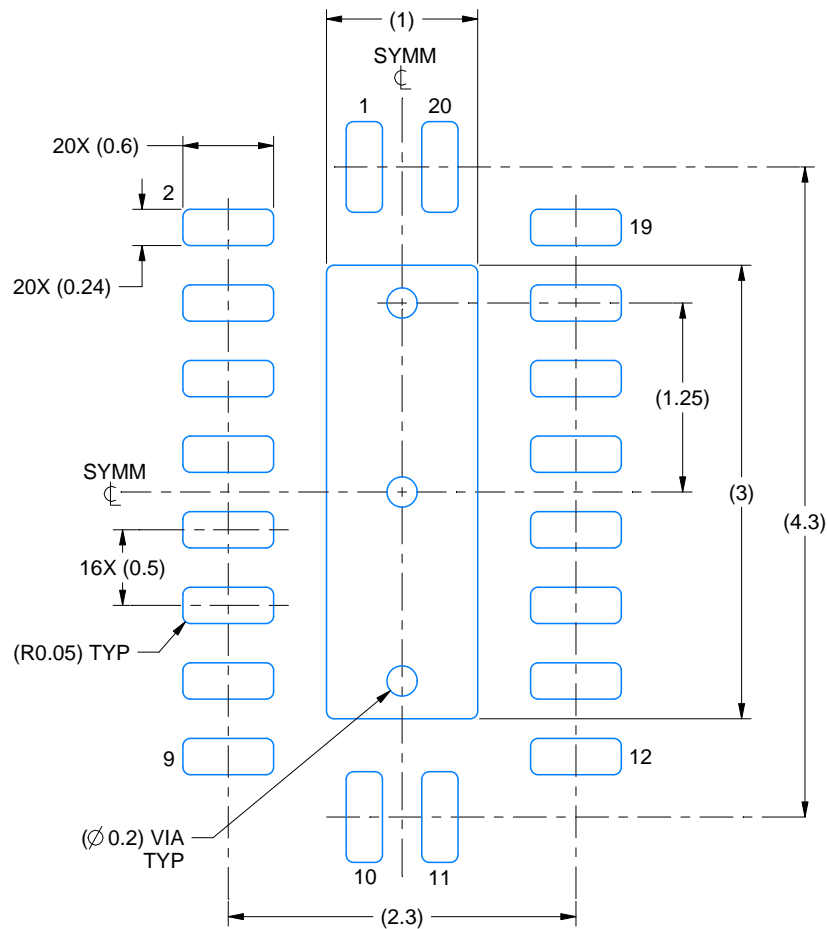


EXAMPLE BOARD LAYOUT

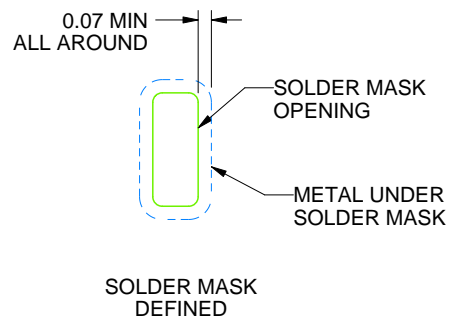
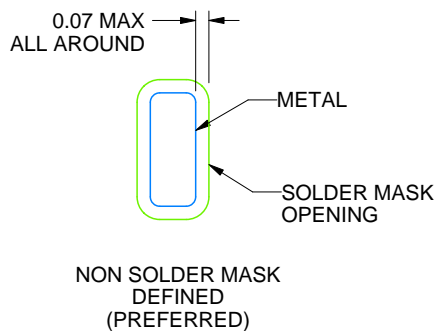
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

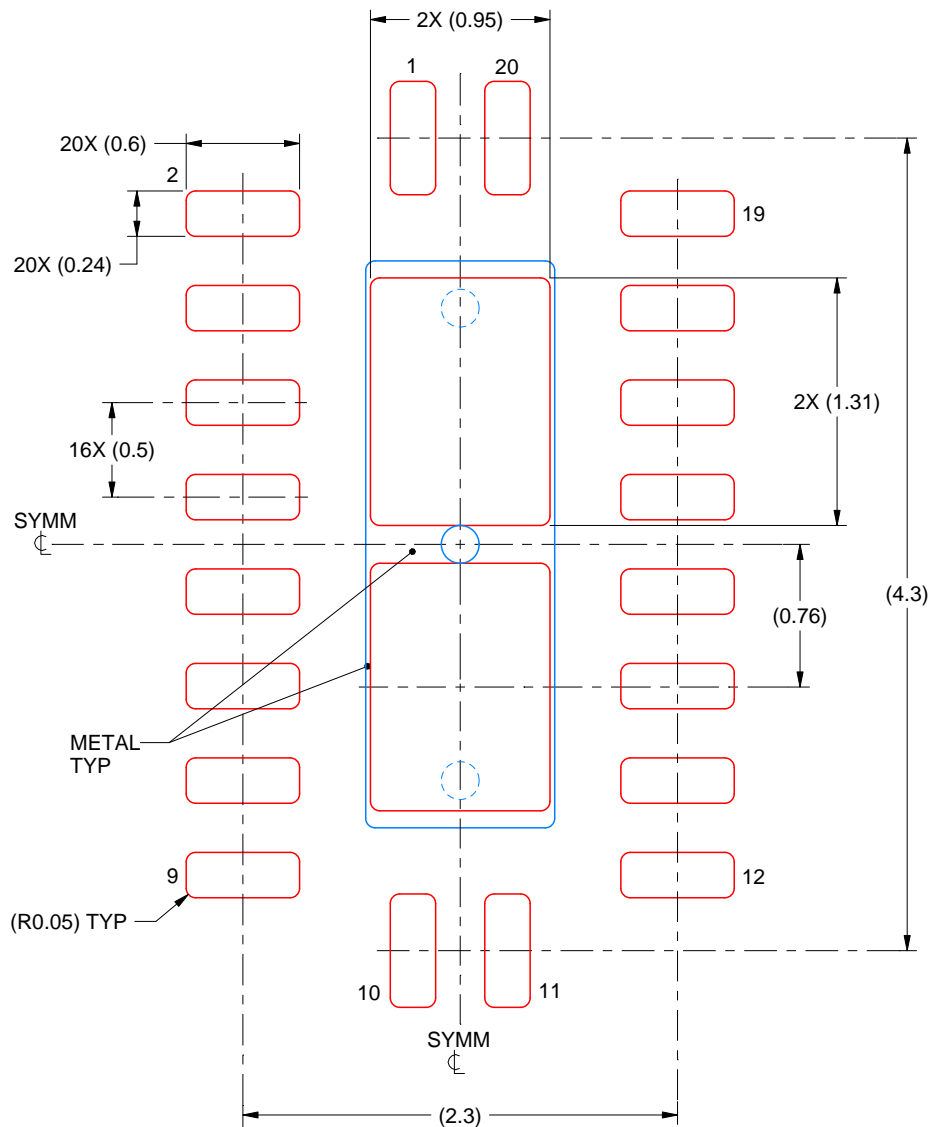
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

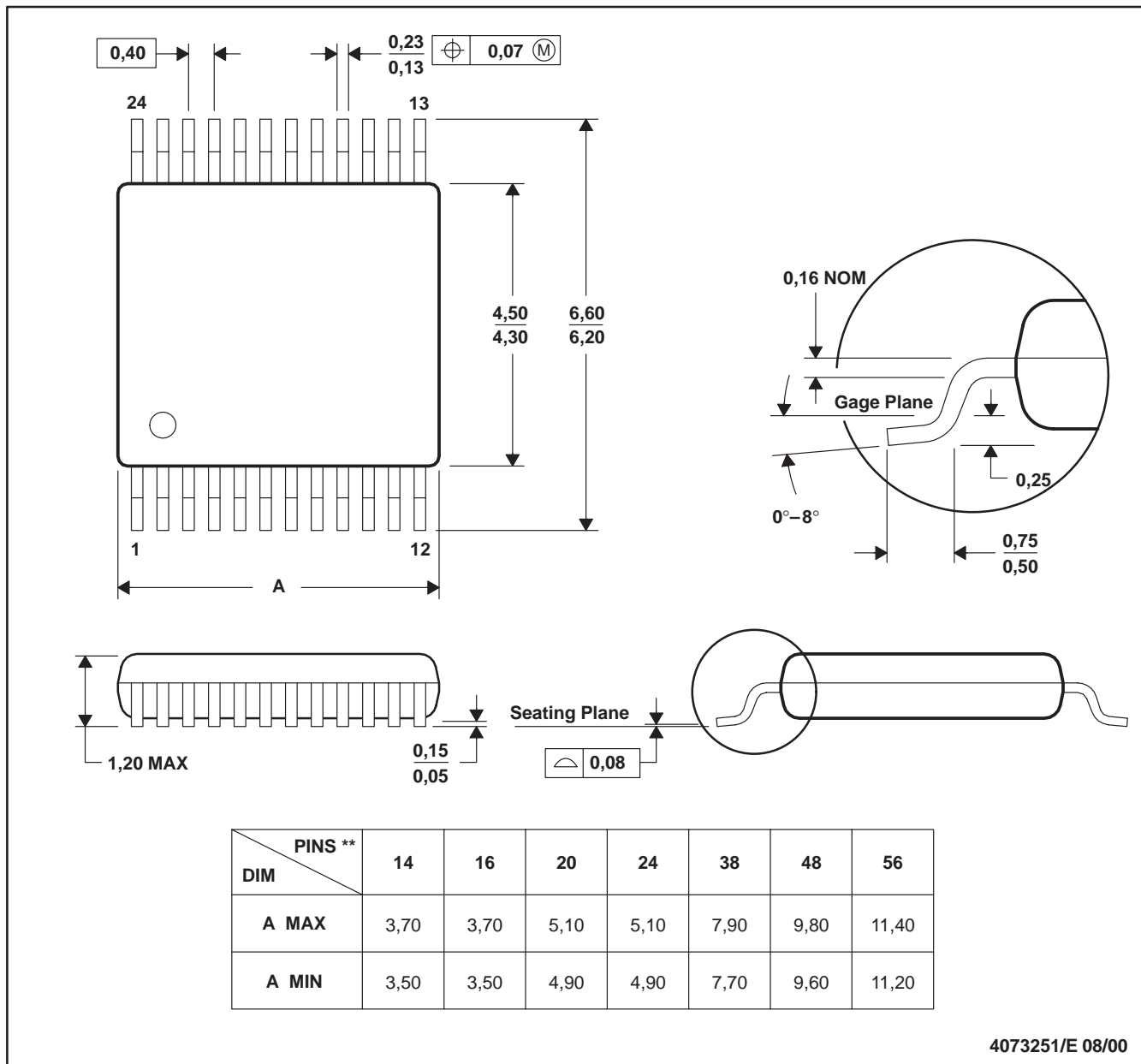
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

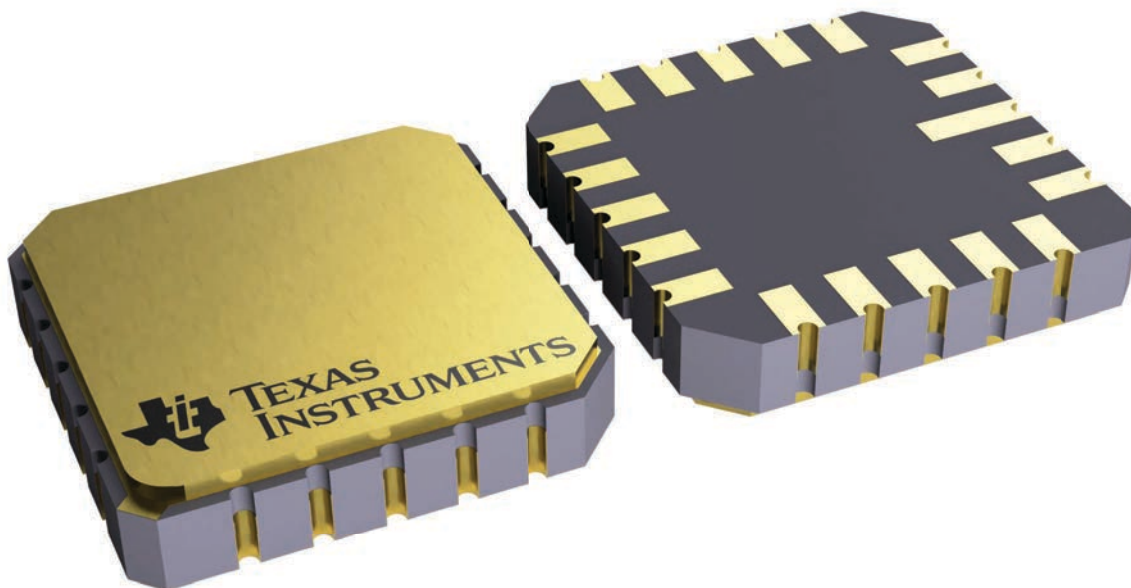
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

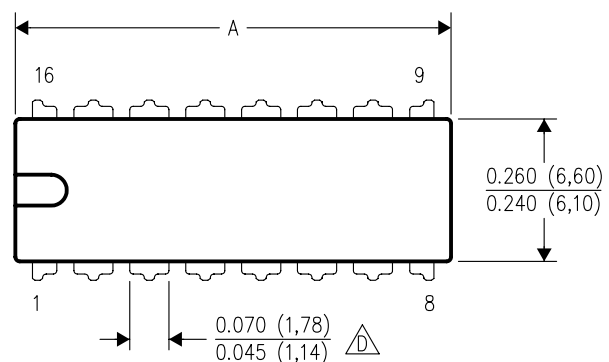


4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





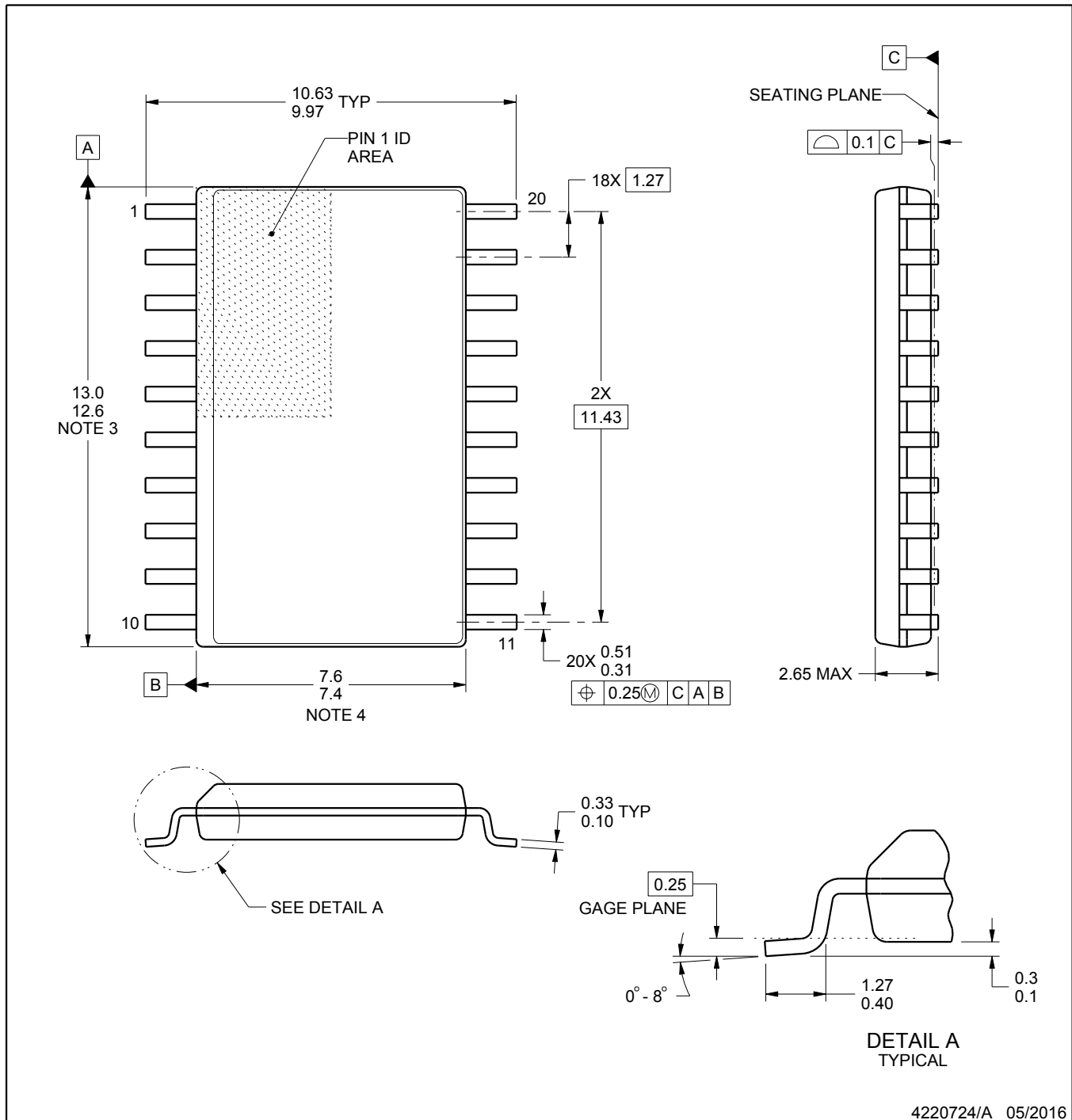
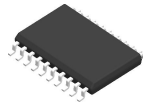
| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



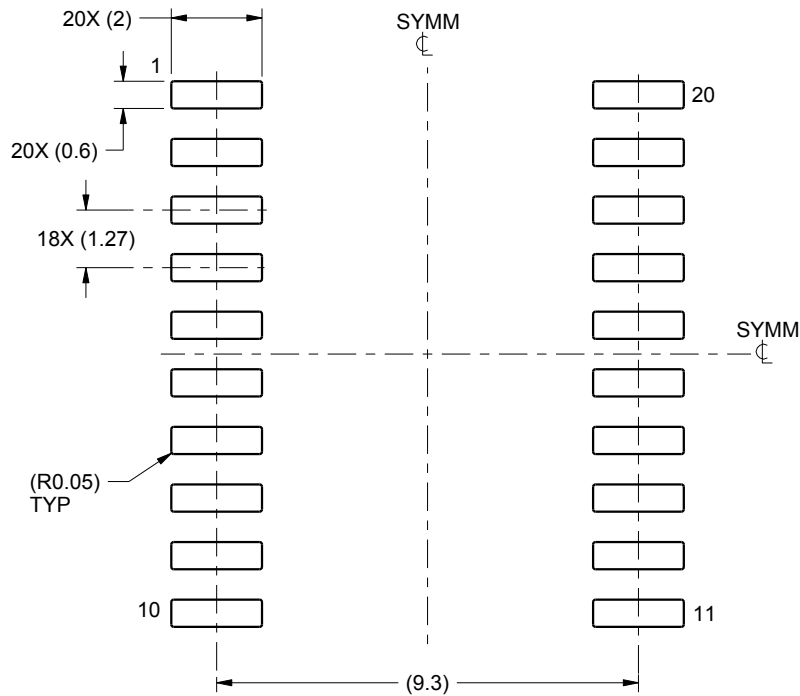
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

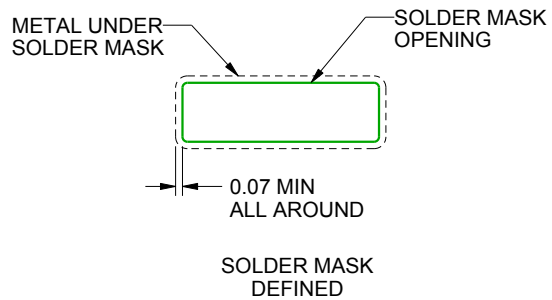
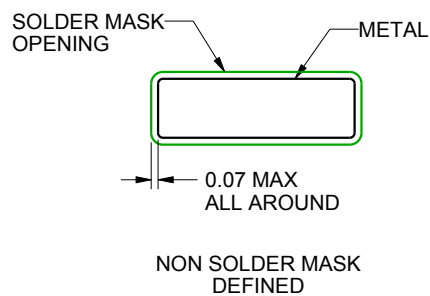
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

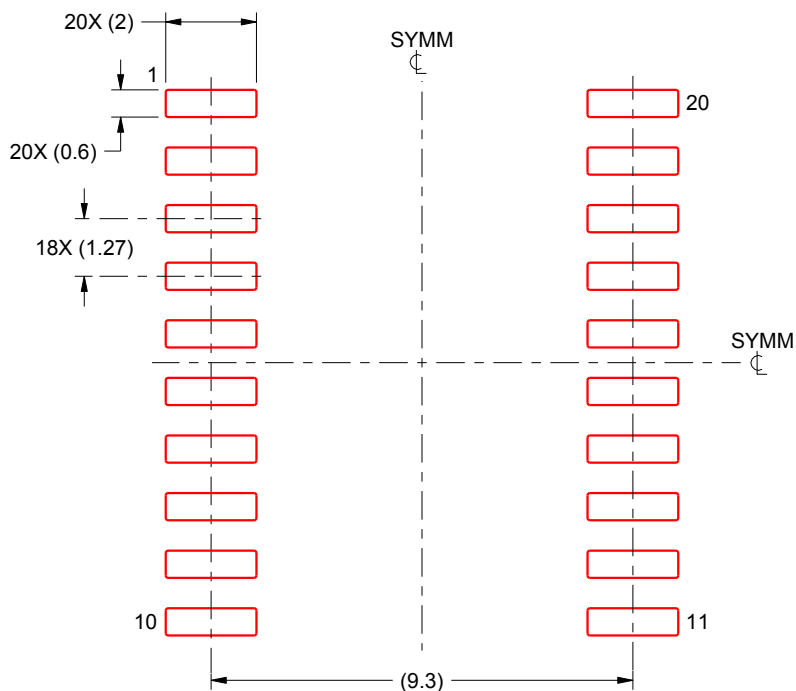
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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